An Investigation of the Interleaved Operation of a Stacked AC-DC Single-Stage Flyback Converter

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A thesis submitted in partial fulfillment of the requirements for the Master of Engineering Science degree in Electrical and Computer Engineering
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Abstract

Low power AC-DC power conversion is typically done with a two-stage converter that consists of an AC-DC front-end boost converter that also performs input power factor correction and an isolated DC-DC back-end converter that is either a flyback or a forward converter. In applications where cost is an overriding factor, single-stage AC-DC converters that use a single power converter to simultaneously perform input power factor correction and AC-DC conversion can be used. In applications where output filtering and hold-up time are important considerations, single-stage AC-DC converters are implemented with a DC bus capacitor.

The main objective of this thesis is to investigate the interleaved operation of a single-stage stacked AC-DC flyback converter that has less cost, size, and component stress than interleaved two-stage converters and interleaved non-stacked single-stage AC-DC converters. In this thesis, the steady-state operation of a stacked converter with interleaving is explained and analyzed in detail by using a computer program that is based on the principle of energy equilibrium. The results of the analysis, which are a set of equations related to key component stresses and losses and a set of graphs of steady-state characteristic curves is then used to select component values using an iterative design procedure. The performance of the stacked converter with interleaving is confirmed with results obtained by PSIM simulation as is the accuracy of the analysis. The thesis concludes with a summary of the thesis contents, conclusions, contributions, and suggestions for future work.

Keywords

AC-DC converter, flyback converter, stacked converter, Zero Voltage Switching, interleaved converter.
Summary for Lay Audience

Power electronics is very closely related to daily life and can be found in many applications, such as in mobile phones, personal computers, and hybrid vehicles. It is the field of electrical engineering that involves the use of semiconductor devices (i.e. switches, diodes, etc.) and other passive elements to convert electrical power from one form to another. The main objective in most applications where power converters are required is to implement converters with as little size, weight, cost, and power losses as possible and with the best performance possible.

Power converter is a device which can convert power from one condition to another condition to meet the requirement of electric power consuming applications. The AC-DC converter can convert the AC power from the power grid to the DC power which can be used by the electrical devices, such as computer, cell phone and other devices. In this research, an investigation of the interleaved stacked AC-DC flyback converter has been done step by step. Flyback converter is one of the basic converters with a transformer, it can adjust the output voltage by using different control signals. The proposed converter is put one flyback converter over another one, which is called stacked structure, to reduce the voltage stress on the components, to shrink the size and the cost of the whole design. The investigation is focused on the new operation mode with interleaved operation. To achieve the interleaved operation, there is some test and analysis have to be done with equations and simulation software. The interleaved operation makes the input current ripple smaller, and increase the total power factor of the converter, which can increase efficiency as well.
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<td>AC</td>
<td>Alternative Current</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>ZCS</td>
<td>Zero-Current Switching</td>
</tr>
<tr>
<td>ZVS</td>
<td>Zero-Voltage Switching</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Current Mode</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Current Mode</td>
</tr>
<tr>
<td>ICS</td>
<td>Input Current Shaper</td>
</tr>
<tr>
<td>PF</td>
<td>Power Factor</td>
</tr>
<tr>
<td>PFC</td>
<td>Power Factor Correction</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s Current Law</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchhoff’s Voltage Law</td>
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## List of Nomenclature

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<tr>
<th>Symbol</th>
<th>Description</th>
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<tr>
<td>$V_O$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$V_{bus}$</td>
<td>Bus voltage</td>
</tr>
<tr>
<td>$D$</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>$N$</td>
<td>Turns ratio</td>
</tr>
<tr>
<td>$L_m$</td>
<td>Magnetizing inductance of transformer</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
</tr>
<tr>
<td>$f_{ac}$</td>
<td>AC signal frequency</td>
</tr>
<tr>
<td>$R$</td>
<td>Output resistance (Loud resistance)</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Input voltage</td>
</tr>
<tr>
<td>$I_{Lin,peak,interval}$</td>
<td>Peak value of the current through the input inductance</td>
</tr>
<tr>
<td>$I_{Lin}$</td>
<td>Current through the input inductance</td>
</tr>
<tr>
<td>$V_{rec,k}$</td>
<td>Voltage during kth interval</td>
</tr>
<tr>
<td>$I_{Lin,rise}$</td>
<td>Rise part of one interval</td>
</tr>
<tr>
<td>$V_{peak}$</td>
<td>Peak value of the source AC voltage</td>
</tr>
<tr>
<td>$t$</td>
<td>Time period of one switching cycle</td>
</tr>
<tr>
<td>$V_{interval}$</td>
<td>Instantaneous voltage on the input inductor</td>
</tr>
<tr>
<td>$L_{lk1}$</td>
<td>Leakage inductance of transformers 1</td>
</tr>
<tr>
<td>$L_{lk2}$</td>
<td>Leakage inductance of transformers 2</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>Output power</td>
</tr>
<tr>
<td>$I_{Cbus1}$</td>
<td>Current in the bus capacitor 1</td>
</tr>
<tr>
<td>$I_{Cbus1}$</td>
<td>Current in the bus capacitor 2</td>
</tr>
<tr>
<td>$I_{Lin,rms, interval}$</td>
<td>The root mean square value of the input inductor current during one</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>$E_{bus-out}$</td>
<td>Output energy</td>
</tr>
<tr>
<td>$E_{bus-in}$</td>
<td>Input energy</td>
</tr>
<tr>
<td>$I_{cap,peak}$</td>
<td>Peak value of the DC bus capacitor current</td>
</tr>
<tr>
<td>$\Delta T_{sw1, on}$</td>
<td>on-Time period in one switching cycle</td>
</tr>
<tr>
<td>$\Delta T_{sw1, off}$</td>
<td>off-Time period in one switching cycle</td>
</tr>
<tr>
<td>$I_{cap,peak,interval}$</td>
<td>Peak value of DC bus capacitor in one interval</td>
</tr>
<tr>
<td>$P_{SW1, cond}$</td>
<td>the current conducting power losses on the main switch</td>
</tr>
<tr>
<td>$V_{clamp}$</td>
<td>Voltage on the active clamp switch</td>
</tr>
<tr>
<td>$I_{CC,peak}$</td>
<td>Peak value of the active clamp switch current</td>
</tr>
<tr>
<td>$I_{CC,rms}$</td>
<td>RMS value of the active clamp switch current</td>
</tr>
<tr>
<td>$t_{dead}$</td>
<td>Dead time</td>
</tr>
<tr>
<td>$R_{ds-on}$</td>
<td>Conducting resistance</td>
</tr>
<tr>
<td>$B_{ac}$</td>
<td>Flux Density</td>
</tr>
<tr>
<td>$R_{pri}$</td>
<td>Conducting resistance of primary winding</td>
</tr>
<tr>
<td>$R_{sec}$</td>
<td>Conducting resistance of secondary winding</td>
</tr>
<tr>
<td>$R_{trd}$</td>
<td>Conducting resistance of tertiary winding</td>
</tr>
<tr>
<td>$I_{Do1},I_{Do2}$</td>
<td>Current of output diodes</td>
</tr>
<tr>
<td>$C_{c}$</td>
<td>Capacitance of Active Clamp Capacitor</td>
</tr>
<tr>
<td>$C_{bus}$</td>
<td>Capacitance of DC Bus Capacitor</td>
</tr>
</tbody>
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Chapter 1

1 Literature review

1.1 Introduction

Power electronics is very closely related to daily life and can be found in many applications, such as in mobile phones, personal computers, and hybrid vehicles. It is the field of electrical engineering that involves the use of semiconductor devices (i.e. switches, diodes, etc.) and other passive elements to convert electrical power from one form to another. The main objective in most applications where power converters are required is to implement converters with as little size, weight, cost, and power losses as possible [1] and with the best performance possible.

The four fundamental power converters are the DC-AC converter, the DC-DC converter, the DC-AC inverter, and the AC-AC converter. The focus of this thesis will be on low-power (< 200 W) AC-DC converters that convert AC voltage taken from the electrical grid into a lower DC voltage that is electrically isolated from the AC grid. Such AC-DC converters are typically two-stage converters: the first stage is an AC-DC converter than converts the input AC voltage into an intermediate DC bus voltage; the second stage is an isolated DC-DC converter that converts the intermediate DC bus voltage into the desired output voltage[2]-[7]. The first stage is typically some sort of boost (step-up) converter that steps the input voltage up and that also shapes the input current so that it is sinusoidal and in phase with the input AC voltage. This helps ensure that a unity power factor is achieved so that the maximum use of power from the input AC supply is achieved; it also minimizes the harmonic content that is injected into the AC grid so that regulatory agency standards on harmonic content are met and the input AC voltage is not corrupted or distorted. The second stage is typically a flyback converter or a forward converter for low power applications. These topologies have a transformer that steps voltage down, in addition to isolating the high-voltage side of the converter, which has high-level AC and DC voltage from the low-voltage side, which has low-level DC voltage, for safety reasons.
Although two-stage AC-DC converters are very popular and widely used, they are implemented with two separate power converters, each with its own controller to regulate its output voltage. Researchers have thus tried to reduce the size and cost of these converter by proposing single-stage converters that use just a single power converter to perform AC-DC power conversion and produce an isolated low-level DC voltage with a near unity power factor. These converters are typically synthesized by combining the AC-DC front-end converter and the DC-DC back-end converter of a two-stage converter then eliminating any redundant components. Since there is only one converter and only the output voltage can be regulated, these converters are implemented with one controller instead of two controllers, which further reduces cost. Although single-stage converters are cheaper and less expensive than two-stage converters, they do not perform as well as they have fewer components and controllers. The choice of whether to use a two-stage or a single-stage approach is ultimately dependent on the application [8]-[12]. Research on single-stage converters has focused on trying to make their performance to be more like that of two-stage converters.

1.2 Fundamental concepts

The following sections of this chapter will provide background on the topics of input power correction and soft-switching methods for converter efficiency enhancement, which are key topics that are related to the work done in this thesis.

1.2.1 Power factor correction

For many years, the simple, passive, diode bridge circuit shown in Figure 1.1(a) was used as the AC-DC front-end converter. The diode bridge takes the input AC voltage and flips the negative portion of it and the capacitor smooths out the result so that the voltage waveform shown in Figure 1.1(b) is obtained. Since the output voltage is generally greater than the absolute value of the input voltage at any instant, the diodes in the diode bridge conduct for only a fraction of the switch cycle, as shown in Figure 1.1(b) This current is not sinusoidal and has many harmonics. It is not considered to be an acceptable current today except in very low power applications (< 75 W) due to the current harmonics it
generates. Regulatory agencies have imposed limits on the harmonics that power supplies, electrical equipment, etc. with AC-DC converter interfaces to the grid can inject onto the grid, given the vast amount of such interfaces that are connected to the grid.

Power factor is a measure of the effectiveness of an AC-DC converter interface in using power supplied by an AC voltage source [1]. Ideally, AC-DC power converters should operate with unity power factor, which means that its input current should be sinusoidal and in phase with the input AC voltage, which ideally is a pure sine wave. The diode bridge rectifier shown in Figure 1.1(b) has a poor power factor and thus alternative converters with better input power factor have been proposed. Most of these converters actively shape the input current so that near unity power factor is achieved; the methods for doing so are called power-factor correction (PFC) in the literature.
Figure 1.1(a) Basic AC-DC full-wave & half-wave converter (b) The wave form of the half-wave and full-wave
One of the most popular power AC-DC converters with input PFC is the AC-DC boost converter shown in Figure 1.2(a). This converter has some similarities with the diode bridge rectifier shown in Figure 1.1(a) except that an inductor, an active switch, and a diode have been added. The converter basically works as follows: When the switch is turned on, the rectified input voltage (voltage at the output of the four-diode bridge) is impressed across the inductor, and the inductor current rises. When the switch is turned off, the current in the inductor falls as the output voltage is greater than the input voltage, given that the converter is a boost converter.

The current in the inductor can either be continuous or discontinuous. For low power applications, discontinuous current mode (DCM) mode of operation is preferred as it is simpler to implement and requires a small inductor. An input current waveform of an AC-DC boost converter operating in DCM is shown in Figure 1.2(b), along with a sinusoidal input AC voltage waveform. It can be seen that the current consists of triangular portions with peaks that are bounded by a sinusoidal envelope. This waveform is essentially a sinusoidal with high frequency current harmonics; these harmonics can be filtered out with an input filter so that the current seen by the AC voltage source is sinusoidal with a small amount of distortion [1],[15]-[16].
Figure 1.2 (a) AC-DC boost converter (b) Waveform of voltage and current in this converter with PFC
1.2.2 Soft Switching Techniques

A power electronic converter with active switches such as the boost converter shown in Figure 1.2(a), the switches are turned on and off in a periodic manner. The length of the switching period or the switching cycle is inversely related to the switching frequency so that it decreases as the switching frequency is increased. Power electronics converters almost always contain energy storage elements such as inductors and capacitors that store and release energy throughout a switching cycle. As the switching frequency is increased, the size of these energy storage elements can be decreased so that the overall converter can be made smaller. Real-life power electronic converters, are not ideal, however, and have various losses such as switching losses. Switching losses are caused by the turning on and off of converter switches so that the higher the switching frequency of the converter, the greater its switching losses will be.

Since switching devices used in power converters cannot turn on and off instantaneously, switching losses are caused by the overlap of switch voltage and switch current during a switching transition, as shown in Figure 1.3. Switching losses, however, can be reduced if either the switch voltage or the switch current is made to be zero during a switching transition. Since power losses during switching transitions are related to the product of switch voltage and switch current during each transition, making either the switch voltage or switch current zero will result in less power being dissipated in the converter switches.

There are, therefore, two general ways of reducing switching losses in power converters; either zero-voltage switching (ZVS) methods are used or zero-current switching (ZCS) methods are used. ZVS and ZCS methods are both considered to be types of soft-switching techniques. The general term “soft-switching” is given to ZVS and ZCS methods as these methods make the switch transitions gradual rather than sudden, which is “hard-switching”. ZVS is the preferred method of soft-switching when MOSFETs are used because they have a parasitic (output) capacitor that prevents a sudden change in voltage. ZCS is often used for IGBTs because the main reason for power loss in an IGBT is a current tail that exists when the device is turning off and that overlaps with the switch voltage to create power losses. ZCS can help eliminate this current tail to reduce turn-off losses. [13]-[16]
Figure 1.3 Soft switching and hard switching [1]

As the converter that is proposed in this thesis operates with ZVS, the general principles of ZVS are explained here. A MOSFET can be considered to be a device with an ideal switch in series with a small on-state resistance, an anti-parallel diode in the body of the device that has its anode at the source of the MOSFET device and its cathode at the drain of the device, and an internal output capacitance. A MOSFET can be turned on with ZVS if current is injected into its anti-parallel body-diode just before it is to be turned on so that the voltage across the device is clamped to almost zero volts when it is turned on. It can be turned off with near ZVS as output capacitance of the device slows down that rate of voltage rise, which reduces the overlap between switch voltage and switch current during a turn-off.

An example of a converter that operates with ZVS is the converter shown in Figure 1.4, which is referred to as an active clamp flyback converter in the literature. The active clamp converter gets its name from the fact that it has a clamping capacitor, C\text{clamp}, that is used to clamp any overvoltage spikes that may occur across the main MOSFET switch, Q1, after it is turned off and from the fact that there is an active switch that is in series with this capacitor, Q2. Both switches can be turned off with ZVS as it is possible for current to flow through the body-diode of each switch before it is turned on. The converter works as follows: At the start of the switching cycle, when the main switch Q2 is on, current flows through the transformer and this switch. When this switch is turned off, given the inductance of the transformer at its primary side, current is forced to flow through the body-
diode of the active clamp switch, so that this switch can be turned on with ZVS. The current in the transformer eventually reverse direction and flows up the transformer primary. Just before the main switch is to be turned on, the active clamp switch is turned off, and current is made to flow through the body-diode of Q2, which allows this switch to be turned on with ZVS. After this switch is turned on, current in the transformer eventually reverses direction and the converter operates in the same way as it did at the start of the switching cycle [19].

![Diagram of a flyback converter with active clamp circuit](image)

**Figure 1.4 Flyback converter with active clamp circuit** [19]

### 1.3 Literature review of low-power single-stage AC-DC converters

A literature review of previously proposed low-power AC-DC single-stage converters that are relevant to the work that has been done in this thesis is performed here [5]-[25]. Since single-stage converters are intended to replace two-stage AC-DC converters in particular applications, especially where cost is an overriding issue, the basic principles of two-stage converters are briefly reviewed in this section before single-stage AC-DC converters are discussed. Single-stage AC-DC flyback converters can be implemented without a DC bus capacitor or with a DC bus capacitor. Both types of converters are reviewed here.
1.3.1 Two-stage AC-DC converter vs single-stage AC-DC converter

A common power electronic application is for an input AC voltage to be converted into a DC output voltage that is isolated from the input voltage. This is typically realized with a two-stage converter structure where a front-end AC-DC converter converts the input AC voltage into an intermediate DC bus voltage and a back-end converter that converts the DC bus voltage into the desired output isolated voltage. The front-end converter is typically a boost converter that performs input power factor correction as explained above in Section 1.2.1, while the back-end converter is an isolated DC-DC converter like a flyback converter. The general structure of a two-stage converter and a two-stage converter with boost front-end and flyback back-end converters are shown in Fig. 1.5.

Two-stage converters are implemented with two separate converters, with each having its own controller so that the output voltage of each converter is regulated. Although two-stage AC-DC converters have excellent performance, the number of components needed to implement these converters and the need for two controllers makes them expensive and large for certain applications. As a result, single-stage converters that can perform AC-DC power conversion and input power factor correction are attractive and thus numerous papers have been written about them. Moreover, these converters are implemented with a single controller so that there is additional cost and size reduction. The main focus of research on single-stage converters has been on lower power converters (< 200 W) given the limitations of these converters. Although they are cheaper and smaller than two-stage converters, the fact that they have fewer components and controllers means that their performance suffers in comparison, but this is less of an issue if the load range is limited.
1.3.2 Single stage AC-DC flyback converter with/without bus capacitor

The converter shown in Figure 1.5 is a very basic single-stage AC-DC flyback converter without a DC bus capacitor. The operation of this converter is very similar to the DCM AC-DC boost converter shown in Figure 1.5 and produces an input current like the one shown in Figure 1.5. When the switch is on, current begins to flow in the primary side of the converter and energy is placed in the transformer. When the switch is turned off, current
stops flowing in the primary side of the converter and the energy that was stored in the transformer is transferred to the output through the secondary diode. The transformer is fully demagnetized so that there is no energy in the transformer when the switch is turned on again.

![Flyback converter without DC bus capacitor](image)

**Figure 1.6 Flyback converter without DC bus capacitor**

This topology is very simple and inexpensive, but has the following drawbacks:

- Since there is no bus capacitor at the primary side of the converter, low frequency harmonics due to the shape of the rectified input voltage will appear at the output. In order to filter out this harmonic so that the output voltage is mostly DC with little AC ripple, the output capacitor must be large. This increases the size of the output capacitor, making it bulkier and large and also slows down the response of the output voltage when the load is changed, which is not acceptable in many applications [30]. The presence of a DC bus capacitor results in less net capacitance in the converter.

- The lack of a DC bus capacitor also means that if the input AC is temporarily lost for even a very brief amount of time, the output DC voltage will sink below its acceptable level. This is not acceptable in many applications, which have “hold-up time” requirements where hold-up time is defined as the length of time that the converter can maintain its output DC when the AC input voltage is missing. If there is no DC bus
capacitor, then the output capacitor must be large, which creates the same problems that are mentioned above.

1.3.3 Single stage AC-DC flyback converter with dc bus capacitor

The first single-stage AC-DC flyback converter with a DC bus capacitor was proposed in paper [19] and is shown in Figure 1.6. This topology has an input section that is like the AC-DC boost converter shown in Figure 1.2(a), but has a flyback converter as its output section. The converter operates as follows: When the switch is turned on, the current in the inductor L_{in} rises and voltage from the DC bus capacitor C_{bus} is impressed across the primary of the transformer. Energy is stored in the transformer when the switch is on. When the switch is turned off, the current in L_{in} flows into the DC bus capacitor C_{bus} instead of the switch and it falls as this voltage is higher than the input voltage, given that the input section of the converter is a boost converter. Energy that was previously stored in the transformer is transferred to the output after the switch is turned off.

The following should be noted about the operation of the converter:

- An input current like the one shown in Figure 1.2(b) can be produced by the converter simply by keeping the converter’s duty cycle fixed throughout the input line cycle. Duty-cycle is the ratio of switch on-time to the duration of the switching cycle.
- The DC bus capacitor filters out the harmonics caused by the rectified input voltage (voltage at the output of the four-diode bridge and provides hold-up time, thus correcting the drawbacks of the single-stage AC-DC flyback converter shown in Figure 1.6 without requiring a large output capacitor.
- Including the DC bus capacitor in the converter, however, introduces a new problem and that is that the DC voltage of this capacitor can be very high, in some cases, as much as 1000 V. Unlike two-stage AC-DC converters where the output of the front-end AC-DC converter can be regulated because it has its own controller, single-stage converters operate with just a single controller that is used to maintain the output voltage at a fixed level. This means that the DC bus capacitor voltage is
uncontrolled and thus floating. This increases the voltage stress that the converter components must handle, which, in turn, increase converter costs as more expensive components that can handle this stress are required.

![AC-DC flyback converter with DC bus capacitor](image)

**Figure 1.7 AC-DC flyback converter with DC bus capacitor**

Ultimately, the DC bus voltage is dependent on the energy equilibrium that exists at the DC bus capacitor. Under steady-state operating conditions, the amount of energy that is placed in this capacitor over an input line cycle must equal to amount of energy that is removed from the capacitor. Otherwise, the DC bus voltage will keep on rising or keep on falling and the converter will not be able to produce the desired output voltage. If the load or the input voltage is changed, the DC bus capacitor is subjected to a new energy equilibrium and its voltage is either higher or lower than the original voltage, before the change.

A new energy equilibrium that can produce a lower DC bus voltage can be achieved if one of the following actions is taken:

- **Increasing the inductance of the input inductor**: Taking this action results in less energy being stored in the inductor when the switch is on, which then results in less energy being transferred to the DC bus capacitor after the switch is turned off. With less energy being transferred to the DC bus capacitor during a switching cycle, a new energy equilibrium that results in a lower DC bus voltage can be achieved, but increasing the input inductor makes it less likely that its current will fall to zero after the switch is turned off. What this means is that instead of the input current
being like the waveform shown in Figure 1.2(a), it will be more like the semi-continuous waveform shown in Figure 1.7. This may lead to the input current being distorted to an extent that the input power factor is too low to be acceptable.

- **Decreasing the turns ratio of the transformer** \( n = \frac{N_1}{N_2} \). What this action does is that it allows more current to be available in the converter’s primary side to discharge the DC bus capacitor, which will then allow the DC bus voltage to decrease. This method, however, has several disadvantages including increased conduction losses due to increased current and increased current stress on the components and switches.

- **Decreasing the magnetizing inductance of the transformer**: What this action does is to increase the current in the converter’s primary side that is available to discharge the DC bus capacitor. This action has similar drawbacks to decreasing the transformer turns ratio as it increases the primary-side current [21].

**Figure 1.8 Waveform of semi-continuous current mode [1]**

1.3.4 **AC-DC boost converter with a counter-voltage**

The problems with the single-stage AC-DC converter with DC bus capacitor can be resolved if the topology is modified as shown in Figure 1.8. In this topology, a tertiary winding taken from the transformer is placed between the switch and the input inductor. What this winding does is to impress a counter-voltage between at the right-hand end of
the inductor when the switch is turned on so that the full input voltage is not placed across the inductor, but only a fraction of it. This results in less energy being placed in the input inductor when the switch is turned on and thus a lower DC bus voltage. The turns ratio of the tertiary winding with respect to the primary winding can be adjusted as desired.

![Diagram of the off-line flyback converter]

**Figure 1.9 Off-line flyback converter with input harmonic current correction [27]**

Although this method can reduce the DC bus voltage, which leads to lower component stress without increasing primary current stresses, it does introduce input current distortion, as shown in Figure 1.9. This distortion can explained by the fact that there will always be voltage at the right-hand side of the inductor even if the input AC voltage is very low so that there will be regions close to the zero-crossings of the input AC voltage when the input voltage is less than the voltage on the right-hand side of the inductor. Since the converter is made to operate in DCM, this means that the diodes of the input diode bridge are reverse-biased so that they do not conduct and thus there is no input current. It should be noted that although the input current is distorted, the power factor of the converter is better than if the input inductor was increased to produce the semi-continuous waveform shown in Figure 1.7. The harmonic content produced by the current shown in Figure 1.9 is considered to be just acceptable to meet regulatory agency standards for low power applications [27].
Figure 1.10 PFC with adjustable tertiary windings (filtered current)

Most AC-DC single-stage converters that have been proposed during the past 20 years can be considered to be variations of the converter shown in Figure 1.8, in principle. Examples of such converters are shown in Figure 1.10. Although these converters may look significantly different than the converter shown in Figure 1.8 and may have better characteristics and performance in many cases, they all use some method to produce a counter-voltage that reduces the amount of voltage that is placed across the input inductor when the switch is on, thus reducing the DC bus capacitor voltage to an acceptable level. All of these converters, however, produce a distorted input current that, although accepted, results in less than unity input power factor.
Figure 1.11 Variations of single stage AC-DC converter with input harmonic current correction [10]
1.3.5 Stacked single-stage ac-dc converter topology

To summarize the discussion on low-power single-stage AC-DC converters thus far: Single-stage AC-DC converters with a DC bus capacitor that is used to filter out low frequency harmonics from the rectified input voltage and to provide hold-up time in case of a temporary removal of the input AC voltage can have a very high DC bus voltage. This is because these converters are typically implemented with a single controller that is used to maintain the output DC voltage at a fixed level and thus the DC bus voltage is left floating.

There are several ways by which this DC bus voltage can be reduced, with the most popular being to somehow prevent the full rectified input voltage from being impressed across the input inductor when the converter switch is on. This results in less energy being placed in the inductor when the switch is on and less energy transferred to the capacitor when the switch is turned off. Since the DC bus voltage is dependent on an energy equilibrium at the DC bus capacitor – the energy stored in this capacitor during an input line cycle must equal the energy that is removed from this capacitor during the same input cycle – the DC bus voltage will reduce so that a more favorable energy equilibrium is established. The reduced DC bus voltage means that component stresses can be reduced so that cheaper and smaller sized components (e.g. the DC bus capacitor) can be used. The main drawback with this method is that the input current must be distorted, which makes the input power less than unity, although still at an acceptable level. An inverse relation exists between input power factor and DC bus voltage.

One approach that seeks to overcome this issue was proposed in paper [39] and is shown in Figure 1.11. What is shown in Figure 1.11 is a stacked converter structure where two single-stage AC flyback converters are stacked one on top of the other. What this does is to reduce the peak voltage stress of the components by half. With this reduction in component stress, it becomes possible to lessen the distortion of the input current so that power factor can be improved. Details of the operation of this converter are presented in Chapter 2 of this thesis.

The following about the converter should be noted:
• The stacked topology also has an active clamp auxiliary circuit across two transformers. With the active clamp circuit, all three switches can work with ZVS, which results in an increase in efficiency increase due to the reduction of switching losses.
• The two switches have a 180° phase shift between them and the active clamp switch has to be turned on before the main switch is turned on.
• Since the converter consists of two single-stage modules, it can be operated at twice the power of one of the single-stage modules. This means that the input current will be higher and the peak of the current, which is a train of triangular pulses, will also be higher as well, which places stress on the converter components.

Figure 1.12 Stacked flyback converter

1.3.6 Interleaved converters

Low-power single-stage AC-DC converters work in DCM mode with a fixed duty-cycle over the input line cycle in order to achieve a near unity power factor. Even if a countervoltage is introduced to reduce the DC bus voltage that may cause the input current to be
distorted, the converter is still operated in DCM mode with a fixed duty-cycle over the input line cycle. This makes the input current have relatively high current peaks, which may be acceptable for low power applications, but become less so for higher power levels. If converters with inductors in their topologies are paralleled, however, then it may be possible to reduce this stress by using interleaving.

The principle of interleaving is shown in Figure 1.12(a) for two boost converter modules; key converter waveforms are shown in Figure 1.12(b). If the current through each inductor is discontinuous, as shown in Figure 1.12(b) and the gating signals used to turn on the switches are shifted by 180° with respect to each other, then the output current fed to the load, which is the sum of the two inductor currents, becomes continuous with less ripple and less peak current. This reduces the required size of the output filter capacitor.
Figure 1.13(a) Basic interleaving DC-DC converter with two interleaved branches
(b) Waveform of interleaving converter
Single-stage AC-DC converters can also be interleaved, as shown in Figure 1.13. In the converter shown in this figure, two single-stage AC converter modules – each module being the same as the one shown in Figure 1.13 – are placed in parallel and are made to operate with DCM. Each converter switch has the same gating signal with the same duty-cycle, but phase-shifted by $180^\circ$ with respect to each other so that the net input current has reduced ripple. When trying to operate a single-stage AC-DC converter with interleaving is that the duty-cycle of the converter D must be greater than 0.5. If it is not greater than 0.5, then there will be very little overlap between the two input inductor currents and thus very little interleaving will occur. The input current, which is the sum of the two input inductor currents, will be like the DCM input current waveform shown in Figure 1.2(b). Given that there are two single-stage AC-DC modules and that the overall power of the converter is twice that of each module, what is an acceptable level of peak input current for a single module, becomes less so for two modules.

![Figure 1.14 Interleaved single-stage AC-DC boost-flyback converter [24]](image)

Operating each module with $D > 0.5$ means that the peak voltage stress of the two converter switches is high. In a flyback converter, the transformer must have no net volt-seconds impressed across it if it is not to saturate, which would create a short-circuit in the converter and result in a catastrophic failure. The number of volt-seconds (product of the amount of voltage applied across the flyback transformer and the length of time that is applied) must
be such that positive volt-seconds and negative volt-seconds match. A duty-cycle of $D > 0.5$ means that more negative voltage is needed to reset the transformer than the positive voltage that was impressed on it. For example, a duty-cycle of $D = 0.75$ means that the negative voltage that is impressed across the transformer must be at least three times the voltage impressed across the transformer when the switch is on. Since the voltage impressed across the transformer in a single-stage AC-DC converter is the DC bus capacitor voltage and since this voltage can be high, there have been few examples prove this phenomenon, in the paper [24], the proposed converter is a series input parallel output interleaved flyback converter, and the voltage stress on the switch is higher based on the mathematical analysis.

1.4 Thesis objectives

It is possible, in theory, to operate the single-stage stacked converter shown in Figure 1.11 with interleaving as it is made up of two single-stage AC-DC modules with its input branches placed in parallel. Operating the stacked converter with interleaving is advantageous because

- The voltage stress of the converter components is lower by a factor of two when a stacked structure is used as opposed to a non-stacked structure. This allows greater flexibility in the design of the converter and less expensive converter components to be used.

- In a two-module interleaved non-stacked structure, four switches must be used if the converter is based on flyback converter modules that operate with ZVS: two switches are needed for the main flyback switches and two switches are needed to help these switch turn on with ZVS. In the stacked structure, only three, lower cost, switches are needed: two switches for the main flyback switches and just one switch to help the main switches turn on with ZVS. This results in further cost savings.
It should be noted that the stacked converter is considerably less expensive than interleaving two, two-stage converters as doing so involves the implementation of four converters: two front-end AC-DC converters and two back-end DC-DC converters.

If the two converter switches are operated with a 180° phase-shift with respect to each other, then interleaving becomes possible if the duty-cycle D is greater than 0.5. Since the stacked structure ensures that the converter components will have half of the peak voltage stresses that an equivalent single single-stage module would if operated under the same conditions, then increase in peak voltage stress that interleaving with D > 0.5 would bring can be offset by the halving of the DC bus voltage. Operating the stacked converter shown in Figure 1.11 in the manner has never been done before and thus the main objective of this thesis is to investigate how this converter can be made to operate with the interleaving of its two branches so that it becomes possible to operate a single-stage converter with interleaving without excessive stress.

The thesis has the following objectives:

- To proposed the use of interleaving in the stacked single-stage converter shown in Figure 1.12, which has never been done previously.
- To perform a mathematical analysis of this converter when it is operating with interleaving so that key steady-state characteristics of this converter can be determined.
- To establish a procedure for the design of the converter and to use this procedure in an example design.
- To confirm the feasibility of the stacked converter when operating with interleaving by using simulation tools like PSIM, a commercially available power electronic circuit simulator.

It should be noted that the stacked converter that is studied in this thesis has been implemented with two modules of a particular single-stage AC-DC flyback converter. This converter was chosen to be the converter used in the stacked converter as it is the simplest type of AC-DC single-stage flyback converter. The stacked converter can be implemented with more sophisticated and more expensive AC-DC single-stage flyback converter
modules to improve performance. Given that the main focus of this thesis is the interleaved operation of the stacked converter modules, this was not done in order to simplify the work.

1.5 Thesis outline

This thesis contains six chapters.

- Chapter 1 presented fundamental power electronic concepts that were relevant to the work that was done in this thesis, reviewed the literature that is related to low-power single-stage AC-DC converters, and stated the thesis objectives, which are related to the introduction of interleaving to a stacked single-stage AC-DC flyback converter.
- Chapter 2 will explain the operation of the stacked flyback converter. The modes of operation that the converter goes through during a switching cycle will be explained in detail.
- Chapter 3 will focus on the analysis of the steady-state characteristics of the converter. This analysis will provide the basis for component selection. Important considerations and parameters will be explained in detail.
- Chapter 4 will present equations that can be used to determine key converter component stresses and losses.
- Chapter 5 will present simulation results obtained from PSIM, a commercially available power electronic circuit software package, that confirm the feasibility of the interleaved stacked single-stage AC-DC converter.
- Chapter 6 will summarize the main points of the thesis, present the contributions of the thesis to the power electronics literature, and provide suggestions for future work.
Chapter 2

2 Modes of operation

2.1 Introduction

The operation of the stacked single-stage AC-DC flyback converter that is used in this work is explained in detail in this chapter.

2.2 Basic concept of the proposed converter

Figure 2.1 shows the proposed converter, which includes two flyback converter, and one stacked on the other one. The front end is a typical AC-DC boost converter with a two terminals Input Current Shape, providing the power factor correction functions. There are two sets of diodes, input inductors, and tertiary windings. With phase shift control of the two main switches, the two sets of components can help the converter achieve interleaving at the front end.

![Figure 2.1 Proposed converter](image-url)
Above and below the DC bus capacitors, there is the stacked section with an active clamp auxiliary circuit. Because of the existing of leakage inductance, and the active clamp circuit, all three switches can work with Zero Voltage Switching during turn-on operation. Transformer can move the energy from the primary side to the output side. One transformer is stacked on the other one, and the output side is connected in parallel.

As discussed in Chapter 1, the tertiary winding can apply a counter voltage to the right side of the input inductor which will eliminate the voltage on the right side of the inductor. Current would rise when switch is on and fall when switch is off. To cancel the DC bus voltage, the turns-ratio of the tertiary winding and the primary winding should be 2:1, because of the stacked structure, DC bus voltage twice higher than the voltage stress on one primary side. The input current will be enveloped by the sinusoidal voltage waveform. By changing the turns-ratio, the power factor can be changed as a zero current interval exists in two cycles, and the DC bus voltage will be reduced with lower power factor.

A PWM gating signal is used to control the proposed converter. This proposed converter can be used with the low and high input (110V<sub>rms</sub> and 220V<sub>rms</sub>) and can work with an interleaved input current. The duty cycle can go beyond 0.5, and can reach a duty cycle of 0.75 in low input voltage situations, achieving interleaving. The main features of this converter will be covered in the following sections.

### 2.2.1 Modes of operations

The modes of operation of the converter in Figure 2.1 are discussed in this section. The key information presented is how to working with ZVS with the help of active clamp circuit. The waveforms for the mainly components will be displayed to aid in describing the converter operation.
At different duty cycles, the basic mode of operation is the same. Although, at duty cycle’s less than 50%, the interleaved phenomenon does not exist. This situation often occurs at low input voltage. In the following discussion, the modes of operation will be discussed with and without interleaving.
Modes of operation with interleaving:

Mode 0 \((t_0 < t < t_1)\)

The main switches S1 and S2 are both on, and S3 is off. Current will continue rising in Lin1 and Lin2. The current in Lin1 and Lin2 flows through S1 and S2 to the transformer T1 and T2 separately.

Mode 1 \((t_1 < t < t_2)\)

The main switch S1 remains on, S2 is turned off, and S3 is off. The S1 current doesn’t change, but there is negative current flow through the body diode of S3 and through S1. In
this state, turning on the active clamp switch with ZVS would let the energy flow through transformer to the output side.

Mode 2 \((t_2 < t < t_3)\)

The main switch \(S_1\) is on, \(S_3\) is turned on with ZVS, and \(S_2\) is off. The current in \(S_1\) is equal to the sum of the active clamp circulating current and the regular \(S_1\) current. The active clamp capacitor \(C_c\) is charging.

Mode 3 \((t_3 < t < t_4)\)

The main switch \(S_1\) is on, \(S_2\) is off, and \(S_3\) is off. The current in \(S_1\) continues without change, and the charged capacitor \(C_c\) drives a small current back through the parasitic diode of \(S_2\). Now the voltage stress is close to 0 and \(S_2\) can be turned on with ZVS

Mode 4 \((t_4 < t < t_5)\)

The main switch \(S_1\) is on, \(S_2\) is on, and \(S_3\) is OFF. The current in \(\text{Lin}_1\) and \(\text{Lin}_2\) continues to rise. The current in \(\text{Lin}_1\) and \(\text{Lin}_2\) flows through \(S_1\) and \(S_2\) to transformers \(T_1\) and \(T_2\) separately.

Mode 5 \((t_5 < t < t_6)\)

The main switch \(S_2\) remains on, \(S_1\) is off, \(S_3\) remains off. \(S_2\) remains on, and the current doesn’t change, but there is negative current flow from the DC bus capacitor \(C_2\) to the body diode of \(S_3\) which goes through \(S_2\). In this state, turning on the active clamp switch with ZVS would let the energy flow through transformer to the output side.

Mode 6 \((t_6 < t < t_7)\)

The main switch \(S_2\) is on, \(S_3\) can be turn on with ZVS in the last step, and \(S_1\) is off. The current in \(S_2\) is equal to the combination of the active clamp circulating current and the regular \(S_2\) current. The active clamp capacitor is charging.

Mode 7 \((t_7 < t < t_8)\)
The main switch S2 is on, S1 is off, and S3 is turned off. Current in S1 continues without change, and the charged capacitor Cc drives a small current back through the body diode of S1. Now S1 can be turned on with ZVS.
Modes of operation without interleaving:

Mode 0 ($t_0 < t < t_1$)

The Interleaving phenomenon doesn’t exist anymore as the duty cycle drop below 0.5. For now, the S1 is on and S2 is off, the principle is basically very similar to the modes of operation with interleaving. The auxiliary winding cancels the voltage and so the energy will flow into T1 through the upper branch, and the energy in T2 will be flow through transformer2 to the output side.

Mode 1 ($t_1 < t < t_2$)
S1 is turned off, and none of the main switches is on, so the only path for the current is flow back through body diode of the active clamp switch because of the negative voltage across it. This step can realize the ZVS for the active clamp switch S3

Mode 2 ($t_2 < t < t_3$)

In this mode, the S3 can be turned on with ZVS as the current pass through its parasitic diode in the last mode, the two primary sides of two transformer provide paths for current, and the current would flow through the leakage inductance and also the primary windings.

Mode 3 ($t_3 < t < t_4$)

In this mode, after turning of the S3, the primary side current and the leakage inductance has to go to somewhere, and the only path now is flowing through the parasitic diodes of two main switches, the two main switches both can be turn on with ZVS.

Mode 4 ($t_4 < t < t_5$)

In this mode, the S2 is on with ZVS after the current flow through the body diode, and S1 is off, the auxiliary winding cancels the voltage and so the energy will flow into T2 through the upper branch, and the energy in T1 will be flow through transformer 1 to the output side.

Mode 5 ($t_5 < t < t_6$)

S2 is turned off, each main switch is off, so the only path for the current is flow back through body diode of the active clamp switch because of the negative voltage across it. This step can realize the ZVS for the active clamp switch S3

Mode 6 ($t_6 < t < t_7$)

In this mode, the S3 can be turned on with ZVS as the current pass through its parasitic diode in the last mode, the two primary sides of two transformer provide paths for current, and the current would flow through the leakage inductance and also the primary windings.

Mode 7 ($t_7 < t < t_8$)
In this mode, after turning off the S3, the primary side current and the leakage inductance has to go to somewhere, and the only path now is flowing through the parasitic diodes of two main switches, the two main switches both can be turn on with ZVS.

### 2.2.2 Basic features about proposed topology

- Compared to the traditional parallel and single stage AC-DC flyback converter; the stacked structure of the proposed converter means only half of the voltage stress appears across the DC bus capacitor.
- All three switches in the topology can work with the ZVS turn on technique. This dramatically reduces the switching power loss and increases the final efficiency for this converter.
- The tertiary windings are introduced to apply a counter voltage and allow the input current rises in the input inductor while the corresponding switch is turned on. By changing the turn-ratio, the power factor can be changed as the input current shape changes. This will further reduce the DC bus voltage.
- When the duty cycle is larger than 50%, interleaving can be achieved. The current in the two inductors will be 180o out of phase, thus the current ripple of the output can be reduced.
- As the duty cycle can exceed 0.5, this topology can be used for the 110V\textsubscript{rms} and 220V\textsubscript{rms} input voltage. With a lower input voltage, the duty cycle is higher and thus interleaving can be achieved.

### 2.3 Conclusion

The modes of operation of the stacked AC-DC single-stage converter that is used in this work are presented in this chapter. For this converter, the duty cycle can be greater than or less than 0.5. When the duty cycle is greater than 0.5, current in Lin1 and Lin2 can be interleaved and the input current will be reduced. When the duty cycle is less than 0.5, there will be no interleaving. The duty cycle is maximized under the low-input full-load situation. In this situation, interleaving will help to reduce input and output current ripple thus reducing current related component stresses.
Chapter 3

3 Circuit analysis

3.1 Introduction

An analysis of the steady-state operation of the stacked single-stage AC-DC converter is performed in this chapter of the thesis. The mathematical analysis presented in this chapter develops equations to describe the current and voltage in key components such as the inductor, transformers, and switches.

3.2 Energy equilibrium in steady state

The analysis performed in this chapter is based on the principle of energy equilibrium at the DC bus – the energy flowing into the DC bus capacitors during an AC line cycle must be equal to the energy flowing out of the DC bus capacitor during the same line cycle in order for the converter to operate in steady-state. In order to simplify the analysis, it is assumed that the voltage across the diodes and the current conduction losses are negligible.

The energy that flows from the AC source into the DC bus can be represented by the input inductor current. Based on previous discussion, the input current has a sinusoidal shape and follows the phase of the input voltage. The current flows into the DC bus when the switch is on. To determine the energy equilibrium, the first step is to determine an equation for the input current.

3.2.1 Mathematical equation analysis

Based on the modes of operation and the circuit topology, Modes 1 - 4 and Modes 5 – 8 are symmetrical, and the current waveform is the same in the two transformers; thus, only half the modes of operation need to be analyzed.

Based on the characteristics of the transformer, the bus voltage can be expressed as:

\[ V_{bus} = \frac{2V_o(1-D)}{DN} \text{ (CCM)} \] or \[ V_{bus} = \frac{2V_o}{D} \sqrt{\frac{2L_{msf}}{R}} \text{ (DCM)} \]
DCM is assumed for the analysis as the converter must work in DCM to ensure that the converter operates with a very good power factor.

The upper and lower flyback converters in the stacked structure work identically, except the gating signals of the switches are phase-shifted with respect to the other. Analysis on the upper and lower flyback converter can be conducted separately.

For a flyback converter, the input current can be determined by the value of the input inductance and the input voltage. Energy flows from the AC source into the input inductance and then into the DC bus. For one input inductor, the DCM current waveform is shown in Figure 3.1.

\[
V_s
\]

\[
I_s
\]

**Figure 3.1 The discontinuous current mode**

For a small interval, the current wave can be assumed to be a triangular wave with a current of

\[
I_{Lin,peak, interval} = dI_{Lin} = \frac{V_{rec,k}}{L_{in}} \times \frac{D}{f_{sw}}
\]

(3 - 1)

The total current in one small interval is
\[ I_{L,in,\text{rise}} = \frac{V_{\text{rec},k}D^2}{L_{\text{in}}f_{\text{sw}}^2} \quad (3 - 2) \]

By summing the current in one switch cycle, the average value of the input current from one input inductor into the DC bus in one AC cycle can be determined:

\[ I_{\text{bus}} = f_{ac} \sum_{k=0}^{n} \frac{V_{\text{rec},k}D^2}{L_{\text{in}}f_{\text{sw}}^2} \quad (3 - 3) \]

where:  
- \( f_{ac} \) – frequency of AC source from the grid (usually 50 – 60 Hz)  
- \( k \) – kth interval in AC frequency

\[ n = \frac{f_{ac}}{f_{\text{sw}}} \]

\[ V_{\text{rec},k} = \left| V_{\text{peak}} \sin \left( \frac{2\pi k}{n} \right) \right| \quad (3 - 4) \]

For mode 0:
Figure 3.2 Mode 0 of operation

In mode 0, the two main switches are on and current flows into the DC bus through the two input inductors. For either input inductor, the current is:

$$I_{Lin, interval}(t) = \frac{|V_{interval}(t)|t}{L_{in}}$$  \hspace{1cm} (3 - 5)

where: $V_{interval}(t)$ – instantaneous voltage on the input inductor

$t$ – time period of one switching cycle

Although the AC input voltage changes slightly during the short-time interval, the change is negligible as the switching cycle is much shorter than the line cycle. $t$ represents the time length of cycle and is

$$t = \frac{D}{2f_{sw}}$$  \hspace{1cm} (3 - 6)

For Mode 1:
Switch Q2 is off and the voltage across the active clamp capacitor will drive a small current back to the source. This small current will not actually change the current direction in the switch Q1, so the energy in the input inductor Lin1 can flow into the DC bus. The voltage stress on the active clamp capacitor can be determined to be

$$\frac{V_{bus}}{2} + (L_{lk} + L_m) \frac{di}{dt} = V_{clamp}$$

For Mode 2:
In Mode 2, Q3 is turned on with ZVS and the current flows through Q3. This current charge the active clamp capacitor and the body capacitor of switch Q3. During this mode,

\[ V_{\text{clamp}} = (L_{ik1} + L_{m1} + L_{ik2} + L_{m2}) \frac{di}{dt} \]  \hspace{1cm} (1. - 6)

For Mode 3:

In this mode, Q3 is off, so Q2 can be turned on with ZVS. Afterwards, the converter enters to Mode 4.
3.2.2 Energy equilibrium and duty cycle determination

To quantify the energy flow into the DC bus and also the energy in the secondary side, the average current of the bus current is the key parameter that must be determined. In an AC cycle, there will be n switching cycles (n=fsw/fac), during one switching cycle and energy will flow through one inductor and into the DC bus. This energy can be represented by the average current of the bus current. For a steady average current, the necessary process is to determine the value over a complete AC cycle. This can be done with a computer program that uses the equations that are developed in this chapter. The flow chart of this program is shown in the flowchart below.
Figure 3.6 Flowchart of duty cycle determination
In this procedure,

\[ I_{bus, out} = \frac{2P_{out}}{V_{bus}} \]  

(3 - 7)

\[ I_{bus, in} = f_{ac} \sum_{k=0}^{n} V_{rec,k} D^2 \frac{L_{in} f_{sw}^2}{L_{in}} \]  

(3 - 8)

If the values of the bus-in value and the bus-out value are very close to each other (less than 0.1 A difference), the duty cycle D can be selected as the correct value. If not, the whole procedure is repeated with a different value of D.

### 3.3 Design curve

With the help of the flowchart in Section 3.2.2 and MATLAB software, different duty cycle values with different combinations of components values were generated. By changing the input voltage, the total power, the value of the input inductance, and the value of the magnetizing inductance, the relationship among these values can be determined through design curves that can be used to select component values for the converter. The following component values are the most critical ones:

- Value of Input Inductor, \( L_{in} \)
- Value of Magnetizing Inductance, \( L_m \)
- Value of Leakage Inductance, \( L_{leak} \)
- Value of Turns Ratio, \( N \)

For this converter, the stacked structure is formed using two identical flyback converters. This means the values of the parameters in each converter should be equal. With this assumption, the two stacked converters should generate the same waveforms on the secondary side.

#### 3.3.1 The impact of input inductor on duty cycle and DC bus voltage

Figure 3.7 illustrates the impact from the input inductor change on the duty cycle under different output voltages. The horizontal axis is the DC bus voltage and the vertical axis
represents the output power. The power range is from 40 watts to 400 watts which matches the range of the horizontal axis of all design curves. To draw the lines which show the impact of one parameter on another, the other non-related parameters must be held constant. Thus, the switching frequency $f_{sw}$ is 50 kHz, the input voltage is 110V, and the output voltage $V_{out}$ is 48V.

In this figure, the voltage of the DC bus increases as the power decreases. With higher input inductance, the voltage will be lower. As seen in the trend of the curve, with increasing power, the DC bus voltage remains stable around 300 V.

Figure 3.7 DC bus voltage changes along the input inductor ($L_m=300\mu H$, $V_{in}=110V$)

In the following figure 3.8, the effect of the input inductor on the duty cycle is demonstrated. Since the purpose of the proposed converter is to maintain the interleaving phenomenon when the input voltage is 110 volts, the input inductor must ensure a duty cycle range between 0.25 and 0.75. This allows the interleaving phenomenon to occur which reduces the output current ripple.
According to the figure, the increase the inductance of input inductor can make the duty cycle increase and the interleaving phenomenon occur. Although to guarantee the input current stays in discontinuous mode, the value of input inductor cannot be too large.

3.3.2 The impact of magnetizing inductance on the duty cycle and DC bus voltages.

Figure 3.9 displays the impact from changing the magnetizing inductance of the transformer. It is clear that with an increase in the magnetizing inductance, the duty cycle will drop, and the interleaving phenomenon will be lost. This indicates the magnetizing inductance cannot be too high to ensure that interleaving occurs.
Figure 3.9 Duty cycle changes along the magnetizing inductor \((L_{\text{in}}=110\mu\text{H}, \ V_{\text{in}}=110\text{V})\)

As shown in figure 3.9, as the magnetizing inductance decreases, the DC bus voltage goes up which lead to a size and cost of the capacitor. There must be a compromise in the design of the transformer. Magnetizing inductance cannot be too high to lose the high duty cycle, but also cannot be too low to increase the voltage stress.
In conclusion, neither the input inductance nor the magnetizing inductance can be too high or too low, because there is a tradeoff between the DC bus voltage and the duty cycle (or interleaving phenomenon). For the inductance value, the key consideration is to ensure a low DC bus voltage and interleaving operation.

### 3.4 Conclusion

This chapter analyzes the design procedure and the method to determine proper values for the components using existing requirements. Based on Chapter 2, the working procedure of the proposed AC-DC stacked flyback converter was used to set up the energy equilibrium. Energy equilibrium means the total power should not change when it is transferred in the converter under the ideal situation (assume there is no power loss). Mathematical equations were used to describe the current and voltage in each of the steps, and with the help of the flow chart, the equations were used to construct the energy equilibrium. This provided the basis for the analysis and curve drawing.

The flow chart in Section 3.2 started by picking an arbitrary duty cycle D to test whether the energy equilibrium was satisfied. The input current was tested at the same time to ensure discontinues current mode. If the chosen duty cycle D satisfied both conditions, the

![DC Bus Voltage changes along the Magnetizing Inductance with Different Output Power](image)

**Figure 3.10 DC bus voltage changes along the magnetizing inductance ($L_{in}=110\,\mu H$, $V_{in}=110V$)**
duty cycle value was recorded. With the help of MATLAB, the procedure for finding the right duty cycle can be repeated many times, with different input power.

The design curve in Section 3.3 displayed the trends for duty cycle and DC bus voltage when changing the values of components and power values. With the design curve, the values for the input inductor and magnetizing inductance can be determined.
Chapter 4

4 Loss analysis & stress analysis

In this chapter, the losses and stresses of key converter components are determined. These calculations will help in the design of the converter.

4.1 Introduction

High frequency power converters offer higher switching frequencies that reduce the size of the whole converter. Although, as the frequency increases, the switching and conduction losses of the switches are no longer negligible. The soft switching techniques mentioned previously have been implemented in this proposed circuit, which reduces the power loss from the switches. Although, current passing through the components results in some conduction losses due to resistance. The switching conducting losses is the main part which affects the converter efficiency. The conducting losses must also be calculated using the resistance in the components and the current rate for the corresponding mode.

4.2 Power loss calculation

Based on the previous work, the bus voltage in the is:

\[ V_{bus} = \frac{2V_o}{D} \sqrt{\frac{2Lmf_{sw}}{R}} (DCM) \text{or} V_{bus} = \frac{2V_o(1 - D)}{DN} \]  

(4 – 1)

Where: N - turns ratio, R - output resistance [25]

4.2.1 Conducting losses on switches

The two main switches (S1 and S2) function identically, thus only S1 and active clamp switch (S3) need to be analyzed. S2 will have the same losses as S1 for the calculation of total loss.
4.2.1.1 Conducting loss on main switches:

When the switch S1 is turned on, the current from the input inductor and the bus capacitor Cbus1 will flow through S1, so the current through S1 is equal to the sum of two components:

$$I_{s1} = I_{Lin} + I_{Cbus1}$$  \hspace{1cm} (4-2)

For the inductor current, there is a rising part and a falling part for each switching cycle. Only the rising part will go to the DC bus. Based on the analysis and the specifications of the inductor, an equation can be determined to describe the rising and falling part of the current.

In the following calculation, k represents the kth switching cycle in one AC cycle, and n is equal to the switching frequency over the AC source frequency

$$\frac{dI_{Lin}}{dt} = \begin{cases} \frac{V_{rec}}{L_{in}} & (0 < t < t_{rise}) \\ \frac{V_{bus} - V_{rec}}{L_{in}} & (t_{rise} < t < t_{fall}) \\ 0 & (t_{fall} < t < T) \end{cases}$$  \hspace{1cm} (4-3)

Where the $t_{rise} = DT$, $t_{fall} = (1 - D)T - t_{dead}$, $V_{rec} = V_{in,peak} \sin \left(\frac{2\pi k}{n}\right)$

For $0 < t < t_{rise}$:

$$I_{Lin,peak,interval} = dI_{Lin} = \frac{V_{rec}}{L_{in}} \times \frac{D}{f_{sw}}$$  \hspace{1cm} (4-4)

For a single switching cycle, the rising portion can be treated as a triangle wave,

$$I_{Lin,rms,interval} = \frac{V_{rec}}{L_{in}} \times \frac{D}{f_{sw}} \times \sqrt{\frac{2}{3}} = \frac{V_{rec}D\sqrt{3}}{L_{in}f_{sw}\sqrt{3}}$$  \hspace{1cm} (4-5)

For an AC cycle, the interval is summed and the RMS value of inductor current is
\[
I_{Lin,rms} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} I_{rms, interval}^2} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} \left( \frac{V_{rec}D\sqrt{D}}{L_{in}f_{sw}\sqrt{3}} \right)^2}
\]  

(4 - 6)

To determine the current of the bus capacitor, the energy equilibrium where flow-in energy equals flow-out voltage is used. With this analysis:

\[
E_{bus-out} = E_{bus-in}
\]

(4 - 7)

For the upper bus capacitor, there are two times each period when the power flows into the bus capacitor. The first is after the upper main switch turns off (mode 2) and the input inductor current is falling to zero; the only path the current can flow through is the upper bus capacitor. The second is during the switching cycle of the lower main switch. During this period, current will flow into the DC bus capacitor as well. All the flow-in energy will be released when the upper switch is on.

According to the analysis above, to determine the peak value of the bus capacitor current.

\[
I_{cap, peak} \Delta T_{sw1,ON} = I_{Lin, peak} \Delta T_{sw1,OFF} + I_{Lin, peak} \Delta T_{sw2,ON} + I_{Lin, peak} \Delta T_{sw2,OFF}
\]

(4 - 8)

\[
\Delta T_{sw1,ON} = \Delta T_{sw2,ON} = \frac{D}{f_{sw}}
\]

\[
\Delta T_{sw1,OFF} = \Delta T_{sw2,OFF} = \frac{(V_{bus} - V_{rec})D}{V_{rec}f_{sw}}
\]

Combining these equations together gives,

\[
I_{cap, peak, interval} = I_{Lin, peak} \left( 1 + \frac{2(V_{bus} - V_{rec})}{V_{rec}} \right)
\]

(4 - 9)

Replacing the \(I_{Lin, peak}\) with \(I_{cap, peak}\) to get the RMS value for the bus capacitor current gives:
\[ I_{\text{cap, rms, interval}} = \left(1 + \frac{2(V_{\text{bus}} - V_{\text{rec}})}{V_{\text{rec}}} \right) \frac{V_{\text{rec}} D \sqrt{D}}{L_{\text{in}} f_{\text{sw}} \sqrt{3}} \]  
(4 – 10)

\[ I_{\text{Lin, rms}} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} I_{\text{cap, rms, interval}}^2} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} \left(1 + \frac{2(V_{\text{bus}} - V_{\text{rec}})}{V_{\text{rec}}} \right) \frac{V_{\text{rec}} D \sqrt{D}}{L_{\text{in}} f_{\text{sw}} \sqrt{3}}^2} \]  
(4 – 11)

Thus, the current conducting power losses on the main switch are:

\[ P_{SW1, \text{cond}} = I_{\text{Lin, rms}}^2 R_{ds-ON} + I_{\text{cap, rms}}^2 R_{ds-ON} \]  
(4 – 12)

### 4.2.1.2 Conducting Losses on the Active Clamp Switch

Power loss on the active clamp switch is:

\[ P = I_{cc}^2 R_{ds-on} \]  
(4 – 13)

S3 is only conducting when the active clamp circuit is working, according to the modes of operation.

\[ (L_{lk1} + L_{lk2} + L_{m1} + L_{m2}) \frac{di}{dt} = V_{\text{clamp}} \]  
(4 – 14)

\[ \frac{di}{dt} = \frac{V_{\text{clamp}}}{(L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \]

\[ di = \frac{V_{\text{clamp}}}{(L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \times \frac{1 - D}{2f_{\text{sw}}} \]

For the current in the active clamp circuit, because of the energy equilibrium, the flow-in energy should be equal to the flow-out energy. This means the average current should be 0. There is a negative peak value and a positive peak value, and the absolute value for the peak value should be equal to the half of the \(di\)

\[ I_{CC, \text{peak}} = \frac{1}{2} \frac{di}{dt} = \frac{V_{\text{clamp}} (1 - D)}{4f_{\text{sw}} (L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \]  
(4 – 15)
\[ I_{CC,\text{rms}} = I_{CC,\text{peak}} \left( \sqrt{\frac{1 - 2DT - t_{\text{dead}}}{3T}} \right) \]

\[ = \frac{V_{\text{clamp}} (1 - D)}{4f_{sw}(L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \left( \sqrt{\frac{1 - 2DT - t_{\text{dead}}}{3T}} \right) \]  
(4 - 16)

\[ P = I_{CC,\text{rms}}^2 R_{ds-on} \]  
(4 - 17)

Where

\[ V_{\text{clamp}} = \left| -2V_0 \frac{N_1}{N_2} \right| \]

4.2.2 Power losses on other components

4.2.2.1 The core losses on the transformers

\[ P_{fe} = P_h = f_{sw}^m \cdot k_h \cdot B_{ac}^n \]  
(4 - 18)

\[ B_{ac} = \frac{\Delta B}{2} = \frac{V_{bus} D}{2N_{pri} A_{ef_{sw}}} \times 10^8 \]  
(4 - 19)

Where the \( m, n, k_h \) are the parameters providing in the data sheet

4.2.2.2 The conducting losses for input inductor

For the previous discussion, the RMS value of the inductor part in the switch is:

\[ I_{\text{Lin,\text{rms}}} = \frac{1}{n} \sum_{k=1}^{n} I_{\text{rms,\text{interval}}}^2 = \frac{1}{n} \sum_{k=1}^{n} \left( \frac{V_{\text{rec}} D \sqrt{D}}{L_{\text{in}} f_{sw} \sqrt{3}} \right)^2 \]  
(4 - 20)

To determine the rms value for the inductor only, the duty cycle value must be replaced with \( D(1 + \frac{(V_{bus} - V_{rec})}{V_{rec}}) \) so that:
\[ I_{\text{Lin},rms} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} I_{\text{rms,interval}}^2} = \sqrt{\frac{1}{n} \sum_{k=1}^{n} \left( \frac{V_{\text{rec}} \sqrt{D \left( 1 + \frac{(V_{\text{bus}} - V_{\text{rec}})}{V_{\text{rec}}} \right)^3}}{L_{\text{in}} f_{\text{sw}} \sqrt{3}} \right)^2} \]  

(4 - 21)

The following equation can be used to determine the power loss of the inductor:

\[ P_{\text{cond-losses,inductor}} = (I_{\text{Lin},rms})^2 R_{\text{Lin}} \]  

(4 - 22)

4.2.2.3 The Conducting Losses for the Transformer

Since the two transformers are working identically, it is easier to determine conduction losses for each separately.

For the upper transformer:

\[ P_{\text{cond-losses,TR}} = I_{\text{pr1}}^2 R_{\text{pri}} + I_{\text{scd}}^2 R_{\text{sec}} + I_{\text{trd}}^2 R_{\text{trd}} \]  

(4 - 23)

For the primary side, when the upper main switch is on, the current will flow through the switch and into the transformer. After the upper switch is off, the current in the primary side is equal to the active clamp circuit until the lower main switch is on. The current will drop to 0 when the lower main switch is on and will be equal to the active clamp circuit current again after the lower main switch is off. Based on this analysis:

\[ I_{\text{pr1}} = \begin{cases} 
\frac{V_{\text{rec}} D \sqrt{D}}{L_{\text{in}} f_{\text{sw}} \sqrt{3}} (0 < t < DT) \\
I_{\text{CC}} (DT + t_{\text{dead}} < t < DT + t_{\text{dead}} + T_{\text{CC}}) \\
0 \left( \frac{1}{2} T < t < \frac{1}{2} T + DT \right) \\
I_{\text{CC}} \left( \frac{1}{2} T + DT + t_{\text{dead}} < t < T - t_{\text{dead}} \right) 
\end{cases} \]  

(4 - 24)

Where
\[ I_{CC} = \frac{V_{\text{clamp}}(1 - D)}{4f_{sw}(L_{tk1} + L_{tk2} + L_{m1} + L_{m2})} \left( \sqrt{1 - 2DT - t_{\text{dead}}} \right) \]  (4 - 25)

For the secondary side, the total current should be equal to the combination of capacitor current and the secondary stage current

\[ I_{\text{scd, rms}} = \frac{V_O}{2(Z_R + Z_C)} \]  (4 - 26)

The tertiary winding is directly connected to the input inductor, so it has the same current with the input inductor.

\[ I_{\text{trd, rms}} = \frac{1}{\sqrt{n}} \sum_{k=1}^{n} \left( \frac{V_{\text{rec}}D\sqrt{D}}{L_{\text{in}}f_{sw}\sqrt{3}} \right)^2 \]  (4 - 27)

By combing these three current equations with the transformer power equation, the total power can be calculated.

4.2.2.4 The conducting losses for the output diodes

The output diode current is equal to the secondary winding current

\[ I_{D01} = I_{D02} = I_{\text{scd, rms}} = \frac{V_O}{2(Z_R + Z_C)} \]  (4 - 28)

\[ P_{\text{cond-losses,diode}} = I_{D01}V_{\text{diode}} + I_{D02}V_{\text{diode}} \]  (4 - 29)

\[ V_{\text{diode}} \] - the voltage drops across the diodes in forward bias.

4.2.3 Voltage and current stress analysis on switches

4.2.3.1 The voltage stress on the mains switches:

For the main switches, the voltage stress can be expressed as the difference of the half of the DC bus voltage and the voltage on one transformer. When main switch S1 is on, main switch S2 is off,
\[ V_{pri1} = \left| -2V_o \frac{N_1}{N_2} \right| \times \frac{1 - D}{D} \]

\[ V_{pri2} = \left| -2V_o \frac{N_1}{N_2} \right| \]

When the main switch S1 is on, switch S2 is off and

\[ V_{pri2} = \left| -2V_o \frac{N_1}{N_2} \right| \times \frac{1 - D}{D} \]

\[ V_{pri1} = \left| -2V_o \frac{N_1}{N_2} \right| \]

\[ V_{sw1,max} = V_{bus} - V_{pri1} - V_{pri2} \]  \hspace{1cm} (4 - 30)

\[ V_{sw1,max} = V_{bus} + \left| -2V_o \frac{N_1}{N_2} \right| - \left| -2V_o \frac{N_1}{N_2} \right| \times \frac{1 - D}{D} \]

\[ V_{sw1,max} = V_{bus} + \left| -2V_o \frac{N_1}{N_2} \right| (2 - \frac{1}{D}) \]

\[ V_{sw2,max} = V_{bus} + \left| -2V_o \frac{N_1}{N_2} \right| \left| 2 - \frac{1}{D} \right| \]  \hspace{1cm} (4 - 31)

### 4.2.3.2 The voltage stress on the active clamp switch:

\[ V_{SW,3} = V_{pri1} + V_{pri2} - V_{clamp} \]  \hspace{1cm} (4 - 32)

It is similar to the calculation process of voltage stress on main switches.

\[ V_{clamp} = \left| -2V_o \frac{N_1}{N_2} \right| \]  \hspace{1cm} (4 - 33)

\[ V_{SW,3} = V_{pri1} + V_{pri2} - |V_{clamp}| = \left| -2V_o \frac{N_1}{N_2} \right| \left| 1 - \frac{1}{D} \right| \]  \hspace{1cm} (4 - 34)
4.2.3.3 The current stress on the main switch:

\[ I_{sw1,peak} = I_{sw2,peak} = I_{Lin,peak} + I_{bus,peak} = I_{Lin,peak} \left( 2 + \frac{2(V_{bus} - V_{rec})}{V_{rec}} \right) \]

\[ = \frac{V_{rec}D}{L_{infsw}} \left( 2 + \frac{2(V_{bus} - V_{rec})}{V_{rec}} \right) \quad (4 - 35) \]

With,

\[ V_{rec} = V_{in,peak} \quad (4 - 36) \]

4.2.3.4 The current stress on the active clamp switch:

The active clamp switch is connected in series to the active clamp capacitor, so the key to calculate the active clamp switch current is to find out the peak value of the current through the connected capacitor.

\[ I_{CC} = \frac{|V_{clamp}|}{(L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \times \left( \frac{1 - D}{2f_{sw}} - t_{dead} \right) \quad (4 - 37) \]

Ignore the small drop we have when the active clamp is working mode3:

\[ I_{CC} = \frac{2V_{o} \frac{N_1}{N_2} + V_{rec}}{(L_{lk1} + L_{lk2} + L_{m1} + L_{m2})} \times \left( \frac{1 - D}{2f_{sw}} - t_{dead} \right) \quad (4 - 38) \]

4.3 Conclusion

In this chapter, the possible power losses, the voltage stresses, and the current stresses in the circuit were calculated. To obtain the equations above, the principle of energy equilibrium was used. This principle means that the energy absorbed by the inductor, capacitor, and transformer should be equal to the released energy. Based on the analysis and calculations, the main power loss associated with the switches is the conducting losses. Due to the ZVS techniques used in this design, the turn-on and turn-off losses have been eliminated.
Chapter 5

5 Design process and result comparison

5.1 Introduction

In this chapter, a process for the design of the stacked AC-DC single-stage converter with interleaving operation is presented. The converter is designed to be used with $110\text{V}_{\text{rms}}$ and $220\text{V}_{\text{rms}}$ input voltage and 48 V output voltage for low power applications (40W - 400W). Simulation results obtained from Power Simulation Software (PSIM) are presented. The results confirm the feasibility of the converter with interleaved operation and the analysis of the converter that was presented in previous chapters.

5.2 Design process

Based on the work done in previous chapters, an appropriate design of the converter can be made. The converter should be designed to meet the following criteria:

1) The converter is to be designed for input voltage $V_{\text{in}} = 110\text{V}_{\text{rms}}$ and $V_{\text{in}} = 220\text{V}_{\text{rms}}$, which are standard voltages in North America and Europe. The maximum output power that the converter is to delivered is to be 400 W.

2) The DC bus voltage should be as low as possible to reduce the voltage stresses on the components, but not too low so that current stresses and conduction losses become high. The converter will be designed for 110V and 220V rms input AC voltage. The voltage across each DC bus capacitor will be targeted to be between $400\text{V}_{\text{dc}}$ and $450\text{V}_{\text{dc}}$, which is standard for single, single-stage AC-DC converter modules.

3) The energy of the leakage inductance should be sufficient to be able to discharge the output parasitic drain-source capacitor of the two main switches and the active clamp switch so that these switches can be turned on with ZVS.

An iterative process is needed to design the converter as the parameters are interrelated. What has been done in this chapter is that the transformer turns ratio has been determined from previous iterations and used to narrow down the range of suitable values for the other
converter parameters. The iteration presented here represents the final iteration after the range of suitable values has been narrowed down.

5.2.1 Value for the components

5.2.1.1 Values for turns ratio $N_1: N_2$

Initially, a DC bus voltage of less than 900V (2 x 450V across each capacitor) is targeted. The design will start with the primary/secondary turns ratio of the transformer. There is an inverse relation between this turns ratio and the DC bus voltage – the DC bus voltage decreases and the turns is increased, but reducing the DC bus voltage results in more current flowing in the converter to deliver the same power and thus more current related stresses and losses.

Based on previous iterations not shown here, the turns ratio has been narrowed to 0.5.

5.2.1.2 Value for the input inductor $L_{in}$

The input inductors for the two input branches of the converter must be such that the current flowing through them is discontinuous so that a very good power factor can be ensured. This means that $L_{in}$ should be as small as possible, but not too small or else the triangular peaks of the current flowing in the inductors will be high. In other words, $L_{in}$ should be small enough to ensure DCM operation, but not smaller.

There is no single, simple, equation that can be used to determine an appropriate value for $L_{in}$. Based on the equations and design curves that are presented in Chapter 3, the relation of the input inductor and other parameters can be determined as:

\[
I_{bus} = \frac{2P_o}{V_{bus}} = f_{ac} \sum_{k=0}^{n} \frac{V_{rec,k} D^2}{L_{in} f_{sw}^2} \quad (5 - 1)
\]

\[
L_{in} = \frac{V_{bus}}{2P_o f_{ac}} \sum_{k=0}^{n} \frac{V_{rec,k} D^2}{f_{sw}^2} \quad (5 - 2)
\]

where $V_{bus}$ is the DC bus voltage, $V_{rec}$ is the input voltage after the rectifier, $P_o$ is the output power, and the $L_{in}$ is the input inductance, $L_{in}$ must be such that the current through an
input inductor can always drop back to 0 before the next switching cycle, which makes the worst case to be the low input voltage, $V_{in} = 110V_{rms}$, and the full load output. Based on the analysis of Chapter 3 and using the computer program and design curves presented in Chapter 3, for $P_o = 400W$, which makes $L_{in} = 132\mu H$, with the help of PSIM, finally, the $L_{in} = 110\mu H$ is selected, because in the simulation, the $L_{in} = 110\mu H$ is the value which can guarantee the input current remains at discontinuous mode.

5.2.1.3 Value for the magnetizing inductance of the transformers $L_m$

The magnetizing inductance value is an inherent value of a transformer which can be adjusted by adjusting the material or the turns of the transformers. Based on the chapter 3 analysis and design curve, there is a relationship between DC bus Voltage, and the turns ratios, and the input inductor. Also, the magnetizing inductance has an effect on the duty cycle, so the value cannot be too high, which would cause the low duty cycle, and it is not possible to be too low, which may bring high DC bus voltage to the converter. So, to maintain the interleaving phenomenon and also the low DC bus voltage for the converter.

According to the design curve, the $L_m = 300\mu H$ is the reasonable value for the magnetizing inductance.

5.2.1.4 Value for the leakage inductance of the transformers $L_{lk}$

The leakage inductance usually is the cause of losses, but in this design, leakage inductance can generate a opposite current flow through the body diode of the active clamp switch to achieve the ZVS. To ensure the ZVS, the stored energy in the leakage inductance should be larger than the stored energy in the parasitic because the parasitic capacitor need to be discharged first. To determine the value of leakage inductance, the maxima energy the body diodes of active clamp switch can hold has to be found:

$$\frac{C_v V_{clamp}^2}{2} < 2 \times \frac{L_{lk} I_{Lin}^2}{2}$$

(5 – 3)

The left side is the equation for the stored energy in the parasitic capacitor of active clamp switch, and the right side is the maximum energy that leakage inductance of two
transformers can hold. Typically, the right side has to be large than the left side, but to ensure the ZVS can happen, the worst case has to be considered in the design process. So, the worst case is assuming the current is always be the maximum value, for the capacitance of parasitic capacitor of active clamp switch usually is less than 20nF. According to the equation, leakage inductance is about 6uH, in the following simulation the value of leakage inductance is set to 10uH.

5.2.2 Design parameters for the proposed converter

Based on the above analysis and calculation, the parameters and values for the main components in the proposed converter has been set down. With the help of PSIM and MATLAB, the values can be checked and defined if they are proper or not. With the repeat iterative work and test, the best combination of specifications and parameters is shown in the following tables.

Table 5-1 Specification and parameters of proposed converter

<table>
<thead>
<tr>
<th>Specification</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Power Range($P_{out}$)</td>
<td>40W-400W</td>
<td></td>
</tr>
<tr>
<td>Input Voltage ($V_{in}$)</td>
<td>110 and 220V$_{rms}$</td>
<td></td>
</tr>
<tr>
<td>Output Voltage ($V_{O}$)</td>
<td>48V</td>
<td></td>
</tr>
<tr>
<td>Main Switch Frequency ($f_{SW}$)</td>
<td>50KHz</td>
<td></td>
</tr>
<tr>
<td>Active Clamp Switch Frequency ($f_{SW,\text{clamp}}$)</td>
<td>100KHz</td>
<td></td>
</tr>
<tr>
<td>Duty Cycle Range ($D$)</td>
<td>0.25-0.75</td>
<td></td>
</tr>
<tr>
<td>Turns ratio ($N_p:N_s$)</td>
<td>1:0.5</td>
<td></td>
</tr>
<tr>
<td>Magnetizing Inductance ($L_m$)</td>
<td>300uH</td>
<td></td>
</tr>
<tr>
<td>Leakage Inductance ($L_{Ld}$)</td>
<td>10uH</td>
<td></td>
</tr>
<tr>
<td>DC bus capacitor</td>
<td>220uF</td>
<td></td>
</tr>
</tbody>
</table>

These parameters and value will be used in the following simulation and calculations.

5.3 Simulation results display

Figure 5.1 shows the circuit diagram that was implemented in PSIM, using the component values listed in Table 5-1.
The following figures show results that were obtained using PSIM with input voltage \(V_{in} = 110V_{rms}\) in order to highlight the converter’s interleaving capability.

Figure 5.2 (a) shows the current flowing through each of the two input inductors separately, over several switching cycles. It can be seen that both currents are discontinuous, which is the necessary condition of ensuring a very good power factor.
Figure 5.3 (a) and (b) shows the same two waveforms, but zoomed out for a whole input AC line cycle. These waveforms are the current in input inductor $L_{\text{in1}}$ and $L_{\text{in2}}$ respectively. Figure 5.3(c) shows a third waveform that is the addition of the first two waveforms, which shows how interleaving the two input current waveforms can produce an input current that is continuous with reduced ripple.
Figure 5.3 The interleaved phenomenon (a) The input current in the Lin1 (I: 2A/div, t: 5ms/div) (b) The input current in the Lin2 (I: 2A/div, t: 5ms/div) (c) The sum of two current(I: 2A/div, t: 5ms/div)

Figure 5.4 shows the current and voltage waveforms of the three switches. It can be seen that the switches can turn on with ZVS as the switch voltage drops when the current in a switch is negative, which means the current is flowing through the body diode of the switch. The switches can be turned on with ZVS after the switch voltage has dropped to zero.
5.4 Results comparison and estimated efficiency

In this section, the results obtained through analysis and results obtained from PSIM simulation are compared and estimated efficiency numbers are given.

5.4.1 Voltage and current stress comparison

The voltage and current stress basically are the highest value the components have to tolerate. If the stress is too high, then more expensive components need to be used. To get
the voltage and current stress, the equations in Chapter 4 will be used to get the calculation results; these results are compared to simulation results in Table 5-2.

**Table 5-2: Comparison about the current stress on switches**

<table>
<thead>
<tr>
<th>P_{out}=400W</th>
<th>Calculation (A)</th>
<th>Simulation (A)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in}=110Vrms</td>
<td>Q_1</td>
<td>18.243</td>
<td>18.710</td>
</tr>
<tr>
<td></td>
<td>Q_2</td>
<td>18.243</td>
<td>18.710</td>
</tr>
<tr>
<td></td>
<td>Q_C</td>
<td>15.124</td>
<td>15.632</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P_{out}=40W</th>
<th>Calculation (A)</th>
<th>Simulation (A)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in}=110Vrms</td>
<td>Q_1</td>
<td>8.649</td>
<td>7.967</td>
</tr>
<tr>
<td></td>
<td>Q_2</td>
<td>8.649</td>
<td>7.967</td>
</tr>
<tr>
<td></td>
<td>Q_C</td>
<td>2.964</td>
<td>3.125</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P_{out}=400W</th>
<th>Calculation (A)</th>
<th>Simulation (A)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in}=220Vrms</td>
<td>Q_1</td>
<td>20.384</td>
<td>19.5</td>
</tr>
<tr>
<td></td>
<td>Q_2</td>
<td>20.384</td>
<td>19.5</td>
</tr>
<tr>
<td></td>
<td>Q_C</td>
<td>6.154</td>
<td>6.612</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P_{out}=40W</th>
<th>Calculation (A)</th>
<th>Simulation (A)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in}=220Vrms</td>
<td>Q_1</td>
<td>7.219</td>
<td>7.862</td>
</tr>
<tr>
<td></td>
<td>Q_2</td>
<td>7.219</td>
<td>7.862</td>
</tr>
<tr>
<td></td>
<td>Q_C</td>
<td>3.037</td>
<td>3.437</td>
</tr>
</tbody>
</table>

**Table 5-3: Comparison about the voltage stress on switches**

<table>
<thead>
<tr>
<th>P_{out}=400W</th>
<th>Calculation (V)</th>
<th>Simulation (V)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{in}=110Vrms</td>
<td>Q_1</td>
<td>284.457</td>
<td>289.063</td>
</tr>
<tr>
<td></td>
<td>Q_2</td>
<td>284.457</td>
<td>289.063</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_c</td>
<td>251.749</td>
<td>256.793</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_1</td>
<td>411.154</td>
<td>445.313</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_2</td>
<td>411.154</td>
<td>445.313</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_C</td>
<td>409.245</td>
<td>437.793</td>
</tr>
<tr>
<td>P_{out}=400W</td>
<td>Q_1</td>
<td>320.692</td>
<td>337.670</td>
</tr>
<tr>
<td>P_{out}=400W</td>
<td>Q_2</td>
<td>320.692</td>
<td>337.670</td>
</tr>
<tr>
<td>P_{out}=400W</td>
<td>Q_C</td>
<td>450.174</td>
<td>485.938</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_1</td>
<td>530.592</td>
<td>575.781</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_2</td>
<td>530.592</td>
<td>575.781</td>
</tr>
<tr>
<td>P_{out}=40W</td>
<td>Q_C</td>
<td>430.167</td>
<td>486.181</td>
</tr>
</tbody>
</table>

From the values in the table, the calculation results match the simulation results, based on these results, the proper components can be found in the following test.

### 5.4.2 Output power and duty cycle comparison

The result from simulation has been posted above, it is clear that all three switches can work with ZVS, and the voltage stress on three switches is in a reasonable range. In this part, the results from simulation is used to compare to the results from the calculation, to see if these two results match each other.

Table 5-4 shows some voltage and current values of key components in this circuits, and the other column shows the calculated results from equation in chapter 3 and chapter 4. All results are tested with L_{m}=300\mu H, L_{in}=120\mu H, and power is 40W and 400W, the input voltage is 110V and 220V.
Table 5-4: The comparison between simulation results and calculation results

<table>
<thead>
<tr>
<th>V&lt;sub&gt;in&lt;/sub&gt;=110V</th>
<th>Simulation</th>
<th>Calculation</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;out&lt;/sub&gt;=400W</td>
<td>V&lt;sub&gt;bus&lt;/sub&gt; (V)</td>
<td>182.35</td>
<td>176.12</td>
</tr>
<tr>
<td></td>
<td>Duty Cycle</td>
<td>0.65</td>
<td>0.6236</td>
</tr>
<tr>
<td>V&lt;sub&gt;in&lt;/sub&gt;=110V</td>
<td>V&lt;sub&gt;bus&lt;/sub&gt; (V)</td>
<td>280.34</td>
<td>270.25</td>
</tr>
<tr>
<td>P&lt;sub&gt;out&lt;/sub&gt;=40W</td>
<td>Duty Cycle</td>
<td>0.2917</td>
<td>0.3026</td>
</tr>
<tr>
<td>V&lt;sub&gt;in&lt;/sub&gt;=220V</td>
<td>V&lt;sub&gt;bus&lt;/sub&gt; (V)</td>
<td>347.213</td>
<td>341.63</td>
</tr>
<tr>
<td>P&lt;sub&gt;out&lt;/sub&gt;=400W</td>
<td>Duty Cycle</td>
<td>0.42</td>
<td>0.4172</td>
</tr>
<tr>
<td>V&lt;sub&gt;in&lt;/sub&gt;=220V</td>
<td>V&lt;sub&gt;bus&lt;/sub&gt; (V)</td>
<td>416.537</td>
<td>410.392</td>
</tr>
<tr>
<td>P&lt;sub&gt;out&lt;/sub&gt;=40W</td>
<td>Duty Cycle</td>
<td>0.167</td>
<td>0.1592</td>
</tr>
</tbody>
</table>

From the comparison table above, the simulation results are pretty close to the calculation results, which means the analysis matches the working process in of the proposed circuit. And also when the input voltage V<sub>in</sub>=220V, and the output power P<sub>out</sub>=40W, which is the extreme situation for the DC bus voltage, and the value if 393V for each of the DC bus capacitor, this phenomenon satisfies the original purpose of the stacked structure, which is reducing the DC bus voltage so the size and the cost can be reduced as well.

There is some difference between the calculated values and the values obtained from PSIM, especially when the converter is operating under high input line and light-load conditions. These errors can be explained as follows:

- Simulations in PSIM must be done with a finite time step. Under high-line and light-load conditions, the duty cycle of the converter is at its narrowest so that the sampling of the PSIM software will be more inaccurate as there is less waveform to sample.
- Approximations were made in the analysis, such as no ripple on the intermediate DC voltage and output voltage waveforms. Moreover, some losses were ignored as Chapter 4 dealt with just the key losses.
The largest difference between calculated values and values obtained from simulation were the peak voltages of the converter components when the converter was operating with high input line and light-load conditions. Some of this was caused by limitation in the time step in PSIM, but some of this was caused by a resonant interaction between switch output capacitance and transformer inductance, which can create an oscillation that results in overvoltage spikes appearing across the switches. Certain voltages in the converter are more likely to be floating when there is little current in the circuit than when there is current flowing when these voltages can be clamped. Since these are parasitic interactions, they can be dealt with in prototypes by introducing some sort of damping mechanism in the converter such as a saturable reactor.

5.4.3 Estimated efficiency

The efficiency is the most important parameters to judge the proposed converter whether having good quality or not. According to the chapter 3 and 4, the equation of losses is given and can be used to calculate the approximate losses. Due to the lack of physical test, there are some losses cannot be calculated, but these losses are not the main part. The main part is the conducting losses on the components, such as DC bus capacitor, the switches, the transformers. With the help of PSIM and the datasheets from websites, the power losses and the estimated efficiency can be defined and the results are shown in table 5-5

<table>
<thead>
<tr>
<th>Input Voltage</th>
<th>Output Power</th>
<th>Estimated Losses</th>
<th>Estimated Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}=110V_{rms}$</td>
<td>$P_{out}=400W$</td>
<td>31.372</td>
<td>92.15</td>
</tr>
<tr>
<td></td>
<td>$P_{out}=300W$</td>
<td>32.019</td>
<td>89.34</td>
</tr>
<tr>
<td></td>
<td>$P_{out}=200W$</td>
<td>24.832</td>
<td>87.58</td>
</tr>
<tr>
<td></td>
<td>$P_{out}=100W$</td>
<td>16.402</td>
<td>83.59</td>
</tr>
<tr>
<td>$V_{in}=220V_{rms}$</td>
<td>$P_{out}=400W$</td>
<td>58.128</td>
<td>85.46</td>
</tr>
<tr>
<td>P_{out}=300W</td>
<td>51.93</td>
<td>82.69</td>
<td></td>
</tr>
<tr>
<td>P_{out}=200W</td>
<td>36.52</td>
<td>81.74</td>
<td></td>
</tr>
<tr>
<td>P_{out}=100W</td>
<td>20.3464</td>
<td>79.65</td>
<td></td>
</tr>
</tbody>
</table>

This Table is the demonstration of the estimated efficiency under different situation. There are two important trends in this table, the first is with the increase of the output power, the efficiency is increase, and the second is the efficiency is higher with lower input voltage, the proposed converter loses less power when it is working under low-input, high-output situation.

**5.5 Conclusion**

In this chapter, the design of the stacked AC-DC single-stage flyback converter with interleaving was discussed and simulation results have been presented. The performance of proposed AC-DC stacked flyback converter was shown to be generally close to the analysis. It was confirmed that the converter can operate with interleaving and with ZVS. It was also shown that the converter can operate with a maximum efficiency of 92.15% in theory, under with low input voltage and full load.

It should be noted that the AC-DC single-stage modules that were used to make the stacked converter were among the simplest single-stage converters. The stacked converter can be implemented with any single-stage converter that has magnetic switches, including converters that are more sophisticated and with perhaps greater efficiency.
Chapter 6

6 Conclusion

6.1 Introduction

This chapter summarizes the main points of this thesis, lists its main contributions, and contains a brief discussion of future work.

6.2 Summary

The main focus of this thesis has been on a new AC-DC single stage stacked flyback converter for low power applications. Single-stage converters have been proposed as a way of reducing the cost of conventional two-stage AC-DC converters that are implemented with two converter stages: an AC-DC front-end converter (typically a boost converter) followed by an isolated DC-DC converter, which can be either a flyback converter or a forward converter for low power applications. This converter is an attempt to address one of the most significant drawbacks of AC-DC single-stage converters – the high peak voltage stress of the flyback converter switch that is due to the fact that the DC bus voltage is uncontrolled and can rise to very high levels under certain operating conditions. This high voltage creates several problems, mainly (i) it makes necessary the use of a switching device with a high peak voltage rating, which can be expensive as such devices are not common; (ii) distortion is introduced in the input current waveform if some method is used to reduce the peak voltage stress of the switch. The stacked structure of the proposed converter helps reduce the peak voltage stress of the switch as it is split between two switches. Although two switches are used in the converter instead of one, the cost of these two switches can be actually cheaper as they are much more readily available. In the end, the cost and size of the proposed stacked flyback converter operating with interleaving is less than that of interleaved two-module, two-stage AC-DC converters and two-module interleaved non-stacked AC-DC single-stage flyback converters.

The contents of the thesis can be summarized as follows:
Chapter 1 began by presenting background knowledge related to power electronics principles that were pertinent to the work performed in this thesis. A literature review of low power single-stage AC-DC converters was then performed and the strengths and weaknesses of previously proposed approaches were stated. Finally, the thesis objectives were stated at the end of the chapter.

Chapter 2 introduced the proposed stacked single-stage AC-DC converter topology. The general operating principles of the converter were discussed generally and the modes of operation that it passes through during a switching cycle were discussed in detail – for the case when the converter’s duty cycle (ratio of switch on-time to switching cycle period) is less than 0.5 and greater than 0.5. The main focus of this thesis is on converter operation with duty cycle greater than 0.5, which increases the possibility of interleaving. Interleaving occurs when the two input branches of the converter have current flowing in them at the same time. This decreases the amount of ripple in the input current, which reduces peak current stress and input current harmonic content. It also decreases the amount of ripple in the output current so that the output DC is purer. The converter also allows its two main switches to operate with zero-voltage switching (ZVS) using just one auxiliary switch that can also operate with ZVS.

Chapter 3 presented the analysis and design of the converter. The analysis of the converter was based on the principle of energy equilibrium of its DC bus capacitors. The amount of charge that is fed into the capacitors must be equal to the amount of charge that is removed from the capacitors during a half line cycle. Since the input line voltage is rectified before it is fed to the DC-DC section of the converter, the frequency of the original AC waveform is doubled so that the period is based on half of the original line cycle. The analysis was performed using a MATLAB program that was developed to generate steady-state operating points for various combinations of converter components (e.g. transformer turns ratio, transformer magnetizing inductance, input inductance, etc.) and these operating points were plotted as curves on graphs of parametric values such as peak switch voltage stress. These graphs illustrated the relation between various parametric values and combinations of component values and were used to design the converter.
Chapter 4 presented equations that can be used to determine key converter component stresses and losses. These equations were based on the analysis that was performed in Chapter 3 and can be used in the design of the converter.

Chapter 5 presented simulation results taken from a converter with parameter values that were selected based on the analysis and design presented in previous chapters. PSIM, a commercially available software package was used to do the simulations. Key waveforms such as the input current and switch voltage and current waveforms were presented. It was confirmed that the proposed converter can operate with a good power factor, an interleaved input current with reduced ripple, with less switch voltage stress that previously proposed single-switch single-stage converters, and with ZVS for all the converter switches.

6.3 Contribution

The main contributions of this thesis to the power electronics literature are as follows:

- A new way of operating a previously proposed single-stage AC-DC stacked flyback converter was examined in this thesis. This manner of operation involves extending the duty cycle of the converter past 0.5 in order to take advantage of interleaving among the two paralleled input branches. Such interleaving results in lower peak component current stresses and less harmonic ripple at the input. The converter can operate with \( D > 0.5 \) and maintain the ZVS operation that it has when operating with \( D \) less than 0.5

- The converter’s characteristics were analyzed and graphs of parametric curves were generated. These curves provide insight as to the steady-stage characteristics of the proposed converter when operating with interleaving.

- A design procedure for the proposed converter operating with interleaving was established and demonstrated. This procedure will allow power electronics personnel to design and implement the proposed converter.

6.4 Future work

The following is suggested as future work to build upon the results of this thesis:
• The results presented here are simulation results obtained from a well-established and widely used power electronic circuit simulation software package. Although these results are considered to be sufficient in the power electronics field to confirm the validity of the work that is presented in this thesis, experimental work should be done to further confirm the validity of this work.

• The converter proposed in this thesis was synthesized by stacking two single-switch, single-stage AC-DC converter modules on top of each other. These modules were based on a simple AC-DC converter that performs input power factor correction based on the magnetic switch concept and this converter can be considered to be among the simplest of this kind. Work can be done to investigate the performance of stacked converters that are synthesized with more sophisticated modules to see what effect this would have on the performance of the overall stacked converter.
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[42] Epoxy N49 Ferrite Core Toroid Type Length Width 23.30mm Diameter 9.00mm Height, 495-76564-ND, B64290L0719X049, TDK Electronics Inc. [Online]. Available: https://www.tdk-electronics.tdk.com/inf/80/db/fer/r_22_1_13_7_7_90.pdf


# Curriculum Vitae

<table>
<thead>
<tr>
<th>Name:</th>
<th>Mengkai Xiong</th>
</tr>
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<tbody>
<tr>
<td>Post-secondary</td>
<td>University of Electronic Science and Technology of China</td>
</tr>
<tr>
<td>Education and</td>
<td>Chengdu, China</td>
</tr>
<tr>
<td></td>
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<tr>
<td></td>
<td>Glasgow, UK</td>
</tr>
<tr>
<td></td>
<td>2014-2018, B.Eng</td>
</tr>
<tr>
<td></td>
<td>Western University</td>
</tr>
<tr>
<td></td>
<td>London, Ontario, Canada</td>
</tr>
<tr>
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</tr>
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<td>Related Work</td>
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<td>Western University</td>
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