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Split DC bus converters for power electronic and AC-DC Microgrid applications

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Abstract

Power electronic converters are used extensively for electrical power conversion in applications such as renewable energy systems, utility applications, and electric vehicles. Such converters are needed as it is rare for a source voltage to fit the needs of a load or a set of loads for any particular application. They consist of active semiconductor switches and passive components that are combined in circuit structures (topologies) that are operated with a control strategy. The focus of this thesis is on AC-DC and DC-DC converters and their applications in AC-DC microgrids.

AC-DC converters are typically two-stage converters that consist of a front-end AC-DC converter followed by a DC-DC back-end converter. The AC-DC front-end converter converts AC voltage from an AC source such as the grid to a DC bus voltage that has been filtered by an intermediate DC bus capacitor; the DC-DC converter then converts this DC voltage into the desired output voltage. A less expensive alternative to this two-stage approach is to have just one converter perform AC-DC and DC-DC conversion.

This thesis examines isolated single-stage AC-DC converters and back-end DC-DC converters for two-stage converters that have a split DC bus, with either two capacitors in series across the bus to split the voltage or with two parallel current paths to split the bus current. These converters have fewer components or fewer light-load losses than converters with conventional topologies. Four new power converters with a split DC bus are proposed in this thesis: a reduced-switch three-phase AC-DC converter, two lower power DC-DC converters, and an AC-DC converter that can be used to simplify the architecture and control of AC-DC hybrid microgrids. The proposed converters increase efficiency and reduce the control complexity of hybrid microgrids.

The operation of each converter is explained, the steady-state characteristics and the dynamic model of each converter are determined by mathematical analysis, and a procedure that can be used for their power and control stages design is developed. Experimental and simulation results are used to confirm the feasibility of the converters and simplified AC-DC hybrid microgrid, and conclusions that resulted from the thesis work are stated.

Lay Summary

Power electronic converters are the electronic circuits that are used to process the electric power in applications such as renewable energy systems, utility applications, and electric vehicles. Such converters are used to interface different electricity generators and consumers. Since electricity is generated in two forms of AC and DC, there are four types of power electronic converters: AC-DC, AC-AC, DC-AC, and DC-DC. This thesis focuses on AC-DC and DC-DC converters.

Some of these converters are built by combining two converters so-called “front-end” and “back-end” converters to perform more complex power processing. Such a structure increases the overall system cost. More advanced structure for the converters are proposed in the literature to offer the same performance with only one converter that reduces the overall system cost, such converters are called “single-stage” converters.

This thesis investigates single-stage AC-DC converters and back-end DC-DC converters for two-stage converters that are using a new structure (split DC bus). These converters are less expensive and more efficient than conventional converters. Four new power converters are proposed in this thesis with the new structure.

The operation of each converter is explained; the mathematical model of the converters is derived. Experimental and simulation results are used to confirm the feasibility of the proposed converters in this thesis.

Keywords: Hybrid AC-DC microgrids, power electronics, DC-DC converters, three-phase single-stage AC-DC converters, split DC bus converters

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Acronyms

AC	Alternate Current
DC	Direct Current
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
EMI	Electro-Magnetic Interference
MOSFET	Metal Oxide Silicon Field Effect Transistor
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation
RMS	Root Mean Square
SSPFC	Single-Stage Power Factor Correction
TL	Three Level
THD	Total Harmonic Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVZCS	Zero Voltage Zero Current Switching

Chapter 1

1 Introduction

Power electronics is the application of solid-state electronics in electric circuit structures (topologies) to the control and conversion of electric power. Power electronic converters generally consist of semiconductor components such as MOSFETs, IGBTs, and diodes and passive components such as capacitors, inductors, and transformers. They are used to convert electric power from an existing power source to the form that is required by some load. Since electrical power can be either AC and DC, power electronic converters can be AC-AC, AC-DC, DC-AC, or DC-DC converters. The focus of the thesis is directed towards AC-DC and DC-DC converters with a split DC bus.

DC-DC converters are generally supplied from a DC source like a battery or they are supplied by a DC bus voltage that has been generated by a front-end AC-DC converter of some kind. It is a common practice in industry to implement AC-DC converters for switch-mode power supplies with two power stages – a front end AC-DC converter that converts input AC from the utility grid to an intermediate DC bus voltage that is then fed to a back-end isolated DC-DC converter that take this voltage and converts it to the required DC voltage needed to supply a load. In recent years, single-stage AC-DC converters that can perform the AC-DC conversion stage and the DC-DC conversion stage with just a single converter have become more popular as a way to reduce the cost of two-stage AC-DC converters. Regardless of whether an AC-DC converter has two converter stages or one, the converter has an intermediate DC bus.

In this thesis, AC-DC converters with a split DC bus will be examined. This split DC bus can be a bus that is implemented with two DC bus capacitors in series with each other, placed across the DC bus so that access to the midpoint voltage, which is half the bus voltage is available. A converter can also have a split DC bus with multiple current paths that allows multiple outputs to be fed by a single converter. The main advantages of implementing a converter with a split DC bus are either that its switches can be exposed

to lower voltages, which helps increase efficiency by reducing switching losses, or a converter stage can be removed, thus reducing cost and size.

In this thesis, the following topics will be examined:

- DC-DC converters with maximum power of 1 kW that are the back-end parts of two-stage AC-DC converters and that are fed from a split DC voltage bus.
- Single-stage AC-DC converters for switch-mode power supplies that have an intermediate DC voltage bus that is split.
- AC-DC interlinking converters for hybrid microgrids for information and communication technology (ICT) that can produce multiple DC voltages that can feed other parts of a microgrid.

In this chapter, a literature review of these topics will be performed, the thesis objectives will be stated, and the outline of the thesis will be given.

1.1 DC-DC converters

DC-DC converters take an input DC voltage and convert it to another DC voltage that is typically less than the original DC voltage to supply a load or a set of loads of some kind. There are numerous DC-DC topologies that can be used in a variety of applications, but in general, it is the pulse-with modulated (PWM) full-bridge converter that is most often used for applications that are more than 500 W, especially when it is operated with phase-shift modulation to achieve zero-voltage switching (ZVS) in its switches. In this section, the operation of the PWM full-bridge is reviewed, its drawbacks are discussed, and a review of converters that have been previously proposed to overcome these drawbacks is performed.

1.1.1 ZVS-PWM full-bridge converter

A circuit diagram of standard ZVS-PWM full-bridge (FB) converter is shown in Figure 1.1. The converter consists of four switches with internal anti-parallel body diodes, a transformer, two secondary output diodes, and an output filter that consists of an inductor

and a capacitor. The four converter switches convert a DC input voltage into a high-frequency (> 20 kHz) AC square waveform that is stepped down by the transformer, rectified by the secondary diodes, the filtered by the output LC filter to produce the DC voltage that is required by a load, represented as a resistor in Figure 1.1.

The converter works as follows: When a pair of diagonally opposed switches is on, the transformer primary winding is exposed to the input DC voltage. In this mode, the converter is in an energy-transfer mode and energy can be transferred from the transformer's primary to its secondary and then to the output. When two top switches (S_1, S_3) or two bottom switches (S_2, S_4) are on the converter works in the freewheeling mode as no voltage is impressed across the transformer primary and current in the converter's primary side and secondary side just circulates or freewheels, without result in any energy transfer. Each converter switch is on for about half of a periodic switching cycle, defined as half the time it takes for the converter to go through two energy-transfer modes (one for each pair of diagonally opposed switches) and two free-wheeling modes (one for the top pair of switches and one for the bottom pair).

The gating signals that are needed to turn on the converter switches and the sequence by which they are turned on are shown in Figure 1.2. The width of the gating signal pulses never changes and the gating signal of a switch is complementary to that of the other

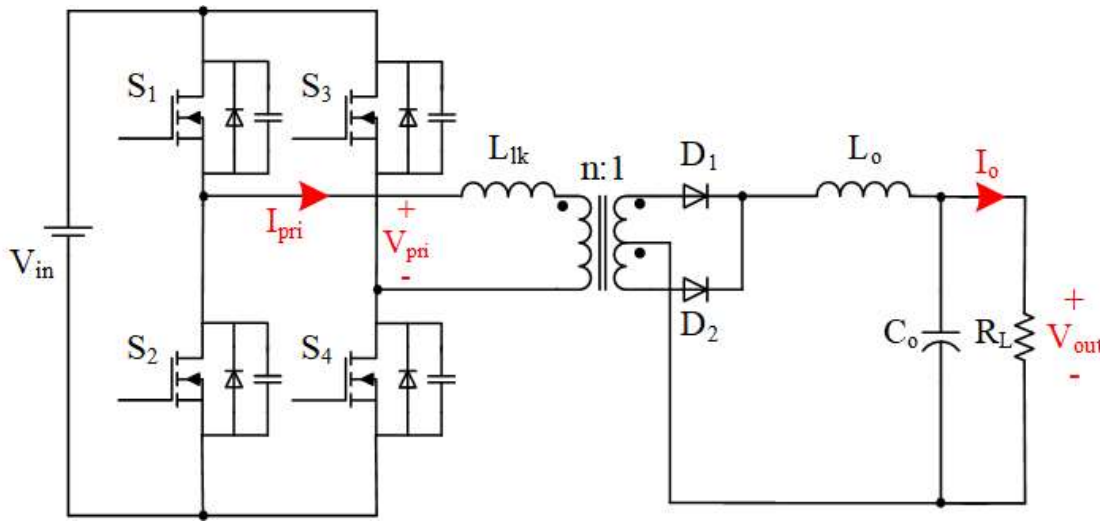


Figure 1.1. ZVS-PWM-FB DC-DC converter

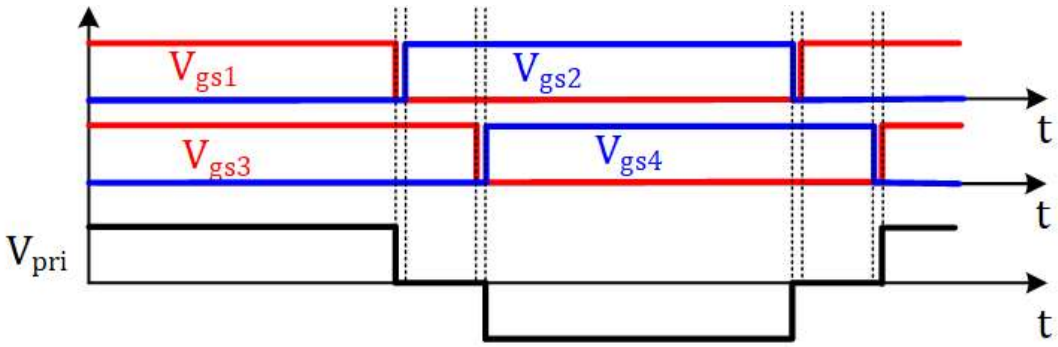


Figure 1.2. ZVS-PWM-FB DC-DC converter typical waveforms

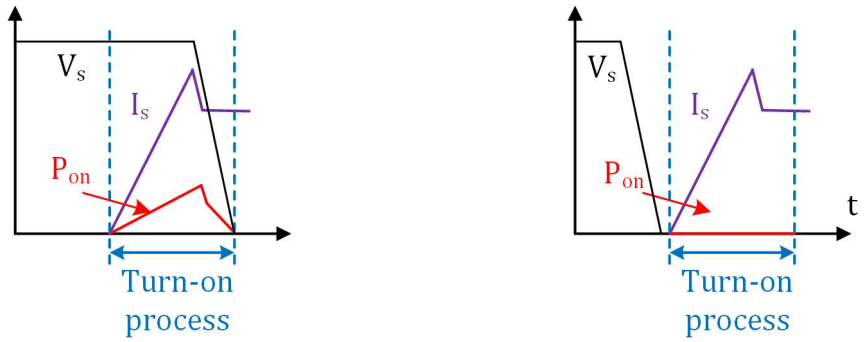
switch in the same leg so that the two switches of a converter leg are never on at the same time. The voltage that appears across the transformer primary, and thus the stepped-down transformer secondary, is dependent on the amount of overlap between diagonally opposed switches S_1 and S_4 and switches S_2 and S_3, with voltage of one polarity placed across the transformer when S_1 and S_4 are on and voltage of the opposite polarity placed across the transformer when switch S_2 and S_3 are on. The converter's voltage is controlled by shifting the fixed-width signals of S_3 and S_4 relative to those of S_1 and S_2 so that the amount of time when diagonally opposed switches are on is increased or decreased. The signal for S_1 is always the same relative to that of S_2 and the signal of S_3 is always the same relative to that of S_4.

During each transition from an energy-transfer mode to a freewheeling mode and vice versa, there is a small amount of time (dead-time) when all switches are off. During this dead-time, energy stored in the leakage inductance of the converter's transformer (as a result of current circulating in the transformer's primary side) is used to discharge the parasitic capacitance of each switch before it is turned on, after its complementary switch in the same leg has been turned off. After this capacitance has been discharged, current can flow through the anti-parallel body-diode that is internal to each switching device so that the voltage across the switch can be clamped to near-zero voltage (one forward-voltage diode drop). With almost zero voltage across it, a switch can be turned on with zero voltage switching (ZVS). Operation with ZVS reduces power losses that can occur during a switching transition in a switch that would otherwise be caused by the overlap of

switch voltage and switch current, as shown in Figure 1.3. In the case where a switch is operating without ZVS, $P_{on} = 1/2(V_s I_S)$ is dissipated in the switch. By making the voltage across a switch to be zero at the time of a turn-on transition, it can be turned on with ZVS. A switch's parasitic capacitance may be sufficient to slow down the rate of voltage rise when it is turned off, thus reducing the amount of overlap between voltage and current significantly. As a result, the switch can turn off with ZVS as well. Additional external capacitance can be added across a switching device if more capacitance is needed to slow down the rate of voltage rise further.

The ZVS-PWM converter has several drawbacks. The ones that will be examined in this these will be

- The converter has conduction power losses that are caused by current circulating in its primary whenever it is in a freewheeling mode of operation.
- The converter loses its ZVS capability when it is operating under light-load conditions as its switching losses increase.



(a) **(b)**

Figure 1.3. Power losses in a typical switch during turn-on process. (a) without ZVS, (b) with ZVS

These drawbacks are explained in detail in the next sections of this chapter.

1.1.1.1 Circulating Current Losses

When the ZVS-PWM converter is in a freewheeling mode of operation, current flows through either S_1 and S_3 or S_2 and S_4. For example, current can flow through S1 and the body-diode of S_3, or S_3 and the body-diode of S_1, or S_2 and the body-diode of S_4, or S_4 and the body-diode of S_2 during a freewheeling mode of operation. If the converter is implemented with MOSFETs, which allow current to flow in direction of source to drain through their switches instead of through their body-diodes, then current can flow through two switches during a freewheeling mode of operation.

The current flowing through two devices during a freewheeling mode of operation, creates conduction losses. These losses may be small when the converter is operating under full-load conditions but become more significant when the converter is operating under light-load conditions as (i) the converter operates more in freewheeling modes of operation, and (ii) conduction losses become larger relative to the amount of power delivered by the converter.

The main method that has been proposed to decrease the circulating current that appears in ZVS-PWM converters when they are operating in freewheeling modes of operation has been to modify their topologies to make them into zero-voltage-zero-current-switching (ZVZCS) converters [1]–[7]. An example of a ZVZCS-PWM full-bridge converter is shown in Figure 1.4. This converter is a ZVZCS converter because some of its switches operate with ZVS while some of its switches operate with ZCS.

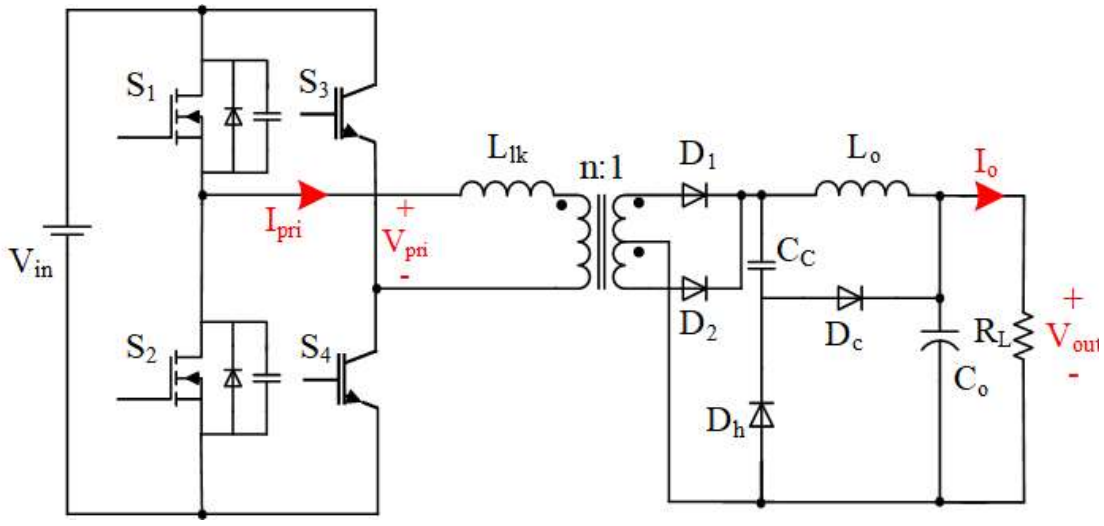


Figure 1.4. ZVZCS-PWM-FB DC-DC converter

The basic principle behind ZVZCS converters like the one shown in Figure 1.4 is that when the converter is in a freewheeling mode of operation, a counter voltage of some kind is impressed across the secondary winding of the transformer, which is then reflected across the primary winding. The counter voltage is impressed across the secondary by means of auxiliary circuit capacitor Cc, which maintains its charge at the start of a freewheeling mode of operation and is then discharged sometime shortly afterwards. Without this counter voltage, current circulates in the converter's primary side and there is almost no voltage to oppose it and to force it down. With this counter voltage, however, the circulating current does encounter as opposing voltage that can force it down to almost zero, thus extinguishing it. As a result, conduction losses caused by freewheeling mode circulating current can be mostly eliminated.

The converter in Figure 1.4 is ZVZCS converter because the switching transitions that change the converter's mode of operation from an energy-transfer mode to a freewheeling mode of operation are ZVS while those that change the converter's mode of operation from a freewheeling mode to an energy-transfer mode are ZCS. The ZVS switching transitions are associated with the switches of one leg, while the ZCS transitions are associated with the switches of the other leg. For example, after circulating current has been extinguished in a freewheeling mode, one of the switch of the ZCS leg can be turned

off with ZCS as there is no current flowing through it while its complementary switch can be turned on with ZCS because the presence of transformer inductance in the primary current path limits the rate of current rise in the switch, which in turn limits the amount of overlap that exists between switch current and switch voltage during this switching transitions. As for the switches of the ZVS leg, they can operate with ZVS because the operation of the converter when it enters a freewheeling mode is identical to that of a standard ZVS-PWM full-bridge converter.

Although a number of ZVZCS-PWM full-bridge converters have been proposed, the main drawback that they have is that half of their four switches operate with ZVS while have their switches operate with ZCS. This means that either the converter is implemented with two MOSFET devices for the ZVS leg (as ZVS is preferable for MOSFETs) and two IGBT devices for the ZCS leg (as ZCS is preferable for IGBTs), which would raise the cost of the converter as multiple types of devices would be required instead of just one or the converter is implemented with IGBTs for all four switches even though two of the switches will need to operate ZVS. ZVZCS-PWM full-bridge converters are rarely, if ever, implemented with four MOSFETs as the MOSFET turn-on losses with no ZVS are significant and result in lower efficiency.

The conventional zero-voltage (ZVS), pulse width modulated (PWM) full-bridge (FB) DC-DC converter is widely used in industry in applications requiring DC-DC power conversion for loads greater than 500W [8]–[11]. This converter is popular because it is a PWM converter that has inherent ZVS operation when operating with heavy loads, as its switches can turn on with ZVS without the need for auxiliary circuitry. Although it is considered to be the standard converter for higher power applications where a four-switch topology is preferred over a one- or two-switch topology, it has a number of issues.

One of these is the fact that the switches of the converter lose their ZVS operating capability when it operates under light-load conditions. Although there is generally sufficient energy to discharge the output capacitances of switches that are turned on when the converter enters a freewheeling operation mode (when either two top switches or two bottom switches are on at the same time), there may not be enough energy to discharge

the output capacitances of switches that are turned on when the converter enters an energy-transfer mode (when either pair of diagonally opposed switches are on at the same time). The main reason for the loss of ZVS in the latter case is that the only energy that is available to discharge the switch output capacitances is that stored in the primary-side leakage inductance of the converter's transformer. As the load is reduced, so too is the amount of this leakage inductance energy and a point is reached where the load is too low for there to be sufficient energy for the ZVS operation of the switches.

Using higher leakage inductance values allows the range of ZVS operation to be extended to a wider range of load variation, but at the cost of increasing duty cycle loss and power losses, thus decreasing converter efficiency for heavy- load operating conditions. As a result, there is a trade-off between leakage inductance and ZVS operation range that must be considered [12]–[15].

Another issue with the ZVS-PWM-FB converter is that when the converter is in a freewheeling mode of operation, current just circulates in the converter without any energy transferred to the secondary. This is because the voltage across the transformer primary is zero when either two top converter switches or two bottom converter switches are on so that the voltage across the transformer secondary is also zero. The circulating current flows through two converter devices and creates conduction losses. Converter switches are subjected to increased RMS current stresses as well for no beneficial reason [16]–[18].

A third issue is that although the control of the converter is simple PWM that regulates the output voltage by adjusting its duty cycle using phase-shift PWM [19], it can be a challenge to ensure that the transformer does not saturate. This can be done either by using sophisticated sensing methods to monitor the volt-seconds applied to a transformer during a switching period then making adjustments to balance the volt-seconds applied with either polarity across the transformer [5], [20], [21] or to put a DC blocking in series with the transformer [15]-[16], but each of these approaches has its own drawbacks.

As a result of these issues, power electronics researchers have proposed other four-switch topologies that offer improved performance to some degree such as increased ZVS

operating range and better light-load efficiency (e.g. [17]-[18]). Many of these alternative converters, however, are either very sophisticated or are simply variations of the conventional ZVS-PWM-FB converter with additional auxiliary circuitry added to the base four-switch topology and thus still have a number of the deficiencies of the ZVS-PWM-FB. Moreover, the addition of auxiliary circuitry adds to the overall cost of the converter.

1.1.1.2 Light Load Efficiency

Power electronic converters are typically required to operate over a wide range of load conditions. Although this is the case, power converters tend to be designed to operate at load levels that are at least 50%-60% of full-load. It has only been in recent years that light-load efficiency has been a topic of concern, given the proliferation of power converters in society and the need to conserved energy from the grid.

ZVS-PWM full-bridge converters lose their ZVS capability when operating under light-load conditions because their transformer primary current is low and there is insufficient energy stored in their transformer leakage inductance that can discharge the parasitic capacitance of their switches so that they can be turned on while current is flowing in their body-diodes. There are several ways by which this drawback can be overcome, including the following:

- The turns ratio of the transformer can be decreased, which increases the amount of current that flows in the converter primary. Such an approach is rarely used, however, because this would increase converter conduction losses and switch turn-off losses as the converter switches would have to turn off higher amounts of current. As a result, the load threshold at which the converter switches cease to be able to operate with ZVS is typically set to be about 40%-50% of full-load as lowering this threshold introduces more losses than would be saved.

- An auxiliary circuit(s) that can generate more circulating current is added to the ZVS-PWM converter topology. Doing so, however, increases the cost of the converter as additional passive and/or active components are needed and also

introduces the same problems as decreasing the transformer turns ratio, though not to the same degree.

- The switching frequency of the converter can be changed when the converter is operating under light-load conditions so that the converter switches do not turn on and off as often as they do when it is operating under full-load conditions. Several converter control methods have been proposed to do this, but they are sophisticated and not easy to implement.

- A combination of the above methods can be used.

1.1.2 Three-leg full-bridge converter

Circuit diagram of a three-leg ZVS-FB-PWM is shown in Figure 1.5. Thee leg ZVS-PWM-FB DC-DC converter. The converter operation principles are the same as the two-leg ZVS-FB-PWM converter. The only difference is using three legs, and more transformers reduce the stress on components that make the converter more desirable for high power applications.

1.2 AC-DC converters

AC-DC converters convert an AC input voltage, which can be obtained from the utility grid or an AC generator, and convert it into a DC voltage that can be used to supply DC-

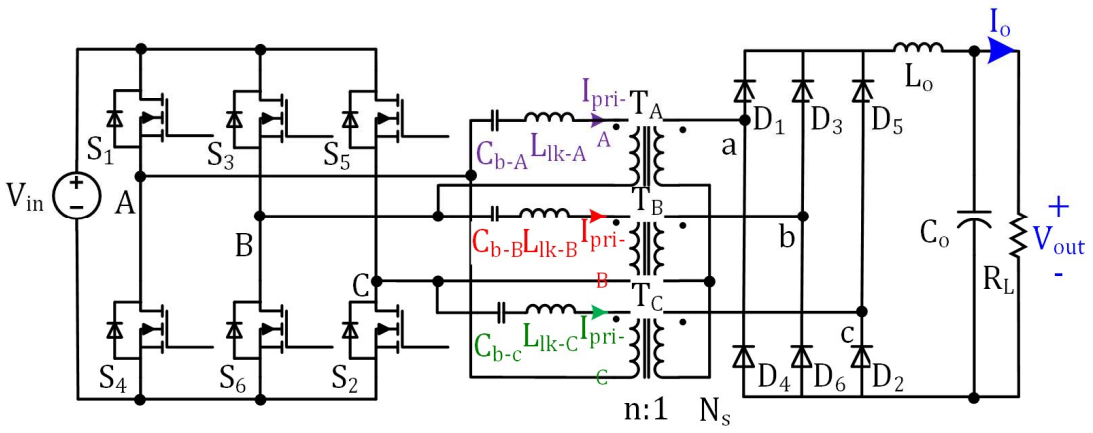


Figure 1.5. Thee leg ZVS-PWM-FB DC-DC converter

DC converters or DC-AC inverters. The input to AC-DC converters can be either single-phase AC or three-phase AC; the focus will be on three-phase AC-DC converters in this thesis.

It is standard practice to implement AC-DC converters with some sort of power factor correction (PFC) as their AC input side is connected to an AC voltage source and it is desired to draw sinusoidal current with a low harmonic content. Input AC current harmonics do not contribute to the power transfer from the AC input to the DC output and only create power losses and voltage distortion in the source, which is typically the grid. Total harmonic distortion (THD) and power factor (PF) are parameters that are associated with input current distortion and used to compare the performance of an AC-DC system. They are defined as [26]

$$PF = \frac{P}{S} \qquad (1-1)$$

$$THD_I = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots}}{I_1} \qquad (1-2)$$

THD and PF are limited by regulatory standards such as IEC 61000-3-2[27], IEC 61000-3-4[28], and IEEE519[29] whenever an AC-DC converter is supplied from the utility grid.

1.2.1 Two-stage isolated AC-DC converters

As stated in the Introduction to this chapter, AC-DC converters can be either two-stage converters with a front-end AC-DC converter followed by a back-end DC-DC converter or single-stage converters that can simultaneously perform AC-DC and DC-DC converter with just one converter. The standard implementation of a two-stage AC-DC converter with a three-phase AC input is shown in Figure 1.6. The back-end DC-DC converter in this figure is a ZVS-PWM DC-DC full-bridge converter; the front-end converter is a six-switch AC-DC converter that can be operated with PWM. Given that the converter has at least 10 switches, without including any auxiliary circuitry that may be added to improve performance, and that the PWM control of the front-end AC-DC converter can be complicated, researchers have tried to simplify the converter shown in Figure 1.6 by simplifying its topology and/or its control. Efforts to do so have focused on:

- simplifying just the front-end AC-DC converter and maintaining a two-stage topology,
- simplifying the overall converter by proposing alternative single-stage topologies,
- modifying the topology to simplify the control of the converter,
- implementing a combination of these methods.

Examples of modified AC-DC converters are reviewed in the next sections of this chapter.

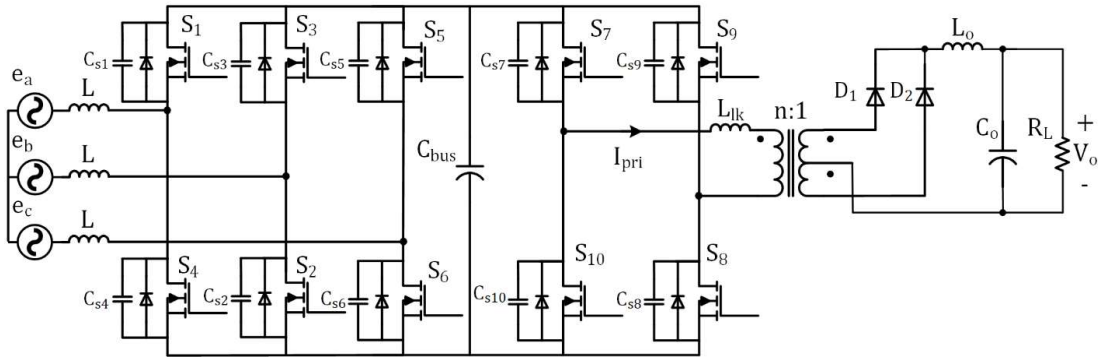


Figure 1.6. circuit diagram of a typical two-stage isolated AC-DC converter

1.2.2 Front-end AC-DC converters for two-stage AC-DC converters

Approaches to simplifying the front-end AC-DC converter of a two-stage AC-DC converter have focused on reducing the number of switches that the front-end converter shown in Figure 1.6 has. Most of these approaches can be categorized as follows:

- Using three separate single-phase AC-DC boost converters as shown in Figure 1.8. Each boost converter module consists of a diode bridge, an input inductor, a

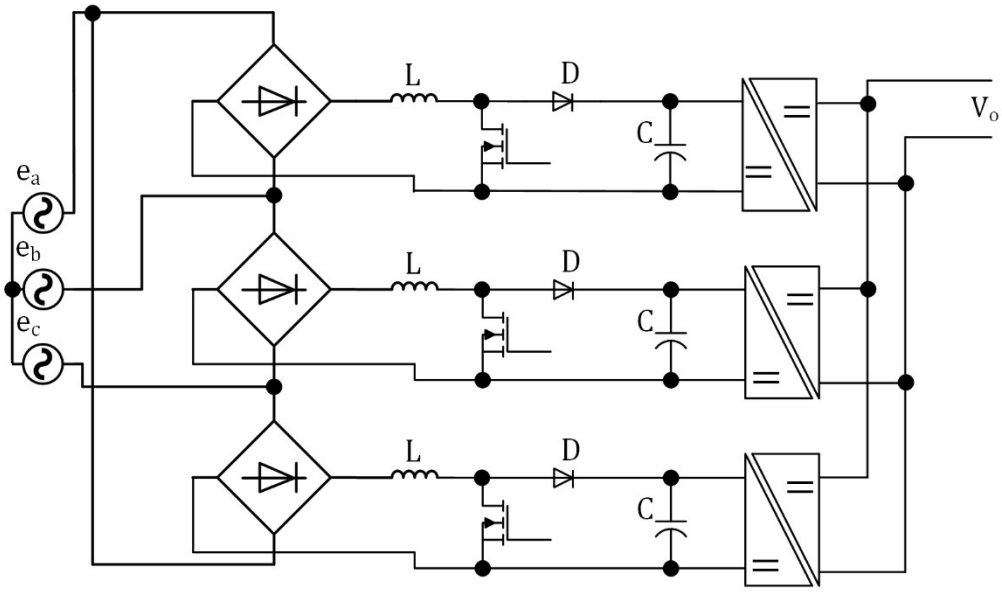


Figure 1.7. Isolate AC-DC converter proposed in [30]

switch, a diode, and a capacitor that acts as a filter. Each converter is implemented with a standard AC-DC boost converter topology or with a topology that is similar to it. Each module works as follows: The input inductor current rises when the switch is turned on and fall when the switch is turned off. By turning the switch on and off in an appropriate manner throughout the input AC line cycle, the input current of a module can be shaped to be sinusoidal and in phase with its input voltage. Each converter can be controlled individually, but its operation needs to be synchronized with the operation of the other modules. The advantages to this approach are that it only needs three active switches and that it is modular and thus can be implemented with commercially available single-phase AC-DC PFC converters. The main drawbacks are that it is expensive as any cost savings obtained from the elimination of three active switches are offset by the need for more passive components and that it can be challenging to synchronize the operation of all three modules, even through the use of sophisticated PWM schemes such as the ones needed to operate the six-switch front-end converter shown in Figure 1.6 are avoided [30].

- Using a single-switch three-phase converter such as the one shown in Figure 1.8 that consists of a diode bridge, three input inductors, a switch, and an output capacitor that acts as an output filter [31]. The converter shown in Figure 1.8 is a boost-type converter, but three-phase single-switch converters have been developed from other topologies such as the buck, buck-boost and Cuk converters [32]–[37]. The converter shown in Figure 1.8 operates as follows: Current in all three input inductors rise when the switch is on and falls when the switch is off as energy is transferred to the output through the diode. If the input currents are discontinuous (i.e. are zero for part of a switching cycle) then they will take the shape of a series of triangular pulses with peaks that are bounded by the input voltage. These input current waveforms are essentially sinusoids with high frequency harmonics that can be filtered out. The advantages of single-switch three-phase converters are that they have a very simple topology and can be operated with very simple control methods – especially since the input current does not have to be monitored or sensed as input PFC can occur naturally as long

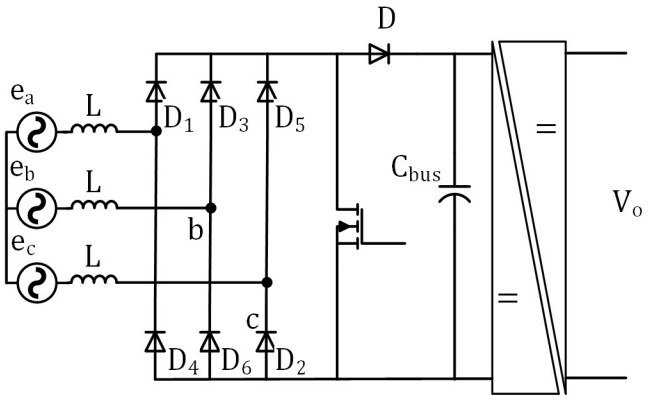


Figure 1.8. Isolate three-phase AC-DC converter with a boost DC-DC stage

as the input currents are discontinuous. The main drawback is that is the converter switch is subjected to high current stresses as the peak current stress is high, since the input current is a set of triangular pulse with high current peaks, and AC-DC power conversion is performed with just one switch. This approach is generally limited to lower power applications where three-phase AC to DC conversion is needed.

- Using a four-switch AC-DC converter as shown in Figure 1.9. This converter can be operated in the same manner as the six-switch front-end converter shown in Figure 1.6 and with the same PWM methods. It is possible to replace two of the switches in the six-switch converter with two capacitors and connect one of the phases to the midpoint of these capacitors instead of to the midpoint of a leg of switches[38], [39]. This is because in a three-phase system, if two of the input currents are controlled, then the third current is constrained so that it does not need to be actively controlled. The main advantage of this converter is that it does require fewer switches. The main drawbacks are that the switches have more stress than the switches in a six-switch converter, although the very high peak current stresses of single-switch three-phase AC-DC converters are avoided, and the control is sophisticated, like that of six-switch AC-DC converters. Moreover, when implemented in a two-stage AC-DC converter, the number of switches in the overall converter remains significant.

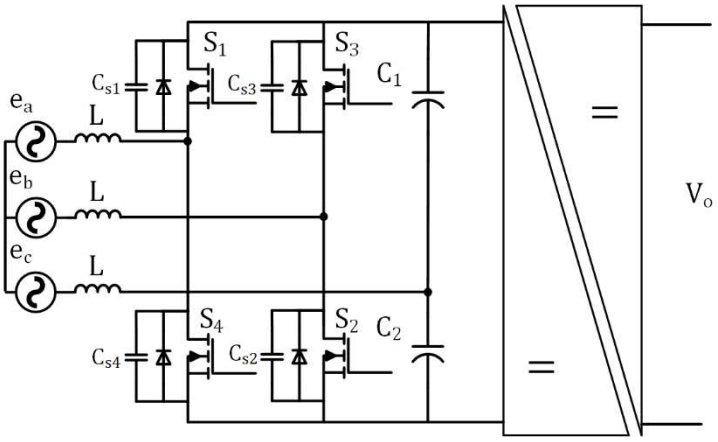


Figure 1.9. Isolate three-phase AC-DC converter by using the reduced switch converter proposed in [38]

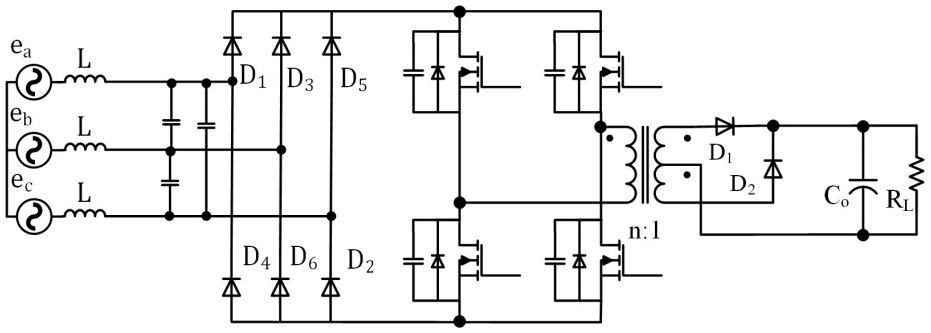
1.2.3 Single stage isolated three-phase AC-DC converters

The standard six-switch topology shown in Figure 1.6 can be further simplified if it is replaced by a single-stage topology. Generally, single-stage topologies fall into one of the following categories:

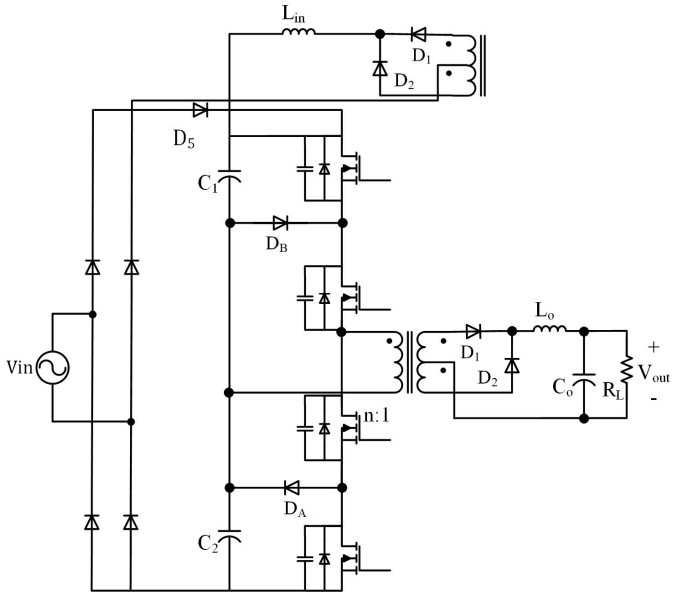
- They are synthesized by combining a single-switch front-end AC-DC converter with a DC-DC full-bridge converter, then removing any redundant components. An example of such a converter is shown in Figure 1.10. This can be done if the original AC-DC front-end converter is made to operate with the same fixed duty cycle as the DC-DC full-bridge converter as this introduces a redundancy in the overall converter that can be eliminated. Since redundant components can be eliminated, the control of the converter can be simplified as well as only one converter stage needs to be controlled instead of two. The main advantage of this approach is that three-phase AC-DC power conversion with isolation can be achieved with just four converter switches and with simple control, unless they are resonant topologies that are operated with a combination of variable-switching frequency control and pulse-width modulation (PWM) [40], [41]. The main drawbacks are that the input currents consist of triangular pulses with high peaks

that are bounded by a sinusoidal envelope, which increases the peak current stress of the converter switches, the converter switches may have to conduct current resulting from both the AC-DC conversion process and the DC-DC conversion process, which increases current stresses, and, if there is an intermediate DC bus voltage, this voltage may become high as it is not regulated since the converter operates with just a single controller that is used to regulate the output voltage. Single-stage converters of this type are generally used for lower power applications.

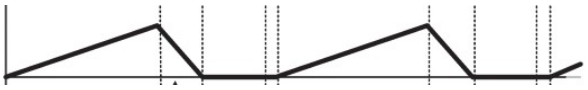
- They still require a significant number of switches, especially when so-called matrix-type topologies, which can require at least six pairs of back-to-back switches (12 switches in total) like the converter shown in Figure 1.11 is used [41]–[43]. In the case of matrix converters such as the one shown in Figure 1.11, power conversion is performed by applying bits and pieces of rectified three-phase AC voltage across the transformer in an appropriate manner. The main advantage of matrix converters is that they are generally more efficient than two-stage converters as power is only processed once by the converter instead of twice by the two stage of a two-stage converter. Moreover, they do not have an input diode bridge that can contribute to conduction losses The main drawback is that the control of these converters can be very sophisticated and the number of converter switches are still significant [44]–[46]. Single-stage converters of this type are generally used for higher power applications.



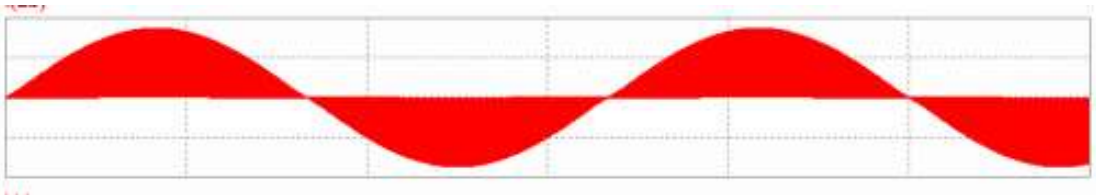
(a). Proposed converter in [111]



(b). Proposed converter in [112]

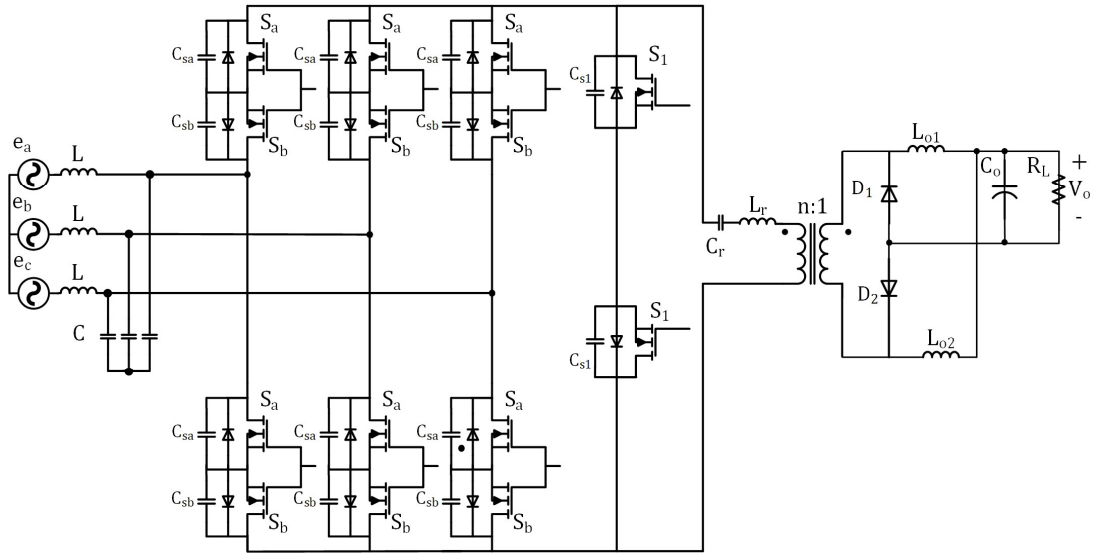


(c) A typical input current waveform in switching frequency scale

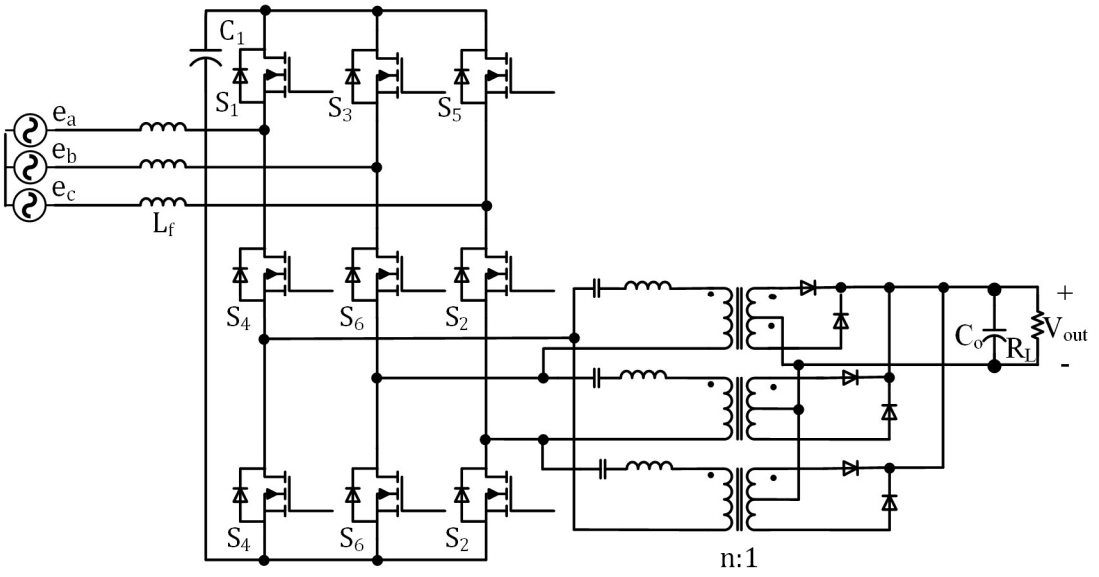


(d) A typical input current waveform in line frequency scale

Figure 1.10. Single stage AC-DC converters and their associated waveforms



(a) Proposed converter in [42]



(b) Proposed converter in [43]

Figure 1.11. Single stage AC-DC converters

1.3 Hybrid AC-DC Microgrids

The use of distributed generation (DG) units in power systems is becoming more popular as they are green, flexible and economical. DGs are connected to the power grid through a power electronic converter, but they are intermittent sources of energy, which creates issues related to system stability, reliability, and power quality. Microgrids (MGs) have been developed to address some of these issues. They are independently operated clusters of small DGs, storage units and loads that can be run either as a stand-alone system (islanded MG) or be connected to a bulk power grid (grid-connected MG), which is more common as this results in higher reliability. MGs increase the resource utilization of small DGs, the resilience of power systems, and the flexibility of system design [1]-[2].

Grid-connected MGs are typically AC MGs (as opposed to DC MGs) since the bulk power system that they are connected to is an AC system. AC MGs, however, have several issues that are related to reactive power, synchronization, and power quality so that the popularity of DC MGs has been increasing as they do not have these issues [49]. Moreover, DC MGs are more efficient than AC MGs as most DG units, energy storage elements, and load work with DC voltage, thus most power conversion losses from AC to DC and vice versa are eliminated [50]. Nonetheless, DC MGs still need to be implemented with AC-DC and DC-AC power converters because they need to be connected to a bulk power AC system to be reliable and some of their DG units and loads require AC voltage to operate and need to be interfaced to DC MGs with power converters.

Hybrid AC-DC MGs (HMGs), which were introduced in [51], combine the advantages of both AC and DC MGs. HMGs consists of two separate sub-grids: an AC sub-grid that is connected to the bulk power system, AC DGs, and loads, and a. DC sub-grid that is connected to DC DGs, energy storage elements, and DC loads. HMGs are more efficient than pure AC or DC MGs because both the AC and DC loads and the DG units are connected to AC and DC sub-grids directly.

In an HMG, both the AC and DC sub-grids can be operated as two separate MGs, with a a unified control strategy that allows power to be transferred between AC and DC sub-grids, which allows AC and DC resources to be managed in a way that makes the operation

of the HMG more efficient and reliable [52]–[57]. This power transfer can be achieved by a bidirectional AC-DC converter that allows power to flow from AC to DC sub-grid and vice versa. This converter is commonly referred to as an interlinking converter (IC) in the literature and is a required element in any HMG, regardless of the complexity of HMG structure. HMG control and operation strategies are designed to optimize the overall system operation and use of AC and DC sub-grid resources, and the output command of the control system is often executed by the IC [51], [58]–[61].

A typical HMG with an AC and a DC sub-grid is shown in Fig. 1. The AC sub-grid consists of an AC bus that is connected to an AC power grid, a typical AC-DG unit, and a lumped AC load that models all AC loads. The DC sub-grid consists of three smaller, generic DC sub-grids that are connected to a common DC main bus. LV BUS-1 models a composite DC sub-grid that consists of a DC DG unit, an energy storage system (ESS), and a lumped load. LV BUS-1 is connected to the main DC bus through a bidirectional DC-DC converter and it injects surplus power or absorbs needed power from the main DC bus. LV BUS-2 models a cluster of DC small DC loads (< 2 kW) that are sensitive to voltage variations such as LEDs. LV BUS-3 models a group of large DC loads (> 2 kW) and has a two level distribution system architecture, which is referred to as an Intermediate Bus Architecture (IBA) in the literature; the IBA is shown in more detail in shown in Fig. 2. The IBA decreases the overall system cost and increases the overall system efficiency for large DC distribution systems (> 2 kW) [62].

In a DC distribution system with an IBA, a front-end converter steps down the main DC bus voltage to the first-level bus voltage and provides galvanic isolation. The first-level bus voltage can be either a semi-regulated DC voltage (i.e. 48V±10%) or a wide range variation voltage (i.e. 36V-75V). Power is distributed among the loads attached to the first-level bus, and a bus converter is used to convert the first-level bus voltage to a regulated secondary bus voltage that is used to supply point-of-load (POL) converters for each load [62]–[65].

In a typical HMG such as the one shown in Fig. 1, a significant number of power electronic converters is needed to supply the DC loads at different voltage levels. This neutralizes

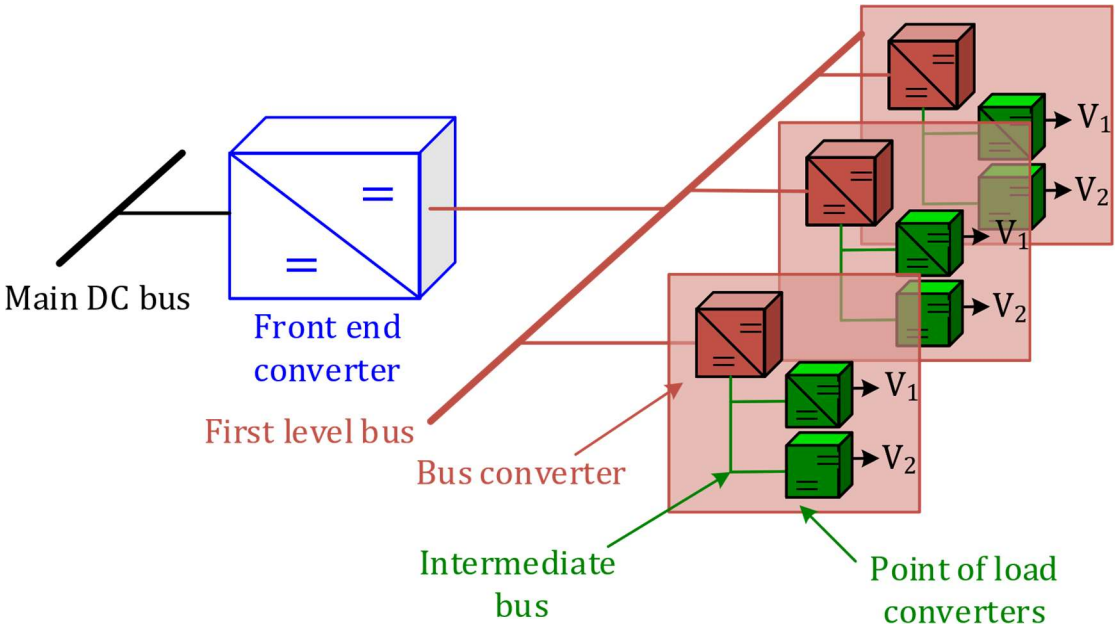


Figure 1.12. DC system with Intermediate Bus Architecture (IBA) [62]

one of the advantages of using HMG, which is that they require fewer power electronic converters than AC MGs or DC MGs. This issue can be addressed by using multi-port converters in an HMG to simplify its HMG architecture and reduce its overall size and cost. Few such converters have been proposed, however, and the ones that have been proposed have at least one of the following disadvantages:

- They need a considerable number of switches as they are interfacing more than one DC bus to three phase systems [66]–[68].
- They need to be operated with very sophisticated control methods so that they can perform AC-DC and DC-DC conversion simultaneously [69]–[71].

1.4 Thesis Objectives

Split DC bus converters are proposed in this thesis to reduce the size and cost of power electronic converters and to improve efficiency. The number of active switches in these converters can be fewer than that of conventional topologies, and/or these switches may be subjected to less voltage stress. The converters presented in this thesis are either completely original or are modified versions of existing topologies.

The main objectives of this thesis are as follows:

- To evaluate the application of split DC bus DC-DC converters as a way of improving light-load efficiency in four-switch PWM full-bridge type converters.
- To evaluate the application of split DC bus DC-DC converters as a way of reducing conduction losses created by freewheeling mode circulating current in four-switch PWM full-bridge type converters.
- To propose a new single-stage AC-DC bridgeless converter with a split DC bus configuration that has galvanic isolation, continuous input current for lower peak stress, and a minimal number of switches.
- To propose a new split DC bus converter that can be used to simplify HMG structures.
- To determine the steady-state characteristics of the new converters proposed in the thesis to derive appropriate design procedures.
- To confirm the feasibility of the proposed converters and the validity of theoretical concept in this thesis with experimental results obtained from proof-of-concept prototypes and simulation results obtained for HMGs.

1.5 Thesis Outline

The thesis consists of the following six chapters. Following is a brief explanation of each chapter.

The focus of chapter 2 is to investigate the properties of a type split DC bus DC-DC converter. This chapter investigates two features of the split DC bus DC-DC converter, including less stress of the switches and reducing circulating current and how these features can be used to improve the DC-DC converter performance.

In Chapter 2, the use of three-level (TL), zero-voltage-zero-current switching (ZVZCS) converters is investigated as a way of improving light-load efficiency in full-bridge

converters with MOSFETS. TL-ZVZCS full-bridge converters are split DC bus converters that are used in high-voltage, high-power applications with IGBT devices, but their use in lower voltage, lower power applications where MOSFETs are generally used has not been investigated. In this chapter, the general operation of an example TL-ZVZCS full-bridge converter is briefly explained and the basic principles as to how it can how improve light-load efficiency are discussed. Experimental results that compare the efficiency of a prototype of the example TL-ZVZCS converter to that of the conventional ZVS-PWM full-bridge and a two-level ZVZCS-PWM converter are presented as well.

In Chapter 3, the operation of the ZVS T-type DC-DC converter, a converter with a split DC bus that has been proposed as an alternative to the conventional ZVS-PWM full-bridge (FB) converter, is reviewed. Although it has a number of advantageous features, the ZVS T-type DC-DC converter is not well known among power electronic engineers working with switch-mode power supplies, and the topology has thus been neglected. In this chapter, the operation of the DC-DC ZVS T-type converter is contrasted to that of the conventional ZVS-PWM-FB DC-DC converter for lower power applications. Results obtained from prototypes of each converter topology are then presented, compared, and discussed, and conclusions which converter is superior for particular applications are made.

In Chapter 4, a new single-stage three-phase AC-DC converter with four switches and galvanic isolation is proposed. The new converter is simple and uses fewer switches than previously proposed AC-DC converters of the same type. It is a bridgeless converter that can operate with continuous input current and with any PWM method suitable for a standard three-phase six-switch voltage source rectifier. In this chapter, the operation, control, analysis and design of the proposed converter are explained and its features are discussed. Experimental results obtained from a prototype that confirm the feasibility of the converter are presented as well.

In Chapter 5, a new split DC bus converter that can be used as an interlinking converter for HMGs is proposed. The new converter, which can be implemented with only 6 active switches and any control method that can be used for conventional six-switch three-phase

AC-DC converters, can replace two converters in HMGs, thus simplifying their structure and reducing their cost. The converter can interface an AC system to a high voltage DC system as a bidirectional converter and to a low voltage isolated DC system as a unidirectional converter. The operation of the novel converter is discussed in detail, and the steady-state converter model is determined. The converter's design procedure is explained and demonstrated with a design example, and feasibility of the proposed converter is confirmed with experimental results from a proof-of-concept prototype, and its operation in a HMG is confirmed with simulation results.

In Chapter 6, the contents of this thesis are summarized, the contributions of this thesis are stated as are suggestions for future work.

Chapter 2

2 Using Multilevel ZVZCS Converters to Improve Light-Load Efficiency in Low Power Applications

2.1 Introduction

The standard ZVS-PWM DC-DC full-bridge converter implemented with MOSFETS as shown in Figure 2.1 is widely used in applications with loads ≥ 500W. Its MOSFET switches can operate with ZVS if inductive energy stored in the transformer leakage inductance (L_{lk}) is used to discharge their output capacitances before they are turned on [72]. When the converter is operating with light loads, however, this energy is not enough and so the switches turn on with switching losses, which results in poor efficiency for light loads. Such efficiency is becoming less acceptable as ever-increasing demands for power are placed on the utility grid to satisfy consumer demands.

In this chapter, the use of three-level (TL), zero-voltage-zero-current switching (ZVZCS) converter topologies that are implemented with IGBTs and that are typically operated at higher power levels (> 1 kW) with high DC input bus voltages (> 800 V) is investigated as a way of improving light-load efficiency in lower power full-bridge PWM converters (< 1 kW) that are implemented with MOSFETs and operated with lower, more standard DC bus input voltages (400 V). The general operation of an example TL-ZVZCS full-

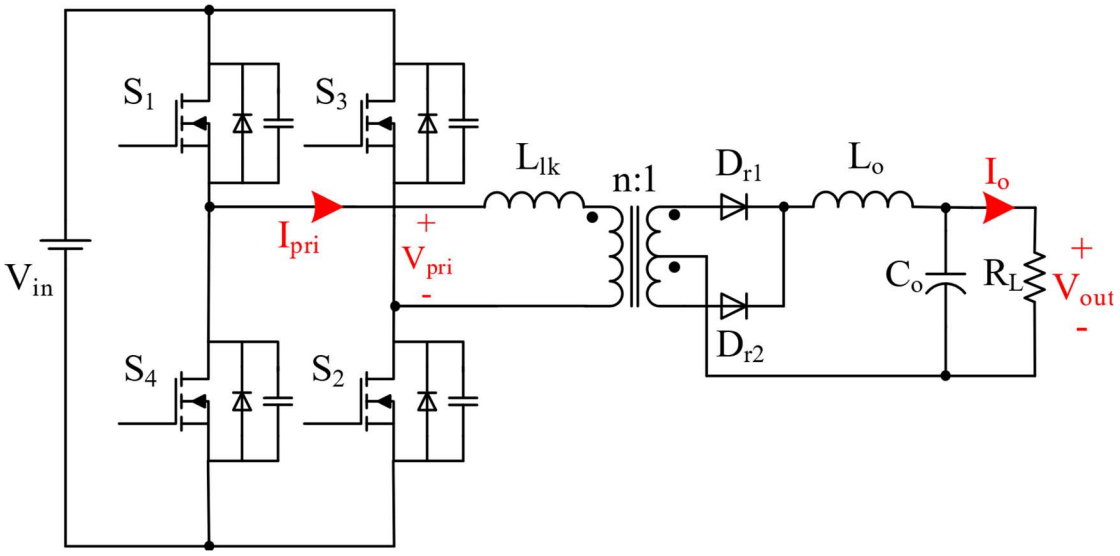


Figure 2.1. FB-ZVS-PWM DC-DC converter

bridge converter is briefly explained in this chapter and the basic principles as to how it can how improve light-load efficiency are discussed. Experimental results that compare the efficiency of a prototype of the example TL-ZVZCS converter to that of the conventional ZVS-PWM full-bridge are presented to confirm the superior light-load efficiency of TL-ZVZCS converters.

2.2 Example TL-ZVZCS DC-DC converter operation

A number of TL-ZVZCS DC-DC converters have been proposed in the literature [7], [73], [74]. The example TL-ZVZCS converter that was used for this study is shown in Figure 2.2; it was selected because it is among the simplest of its type. It is a standard three-level DC-DC converter with a secondary auxiliary circuit that consists of C_{aux}, D_1, D_2 and D_f. Since the operation of the standard three-level DC-DC converter is well-known and can be found in the literature (i.e. [75], [76]), it is only briefly summarized in this section. Only the operation of the secondary auxiliary circuit is discussed in detail.

The example TL-ZVZCS converter Modes of operation for the TL-ZVZCS converter is shown in Figure 2.2. The converter consists of four switches (S_1-S_4), a split-capacitor DC bus (C_1 – C_2), two diodes (D_a – D_b), a transformer, two secondary rectifying diodes (D_{r1}-D_{r2}) and output inductor (L_o), an output capacitor (C_o), and a secondary auxiliary circuit that consists of C_{aux}, D_1, D_2 and D_f.

The converter shown in Figure 2.2 is in an energy-transfer mode that allows energy from the primary to be transferred to the secondary when either S_1 and S_2 or S_3 and S_4 are on. It is in a freewheeling mode when either S_2 or S_3 are on and current just circulates in the primary with no primary/secondary energy transfer taking place. If the input voltage of a TL converter is the same as that of a ZVS-PWM converter, its switches are exposed to less voltage, so that CV^2 turn-on losses are automatically reduced, but exposed to more current and thus more conduction losses as it is essentially a half-bridge converter.

The modes of operation of the example TL converter for a switching cycle are explained below with an equivalent circuit diagram for each The modes of operation of the TL

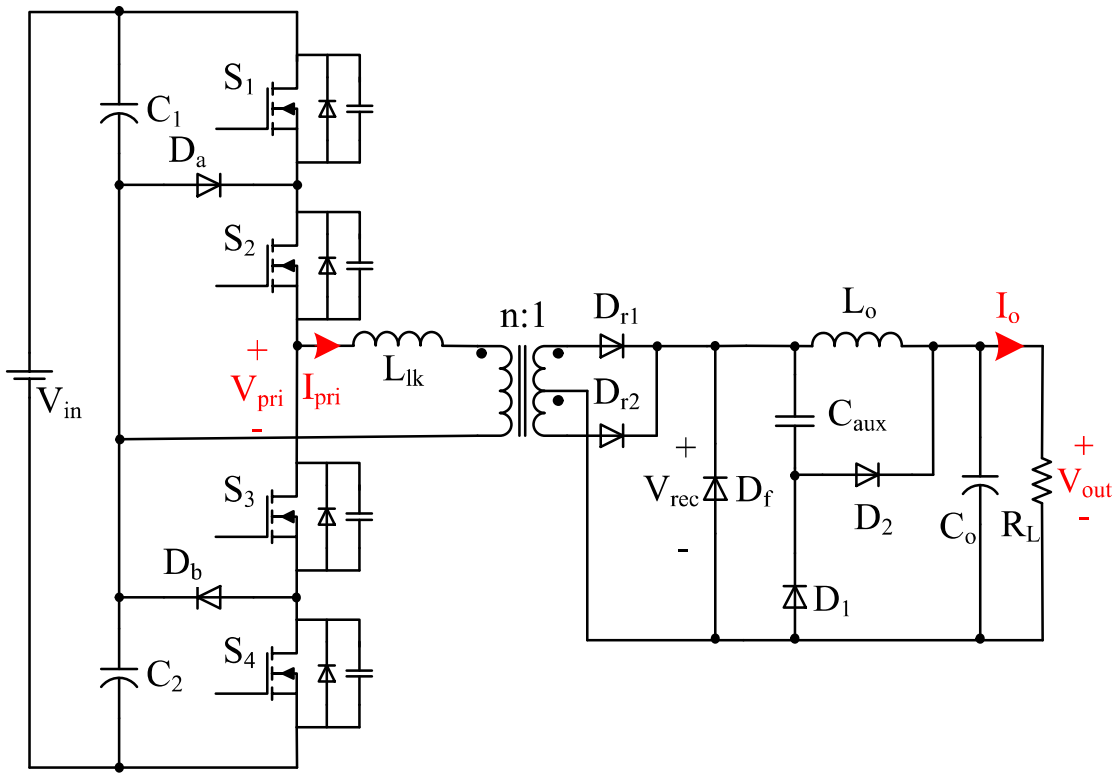


Figure 2.2. TLDC-DC converter with secondary clamp circuit

converter for a switching cycle are explained below with an equivalent circuit diagram for each mode shown in Figure 2.3.

Mode 1 ($t_0 < t < t_1$):

During this mode, switches S_1 and S_2 are turned on with ZCS as there is no primary current at $t=t_0$. Half the input voltage is applied to the transformer primary and the primary current increases linearly. The secondary rectifier output voltage V_{rec} is zero during this mode and secondary current circulates through diode D_f; power is not transferred from the input to the output. The primary current reaches I_o/n, the reflected output inductor current, by the end of this mode.

Mode 2 ($t_1 < t < t_2$):

During this mode, the primary current goes beyond I_o/n and secondary diode D_{r1} conducts. Current flows through a resonant circuit made up of L_{lk} and C_{aux} so that switches S_1 and S_2 conduct a resonant current in addition to the reflected load current. Auxiliary capacitor

C_{aux} charges and D_2 conducts this capacitor's current for a half cycle of resonant frequency and thus the voltage across C_{aux} increases. At the end of this mode, D_2 stops conducting and D_{r1} conducts all the load current and the rectifier output voltage V_{rec} becomes equal to the reflected primary voltage.

Mode 3 ($t_2 < t < t_3$):

During this mode, rectifier diode D_{r1} is on and the power is transferred from the input to the output. No component in the auxiliary circuit conducts current so that the auxiliary circuit can be considered to be disengaged from the converter.

Mode 4 ($t_3 < t < t_4$):

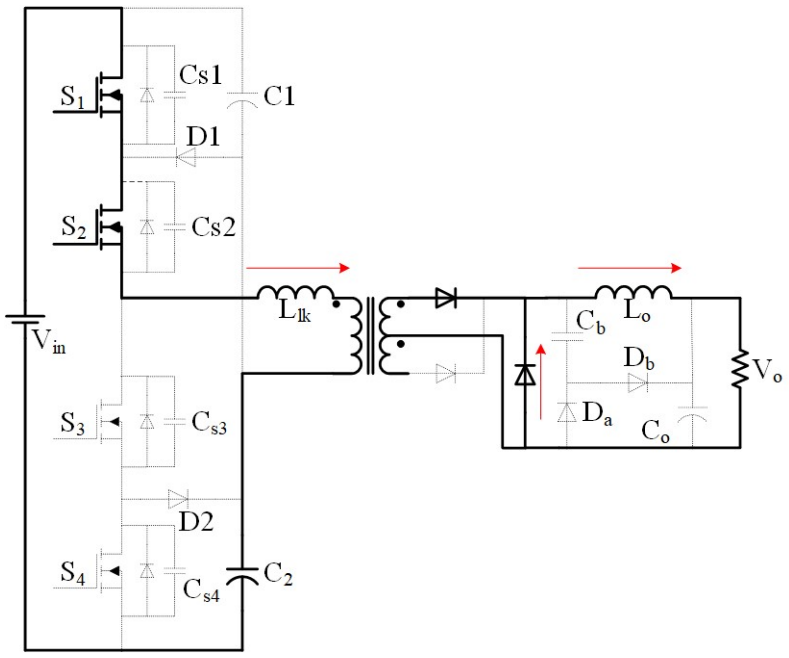
At the start of this mode, S_1 is turned off, but S_2 is still on. The primary current is constant and equal to I_o/n and this current charges the output capacitance of S_1, C_{s1}, linearly. The voltage across the transformer primary voltage decreases as does the rectifier output voltage V_{rec}. At the end of this mode, V_{rec} is equal to the voltage across auxiliary capacitor C_{aux}.

Mode 5($t_4 < t < t_5$):

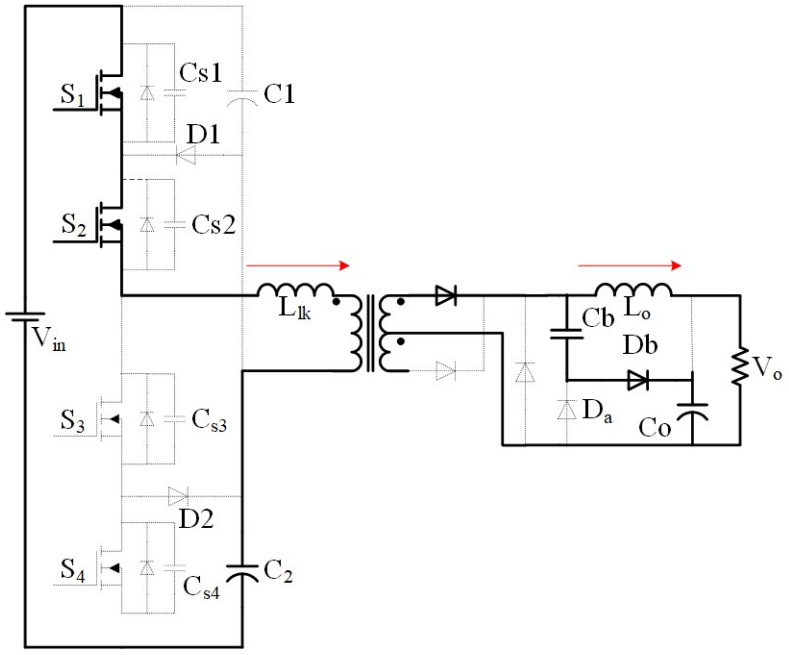
At the start of this mode, since V_{rec} is equal to the voltage across auxiliary capacitor C_{aux} and D_1 starts to conduct and it is no longer reverse biased. C_{aux} supplies the output current and its voltage decreases. The voltage across C_{aux} is reflected to the primary so that it acts as a counter voltage mechanism by which the current that is freewheeling in the primary is reduced. This mode ends when the current in the primary has been fully extinguished.

Mode 6($t_5 < t < t_6$):

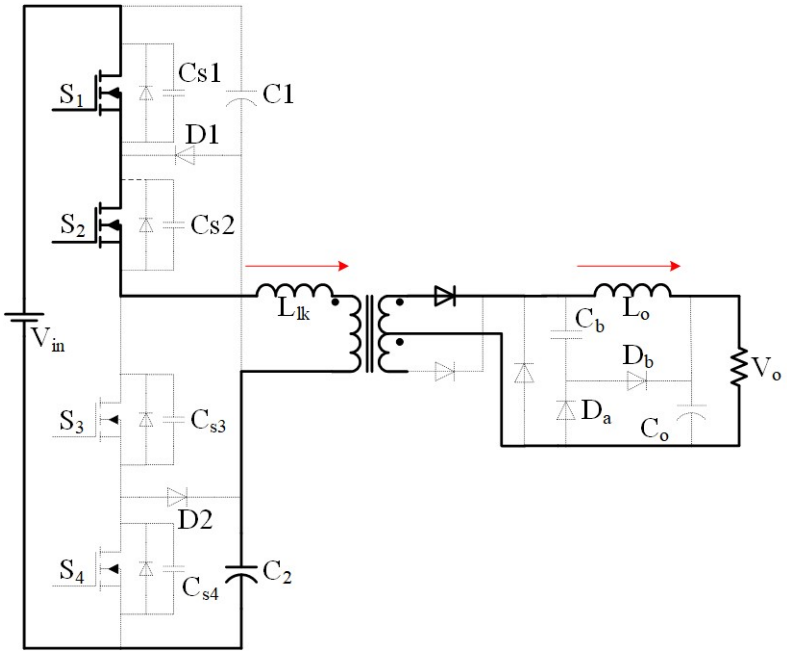
In this mode, the current flowing through the converter's primary is zero and C_{aux} continues to discharge. This mode ends when C_{aux} is fully discharged. During this mode, S_2 can be turned off with ZCS. At the end of this interval freewheeling diode (D_f) will conduct.



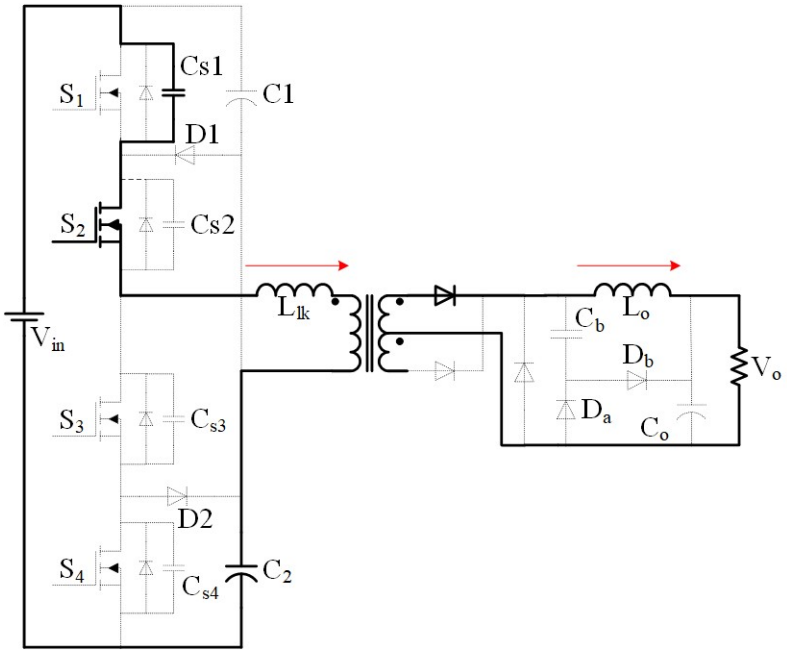
(a) Mode 1 ($t_0 < t < t_1$)



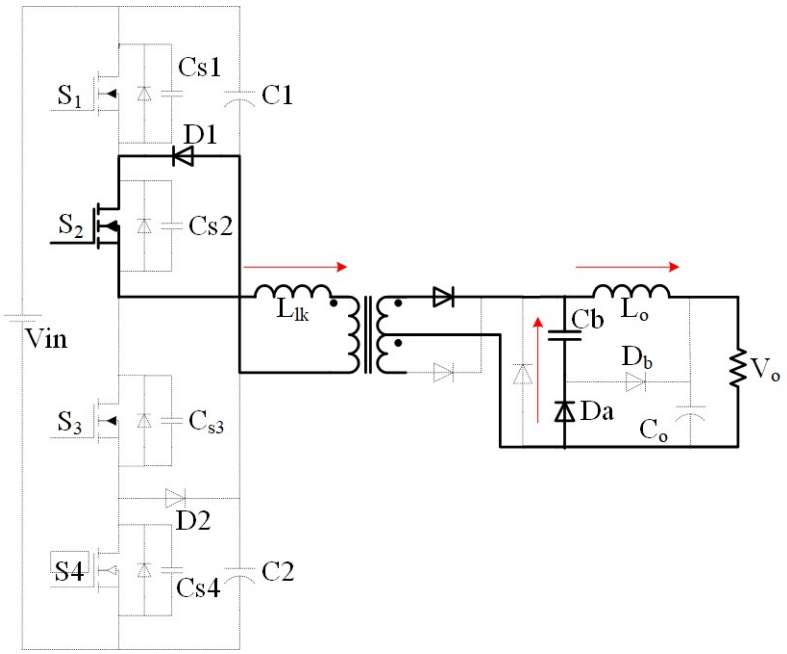
(b) Mode 2 ($t_1 < t < t_2$)



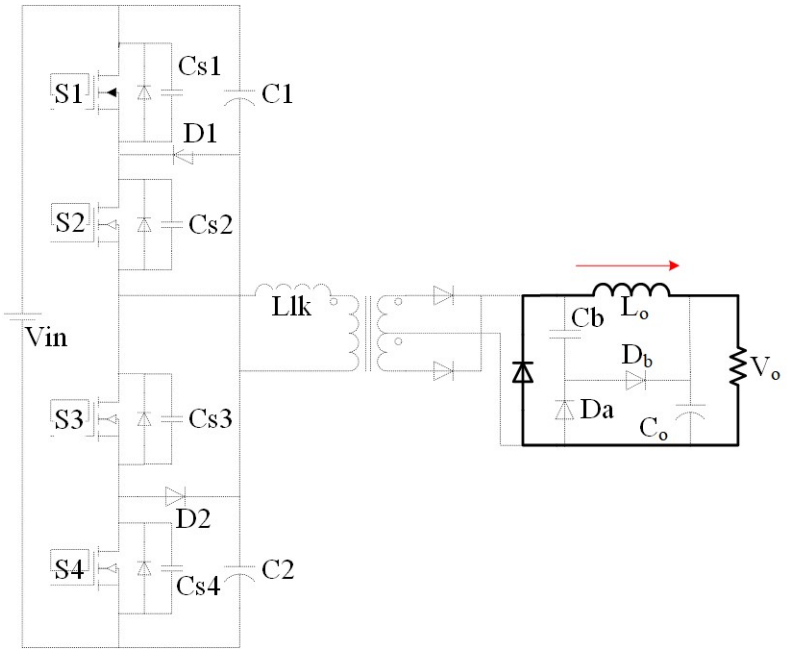
(c) Mode 3 (t2 < t < t3)



(d) Mode 4 ($t_3 < t < t_4$)



(e) Mode 5 ($t_4 < t < t_5$)



(f) Mode 6 ($t_5 < t < t_6$)

Figure 2.3. TL DC-DC converter modes of operation

2.3 Comparison of TL and ZVS-PWM-FB Converters

2.3.1 ZVS range

The minimum leakage inductance needed to achieve ZVS in a standard ZVS-PWM converter can be expressed as [77]

$$L_{lk-mi} = \frac{8}{3.\mathrm{I}_{\mathrm{crit}}^2}.C_{oss}.V_{in}^2 \qquad (2-1)$$

where I_{crit} is the minimal critical/boundary current in the primary for ZVS to be achieved and C_{oss} is the output capacitance of the converter switches. The leakage inductance for the TL-ZVZCS converter, however, can be as small as possible as there is no need for inductive energy to discharge the converter switches because the devices work with virtual ZVS, which will be explained later.

2.3.2 Efficiency

In terms of an efficiency comparison between the standard TL DC-DC converter and the standard ZVS-PWM converter, what this means is that the TL converter has better light-load efficiency than the ZVS-PWM converter. This is because

- Neither converter has sufficient primary transformer inductance energy to discharge the output capacitances of their switches before that are turned on
- The TL converter has less voltage across its switches before they are turned on
- Conduction losses are not dominant at light-load operation. The TL converter has worse heavy-load efficiency than the ZVS-PWM converter because the ZVS-PWM converter can operate with ZVS as there is sufficient primary transformer inductance energy to discharge the output capacitances of its switches before that are turned on; (ii) conduction losses are more dominant at heavy loads and the primary current of the ZVS-PWM converter is half that of the TL converter.

Conduction losses in the TL converter caused by freewheeling primary current can be reduced by adding the passive auxiliary circuit at the secondary to extinguish this current

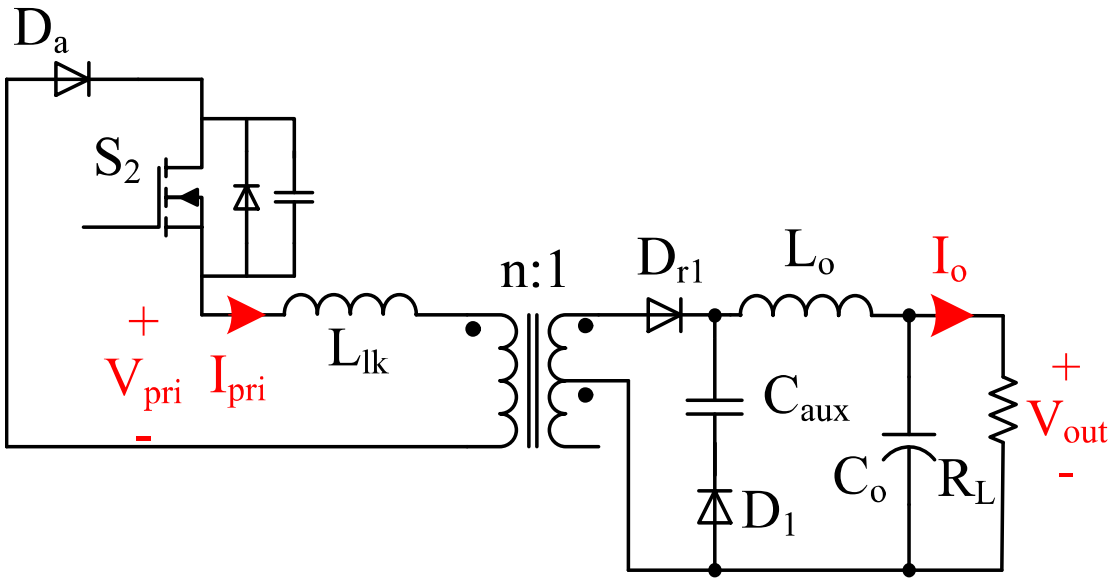


Figure 2.4. Start of freewheeling mode of operation

when the converter is in a freewheeling mode of operation, as shown in Figure 2.4. In Figure 2.4, it can be seen that (i) output current circulates though D_1 and C_{aux} and (ii) C_{aux}, which has been charged from a previous mode, is placed across the transformer's secondary winding. The voltage across C_{aux} is reflected to the primary winding where it puts a negative voltage across the leakage inductance, thus extinguishing the current in the primary eventually. The required time to extinguish the leakage inductance current can be expressed as

$$\Delta t = \frac{< I_{L_o} > L_{lk}}{nV_{C_{aux(t2)}}} \qquad (2-2)$$

where $V_{C_{aux(t2)}}$ is the value of $V_{C_{aux}}$ at t_2, and $< I_{L_o} >$ is the average output inductor current. C_{aux} resonates with L_{lk} at the start of a power transfer mode for a half cycle of their resonant frequency and the voltage across C_{aux} becomes twice the voltage across the tank. Since $V_{C_{aux}}$ does not change from t_1 to t_2, the $V_{C_{aux(t_1)}} = V_{C_{aux(t_2)}}$. $V_{C_{aux(t_1)}}$ can be expressed as

$$V_{C_{aux(t_1)}} = 2.\left(\frac{V_{in}}{2n} - \mathrm{V_o}\right) \qquad (2-3)$$

Since a portion of the load current flows through C_{aux} at the start of a power transfer mode, $< I_{L_o} >$ can be expressed as

$$< I_{L_o} >= I_o - 2f_{sw}C_{aux}\left(\frac{V_{in}}{2n} - \mathrm{V_o}\right) \qquad (2-4)$$

Using the following definition,

$$I_o = \frac{V_o}{R_L} = \frac{\left(\frac{V_{in}D}{2n}\right)}{R_L} \qquad (2-5)$$

By combining Eq. (2), Eq. (3), Eq (4) and Eq. (5), the time needed to extinguish the current can be expressed as

$$\Delta t = \frac{L_{lk}[\frac{D}{2} + f_{sw}C_{aux}(D-1)R_L]}{nR_L(1-D)} \qquad (2-6)$$

Afterwards, with no current flowing in the primary, the DC bus voltage is evenly divided across the four switches so that the voltage across each switch only has $V_{in}/4$ volts across it when it is turned on.

Typical converter waveforms are shown in Figure 2.5 The following should be noted:

- The drain-source voltages of S_3 and S_4 are identical to those of S_2 and S_1 respectively, but phase-shifted by 180°.
- Unlike a ZVS-PWM full-bridge converter, the gating signals of S_1 and S_4 have a pulse width of less than 50%. It is this pulse width that sets the converter's duty cycle.
- The converter switches turn on with virtual ZVS. Since each switch is turned on with $V_{in}/4$ volts across it, the CV^2 losses of a switch are naturally reduced to 1/16 (6%) of those of a switch in a ZVS-PWM converter. Since this 6% can be considered practically negligible, it can be said that the converter switches operate with virtual ZVS.

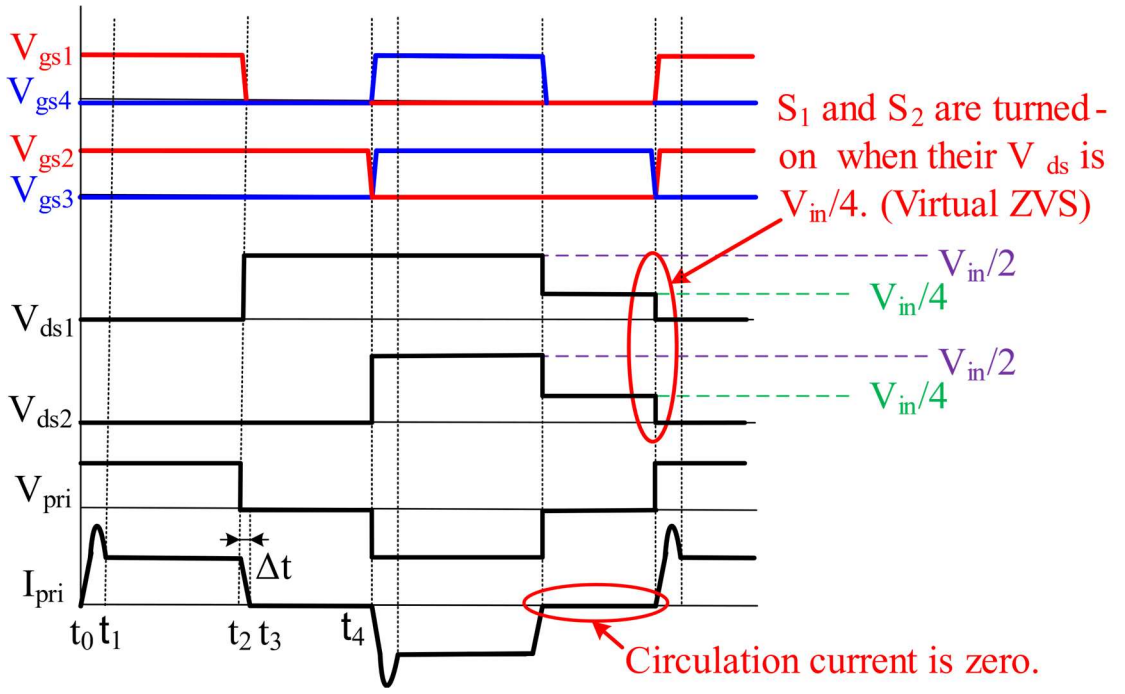


Figure 2.5. Typical waveforms of the TL DC-DC converter

- When a full-bridge converter is operating with light-loads, it operates with a small duty cycle so that freewheeling modes (and thus the flow of freewheeling mode circulating current) occur for most of the switching cycle. The secondary auxiliary circuit helps to further increase light-load efficiency by eliminating any circulating current during freewheeling modes of operation. This allows the converter switches to operate with ZCS and virtual ZVS when the converter is operating with light loads.

- The primary current has some resonant humps in its waveform. This is due to the charging of C_{aux} as the converter gets out of a freewheeling mode.

- More details about how the auxiliary circuit can extinguish primary current can be found in [78], which shows a two level full-bridge converter with the same auxiliary circuit (2L-ZVZCS-PWM converter).

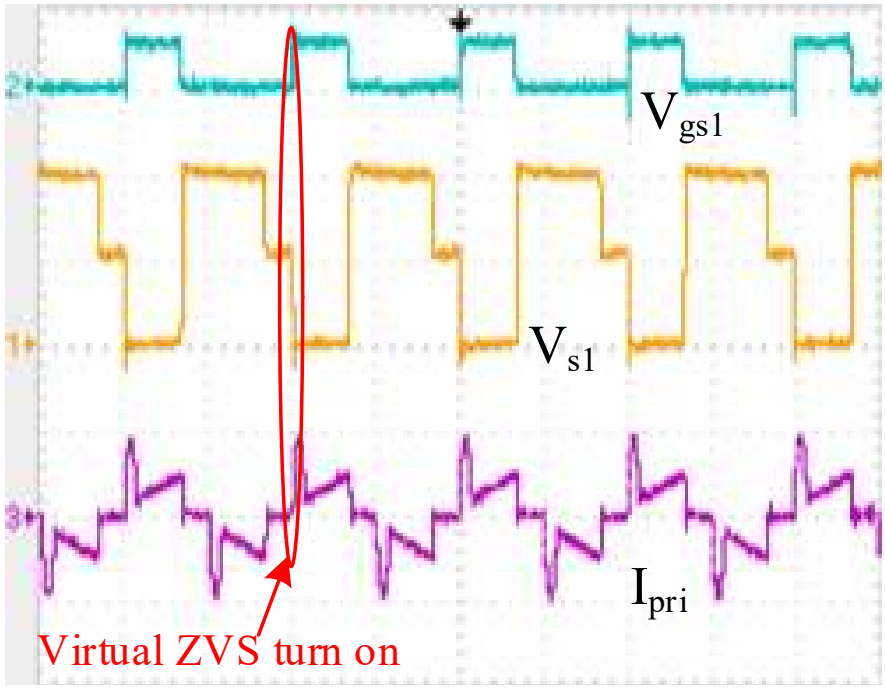
2.4 Experimental Results

Prototypes of the example TL-ZVZCS converter, the standard ZVS-PWM full-bridge converter, and the 2L-ZVZCS-PWM converter in [78] were built to compare their

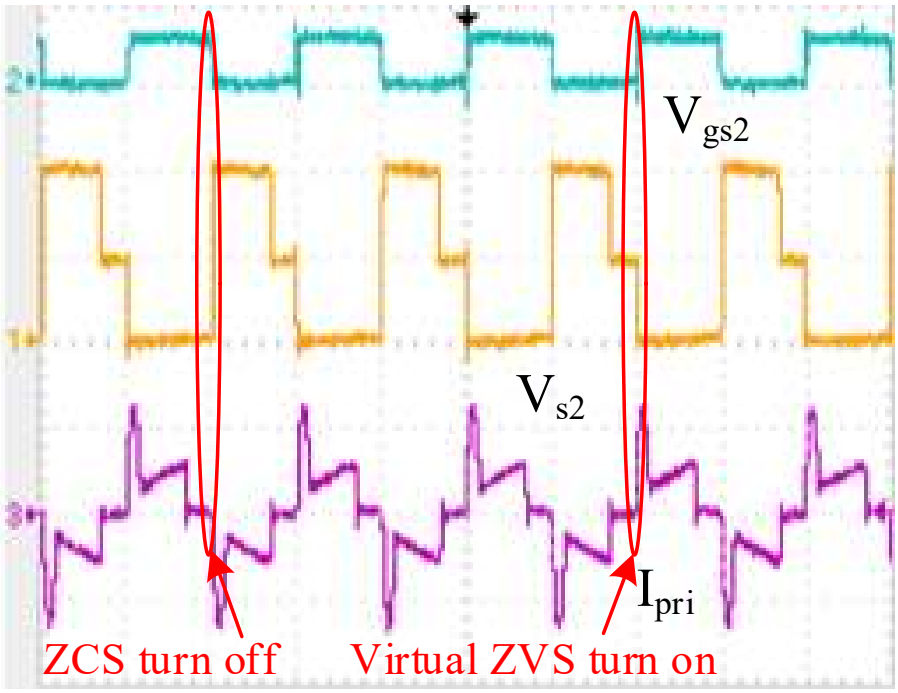
efficiency. The specifications of the prototypes were: Input voltage V_{in} =400V, the output voltage V_o = 48 V, maximum output power $P_{o,max}$ = 900W, switching frequency, f_{sw} = 50 kHz. For the ZVS-PWM converter prototype and the 2L-ZVZCS-PWM converter, FDP18N50 MOSFETS were used as the main switches and RURG3060 diodes were used as the secondary rectifier diodes. For the TL-ZVZCS converter prototype, FDP51N25 MOSFETS were used as the main switches, BYV29 were used as primary side diodes and secondary diodes are same as the two level converters. The ZVS-PWM converter was designed according to [79], the 2L-ZVZCS-PWM converter was designed according to [78], and the TL-ZVZCS converter was designed according to [75] with the secondary auxiliary circuit designed according to [78].

It should be noted that the MOSFETs used as the switches in the TL-ZVZCS prototype had lower voltage ratings than those used as the switches in the two-level prototypes as they need to block only half the DC bus voltage. Such MOSFETs usually have superior switching characteristics and lower on-state drain-source resistance than MOSFETs with higher voltage ratings, and this can partially offset the drawbacks associated with higher primary current that can still exist in TL converters.

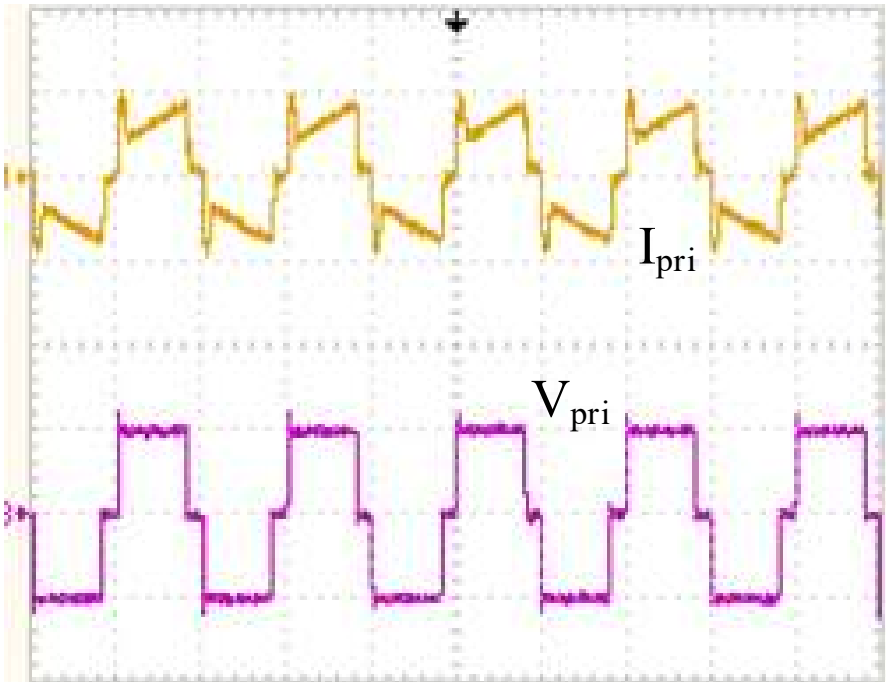
Error! Reference source not found. shows various voltage and current waveforms for the example TL-ZVZCS converter (Figure 2.2) operating at 100 W load in **Error! Reference source not found.**(a) and **Error! Reference source not found.**(b) and at 250 W load in **Error! Reference source not found.**(c). It can be seen that: the peak switch voltage is 200 V (50% of the DC bus voltage), the voltage across the S_1 and S_2 switches when they turn on is half of that (25% of the DC bus voltage) so that they turn on with just 6% of the typical turn-on losses (virtual ZVS), that the primary current falls to almost zero in the freewheeling mode, with the remaining current being just the transformer magnetizing current, and that the primary current has a resonant hump due to the charging of C_{aux}.



(a) (Vgs1:25V/div., Vs1:200V/div., Ipri:1A/div., t:10µs/div.)



(b) (Vgs1:25V/div., Vs1:200V/div., Ipri:1A/div., t:10µs/div.)



(c) (Vgs1:25V/div., Vs1:200V/div., Ipri:1A/div., t:10µs/div.)

Figure 2.6. TL-ZVZCS converter waveforms

Efficiency curves are shown in Figure 2.7 for the three converters; the following should be noted:

- The TL-ZVZCS converter has the better light-load efficiency. As mentioned above, this is because its switches operate with virtual ZVS and with ZCS under light-load conditions. It has no freewheeling mode circulating current thus less conduction losses.

- All two converters operate with nearly identical medium-load efficiency. The two, two-level converters operate with slightly higher heavy-load efficiency. This is because the TL-ZVZCS converter has more conduction losses due to the fact that it essentially has a half-bridge topology so that its primary current is double that of the ZVS-PWM converter. Moreover, the freewheeling mode of operation is short when the converter is operating with heavy loads so that the amount of time that freewheeling current circulates in the primary is short as well. This means that

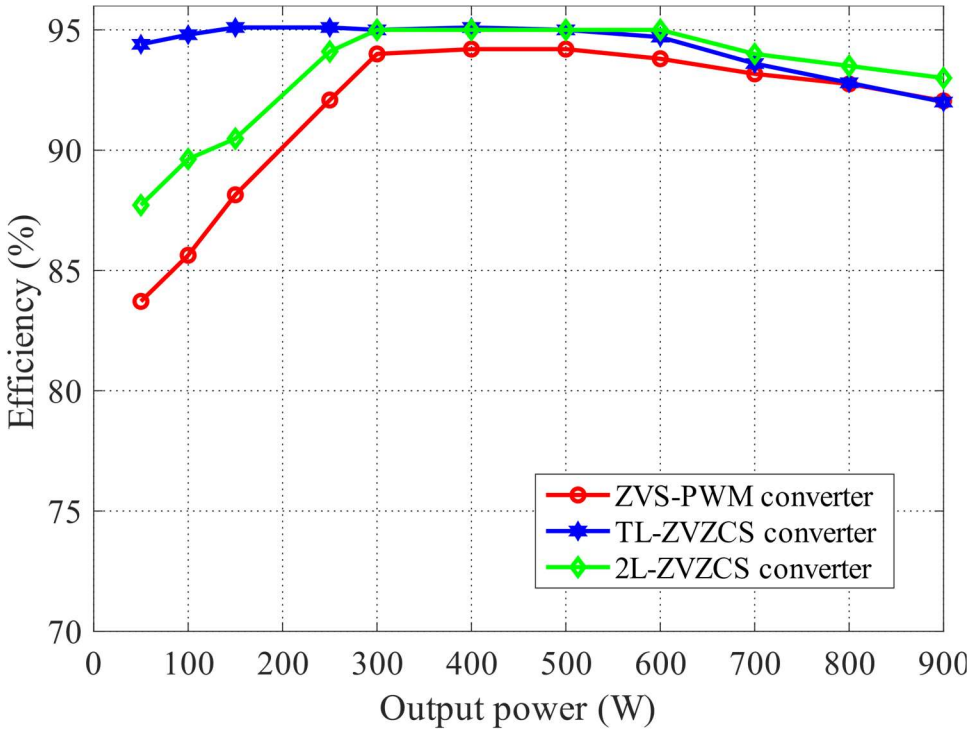


Figure 2.7. Three-level and two-level converter efficiency comparison

few losses are actually saved by the elimination of primary circulating current by the auxiliary circuit.

- The passive auxiliary circuit in the ZVZCS converters allows the secondary diodes to turn off softly, which is not the case for these diodes in the ZVS-PWM converter. The loss of ZVS of two of the switches in the 2L-ZVZCS converter is offset by the savings in efficiency due to reduced current-related losses. This is why the two two-level converters have comparable heavy-load efficiency.

- The TL-ZVZCS converter has some extra components compared to the ZVS-PWM converter: two diodes in the primary side and three diodes and a capacitor in the secondary side. Most of these components are relatively inexpensive components that can be offset by using cheaper MOSFETs with lower voltage ratings. The auxiliary circuit is analogous to the ones added to PWM DC-DC boost converters to allow their main switch to operate with ZVS (i.e.[17]-[18]) except that the auxiliary circuit is purely passive and the result is superior light-load performance.

- If desired, other, more sophisticated auxiliary circuits that make the converter into a ZVZCS converter can be used, such as the one proposed in [82], [83], which is an active auxiliary circuit that causes the primary current to have a much smaller resonant hump. The passive secondary auxiliary circuit used for the ZVZCS converter in this study was chosen because it was the simplest approach to ZVZCS operation.

2.5 Conclusion

This chapter was a study of how TL-ZVZCS converter topologies, which are typically used in high voltage / high power applications can be used to improve the light-load efficiency of full-bridge converters that are implemented with MOSFETs. Light-load efficiency has become a source of concern in recent years due to vast proliferation of power converters supplied by the utility grid and the fact that power converters often do not operate at full load, or even medium load. The compared the efficiency of an example TL-ZVZCS converter to that of a standard ZVS-PWM full-bridge converter.

In this chapter, the general operation of an example TL-ZVZCS converter was briefly explained as was how its MOSFET switches can naturally operate with virtual ZVS and with ZCS. Efficiency results of the two converters were then presented. These results showed that the example TL-ZVZCS converter has a much better light-load efficiency (about 10% better) than the ZVS-PWM converter, an identical medium-load efficiency, and a slightly worse heavy-load efficiency (about 1%).

It should be noted that the novelty of this chapter is not with the topology, as TL-ZVZCS converters are well-known in the literature, but with the use of such converters to improve light-load efficiency. Further improvements in light-load efficiency can be achieved more sophisticated control methods such as burst-mode control if desired. Any additional method that can be used to improve light-load efficiency in a ZVS-PWM converter can be used to improve light-load efficiency in a TL-ZVZCS converter.

It should be noted that the novelty of the research is not with the example TL-ZVZCS topology, but with the way this topology is used to improve light-load efficiency in lower power full-bridge converters with MOSFETs.

Chapter 3

3 A Study of T-Type and ZVS-PWM Full-Bridge Converters for Switch-Mode Power Supplies

3.1 Introduction

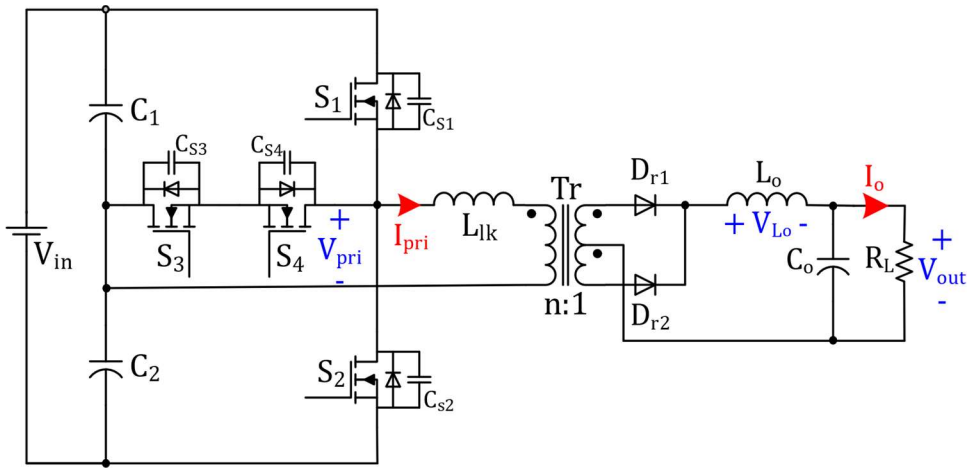
An alternative to the conventional ZVS-PWM-FB DC-DC converter was proposed in [84]. This converter, shown in Figure 3.1. The ZVS T-type DC-DC converter(a), has its roots in the T-type inverter topology that was proposed in [85] and thus was called a T-type DC-DC converter by the authors of [84]. Like the conventional ZVS-PWM-FB DC-DC converter, the switches of the T-type DC-DC converter can also operate with ZVS. Although the authors explained the operation of the DC-DC ZVS T-type converter, analyzed its steady-state characteristics, and confirmed its feasibility with experimental work, no comparison between its performance and that of the conventional ZVS-PWM-FB DC-DC converter was made. As a result, this topology has been neglected in the power electronics literature even though it has a number of features that may make it superior to the conventional ZVS-PWM-FB DC-DC converter for particular operating conditions.

In this chapter, the operation of the DC-DC ZVS T-type converter is reviewed and contrasted to that of the conventional ZVS-PWM-FB DC-DC converter. The implementation of prototypes of each of the two converter topologies is then explained, and experimental results obtained from each prototype are presented. These two sets of experimental results are discussed and compared and conclusions about the performance to the two converters, which converter is superior to the other under which operation conditions, are made. The work presented in this chapter is an extension of work that was previously presented in [86], but with more detailed explanations, more analysis, and more experimental work.

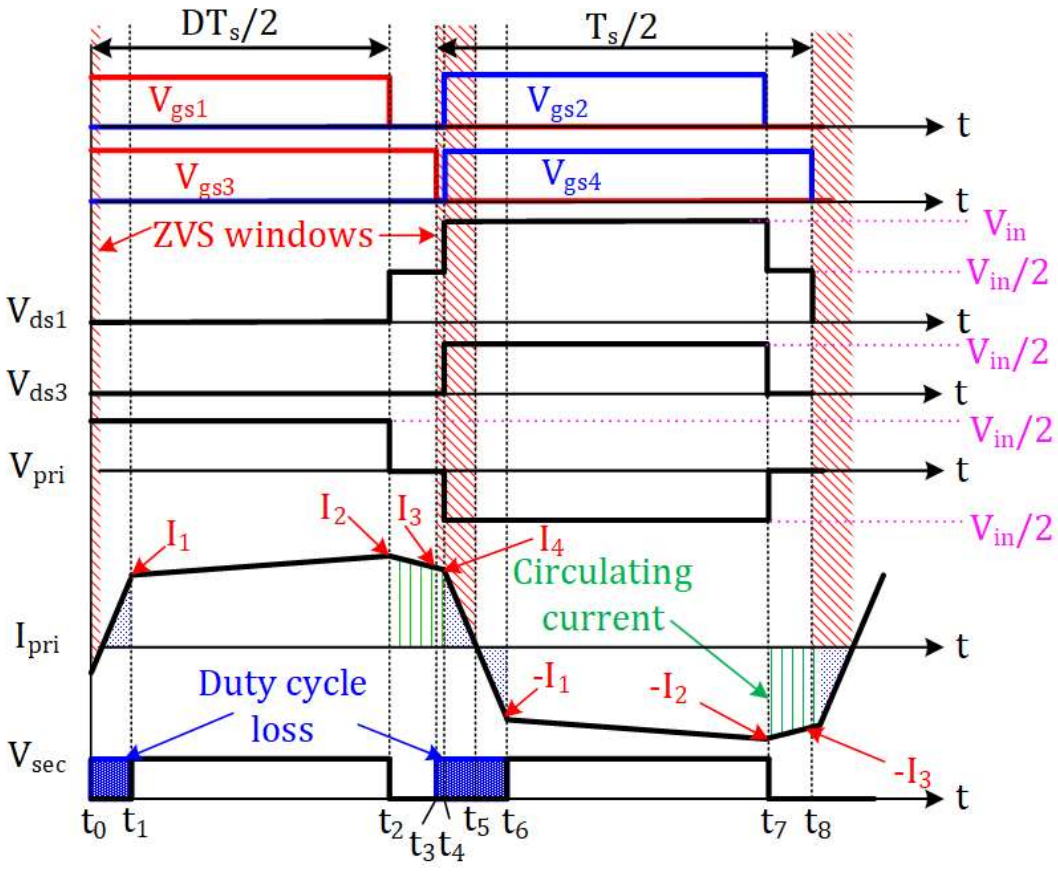
3.2 Operation Principles

The DC-DC ZVS T-type converter, shown in Figure 3.1(a), has four switches (S_1-S_4), a split-capacitor DC bus ($C_1 – C_2$), a transformer, two secondary rectifying diodes (D_{r1}-D_{r2}) and output inductor (L_o) and an output capacitor C_o). S_1 and S_2 are connected together as

one converter leg just as in a conventional ZVS-PWM-FB converter. The other two switches, S_3 and S_4, are connected in series with each other with one end of the combined series combination connected to one end of the transformer (with its leakage inductance L_{lk} has shown separately) and its other end to the mid-point of the two bus capacitors in a T-type configuration. The secondary side of the converter is identical to that of a conventional ZVS-PWM-FB converter.



(a) Converter schematic



(b) Typical waveforms

Figure 3.1. The ZVS T-type DC-DC converter

The converter operates as follows: Voltage is impressed across the transformer primary whenever S_1 or S_2 is on. In this case, one end of the transformer primary will have a voltage that will either be the DC bus voltage or zero voltage and the other end of the primary will have a voltage that is half the DC voltage; note that the voltage at this end of the primary will be fixed and will always be half the DC bus voltage $V_{in}/2$. As a result, a voltage of $V_{in}/2$ will be impressed across the transformer primary, either with positive polarity if S_1 is on or with negative polarity if S_2 is on. This primary voltage is stepped down by the transformer, rectified by the secondary diodes and filtered by the output LC filter. The converter is in an energy-transfer mode of operation whenever S_1 or S_2 is on. The converter is in a freewheeling mode of operation when both S_1 and S_2 are off, and either S_3 or S_4 is on, depending on the direction of the current that circulates in the converter. In this mode, the current will flow through one switch and through the body-diode of the other switch and the voltage impressed across the transformer primary will be zero.

The modes of operation of the T-type converter for a switching cycle are explained below with an equivalent circuit diagram for each mode shown in Figure 3.2.

Mode 1 ($t_0 < t < t_1$):

During this mode, the primary voltage is applied to the leakage inductance (L_{lk}) and I_{pri} increase with the rate of $V_{in}/(2L_{lk})$. The primary current (I_{pri}) is less than I_o/n due to switch S_1 being turned on in a previous mode. In the output side, the energy transferred from the output inductor to the output capacitor and load. $I_{pri}(t)$ in this mode can be expressed as

$$I_{pri}(t) = (-I_4) + \frac{V_{in}}{2L_{lk}}(t) \qquad (3-1)$$

This mode ends when the I_{pri} becomes equal to $I_1(I_o/n)$.

Mode 2 ($t_1 < t < t_2$):

During this mode, switch S_1 conducts current. Half the input voltage is applied to the transformer primary and I_{pri} increases. Energy is transferred from the input side to the

output inductor and the load. At the secondary side, D_{r1} is conducting, and energy is transferred to the load. $I_{pri}(t)$ in this mode can be expressed as

$$I_{pri}(t) = I_1 + \frac{\left(\frac{V_{in}}{2} - nV_o\right)}{L_o} t \qquad (3-2)$$

The primary current reaches I_2 at the end of this mode.

Mode 3 ($t_2 < t < t_3$):

This mode begins when switch S_1 is turned off. I_{pri} is positive, and it continues to flow through the S_3 (which was turned on during Mode 1 and the body diode of S_4. This mode is a freewheeling mode as the transformer primary voltage (V_{pri}) is zero. At the secondary side, the output inductor current circulates through D_{r1} and D_{r2}. $I_{pri}(t)$ in this mode can be expressed as

$$I_{pri}(t) = I_2 e^{-\left(\frac{R_{DS_3}}{L_{lk}}\right)t} \qquad (3-3)$$

The primary current reaches I_3 at the end of this mode.

Mode 4 ($t_3 < t < t_4$):

At the start of this mode, S_3 is turned off, $I_{pri}(t) = I_3$, and the primary current is divided among C_{s1}, C_{s2}, and C_{s3}. Considering the initial voltage of the parasitic capacitors are 0, $\frac{V_{in}}{2}$, and V_{in}, respectively for C_{s1}, C_{s2}, and C_{s3}. $I_{pri}(t)$ in this mode can be expressed as

$$I_{pri}(t) = I_3 \cos \omega_0(t) \qquad (3-4)$$

where ω_0 is the angular resonance frequency between leakage inductance and MOSFET's output capacitance.

$$\omega_0 = \frac{1}{\sqrt{L_{lk}(C_{s1} + C_{s2} + C_{s3})}} \qquad (3-5)$$

At the end of this mode, the primary current reaches I_4. The necessary condition for ZVS operation is that the voltage across the C_{s2} falls to zero before turning on S_2. The voltage across the C_{s2} can be expressed as

$$V_{C_{S_2}}(t) = \frac{V_{in}}{2} - \int_0^t \frac{C_{s2} \times I_{pri}(\tau)}{(C_{s1} + C_{s2} + C_{s3})} d\tau = \frac{V_{in}}{2} - \frac{C_{s2} \times I_3 \sin\omega_0(t)}{(C_{s1} + C_{s2} + C_{s3})} \quad (3-6)$$

Two conditions should be satisfied in order to achieve ZVS in S_2:

The leakage inductance energy should be enough to discharge C_{s2} and charge C_{s1} and C_{s3}.

There must be a minimum deadtime between the turn-off of S_3 and the turn-on of S_2 to allow the output capacitor of S_2 to be discharged.

The minimum value of the required inductive energy can be determined as follows:

$$\frac{1}{2} L_{lk} I_2^2 \geq \left(\frac{V_{in}}{2}\right)^2 \left(\frac{2}{3} C_{s1} + \frac{2}{3} C_{s2} + \frac{2}{3} C_{s3}\right) \quad (3-7)$$

The minimum deadtime for successful ZVS should be equal or larger than the time that is needed to discharge C_{s2} to zero. The time can be determined by rearranging (6) as follows:

$$t_{dt} \geq \frac{1}{\omega_0} \sin^{-1}\left(\frac{V_{in}(C_{s1} + C_{s2} + C_{s3})}{2C_{s2}}\right) \quad (3-8)$$

Mode 5 ($t_4 < t < t_5$):

At the start of this mode, S_2 and S_4 are turned on with ZVS, but only S_2 conducts. A voltage of $-V_{in}/2$ is applied to the leakage inductance and since the primary current (I_{pri}) is more than $-I_o/n$, no energy is transferred to the output. In the output side, energy is transferred from the output inductor to the output capacitor and load. This mode ends when I_{pri} becomes equal to $-I_o/n$.

Mode 6 ($t_5 < t < t_6$):

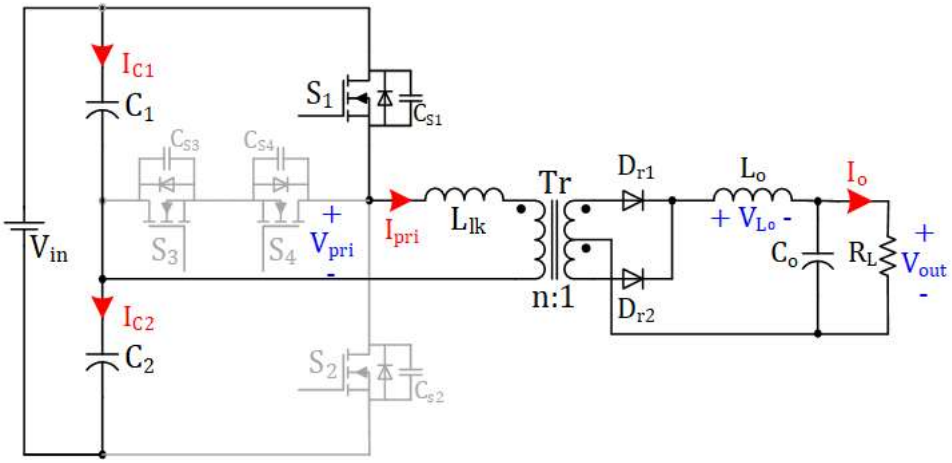
During this mode, switch S_2 is conducting current. Half the input voltage is applied to the transformer primary and I_{pri} decreases at the rate of $-(V_{in}/(2n)-V_o)/L_o$. Energy is transferred from the input side to the output inductor and the load. At the secondary side, D_{r2} is conducting, and energy is transferred to the load.

Mode 7($t_6 < t < t_7$):

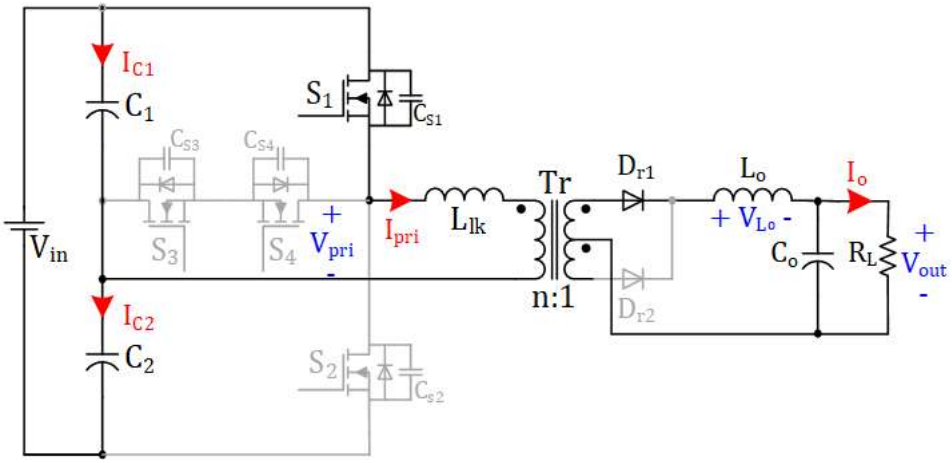
This mode begins when switch S_2 is turned off. I_{pri} is negative and continues to flow through S_4 (which was turned on during Mode 5) and the body diode of S_3. This mode is a freewheeling mode as the transformer primary voltage (V_{pri}) is zero. At the secondary side, the output inductor current circulates through D_{r1} and D_{r2}.

Mode 8($t_7 < t < t_8$):

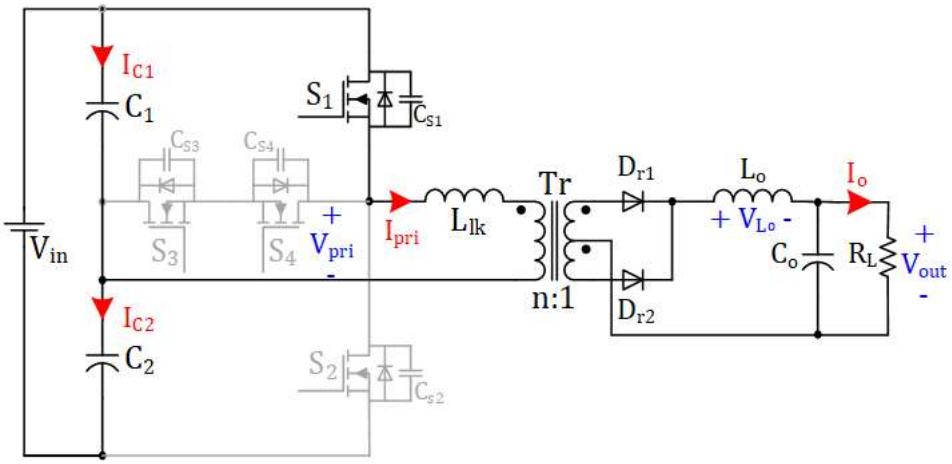
At the start of this mode, S_4 is turned off. I_{pri} is negative, and this current discharges the parasitic capacitor of S_1. Current then flows through the body diode of S_1 and S_1 can be turned on with ZVS. Once S_1 is turned on, the converter enters to Mode 1, and another switching cycle begins.



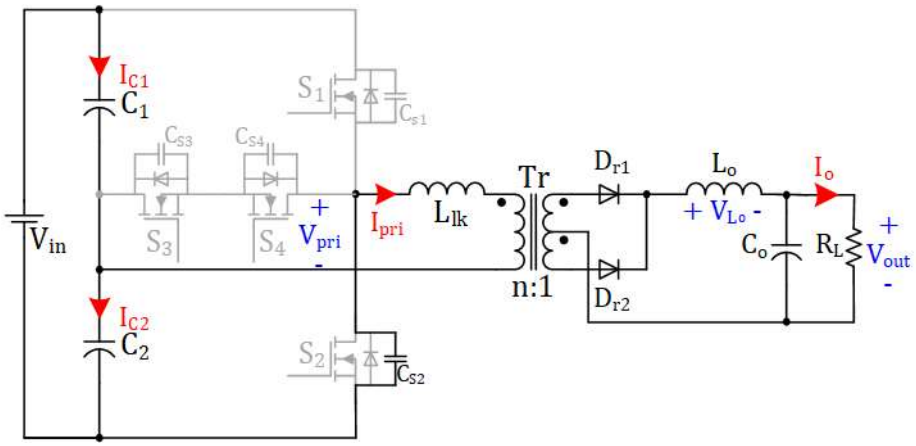
(c) Mode 1 ($t_0 < t < t_1$)



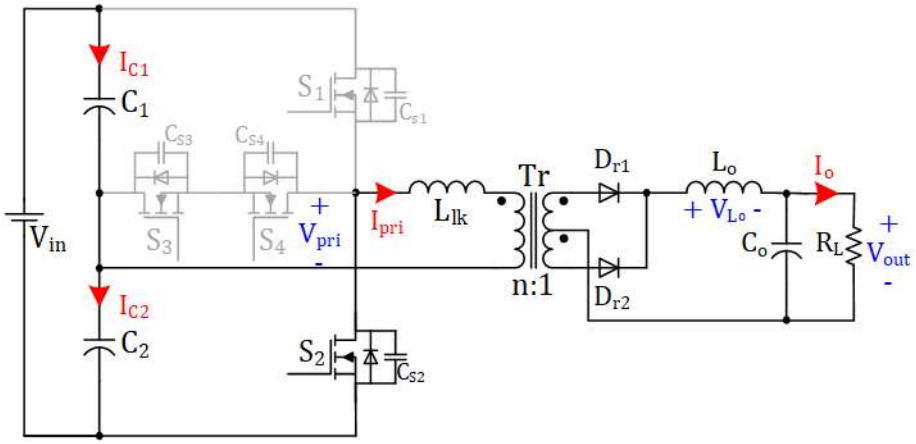
(d) Mode 2 ($t_1 < t < t_2$)



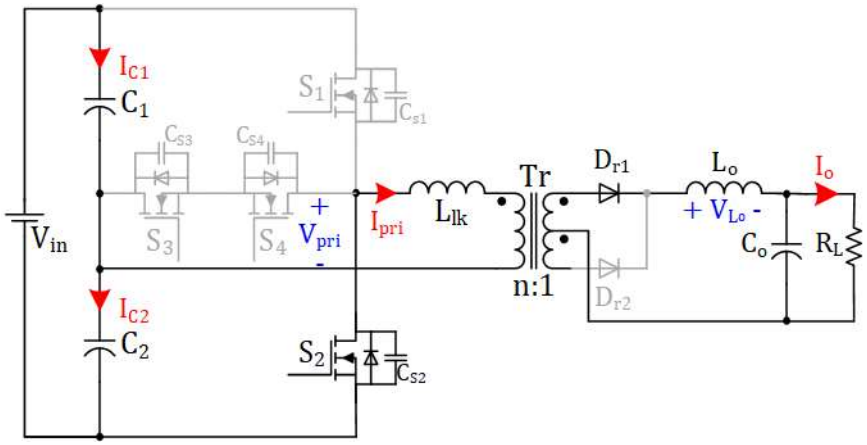
(e) Mode 3 ($t_2 < t < t_3$)



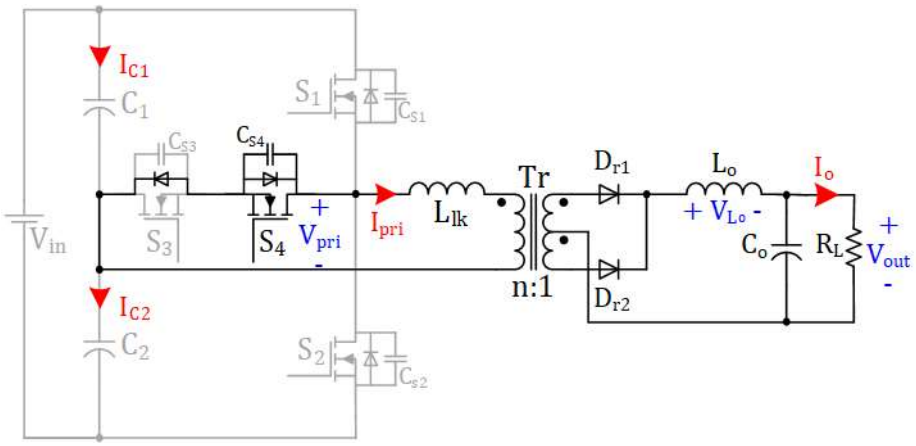
(a) Mode 4 ($t_3 < t < t_4$)



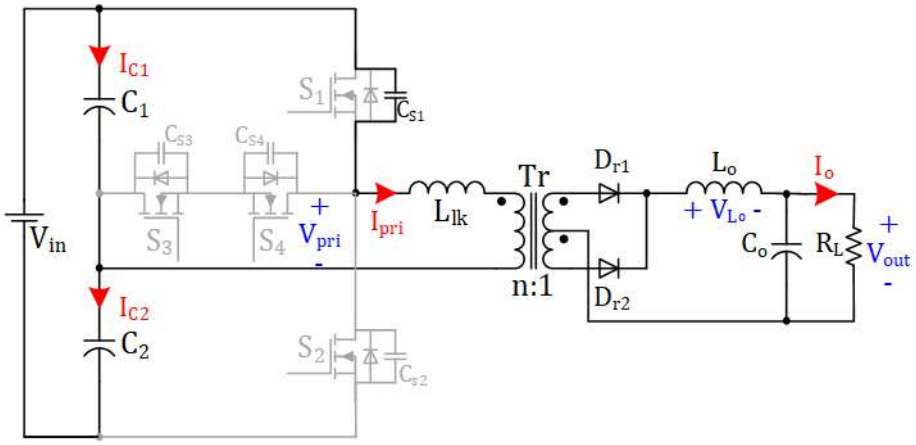
(b) Mode 5 ($t_4 < t < t_5$)



(c) Mode 6 ($t_5 < t < t_6$)



(d) Mode 7 ($t_6 < t < t_7$)



(e) Mode 8 ($t_7 < t < t_8$)

Figure 3.2. The ZVS T-type DC-DC converter modes of operation

3.3 Converter Features

The DC-DC T-type ZVS-PWM converter has the following features:

- All its switches are exposed to a voltage of $V_{in}/2$ before they are turned on instead of V_{in}, which is the case for the switches in the conventional ZVS-PWM-FB converter. Switches S_1 and S_2 have a voltage of $V_{in}/2$ across them before either one is turned on because the end of the transformer primary winding that is connected to the mid-point of their series connection is $V_{in}/2$, due to S_3 or S_4 being on during a freewheeling mode of operation. This means that S_1 has a voltage of V_{in}-$V_{in}/2 = V_{in}/2$ across it before it is turned on and S_2 has a voltage of $V_{in}/2 – 0 = V_{in}/2$ before it is turned on. Switches S_3 and S_4 have a voltage of $V_{in}/2$ before they are turned on because these switches are connected to the mid-point $V_{in}/2$ voltage of the DC bus capacitors. As a result, especially if the load is light and output switch capacitances have not been discharged, these switches will turn on with ¼ of the CV^2 losses of the switches in a conventional ZVS-PWM-FB converter, which results in better light-load efficiency.

- Switches S_1 and S_2 conduct current only when the converter is in an energy-transfer mode and switches S_3 and S_4 conduct current only when the converter is in a freewheeling mode of operation. This is in contrast to the switches in a conventional ZVS-PWM-FB converter where they all must conduct current during an energy-transfer mode and a freewheeling mode and thus less expensive; lower current-rated devices can be used in the converter.

- Switches S_3 and S_4 are never exposed to more than half the DC bus voltage due to their connection to the mid-point of the DC bus capacitor; therefore, cheaper, lower voltage rated devices with lower values of on-state resistance $R_{DS(ON)}$ can be used for these switches. Switches S_1 and S_2 can be exposed to the full DC bus voltage V_{in} whenever one of these switches is off, and the other is on. This helps reduce conduction losses caused by circulating current in a freewheeling mode of operation.

- There is inherent volt-seconds balancing across the primary of the transformer as one end of the transformer primary winding is connected to the mid-point of the DC bus capacitors. If for some reason a net amount of voltage-seconds is applied to the transformer during a switching cycle, there will be a slight adjustment in the mid-point voltage to compensate to for this so that there is no more volt-seconds imbalance. This keeps the transformer from saturating with the need for any additional means, as is the case with the conventional ZVS-PWM-FB converter.

3.4 T-Type converter design

In this section, a procedure for the design of the T type DC-DC converter is presented and then demonstrated with an example. The design procedure and example that is presented here will focus on certain key parameters. The following specifications are used to design the example T-type DC-DC converter: Input voltage V_{in} = 400V, output voltage V_o = 48 V, maximum output power $P_{o,max}$ = 900, minimum output power $P_{o,min}$ = 45W, and switching frequency f_{sw} = 50 kHz. The converter is designed so that the high voltage switches operate with ZVS when the load is more 30% of $P_{o,max}$ .The converter is designed to deliver the nominal voltage with $D_{eff} = 0.6$, where D_{eff} is defined as the time span from t_1 to t_2. The relation between D_{eff} and D is derived in [77] and is as follows:

$$D = D_{eff}(1 + \frac{4L_{lk}}{n^2 R_L} f_{sw}) \qquad (3-9)$$

where f_{sw} is the switching frequency. The output filter is designed based on the method that is presented in [87].

3.4.1 Voltage divider capacitors (C_1 and C_2)

As shown in Figure 3.3 the current of voltage divider capacitors is half of the primary current during the time span from 0 to $\frac{DT_s}{2}$. The voltage variations of C_1 and C_2 are expressed as

$$|\Delta V_C| = \frac{I_1 + I_2}{4\,C} DT_s \qquad (3-10)$$

where $C = C_1 = C_2$. According to (10), the minimum value needed to limit the voltage variations of these capacitors to ±5% of their nominal value is 1.25 µf.

3.4.2 High voltage switches (S_1 and S_2)

As shown in Figure 3.1(b), the high voltage switches of the T-type DC-DC converter must block the full DC bus voltage (V_{in}) when they are off. The transformer primary current flows through the high voltage switches during a time span from 0 to DT_s. The average switch current can be calculated from the current waveform in Figure 3.1(b) as

$$I_{S1-av} = I_{S2-ave} = \left(\frac{I_1 + I_2}{2}\right)\frac{D}{2} \qquad (3-11)$$

In this design example, the maximum value of $I_{S1-ave} = I_{S2-ave} = 2.25A$.

The RMS value of high voltage switches current can be expressed as

$$I_{S1-rm} = I_{S2-rms} = \frac{\sqrt{2D(12I_1^2 - 6I_1I_2 + 3I_2^2)}}{6} \qquad (3-12)$$

In this design example, the maximum value of $I_{S1-rm} = I_{S2-rms} = 4A$.

3.4.3 Low voltage switches (S_3 and S_4)

As shown in Figure 3.1(b), the low voltage switches of the T-type DC-DC converter must block half of the DC bus voltage ($V_{in}/2$). The transformer primary current flows through the low voltage switches during a time span from DTs to Ts. The average switch current can be calculated from (3), which is the current equation over the time span from DTs to Ts. Using (3) the average current of the low voltage switch can be calculated as

$$I_{S3-av} = I_{S4-ave} = I_2 f_{sw}\tau_{LV}.\left(e^{-\frac{(1-D)}{f_{sw}\tau_{LV}}} - 1\right) \qquad (3-13)$$

where the time constant is defined as $\tau_{LV} = \frac{L_{lk}}{R_{ds_3}} = \frac{L_{lk}}{R_{ds_4}}$. Using the design example parameters, the maximum value of $I_{S3-ave} = I_{S4-av} = 1.5A$.

Also, the RMS value of low voltage switches current can be expressed as

$$I_{S3-rm} = I_{S4-rm} = \frac{I_2}{2}.\sqrt{2.f_{sw}\tau_{LV}(e^{-\frac{(1-D)}{f_{sw}\tau_{LV}}} - 1)} \qquad (3-14)$$

In the design example, the maximum value of $I_{S1-rm} = I_{S2-rm} = 4.3A$.

It should be noted that the average and RMS value of the current for low voltage switches include the switch and body diode current components.

3.4.4 Transformer turns ratio (n) and leakage inductance (L_{lk})

The transformer turns ratio (n) of the T-type DC-DC converter can be determined with the same procedure as that for the conventional full bridge ZVS-PWM-FB converter. The only difference is the applied voltage to the primary is half of the voltage with respect to ZVS-PWM-FB converter. Using

$$n = \frac{V_{in}}{2V_o} D_{eff} \qquad (3-15)$$

a value of n = 2.5 can be chosen for this design example.

The leakage inductance (L_{lk}) of the T-type converter helps ensure the converter switches work with ZVS., just like that in the conventional ZVS-PWM FB converter. According to Eq. (7), the minimum L_{lk} need to achieve ZVS can be expressed as

$$L_{lk} \geq \frac{V_{in}^2(C_{s1} + C_{s2} + C_{s3})}{6.I_2^2} \qquad (3-16)$$

Based on this equation, the leakage inductance is selected to be 5.5μH. Using (9), the associated duty cycle loss is 0.0124 or 1.24% in the full load.

3.5 Comparison of T-Type and ZVS-PWM-FB Converters

This section compares the T-type converter and the ZVS-PWM-FB-FB converter in terms of magnetic components size, ZVS operation region, duty cycle loss, and efficiency over the full load range. It should be mentioned that the transformer secondary winding and

output rectifier are the same for both converters and, therefore, are not considered in this comparison.

3.5.1 Magnetic component size

A standard procedure for designing power transformers can be found in [23]. This procedure considers several parameters such as maximum flux density(B_m), peak current(I_{peak}), rms current(I_{rms}), regulation(α), window utilization factor(K_u), frequency (f_{sw}), maximum output power(P_t) to approximate the core size for the transformer. The procedure is used to compare the size of the main power transformer of the T-type converter and the ZVS-PWM-FB converter in this section.

3.5.1.1 Core selection:

A core geometry factor, K_g, that reflects the parameters' effect on core size is introduced in [88]. This core geometry factor is defined as

$$K_g = \frac{P_t}{2.k_f^2 B_m^2 f_{sw}^2 10^{-4}} \qquad (3-17)$$

where K_f is a constant value concerning voltage waveform; thus, it is the same for both T-type and ZVS-PWM-FB converters.

The maximum value of B_m is selected according to the core material. If the same core type is used for both the converters and the maximum value of B_m is the same, then the value of K_g is also the same.

3.5.1.2 Primary turns number

The primary turns number for the T-Type converter can be determined to be

$$N_{pri,T} = \frac{V_{in}(10^4)}{2.k_f B_m f_{sw} A_c} \qquad (3-18)$$

Similarly, the number of primary turns for the ZVS-PWM-FB converter can be determined

$$N_{pri,FB} = \frac{V_{in}(10^4)}{k_f B_m f_{sw} A_c} \quad (3-19)$$

The ratio of transformer primary turns of T-Type converter to ZVS-PWM-FB can be expressed as

$$\frac{N_{pri,T}}{N_{pri,FB}} = \frac{1}{2} \quad (3-20)$$

In other words, the T-type converter needs half as much primary winding turns in its main transformer as does the ZVS-PWM-FB converter.

3.5.1.3 Conductor size

The value of peak current (I_{peak}) and rms current(I_{rms}) of the T-type converter transformer are double that of the ZVS-PWM-FB converter transformer as only half the DC bus voltage is impressed across its primary. Considering the same current density (j) in the primary winding, the effective cross section area of a wire in the T-type converter should be twice that of a wire in the ZVS-PWM-FB converter, i.e.

$$\frac{A_{wire,T}}{A_{wire,FB}} = 2 \quad (3-21)$$

As a result, the effective resistance of a primary winding in the T-type converter is almost a quarter of that in the ZVS-PWM-FB converter. Since the RMS current in the primary side of the T-Type converter is twice that of the ZVS-PWM-FB converter, the ohmic losses of the primary are almost the same.

3.5.1.4 Regulation

α is defined as the ratio of the voltage drop across the transformer windings.

$$\alpha = \frac{\Delta V_{pri}}{V_{pri}} + \frac{\Delta V_{sec}}{V_{sec}} \quad (3-22)$$

where ΔV_{pri} and ΔV_{sec} are defined as the voltage drop across the primary and secondary windings respectively and $V_p$and V_s are the voltage of the primary and secondary windings, respectively. As stated in conductor size section, the effective resistance of the primary side of the transformer for a T-type converter is a quarter of that for a ZVS-PWM-FB converter. On the other hand, the current magnitude is double in the T-type converter; thus, the voltage drop across the resistance of the T-type converter transformer is half that of the transformer of ZVS-PWM-FB converter. Since the applied voltage to the transformer in T-Type converter is half of the voltage in ZVS-PWM-FB converter the voltage drop ratio $\frac{\Delta V_{pri}}{V_{pri}}$ is same for both converters. It should be mentioned that the secondary winding parameters is the same for the both converter; thus, they are not considered in the comparison.

To summarize the above discussion: On the one hand, the transformer used in a T-type converter should be smaller than that used in a ZVS-PWM-FB converter as only half the bus voltage is impressed across it and the number of primary turns is half of the ZVS-PWM-FB. On the other hand, the transformer used in a T-type converter should be larger than that used in a ZVS-PWM-FB converter because the size of wires is larger. Since these two criteria offset, the transformer size for both converters is approximately the same.

3.5.2 ZVS operation region

The ZVS mechanism in both converters is based on the stored energy in the leakage inductance of the transformer. The stored energy in the leakage inductance is used to discharge the output capacitors of the switches. Generally, the stored energy in the leakage inductance of the transformer can be expressed as

$$E_{lk} = \frac{1}{2} L_{lk} I_{pri}^2 \qquad (3-23)$$

Based on Eq. (7) for the T-type DC-DC converter, E_{lk} is used to discharge the output capacitors of the one of the high voltage switches (S_1 or S_2) and charge the output capacitor of another switch and charge one of the low voltage switch capacitors. The voltage

variation for all charging and discharging is $V_{in}/2$. On the other hand, in the ZVS-PWM-FB converter, E_{lk} is used to charge/discharge the output capacitance of the high voltage switches, where the voltage variation range is equal to the input voltage. The ratio of E_{lk} to achieve soft switching in a T-type converter with respect to the soft-switching of a ZVS-PWM-FB can be expressed as

$$\frac{E_{lk-T}}{E_{lk}} < \frac{1}{8}\left(2 + \frac{C_{oss-LV}}{C_{oss-}}\right) \qquad (3-24)$$

where C_{oss-} is the high voltage switch output capacitance and C_{os} the low voltage switch output capacitance. Based on (24), a T-type converter needs less inductive energy to operate with same soft switching range.

3.5.3 Duty cycle loss

Larger leakage inductance increases the ZVS operation range of the converter and reduces the slope of current variations when the converter enters a power transfer mode. As discussed in ZVS operation range section, the stored inductive energy for a T-type converter is less than that for a conventional ZVS-PWM-FB converter. It should be noted that in a T-type converter, the current in primary side is twice that of a ZVS-PWM-FB converter. If the output capacitance of the high voltage switches are the same, the ratio of leakage inductances required to ensure ZVS operation for both ZVS-PWM-FB and T-type converters can be expressed as

$$\frac{L_{lk-T}}{L_{lk-F}} < \frac{1}{32}\left(2 + \frac{C_{oss-}}{C_{oss-HV}}\right) \qquad (3-25)$$

(25) shows that a T-type converter needs a much smaller leakage inductance in comparison to the ZVS-PWM-FB to operate in the same ZVS range. Lower leakage inductance reduces the duty cycle loss in the T-type converter.

3.5.4 Efficiency comparison

In this section, a comparison of efficiency is made based on three sources of power losses: switch losses, transformer, and secondary side circuit losses. Transformer losses are the

same for both converters, however, because as stated in Section V.A, the size of the cores and maximum flux density(B_m) are the same. Core losses are the same as are resistive losses and thus overall transformer losses are not considered in the comparison. Also, the secondary side circuit is exactly the same for both the converters; thus, secondary side circuit losses are the same and are not considered in the comparison. The focus of the efficiency comparison is therefore on switch losses.

Switch losses can be expressed as the sum of switching losses and conduction losses. The switching losses and conduction losses for both the converters are compared as follows:

3.5.4.1 Switching losses

All converter switches in both T-type and ZVS-PWM-FB converters can operate with ZVS when the converters are operating under heavy-load conditions. Under light-load conditions, however, the switches turn on with partial ZVS or even without ZVS if (7) or (8) are not satisfied. In this section, the efficiency of both converters is compared when the converters are operating with partial ZVS, which is a more general case and includes both ZVS and non-ZVS operation; 100% ZVS is considered to be full ZVS converter operation and 0% ZVS is considered to be full non-ZVS operation. It should be noted that the same analysis for a typical ZVS-PWM-FB converter has been done in [79] and thus is not repeated here.

When examining the switching losses of the T-type converter, the voltage across S_1 or S_2 when either switch is turning on can be expressed as

$$V_{S_1}(\mathrm{t}_0) = \frac{V_{in}}{2} - Z_o I_3 \sin\big(\omega_0(t_4 - t_3)\big) \qquad (3-26)$$

where Z_o is the characteristic impedance and defined as

$$Z_o = \sqrt{\frac{L_{lk}}{3C_s}} \qquad (3-27)$$

and the equation for $V_{S2}(t_0)$ is the same.

In the case when the switch voltage does not reach zero before the turning on of S_1 and S_2 because of low circulating current, the switching losses for these switches can be determined to be [12]:

$$P_{sw_{S_1}} = f_{sw}\left(\frac{1}{2}C_{oss-H}\ V_{s1}^2(t_0)\right) \qquad (3-28)$$

The same expression is valid for the switches in a ZVS-PWM-FB converter.

According to the T-type converter waveforms in Figure 3.1(b), even if S_1 and S_2 do not work with ZVS, the voltage across these switches are half of the input voltage before they are turned on. When a ZVS-PWM-FB converter is operating under light-load conditions without ZVS, the voltage across the switches is equal to input voltage before they are turned on.

Given this context, if the same switches are used, and the same operation condition is considered, the switching losses for S_1 and S_2 is a quarter of a typical switch in ZVS-PWM-FB converter, since the voltage across the switch in T-type converter is half of the voltage across a switch in a ZVS-PWM-FB converter during the turn-on process.

According to the T-type converter waveforms in Figure 3.1 (b), before the middle leg turned-on, the voltage across the switch is zero. As a result, the overall switching losses in a T-type converter are less than those of a ZVS-PWM-FB converter when each converter is operating under light-load conditions, and their switches do not operate with ZVS.

It should be noted that if a proper gate drive circuit is used, or the switches' turn-off losses are negligible and are thus not considered as part of switching losses [12].

3.5.4.2 Conduction losses

A MOSFET can be modelled as a resistance ($R_{ds(on)}$) when it is on. The power dissipation in this mode can be determined using the RMS value of the current through the switch.

S_1 and S_2 carry the primary current in the energy transfer mode, and S_3 and S_4 carry the primary current in the freewheeling mode. If duty cycle loss is disregarded, the RMS current for the energy transfer and the freewheeling modes can be expressed as

$$I_{et-r} = \sqrt{\frac{2}{T_s}\int_0^{DT_s} I_{pri}^2 dt} = \sqrt{\frac{2}{T_s}\int_0^{DT_s} \left(I_1 + \left(\frac{I_2 - I_1}{DT_s}\right)t\right)^2 dt}$$

$$= \sqrt{2D(I_2 I_1 + \frac{1}{3}(I_2 - I_1))^2} \qquad (3-29)$$

$$I_{fw} = \sqrt{\frac{2}{T_s}\int_{DT_s}^{\frac{T_s}{2}} I_{pri}^2 dt} = \sqrt{\frac{2}{T_s}\int_{DT_s}^{\frac{T_s}{2}} \left(I_2 + \left(\frac{I_3 - I_2}{DT_s}\right)t\right)^2 dt}$$

$$= \sqrt{(1-2D)(I_3 I_2 + \frac{1}{3}(I_3 - I_2))^2} \qquad (3-30)$$

During an energy transfer mode, S_1 or S_2 carries the primary current; thus, the conduction losses for these switches can be expressed as

$$P_{et} = I_{et}^2 \times R_{ds(on)_1} \qquad (3-31)$$

For the ZVS-PWM-FB, the conduction losses for the energy transfer period can be calculated with the same equation. It should be noted that the current magnitude of the T-type converter is twice as ZVS-PWM-FB converter as only half the DC bus voltage is impressed across its transformer primary. In the T-type converter, however, the primary current passes through only one switch whereas, in ZVS-PWM-FB converter the primary current passes through two switches so that the resistance of the current path is half in T-type converter.

During a freewheeling mode, the body diode of one of the switches in the middle leg (S_3 or S_4) is turned on and can be modeled as a resistor and the other switch is off and the current flows through its anti-parallel body diode of the transistor. The conduction losses for the first half cycle where S_3 is on in freewheeling modes can be expressed as

$$P_{fw} = I_{fw-rms}^2 \times R_{ds(on)_3} + I_{fw-} \times V_{D_{S_4}} \quad (3-32)$$

where $V_{D_{S_4}}$ is the voltage drop across the anti-parallel body diode of S_4 and I_{fw-a} is the average current in freewheeling mode and can be expressed as

$$I_{fw-av} = \frac{2}{T_s}\int_{DT_s}^{\frac{T_s}{2}} I_{pri}\, dt = \frac{2}{T_s}\int_{DT_s}^{\frac{T_s}{2}} \left(I_2 + \left(\frac{I_3 - I_2}{DT_s}\right)t\right) dt$$
$$= \frac{1-D}{D}((I_3 + I_2)D + (I_3 - I_2)) \quad (3-33)$$

The turn-on losses for S_4 can be determined in the same way.

For the ZVS-PWM-FB, the conduction losses for the freewheeling mode can be calculated from the RMS value of the freewheeling current in (31). Since the T-type converter current in the freewheeling mode is twice that of the ZVS-PWM-FB converter, however, the middle leg switches can be implemented with lower voltage rated devices with lower $R_{ds(on)}$. It is thus expected that the power losses are close to those of typical switches in a ZVS-PWM-FB converter. The total switch losses in a T-Type converter can be expressed as:

$$P_{total-sw-loss} = 2 \times \left(P_{sw_{S_1}} + P_{sw_{S_3}}\right) + P_{et} + P_{fw} \quad (3-34)$$

In summary,

- Under light-load conditions when the converter switches do not operate with ZVS, the switching power losses in the converter switches of a T type converter are less than those in a ZVS-PWM-FB converter, since the voltage across the switches in a T-type converter is half of the voltage across the switches in a ZVS-PWM-FB converter before switches are turned on. Under light-load conditions, the conduction losses are negligible since the primary current magnitude is low.

- Under heavy-load conditions, when the converter switches operate with ZVS, the switching losses for both the converters are negligible. The magnitude of the primary current increases, however, and since the primary current of the T-type converter is twice that of the ZVS-PWM-FB converter, more conduction losses are expected in the T-type converter.

- Given this context, it is expected that the T-type converter has better efficiency than the ZVS-PWM-FB converter under light-load conditions since switching losses are the dominant power losses under light-load operating conditions. On the other hand, it is expected that the ZVS-PWM-FB converter is more efficient under heavy-load conditions since conduction losses are the dominant power losses.

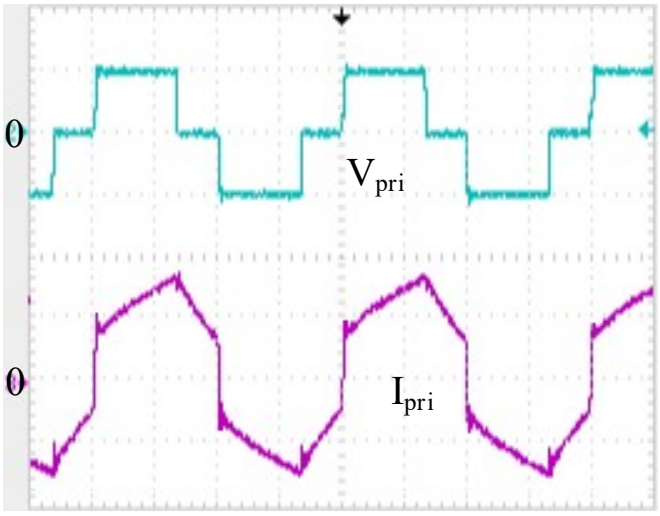
3.6 Experimental Results

Prototypes of the conventional ZVS-PWM FB converter and the T-type-ZVS-PWM converter were built. Both prototypes were built according to the specifications in Table 3-1. For the T type converter prototype, S_{HV} MOSFETs were used as S_1 and S_2 and S_{LV} MOSFETs were used as S_3 and S_4. For the ZVS-PWM-FB converter, S_{HV} devices were used. Both converters were designed to work with 0.6 efficient duty cycle (primary duty cycle minus duty cycle loss), and the transformer core used in each prototype was the same.

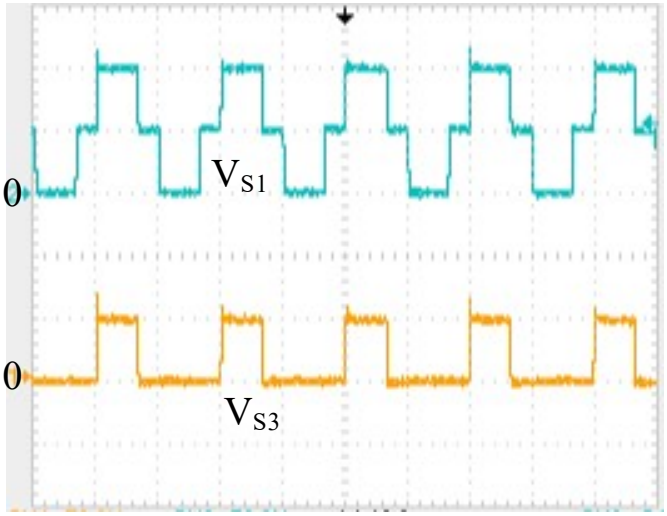
TABLE 3-1: SPECIFICATION OF THE CONVERTER COMPONENTS

Symbol	Item	Value
V_{in}	Input voltage	400V
V_o	Output voltage	48V
$P_{o,max}$	Maximum output power	900W
$P_{o,min}$	Minimum output power	45W
f_{sw}	Switching frequency	50 kHz
L_o	Output filter inductor	200 µH
C_o	Output filter capacitor	56 µf
L_{lk_T}	Leakage inductance of the T-Type converter	5.5µH
L_{lk_FB}	Leakage inductance of the ZVS-PWM-FB	25µH
S_{HV}	500V MOSFET type	FDP18N50
S_{LV}	250V MOSFET type	FDP51N25
$C_{oss\text{-}HV}$	500V MOSFET parasitic capacitor	330pf
$C_{oss\text{-}LV}$	250V MOSFET parasitic capacitor	530pf
$R_{DS(on)\text{-}HV}$	500V MOSFET turn on resistance	220 mΩ
$R_{DS(on)\text{-}LV}$	250V MOSFET turn on resistance	60 mΩ
D_{r1} & D_{r2}	Rectifying diodes	STPS30H100C
n_T	The turns ratio of the transformer in the T converter	2.5:1:1
n_{fb}	The turns ratio of the transformer in the ZVS-PWM-FB converter	5:1:1
Tr-Core size	Core size for the both the converters	ETD49

As the waveforms of the conventional ZVS-PWM-FB are well known, only typical waveforms of the T-type converter are shown in Figure 3.3. Figure 3.3(a) shows the voltage and current waveforms of the transformer primary. It can be seen that the waveforms in Figure 3.3(a) are the same as those that would be found in a ZVS-PWM-FB converter. Figure 3.3(b) shows the voltage of switches S_1 and S_3.



(a) Voltage and current waveforms of the transformer primary (I: 1A/div., V: 200V/div, t: 5 µs/div.)



(b) Voltage across switches S_1 and S_3. (V: 200V/div, t: 10 µs/div.)

Figure 3.3. Typical converter waveforms of a ZVS T-type converter

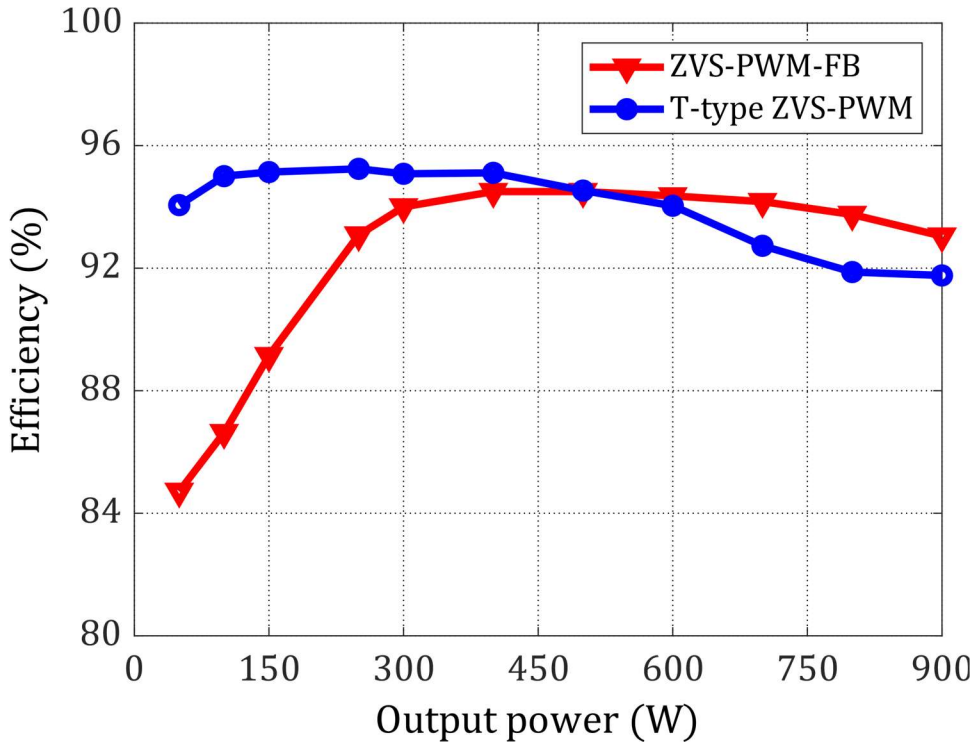


Figure 3.4. Graph of efficiency vs output power for the full bridge-ZVS-PWM and T-type converters

Figure 3.4 shows a graph of efficiency vs load for the T-type and the ZVS-PWM-FB converters. It can be seen that the T- type converter is the more efficient converter for the lighter loads. This is because the voltage across the converter switches is half of the input voltage at the time of turn-on so that less leakage inductance energy is needed to discharge their output capacitors before they are turned on; less leakage inductance energy is available during light-load operation. Moreover, switches S_3 and S_4 are low voltage switches with low $R_{DS\text{-}ON}$ values so that freewheeling current conduction losses are lower than those found in a ZVS-PWM-FB converter.

For heavier loads, the ZVS-PWM-FB converter is the more efficient converter. This is because the T-type converter places just half the input voltage across the transformer primary, which means twice as much current circulates in the primary as compared to that in a ZVS-PWM-FB converter. The higher current means more conduction losses so that the T-type converter becomes less efficient than the ZVS-PWM-FB converter for heavier loads.

3.7 Conclusion

The T-type PWM DC-DC converter was proposed in the literature several years ago as an alternative to the conventional zero-voltage switching (ZVS) PWM full-bridge (FB) converter. Although it has several advantageous features, its characteristics are not well-known, and its performance has not been compared to that of the conventional ZVS-PWM-FB converter. As a result, it has been neglected as a possible converter topology option, despite its strengths.

In this chapter, the operation of the T-type converter was explained, its features were stated, and a comparative study between it and the ZVS-PWM-FB converter was made with experimental work. The main conclusions of this study are as follows:

The T-type converter has a better light-load efficiency than the ZVS-PWM-FB converter, but a worse heavy-load efficiency as it is based on a half-bridge topology. Such a characteristic is attractive in applications where the converter must spend a considerable amount of time operating with light loads.

The switches in the T-type converter have fewer current and voltage stresses that do the switches of the ZVS-PWM-FB converter. The switches in the T-type converter either conduct the power-transfer mode current or the freewheeling mode current and never conduct current in both these modes and the switches that are placed in series with the transformer must block only half the DC bus voltage. The T-type converter can be implemented with less expensive lower current rated devices and lower voltage devices (for half its switches).

The T-type converter does not need any additional methods to prevent its transformer from saturating as it has inherent voltage/seconds balancing due to its half-bridge structure.

The size of the main power transformer in the two converters is about the same. On the one hand, the transformer used in a T-type converter should be smaller than that used in a

ZVS-PWM-FB converter as only half the bus voltage is impressed across it and the number of primary turns are half of the ZVS-PWM-FB. On the other hand, the transformer used in a T-type converter should be larger than that used in a ZVS-PWM-FB converter because the size of wires are larger. Since these two criteria offset, the transformer size for the both converters is approximately the same.

Chapter 4

4 Four switch AC-DC converter with galvanic isolation

4.1 Introduction

Three-phase AC-DC converters that have galvanic isolation are widely used in industrial applications. The harmonic content of these converters are restricted to the limits placed by the harmonic standards of regulatory agencies; the converters are thus implemented with some form of input power factor correction (PFC). Typical converters are two-stage converters with an input three-phase AC-DC stage followed by a DC-DC stage that includes an isolation transformer.

In this chapter, a new single-stage power factor corrected (SSPFC) AC-DC is proposed. The outstanding features of the proposed converter are that it has only four switches in its topology, it is bridgeless, its input currents are continuous, and it can be implemented with any control method used in standard three-phase, six-switch VSRs. In this chpater, the converter's general operation and its modes of operation are explained in Section 4.2, its features are stated in Section 4.3. a steady-state mathematical model of the converter is developed in Section 4.4, a design procedure of the converter is developed and demonstrated with a design example in Section 4.5, and experimental results from a simple proof-of-concept prototype are presented in Section 4.6. The main points of the chapter are summarized and conclusions are made in Section 4.7.

4.2 Converter operation

The proposed three phase AC-DC converter is shown in Figure 4.1. The converter consists of three input inductors L with internal resistance equal to R, a four-switch three-phase rectifier with switches S_1- S_4 and capacitors C_1 and C_2, a dc blocking capacitor C_b, an isolation transformer with n:1 turns ratio and leakage inductance L_{lk}, two output rectifying diodes D_1 – D_2, an output filter inductor L_o, and an output capacitor C_o.

The converter is a combination of a four-switch three-phase AC-DC rectifier and a FB-ZVS-PWM DC-DC converter in its topology. Figure 4.2 shows the circuit diagram of the

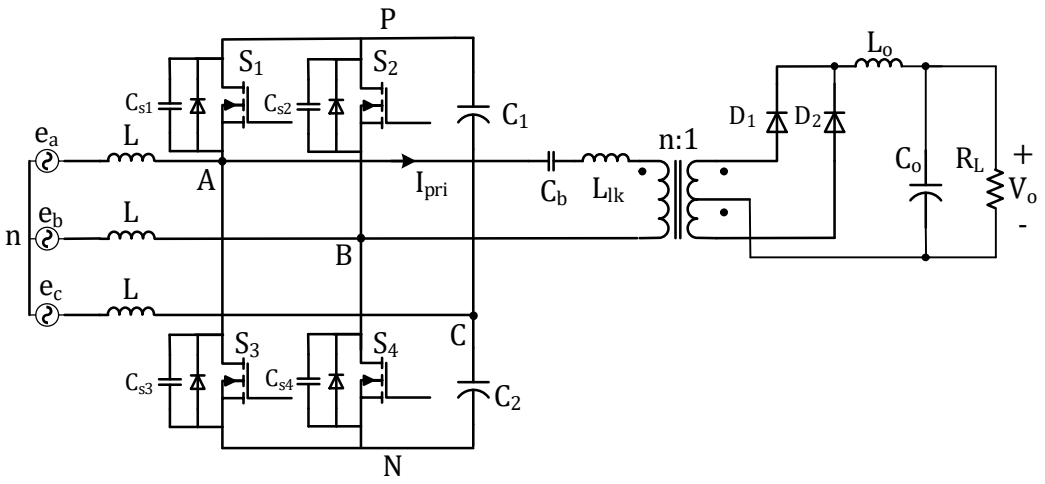


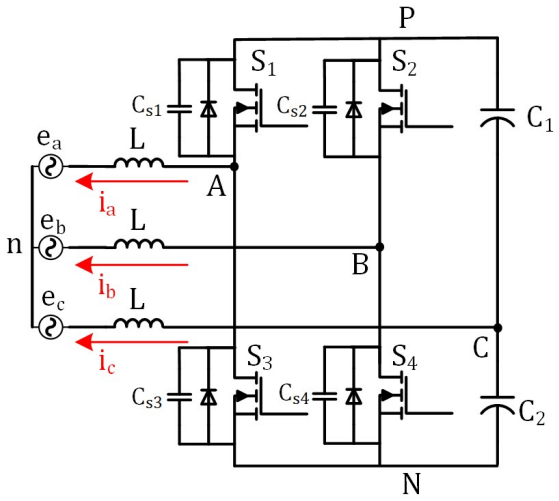
Figure 4.1. Proposed three-phase AC-DC single-stage converter

two sub-converters; the operation of each sub-converter is explained in this section. The following should be noted:

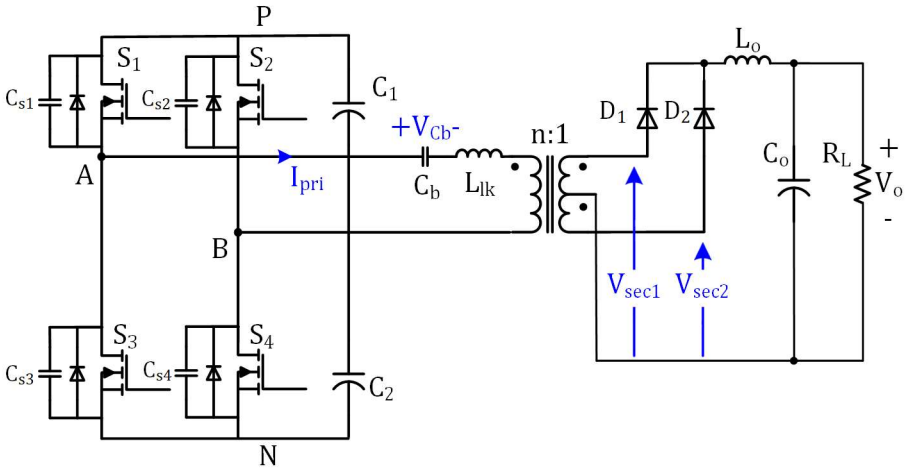
- The operation of the proposed converter is based on three-phase PWM theory and thus differs from that of a number of other, previously proposed AC-DC converters where the converter is made to operate with a fixed duty-cycle and the input currents are made to be discontinuous with high current peaks. Information about the operation of three-phase, six-switch voltage source rectifiers/inverters and three-phase PWM can be found in standard textbooks such as [26], [89], [90].

- More information about the operation of the three-phase, four-switch sub-converter can be found in papers such as [38], [91]. What is presented here is a brief explanation of how a six-switch converter can be transformed into a four-switch converter. It should be especially noted that the transformation alters just the phase relationships between the gating signals of two legs and not the PWM pattern; any PWM method that can be in a six-switch converter can be used in a four-switch converter. In a balanced three-phase system, if two of the input currents are controlled by two phase legs, then the third input current will automatically be such that when the three input current waveforms are added up, the sum is zero.

- During steady-state operation, switches S_1 and S_3 turn on and off so that the voltage at point A in the circuit diagram shown in Figure 4.1 is either the bus voltage V_{PN} or 0 at any instant of a switching cycle. Likewise, switches S_2 and S_4 turn on and off so that the voltage at point B in the circuit diagram is either the bus voltage V_{PN} or 0 at any instant of a switching cycle. As a result, voltage V_{AB} will either be $+V_{PN}$, $-V_{PN}$, or 0 at any instant of a switching cycle. As there is a transformer between points A and B, switches S_1, S_3, S_2, and S_4 are indeed like a DC-DC full-bridge converter where $+V_{PN}$, $-V_{PN}$, or 0 are also impressed across its



(a) AC-DC stage



(b) DC-DC stage

Figure 4.2. AC-DC converter stages

transformer's primary, with one key difference – the duty-cycle of this full-bridge is not fixed, but varies throughout an AC input line cycle. The four converter switches are operated in accordance with a PWM method to ensure that the three input currents are sinusoidal and in phase with the three-phase input voltages, and the DC-DC conversion part of the converter is just tapped off points A and B with the transformer. Blocking capacitor C_b has been added to prevent transformer saturation.

4.2.1 AC-DC converter

The AC-DC converter stage (Figure 4.2(a)) is a four switch PWM VSR. This converter should perform PFC and absorb the required active power from the grid to supply the load and store it in the two capacitors (C_1 and C_2) at the intermediate DC bus. To perform these operations, the four-switch converter should apply a proper three phase balanced voltage at the converter terminals A, B and C and since only two legs of the converter have active switches, the phase difference between the voltages of the two active legs (phase A and B) is 60^o instead of 120^o.

The aforementioned operation method can be explained based on the phasor diagram of phase voltages shown in Figure 4.3. Figure 4.3(a) shows a three-phase star connected voltage source that is connected to a three-phase load. In Figure 4.3 (b), three voltage sources having the same amplitude and 180^o phase shift with phase 'C' voltage are connected in series to each phase voltage source. The new system phasor diagram is shown in Figure 4.3 (c). In phase 'C' the overall voltage is zero; for phase 'A' and 'B' the voltages become V_a and V_b, respectively. The current that flows in the leg with split capacitors, phase 'C', is the sum of the current in phase 'A' and 'B'; as a result, current flows in phase 'C' without any voltage source.

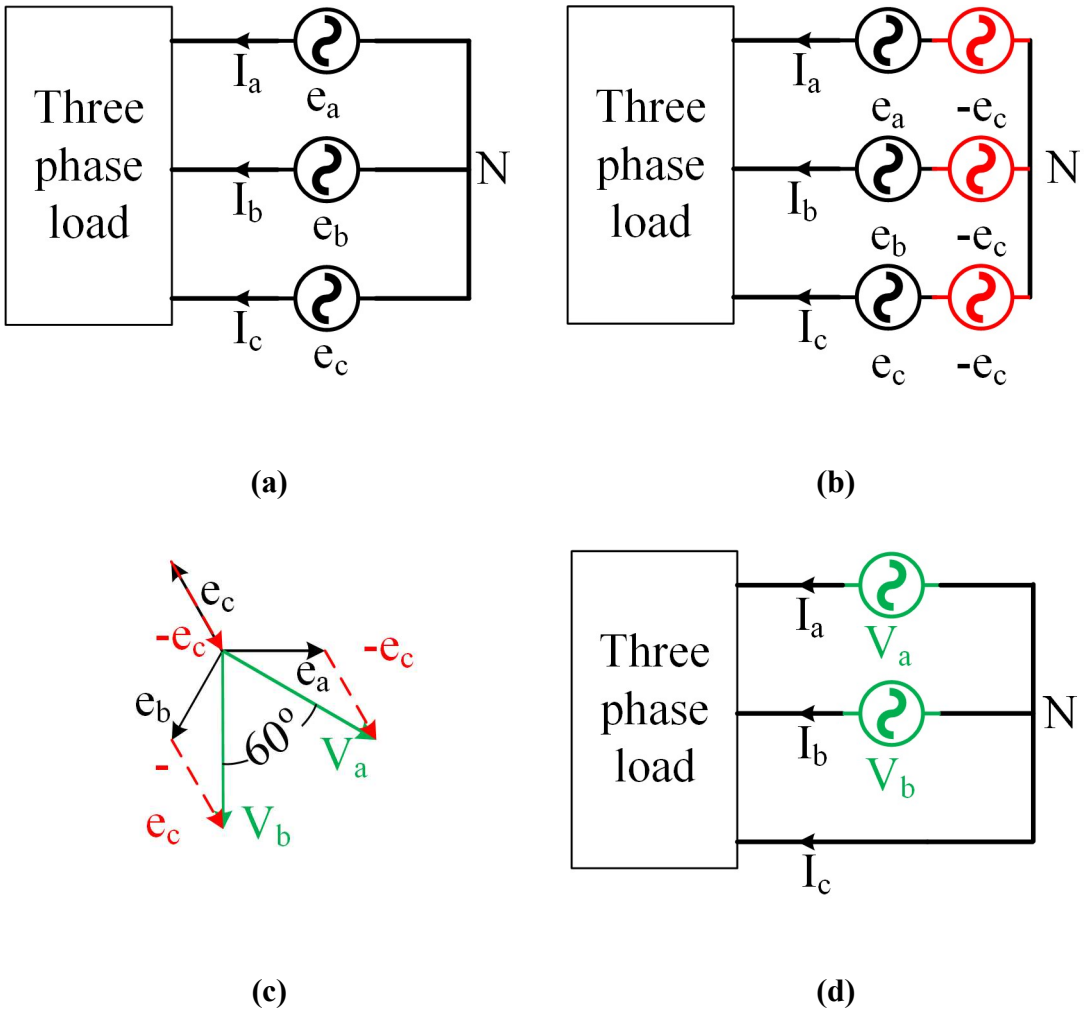


Figure 4.3. Three phase load supply by two voltage sources

Figure 4.4 shows some typical control signals of phase 'A' and 'B' within a line cycle (note the 60^o phase shift in modulation signals). Since any PWM method that can be used for six-switch voltage source converters can be used in the proposed AC-DC converter to generate the switching signals, sinusoidal PWM (SPWM) was used in this work at it is one of the simplest PWM methods.

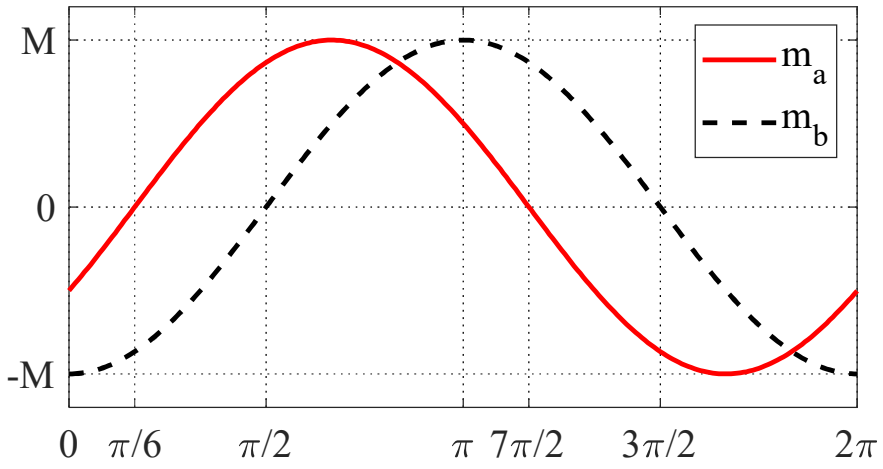


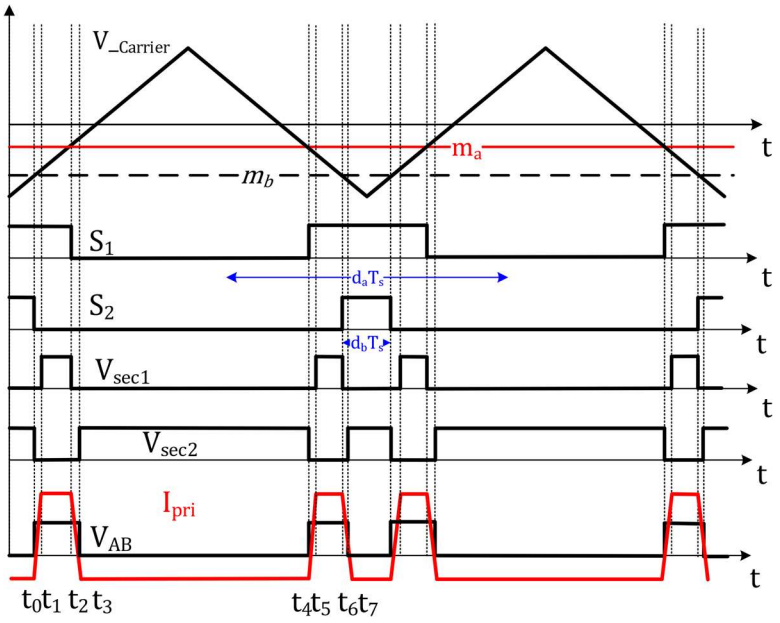
Figure 4.4. Modulation signals in line frequency

4.2.2 DC-DC converter

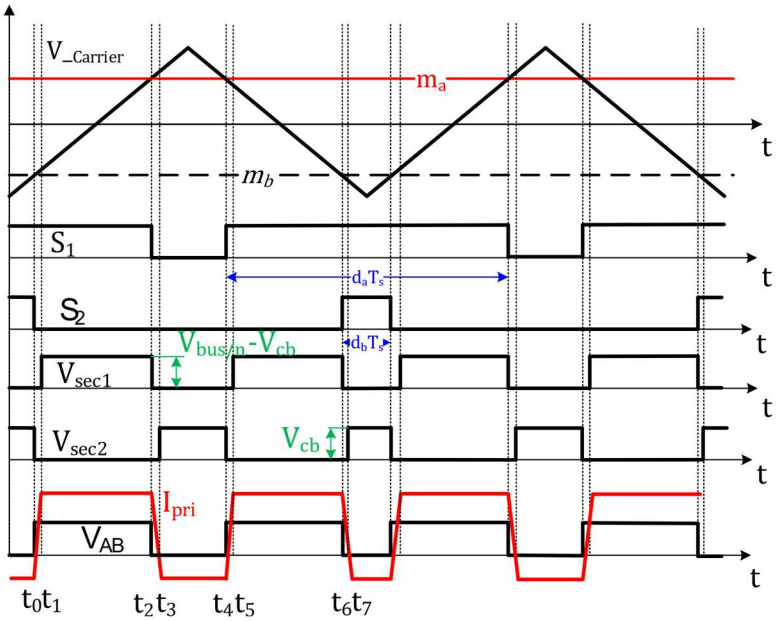
The DC-DC sub-converter is shown in Figure 4.2(b). The converter is a conventional FB-ZVS-PWM converter, but with its gating signals generated with a SPWM pattern. Consequently, the modes of operation of the DC-DC stage can be explained with respect to the SPWM switching sequence. The gating pulses are generated with comparison of the modulation signals, as shown in Figure 4.4 with a triangular carrier.

Figure 4.5 shows some typical gating signal waveforms for a switching cycle with respect to the modulation signals within the range of $\pi/6 < \omega.t < \pi/2$. The gate pulses for the upper switches of the legs (S_1 and S_2) are shown, with the carrier and modulating signals of the SPWM pattern, voltage V_{AB} and primary current I_{pri}. It should be noted that S_3 and S_4 are complementary to S_1 and S_2, respectively.

The four switches of the converter act as a FB-ZVS-PWM converter and V_{AB} is a square wave PWM waveform with varying duty cycle. The voltage of V_{AB} has a DC component in the switching cycle and a blocking capacitor C_b is used to prevent this component from saturating the transformer.



(a) $0 \leq \omega t \leq \pi/6$



(b) $\pi/6 \leq \omega t \leq \pi/2$

Figure 4.5. Modulation signals in switching frequency scale, gate signals, secondary voltages, primary voltage and current

The modes of operation of the DC-DC sub-converter with respect to the gate pulses that is shown in Figure 4.5 are explained for each switching cycle. Also, an equivalent circuit for each mode shown in Figure 4.6. it is assumed that S_1 and S_2 are on and that there is a dead-time between switching transitions.

Mode 1 ($t_0 < t < t_1$)

At the start of this mode, S_2 turns off and the transformer primary current (I_{pri}) starts to flow through the body diode of S_4. V_{AB} is equal to DC bus voltage (V_{PN}), and I_{pri} increases linearly. Sometime during this mode, S_4 can be turned on with zero-voltage switching (ZVS) before I_{pri} reaches zero. During this mode, both V_{sec1} and V_{sec2} are zero and the output inductor current circulates through the secondary side diodes. This is a freewheeling mode and no energy is transferred from the primary side to the output.

Mode 2 ($t_1 < t < t_2$)

At the start of this mode, I_{pri} becomes positive and it flows through S_1 and S_4. V_{AB} is equal to the DC bus voltage. The transformer primary voltage is positive and energy from the DC bus capacitors is transferred to the output as the V_{sec1} is positive and diode D_1 is conducting.

Mode 3 ($t_2 < t < t_3$)

At the start of this mode, S_1 turns off and I_{pri} flows through the anti-parallel diode of S_3. The voltage across V_{AB} is zero; as a result, blocking capacitor voltage (V_{Cb}) is applied to the transformer primary winding and I_{pri} decreases linearly. In this mode, energy is not transferred from the primary side to the secondary side and output current circulates through the secondary rectifier diodes. S_3 can be turned on with ZVS sometime during this mode.

Mode 4 ($t_3 < t < t_4$)

At the start of this mode, I_{pri} becomes negative and it flows through S_3 and the anti-parallel body diode of S_4. A voltage $-V_{Cb}$ is applied to the transformer primary winding. During this mode, V_{sec2} is positive and equal to the reflected value of V_{Cb}, diode D_2 is conducting,

and the output inductor current (I_{Lo}) increases. The energy is transferred from the C_b to the output during this mode.

Mode 5 ($t_4 < t < t_5$)

At the start of this mode, S_1 turns on. This mode is the same as Mode 1.

Mode 6 ($t_5 < t < t_6$)

At the start of this mode, the direction of I_{pri} changes. This mode is the same as Mode 2. At the end of this mode S_4 turns off and I_{pri} flows through the anti-parallel body diode of S_2.

Mode 7 ($t_6 < t < t_7$)

At the start of this mode, S_2 turns on with ZVS. The voltage across the V_{AB} is zero; as a result, blocking capacitor voltage (V_{Cb}) is applied to the transformer primary winding and I_{pri} and decreases linearly. In this mode, energy is not transferred from input to output and output current circulates through the secondary rectifier diodes.

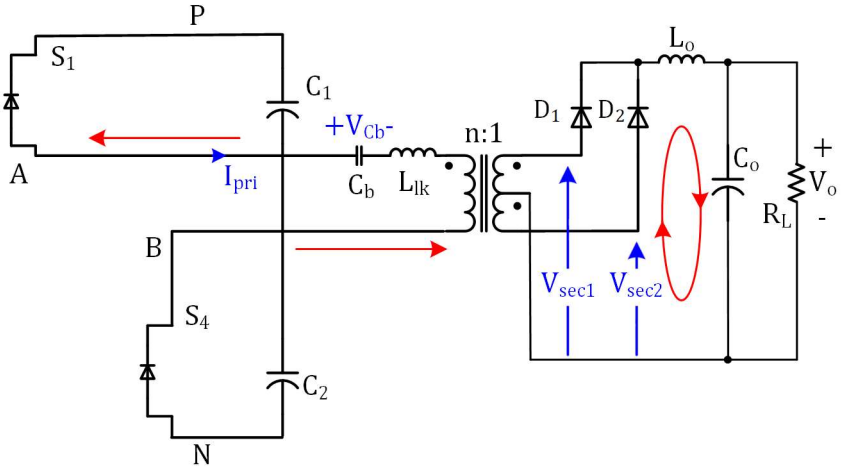
Mode 8 ($t_7 < t < t_8$)

At the start of this mode, I_{pri} becomes negative and it flows through S_1 and S_3. A voltage of $-V_{Cb}$ is applied to the transformer primary winding. The voltages and currents in the transformer and secondary are the same as in Mode 4.

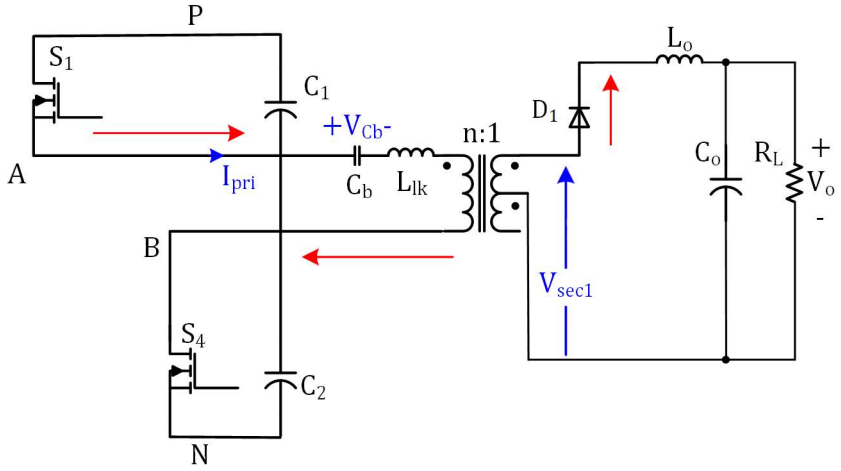
4.3 Converter Features

The proposed converter has the following features:

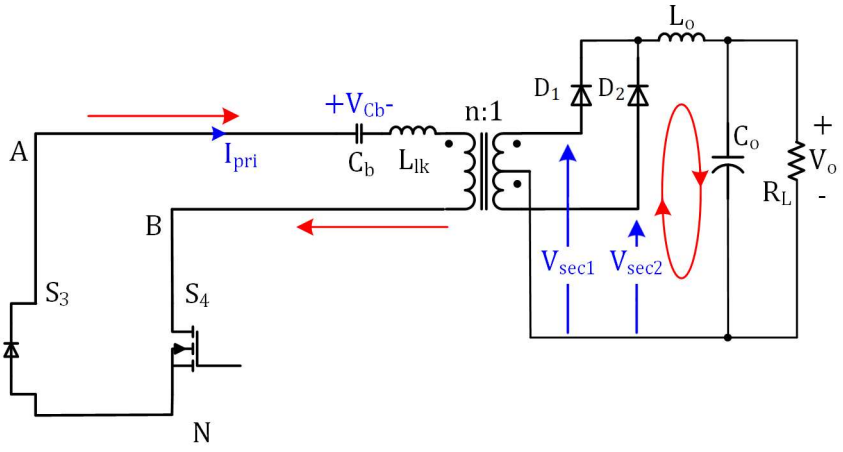
- Any control method used for three phase rectifiers/inverters can be used to operate the proposed converter. Decoupled power control and PWM used in this converter were selected because of their straightforwardness. Other, more complex methods that may result in better performance can be used as well.



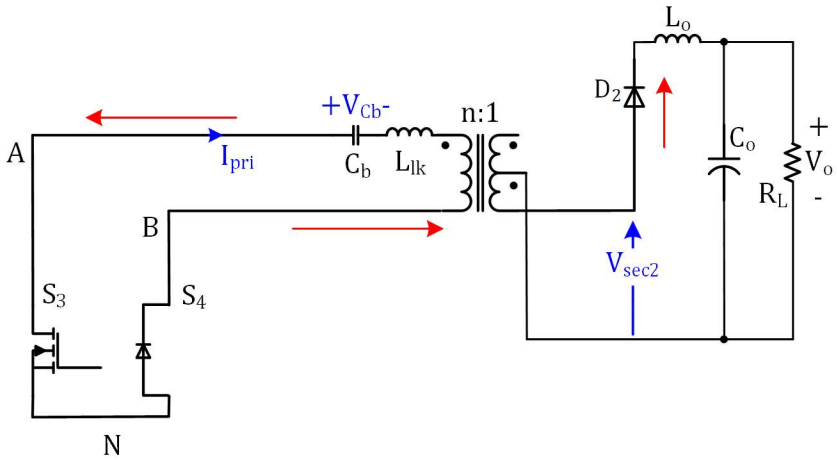
(a) Mode 1 ($t_0 < t < t_1$)



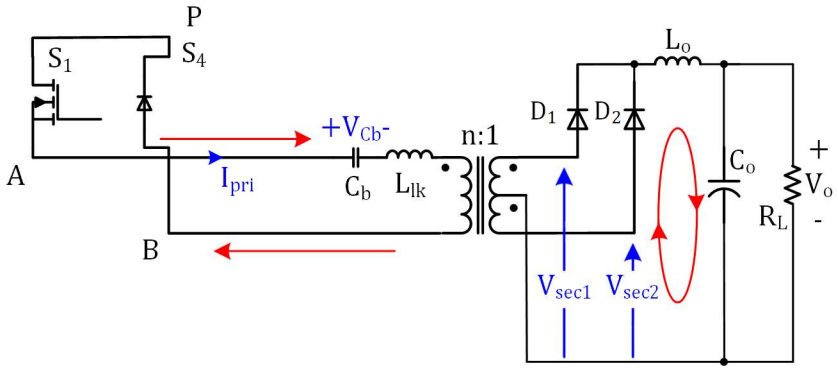
(b) Mode 2 ($t_1 < t < t_2$)



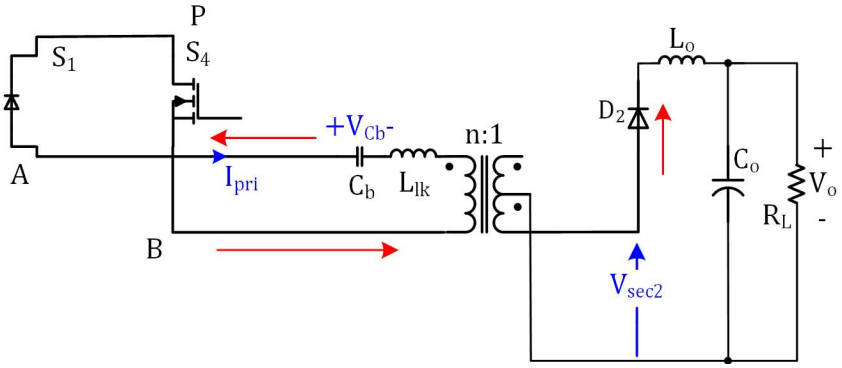
(c) Mode 3 ($t_2 < t < t_3$)



(d) Mode 4 ($t_3 < t < t_4$)



(e) Mode 5 ($t_4 < t < t_5$)



(f) Mode 6 ($t_5 < t < t_6$)

Figure 4.6. Modes of operation

- Only four active switches are used for three-phase AC-DC power conversion with galvanic isolation.
- The converter can be operated with near unity input power factor.
- The input current is continuous; thus, the peak current stress of components is not excessive.
- The converter switches can operate with ZVS

4.4 Converter control

In the control system used to control the converter, measured line voltages and currents are transformed to the dq frame and, because the rotating reference frame is synchronized with the grid frequency, measured parameters are transformed to DC values so that the controller deals with DC values. Current mode control is used; current mode control of four switch inverters in the dq frame is comprehensively explained in the literature [23]-[24]. The block diagram of the control system is shown in Figure 4.7.

Two decoupled loops are used to control the converter input current. A controller is used to control the d-axis current based on the load value and another controller sets the q-axis current equal to zero to ensure PFC in the converter. Both these current control loops have the same structure. The measured current value is transformed to a synchronous reference frame. The transformed value is compared with a reference value and an error signal is fed to a PI controller. Decoupling terms are added to the PI controller output and reference voltages are generated. A dq-transformation is then performed according to (13) and a modulation signal is used to generate the switching sequence as shown in Figure 4.7. [93]–[100].

As shown in (12) and (13), the dynamics of the current control loop of the proposed converter is the same as conventional four-switch voltage rectifier and the controllers are designed with same procedure; thus, the current controllers can be designed with the same procedure as that shown in [101].

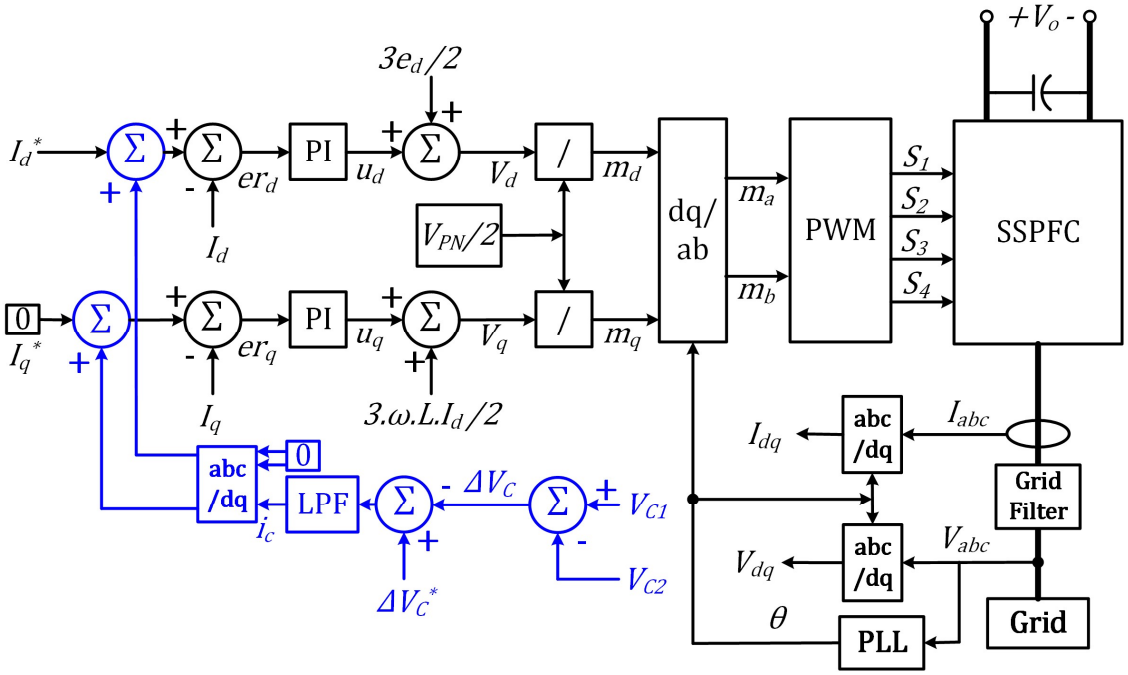


Figure 4.7. Control system (voltage balancing control system is in blue)

It should be noted that the voltage control loop is not shown in Figure 4.7, because this loop is standard and well-known method and thus was not a focus of this work [102].

A control loop, shown in blue in the control system block diagram (Figure 4.7), was used to balance the voltages of the DC capacitors; capacitor voltage balancing is discussed in detail in [101]. As a result, the DC component of the voltage of the capacitors is assumed to be identical ($\frac{V_{PN}}{2} = V_{C1} = V_{C2}$) in the modelling process,

It should be noted that there is no novelty in the design of the control in the proposed converter as conventional schemes can be used. This has been confirmed by simulation.

4.5 Converter Design

In this section, a procedure for the design of the converter is shown and an example is used to demonstrate the design procedure. The example converter is designed based on the following specifications: Input voltage V_{LL} =120V, output voltage V_o = 48 V, maximum output power $P_{o,max}$ = 1 kW and switching frequency f_{sw} = 50 kHz The key

parameters values in the design of the converter are DC bus voltage (V_{PN}), DC blocking capacitor (C_b), Switches RMS current ($I_{SW\text{-}RMS}$) and transformer turns ratio (n). The values of the DC bus capacitors and input inductor can be selected based on the procedure that is presented in [91]. The following should be considered in the selection of the above-mentioned components:

4.5.1 DC blocking capacitor C_b

The DC blocking capacitor prevents the transformer from saturation. The value of C_b should be large enough to keep its voltage constant when the direction of the transformer primary current changes because the capacitor should supply the output load during some operation modes. The variation in the voltage across C_b can be expressed as

$$\Delta V_{Cb} = \frac{I_o}{2 \cdot nC_bF_{sw}} \qquad (4-1)$$

where I_o is output current, n is the transformer turns ratio, and F_{sw} is switching frequency. In order to limit ΔV_{Cb} to 10% of DC bus voltage, a value of $C_b = 1\mu f$ is chosen.

4.5.2 RMS current of the switches

The switch RMS current consists of two components, AC-DC stage RMS current and DC-DC stage RMS current. The total RMS current can be expressed as

$$I_{rms} = \sqrt{(I_{rmsAC-DC})^2 + (I_{rmsDC-DC})^2} \qquad (4-2)$$

The AC-DC converter current is calculated based on the fact that power factor of converter output voltage and current is almost 1 and by applying the method introduced in [103], using

$$I_{rmsAC-DC} = \frac{I_l}{\sqrt{2}} \qquad (4-3)$$

where I_l is the input line current.

The DC-DC converter current component can be calculated based on power transferred to the load. The averaging method can be used to calculate the low frequency component of

I_{pri}. The secondary current is transferred as a constant current over a switching period to the primary. The transferred current is modulated by the PWM pattern and flows through the converter leg; therefore, the low frequency component of the current is a sinusoidal current. The reflected current from the secondary is equal to $\frac{I_o}{n}$. The average value of the switch duty cycle for a line cycle can be expressed as

$$D_{av} = \frac{1}{T}\int_0^T \left| M \cdot \sin\left(\omega.\tau + \frac{\pi}{6} + \varphi\right)\right| d\tau = \frac{2M}{\pi} \qquad (4-4)$$

The RMS value of the current can be calculated from (4)

$$I_{rmsDC-DC} = \frac{1}{T_s}\int_0^{D_{av}T_s} \sqrt{\left(\frac{I_o}{n}\right)^2}\, dt = \sqrt{\frac{2M}{\pi}}\frac{I_o}{n} \qquad (4-5)$$

The total I_{rms} for the switches is equal to 7.5A. It should be noted that this is an initial approximation.

A good approximation of switch peak current is when the AC-DC sub-converter and DC-DC sub-converter operates at maximum current and both the current are added up. The switch current stress can be expressed as:

$$I_{sw-m} = |I_{AC-D} + I_{DC}| = P_{out}\left(\frac{2}{3\hat{e}} + \frac{1}{nV_o}\right) \qquad (4-6)$$

where $\hat{e}$ is the peak input line-to-neutral voltage. The switch current stress from (6) is 15.13 A.

4.5.3 Transformer turns ratio (n)

Under steady-state conditions, the power delivered by the input should match the power absorbed by the output. In the proposed converter, the input power is controlled by the control variable I_d that is associated with the magnitude of the input current and output power is associated with the output voltage.

The output voltage is a function of the duty cycle of the switches, DC bus voltage, and n. In single stage converters, the DC bus voltage is a function of duty cycle and n; thus, it cannot be used as an independent control variable to balance the energy in the converter. In the proposed converter, n should be selected as a coarse-tuning control parameter and modulation index should be used as a fine- tuning control parameter for the output voltage and thus the output power.

In this sub-section, the output voltage relation is developed as a function of transformer turns ratio (n) and the load resistance (R_L). A value of n is selected based on the range of output voltage and load resistance variations. The value of n must be such that it can ensure that the converter's input power can be made equal to the output power for a particular modulation index. Since the same modulation index is applied to both the AC-DC and the DC-DC converter sections, a value of n should be selected such that V_o is equal to 48V.

Based on this explanation,

$$P_{in} = \frac{3}{2} e I_d = \frac{{V_o}^2}{R_L} = P_{out} \qquad (4-7)$$

To determine the transformer turns ratio, a relationship between V_o and V_{PN} needs to be determined. A state-space equation of the converter can be written and a steady state model for the converter can be developed with the following considerations.

Remark 1: The converter components are assumed ideal. For the purpose of modelling the converter at the line frequency, high switching frequency components are ignored. The loading effect of the DC-DC power conversion is modeled as a constant load in the DC bus.

Remark 2: The grid voltages are defined as follows:

$$\begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix} = \begin{bmatrix} \hat{e} \cdot cos(\omega t) \\ \hat{e} \cdot cos\left(\omega t - \frac{2.\pi}{3}\right) \\ \hat{e} \cdot cos\left(\omega t + \frac{2.\pi}{3}\right) \end{bmatrix} \quad (4-8)$$

Remark 3: The power transfers from the grid to the converter occurs at power system frequency so that AC-DC converter operation is explained based on the low frequency model.

As demonstrated in [91], assuming balanced voltage and current operation, converter, the following state-space equations can be written:

$$\frac{di_a}{dt} = -\frac{R}{L} i_a + \left(\frac{-2S_a + S_b}{3L}\right) v_{C1} + \left(\frac{-2S_a + S_b + 1}{3L}\right) v_{C2} + \frac{e_a(t)}{L} \quad (4-9)$$

$$\frac{di_b}{dt} = -\frac{R}{L} i_b + \left(\frac{S_a - 2S_b}{3L}\right) v_{C1} + \left(\frac{S_a - 2S_b + 1}{3L}\right) v_{C2} + \frac{e_b(t)}{L} \quad (4-10)$$

$$\frac{di_c}{dt} = -\frac{R}{L} i_c + \frac{2S_a}{3L} v_{C1} + \left(\frac{S_a + S_b - 2}{3L}\right) v_{C2} + \frac{e_c(t)}{L} \quad (4-11)$$

$$C\frac{dv_{PN}}{dt} = 2S_a i_a + 2S_b i_b + i_c - \frac{2P_{out}}{\mathrm{V_{PN}^2}} \quad (4-12)$$

where R is the inductor resistance, P_{out} is the output power, and $S_a$and S_b are the switching functions of the legs that are connected to phase ‘A’ and ‘B’, respectively and defined as

$$S_j = \begin{cases} 1 & Upper\ switch\ is\ close \\ 0 & Lower\ switch\ is\ close \end{cases} \quad j \epsilon a, b$$

Applying averaging method shown in [87] to (8) to (11) and using the Park transformation, the average state space equations for currents of the AC-DC converter can be written in the dq frame as

$$L\frac{di_d}{dt} = -Ri_d - L\omega i_q - \frac{V_{PN}}{3}m_d + e_d \qquad (4-13)$$

$$L\frac{di_q}{dt} = -Ri_q + \omega L i_d - \frac{V_{PN}}{3}m_q \qquad (4-14)$$

where m_d and m_q are the average values of S_a and S_b that are transferred to dq frame.

The AC-DC converter works as an ideal rectifier so that current and voltage should be in phase; if the d-axis is aligned with the phase 'A' voltage, then the current and voltage at the q axis is zero and $e_d = \hat{e}$, the peak input line-to-neutral voltage. Considering this condition, the steady-state converter state-space equations can be expressed as

$$\hat{e} = -RI_d - \frac{V_{PN}}{3}m_d \qquad (4-15)$$

$$\omega I_d = \frac{V_{PN}}{3L}m_q \qquad (4-16)$$

The value of the modulation indices in the dq reference frame (M_d and M_q) from the (7) and (8) results in

$$m_d = \frac{3(\hat{e} - R \cdot I_d)}{V_{PN}} \qquad (4-17)$$

$$m_q = \frac{3 \cdot \omega \cdot L \cdot I_d}{V_{PN}} \qquad (4-18)$$

The modulation signals for the legs are calculated by using an inverse reduced Park transform that is an upper-left 2 by 2 Park transform matrix T_R^{-1} as shown here

$$T_R^{-1} = \frac{2}{\sqrt{3}}\begin{bmatrix} -\cos\left(\omega t + \frac{\pi}{3}\right) & \sin\left(\omega t + \frac{\pi}{3}\right) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix} \quad (4-19)$$

$$\begin{bmatrix} m_a \\ m_b \end{bmatrix} = T_R^{-1} \cdot \begin{bmatrix} m_d \\ m_q \end{bmatrix} \quad (4-20)$$

The modulation signals for the legs can be expressed as

$$\begin{bmatrix} m_a \\ m_b \end{bmatrix} = \begin{bmatrix} Mcos\left(\omega . t - \frac{\pi}{6} + \varphi\right) \\ Mcos\left(\omega . t - \frac{\pi}{2} + \varphi\right) \end{bmatrix} \quad (4-21)$$

and the modulation signal parameters, including modulation index M and phase shift φ can be expressed as

$$M = \frac{2\sqrt{3}}{V_{PN}}\sqrt{(\hat{e} - R.I_d)^2 + (\omega L I_d)^2} \quad (4-22)$$

$$\varphi = tan^{-1}\frac{\omega L I_d}{\hat{e} - R.I_d} \quad (4-23)$$

Since the DC-DC stage operates with same PWM pattern that is generated with respect to (16), the output voltage of the proposed converter can be expressed as

$$V_o = \frac{V_{PN} \cdot \omega}{2 \cdot n \cdot \pi}\int_T^{T+\frac{\pi}{\omega}} |m_a(\tau) - m_b(\tau)|\, d\tau = \frac{V_{PN} \cdot M}{n \cdot \pi} \quad (4-24)$$

Combining (17) and (19), the output voltage can be expressed as a function of I_d as follows:

$$V_o = \frac{2\sqrt{3} \cdot \sqrt{(\hat{e} - R.I_d)^2 + (\omega L I_d)^2}}{n.\pi} \qquad (4-25)$$

where n is the transformer turns ratio.

By calculating I_d from (25) and plugging in (22), the value of V_o for steady-state operation can be expressed as

$$V_o = \frac{\sqrt{3}\hat{e}\sqrt{2(R_L n\pi)^2 - 2\sqrt{(R_L n\pi)^4 - 256(R_L \omega L)^2}}}{8\omega L} \qquad (4-26)$$

n can be then selected based on (26). It should be mentioned that R, which is the internal resistance of an input inductor, is neglected in (26). Figure 4.8 shows the variation of output voltage with respect to R_L and n. As shown in Figure 4.8 the value of n=2.25 and the load variation from 10% to 100% does not change the energy equilibrium point considerably.

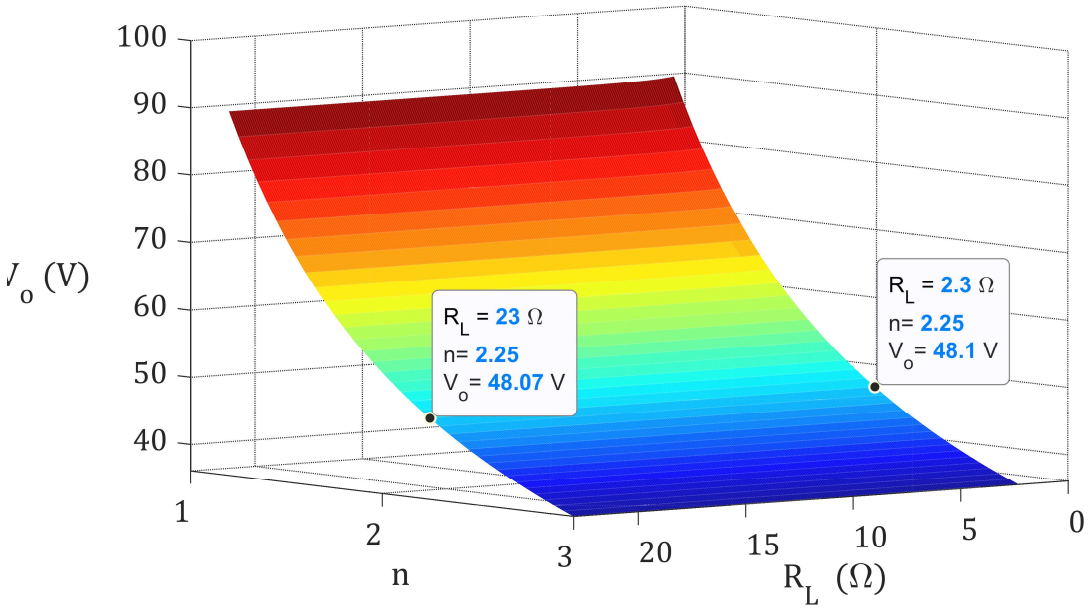


Figure 4.8. Output voltage variation with respect to the RL (x- axis) and transformers turns ratio (y-axis)

4.5.4 DC bus voltage

The DC bus voltage should be sufficiently large to ensure that there is sufficient output voltage when the converter operates at full load condition[102]. The minimum value of the DC bus voltage for a four-switch rectifier in general should be

$$2\sqrt{3}\hat{e} < V_{PN} \qquad (4-27)$$

where $\hat{e}$ represents the peak value of the grid line-to-neutral voltage.

The intermediate DC bus voltage in SSPFCs is not controlled and is dependent on the energy balance between power from the input and power transferred to the output under steady-state conditions. The maximum value of the intermediate DC bus voltage is thus used to determine the voltage rating of DC bus capacitors. The DC bus voltage equation for the low-frequency model is shown in (3). In this part, the constant power model is replaced by a more precise model for the DC-DC stage to calculate the intermediate DC bus current and voltage.

Power transfer from the intermediate DC bus capacitors to the output occurs during a switching cycle, and the switches' duty ratio varies with a low frequency (60Hz) so that the conventional averaging method cannot be used. A method presented in [104] is used instead in this thesis to determine DC bus voltage variations based on output power variations. The method is based on the multi-frequency averaging method that was introduced in [105] that considers the variation of the switches' duty ratio and is used in this thessis to calculate the power transfer in the DC-DC stage.

The power that is transferred to the output can be expressed as

$$P_{out} = \frac{{V_o}^2}{R_L} = < \mathrm{v}_{AB} >_1 < \mathrm{I}_{pri} >_1 \qquad (4-28)$$

where $< x >_k$ shows the kth coefficient of Fourier series of parameter x as defined in [105]. It should be mentioned that blocking capacitor (C_b) blocks the DC component (index-0) of the current. Since the AC component of V_{PN} is much smaller than the DC component of V_{PN}, (28) can be simplified to be

$$P_{out} = \frac{{V_o}^2}{R_L} = V_{PN} < \mathrm{S}_a - \mathrm{S}_b >_1 < \mathrm{I}_{pri} >_1 \qquad (4-29)$$

Considering (29) and (12), the first coefficient of Fourier series for the intermediate DC bus can be expressed as

$$< C\frac{dV_{PN}}{dt} >_1 = < 2\mathrm{S}_a - 1 >_1 i_a + < 2\mathrm{S}_b - 1 >_1 i_b + 2 < \mathrm{S}_b - \mathrm{S}_a >_0 < \mathrm{I}_{pri} >_1 \qquad (4-30)$$

$< \mathrm{I}_{pri} >_1$ for a typical switching period can be determined to be

$$< \mathrm{I}_{pri} >_1 = \frac{< 2\mathrm{S}_a - 1 >_1 i_a + < 2\mathrm{S}_b - 1 >_1 i_b - < C\frac{\Delta \times V_{PN}}{\mathrm{T}_s} >_1}{-2(d_b - d_a)} \qquad (4-31)$$

where $\Delta \times V_{PN}$ is the variation of thevDC bus voltage in each switching cycle due to current that passes through the capacitors; d_b and d_a are the duty-ratios of S_1 and S_2 as shown in Figure 4.5. Substituting (31) in (29), the equation of steady state operation for intermediate DC bus voltage can be written as

$${V_{PN}}^2 \frac{\Delta < \mathrm{S}_a - \mathrm{S}_b >_1}{-2\mathrm{T}_s(d_b - d_a)} + V_{PN}\frac{< 2\mathrm{S}_a - 1 >_1 i_a + < 2\mathrm{S}_b - 1 >_1 i_b}{-2(d_b - d_a)} - P_{out} = 0 \qquad (4-32)$$

The first Fourier series coefficient of the switching functions can be determined from the complex Fourier transform definition in [105] and can be written as

$$< \mathrm{S}_i >_1 = \frac{1}{T}\int_{t-T}^{t} \mathrm{S}_i(\tau) e^{-j\omega_s \tau} d\tau \qquad (4-33)$$
$$i \in a, b$$

The switching functions are shown in Figure 4.5. Considering the integration period from one of the positive peaks of the carrier waveform up to the next positive peak, (33) can be solved and the result can be expressed as

$$< \mathrm{S}_i >_1 = \frac{-1}{\pi} \sin(d_i \pi) \qquad (4-34)$$
$$i \in a, b$$

with the value of $< \mathrm{S}_i >_1$ beings a real value. By replacing (34) in (32), a second order linear equation can be derived in terms of V_{PN} and then used to plot the DC bus voltage variation as shown in Figure 4.9. i_a and i_b are the phase current magnitudes and d_a and d_b are limited between 0 and 1.

The DC bus voltage in the proposed converter is not fixed as it is in a two-stage converter because the converter is a single-stage converter that has just a single controller that is used to regulate the output voltage. This voltage is dependent on the energy equilibrium that exists between the energy that is fed to the DC bus from the input and the energy that is transferred from the DC bus to the output.

The proposed converter has the characteristic that its DC bus voltage rises as its load increases; the converter presented in [104] has the same characteristic. This characteristic differs from what is typically found in most other single-controller, single-stage AC-DC converters. This is because for both the proposed converter and the converter in [104], the difference in the PWM pattern that produces V_A and V_B at both ends of the transformer, V_{AB}, becomes smaller so that V_{AB} is zero more often, which results in less opportunity for energy to be transferred from the DC bus to the output, which affects the DC bus energy equilibrium so that the DC bus voltage is increased. This characteristic is actually advantageous because issues with high DC bus voltage are only encountered during heavy load operation and the load can be limited, whereas in most other single-stage converters, these issues are encountered when the converter operates with light loads, which is generally unavoidable unless the load is fixed.

It should be noted that the DC bus voltage is the peak switch voltage stress.

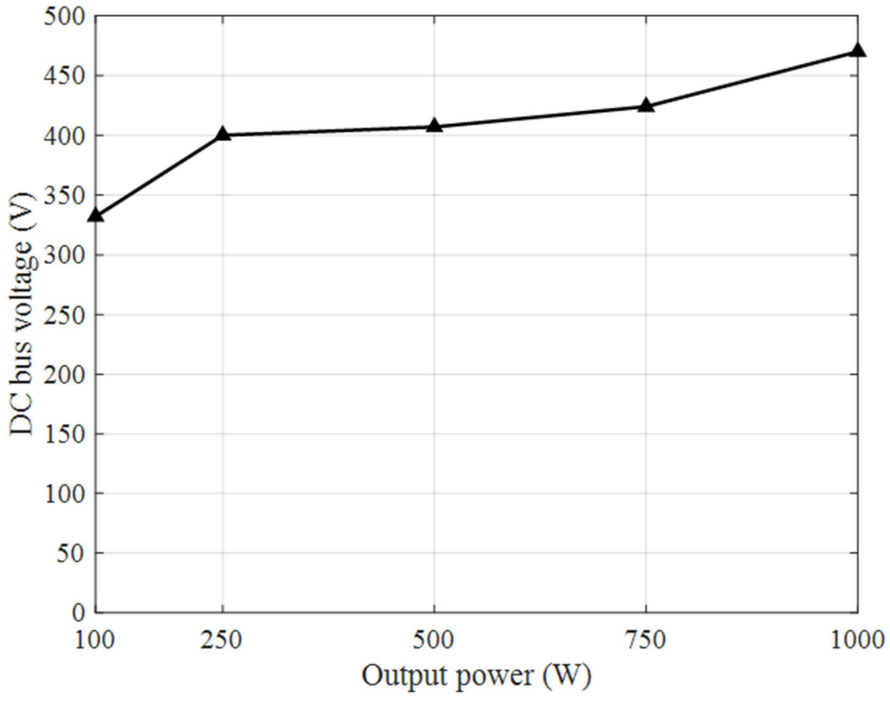


Figure 4.9. Maximum DC bus voltage

4.5.5 ZVS range

To achieve ZVS in the converter switches as discussed in Section II.B, the magnitude of DC-DC converter current component should be larger than AC-DC converter current component over the AC line cycle

$$|I_{DC-D}\ | > |I_{AC-D}\ | \qquad (4-35)$$

The magnitude of DC-DC converter can be expressed as

$$|I_{DC-DC}| = \frac{I_{L_O}}{n} \qquad (4-36)$$

so that the magnitude of the primary current of the DC-DC converter is equal to I_{L_O}. I_{L_O} can be approximated by a DC current that is the sum of the load current and a component with double frequency (120 Hz). Neglecting the voltage drop across the input filter at line frequency, I_{L_O} can be expressed as [26]:

$$I_{L_O} = \frac{P_o}{V_o} - \frac{\sqrt{3}e_a}{3\pi\omega L_O}\cos(2\omega t) \qquad (4-37)$$

where $\omega = 2\pi 60$, and P_o is the output power. The AC-DC sub-converter current can be calculated as

$$I_{AC-DC} = \frac{\sqrt{2}P_o/\eta}{3e_a}\sin(\omega t) \qquad (4-38)$$

Combining (35) and (38) and rearranging the result results in

$$L_o \geq -\frac{\sqrt{3}e_a^2\cos(2\omega t)\,V_o}{\pi P_o\omega(\sqrt{2}\sin(\omega t)\ V_o\eta n - 3e_a)} \qquad (4-39)$$

where $0 \leq t \leq 1/f_{line}$.

The positive part of the right-hand side of (39) is plotted in Figure 4.10 with respect to time and output power. As shown in Figure 4.10, the upper limit of the right side of (39) occurs at minimum output power. The value of L_o needed to achieve ZVS in the proposed converter can then be selected based on the upper limit. It means such other converters the minimum load is the key factor to select L_o. In order to achieve ZVS in the converter switches for at least 25% of the nominal full load, the value of L_o is chosen to be 9.4 mH.

4.6 Simulation and Experimental results

The output inductor value that was derived in the previous section is generally considered to be very high for most applications. This inductor has a high value because of the converter has a large low-frequency component (2 x 60 Hz = 120 Hz) at its output as the transformer primary voltage varies with the input line cycle. This makes the proposed converter most suitable for applications such as aerospace like the converter proposed in [104] where the input line frequency is 400 Hz, which results in less current ripple and thus less inductance at the output or for applications where the converter's output is connected to a battery such as a battery charger or a telecom power system with battery backup.

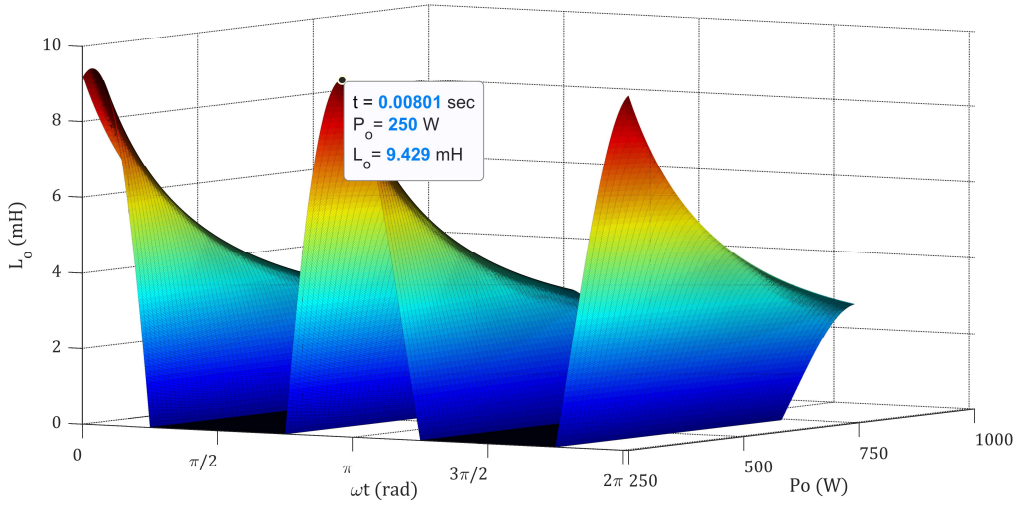


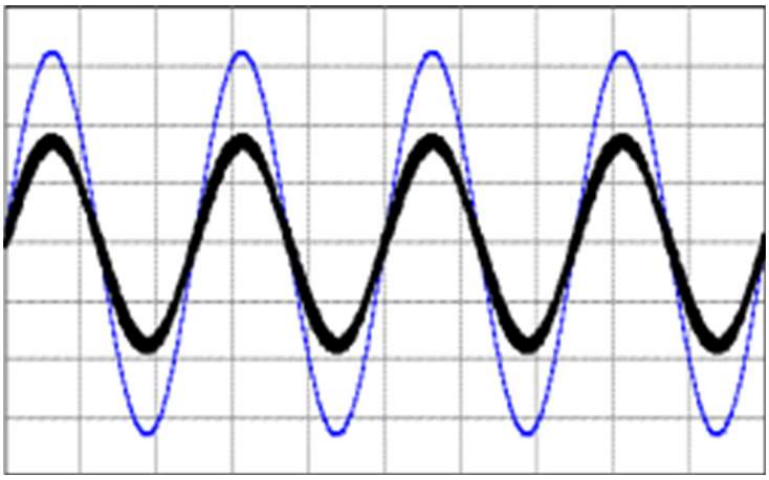
Figure 4.10. The minimum value of L to achieve ZVS

In order to see how the proposed converter would work with a 400 Hz input voltage supply, computer simulations were performed using PSIM software. The converter was simulated with the following parameters, which were almost the same as those used in [104]: Input voltage V_{LL}=115V, f=400Hz, output voltage V_o = 28 V, maximum output power $P_{o,max}$ = 2kW and switching frequency f_{sw} = 50 kHz. The input inductors were 1.2mH, C_b=180 nF and L_r=2 µH, and the transformer turns ratio was 8:1, The values of L_o and C_o values were L_o=800 µH, and C_o=3000 µF. It should be noted that the value of L_o is much smaller than it would be if the converter was implemented with 60 Hz input frequency.

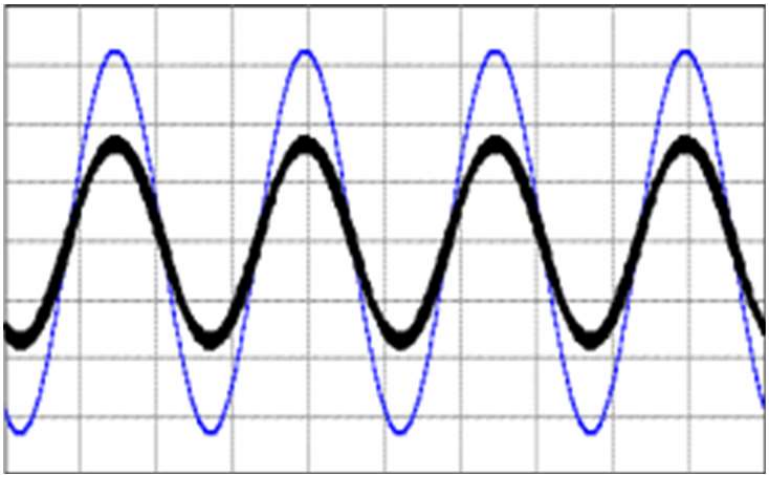
Figure 4.11 shows typical waveforms of the simulated converter. The phase currents and phase voltages for phase A, B, and C are shown in Figure 4.11 (a), Figure 4.11(b), and Figure 4.11(c). It can be seen that the input current is continuous and in phase with input voltage for all phases. Figure 4.11(d) shows the output voltage; it can be seen that output voltage is 28V with an 800Hz (twice the line frequency) ripple. Voltage V_{PN} is shown in Figure 4.11(e); it is an 800 V DC voltage. Figure 4.11(f) shows V_{AB}, the voltage across the transformer primary and blocking capacitor, and the primary current $I_{pri;}$ it can be seen that they are square waveforms that are similar to what can be found in a typical DC-DC

PWM full-bridge converter. The DC component of the voltage waveform can be removed by the blocking capacitor.

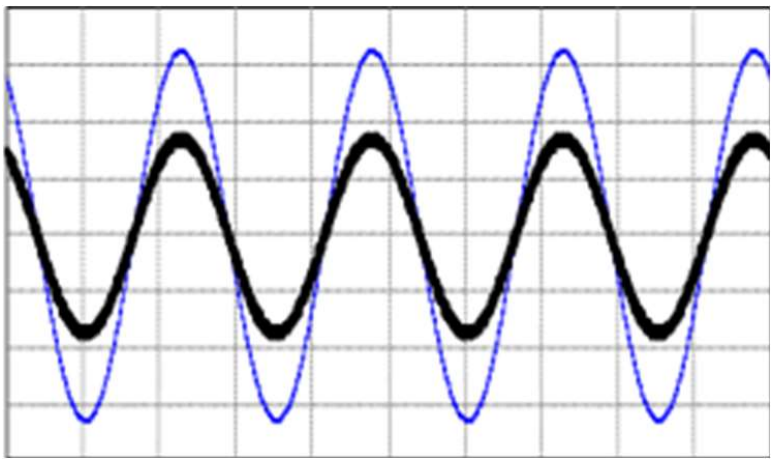
A simple proof-of-concept prototype of the proposed converter was built to verify its feasibility. The following specifications are used to build the prototype: Input voltage V_{LL}=120V, output voltage V_o = 48 V, maximum output power $P_{o,max}$ = 1kW and switching frequency f_{sw} = 50 kHz. The devices used for switches S_1-S_4 were FCA20N60 MOSFETs, D_1-D_2 and RURG3060 devices were used for the output rectifying diodes. The input inductors were 1.2mH, C_b=1 μF and L_r=5.5 μH, and the transformer turns ratio was 2:1, L_o and C_o values were L_o=9 mH, and C_o=4700 μF. The converter was implemented with the decoupled power flow control method and with conventional SPWM, using a TMS320F28069M DSP.



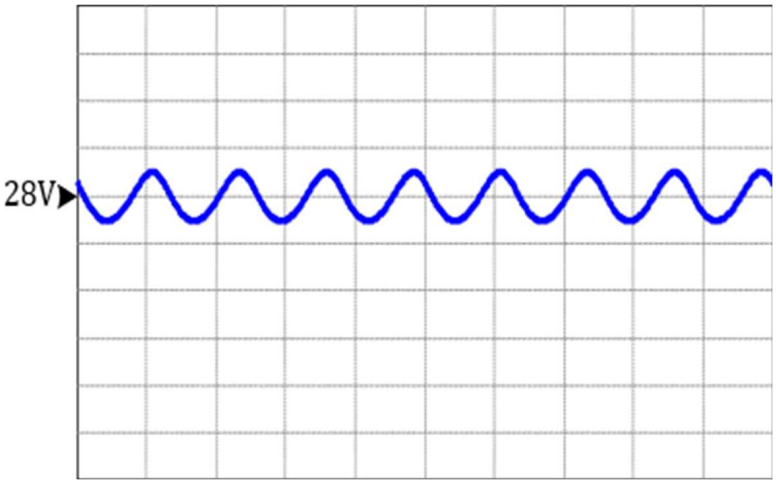
(a) phase A voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)



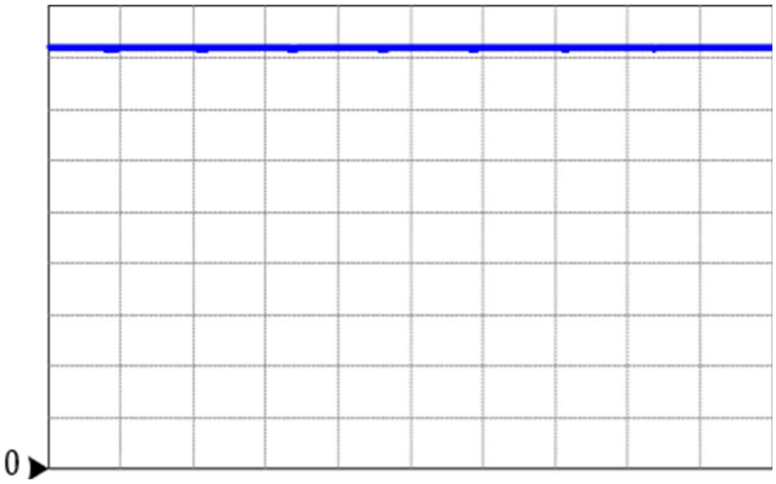
(b) phase B voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)



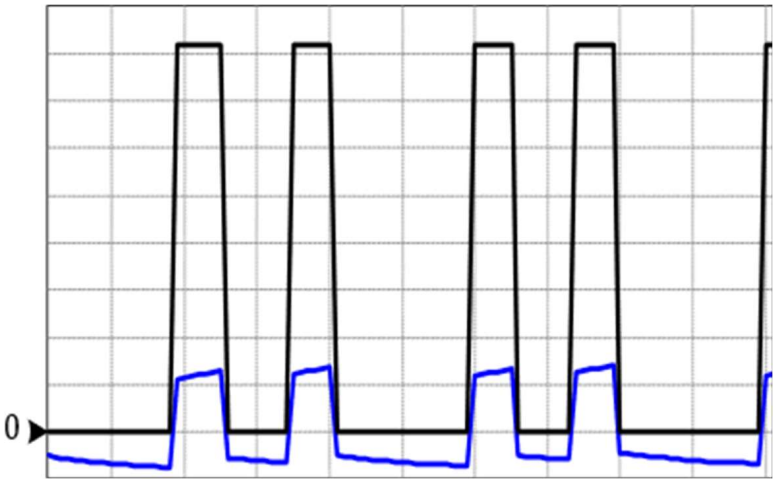
(c) phase C voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)



(d) phase A voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)



(e) phase B voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)

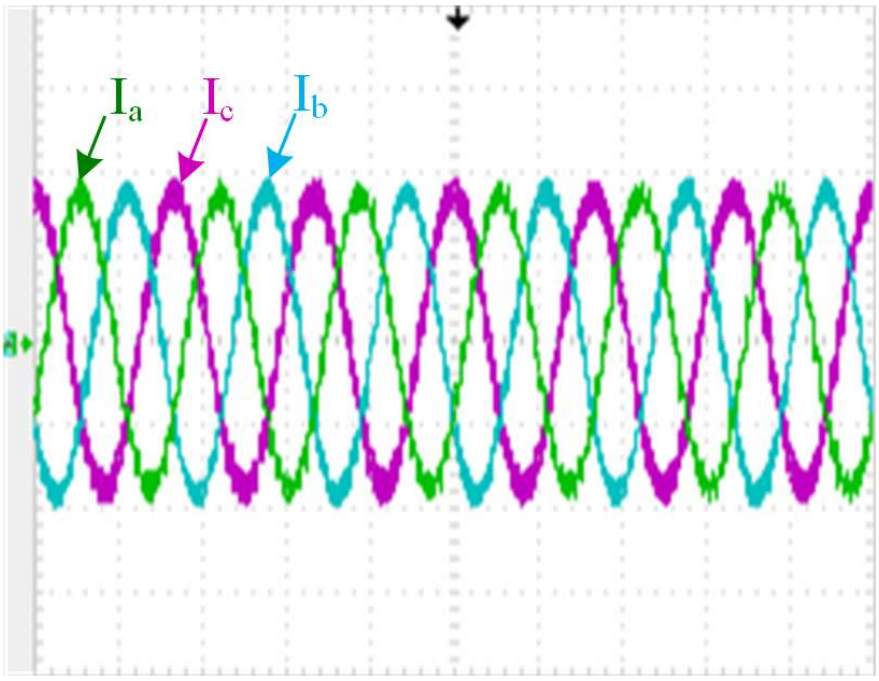


(f) phase C voltage and current (I: 10A/div., V: 100V/div., t: 1 ms/div.)

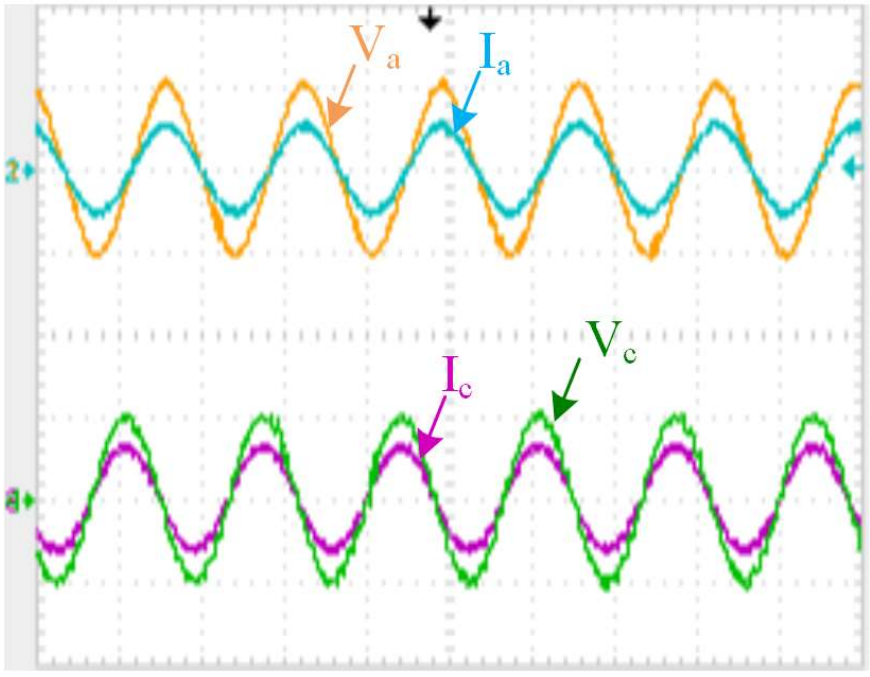
Figure 4.11. Simulated converter waveforms

Figure 4.12 shows typical converter waveforms at full load. The three phase input currents are shown in Figure 4.12(a) and two phase currents and voltages (phase A and C in Figure 4.1) are shown in Figure 4.12(b). As can be seen, the three-phase input currents are all sinusoidal and in phase with the input voltage. The harmonic contents of the input current for a typical phase (phase A) is shown in Figure 4.12(c) for full load and half load. It can be seen that the harmonics are lower than the limits specified by the IEC61000-3-2 Class A standard; moreover, the power factor was about 0.99 for full load and half load. A typical waveform of the voltage across a switch (S_1) is shown along with its gate source voltage and complementary switch gate source voltage in Figure 4.12(d). It can be seen that it is similar to a switch voltage waveform commonly seen in a DC-DC full-bridge converter; also, after S_3 turns off, the primary current discharges the output capacitance of S_1 during the dead-time and S_1 turns on with ZVS. Voltage V_{AB}, the voltage across the transformer primary and blocking capacitor, and I_{pri} are shown in Figure 4.12(e). It can be seen that the waveforms are similar to what can be found in a typical DC-DC PWM full-bridge converter. The output rectifier current is shown in Figure 4.12(f); it can be seen that it is a DC current with a 120 Hz ripple. The 120 Hz ripple is due to the change in duty cycle over a line cycle; however, C_b attenuates the low frequency components of the voltage that is applied to the transformer primary winding so that the transformer does not saturate.

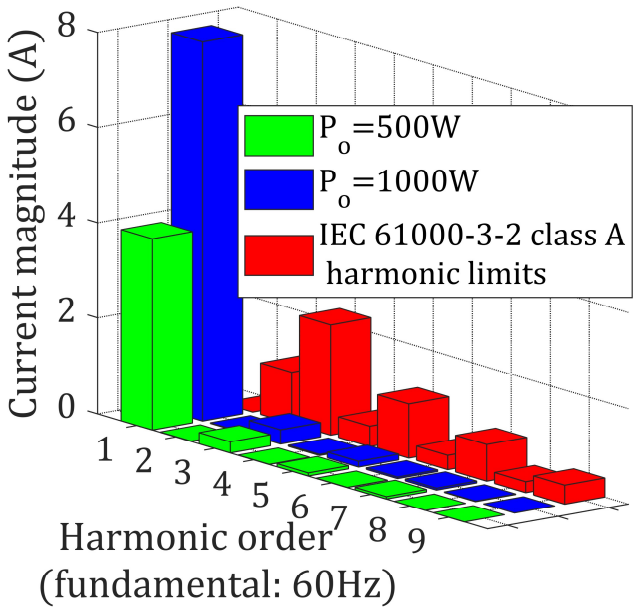
Figure 4.13 shows a graph of curves of efficiency versus output load for the proposed converter. A maximum efficiency of about 87% was obtained for the converter prototype. It should be noted that an efficiency of 98% was reported for the three-phase six-switch single-stage converter in [104], which used SiC devices and output synchronous rectifiers. A higher efficiency can be obtained for the proposed converter if a similar implementation is used.



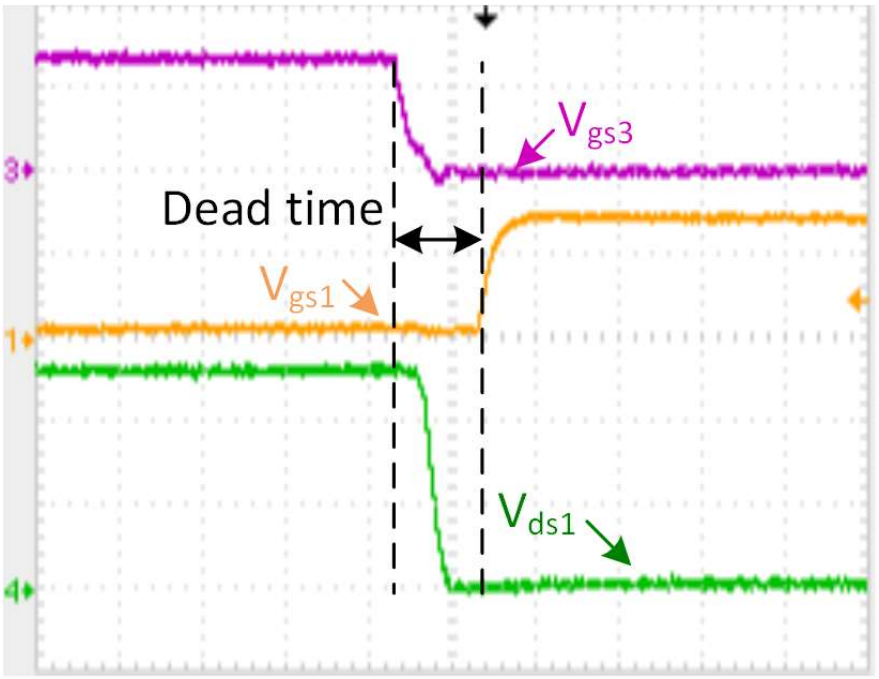
(a) Three phase input currents (I: 5A/div, t: 10 ms/div.)



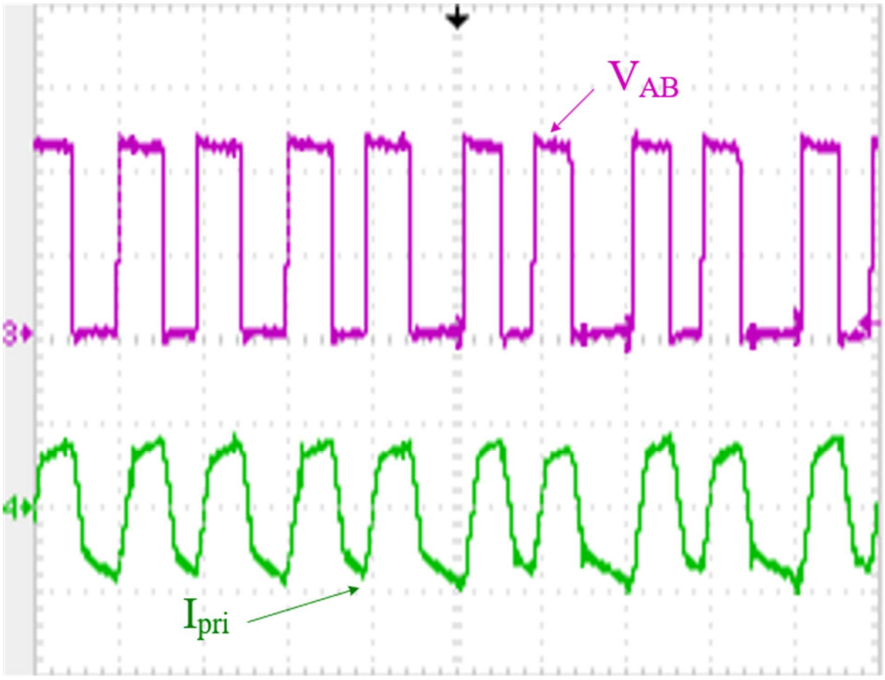
(b) phase A and Phase C voltage and current (I: 10A/div., V: 100V/div., t: 10 ms/div.)



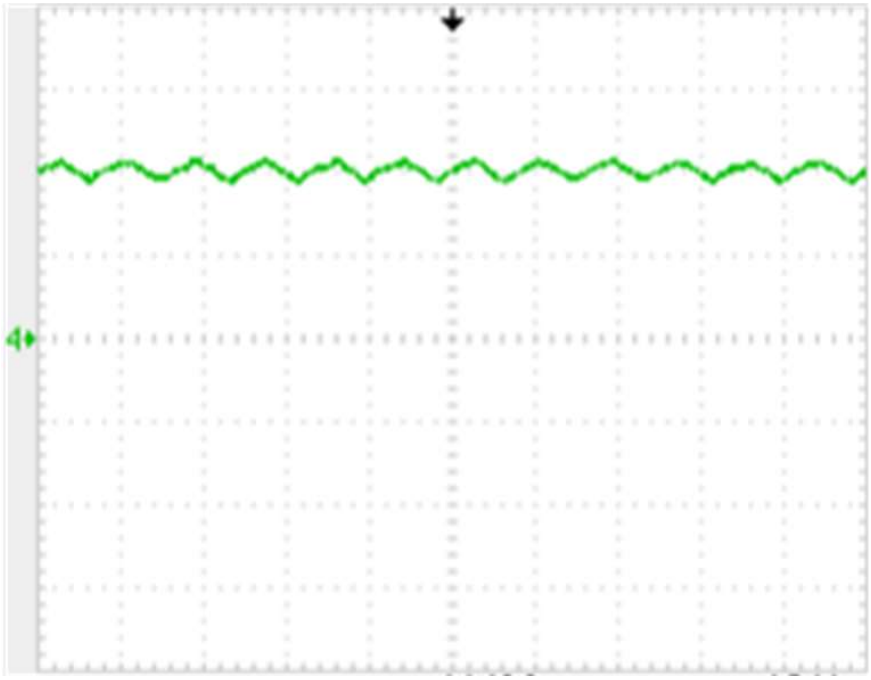
(c) Harmonic contents of phase A at full load and current and IEC61000-3-2 harmonic limits for class A equipment



(d) S_1 and S_2 gate source voltage (V: 10V/div., t: 500 ns/div.), and S_1 drain source voltage (V: 200V/div., t: 500 ns/div.)



(e) V_{AB}, and I_{pri} (V: 200V/div., I: 10A/div, t:10µs/div.)



(f) Output current (I: 10A/div., t: 10 ms/div.)

Figure 4.12. Typical converter waveforms

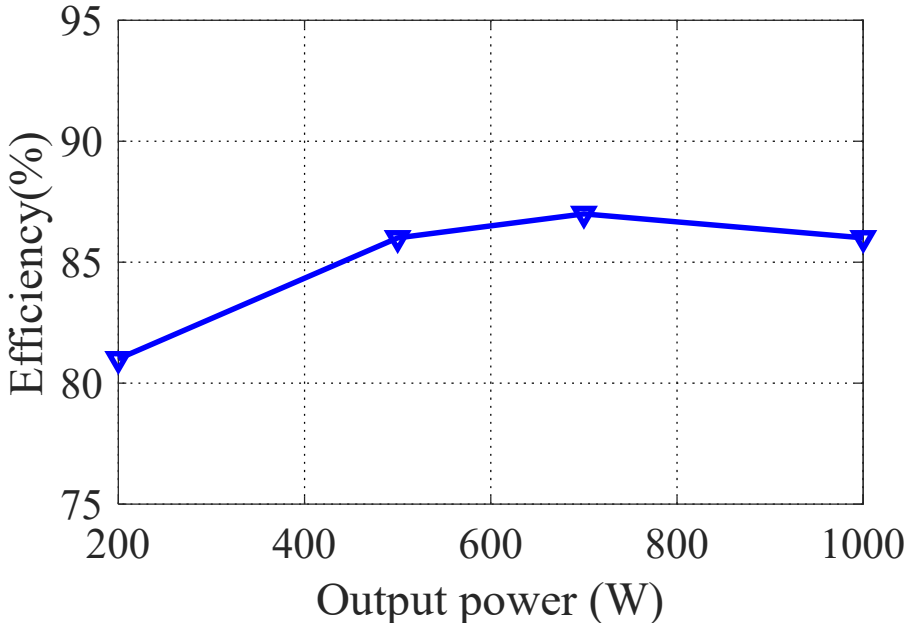


Figure 4.13. Converter efficiency

4.7 Conclusion

A new three-phase, four-switch AC-DC converter with transformer isolation was proposed in this chapter. In the chapter, the converter's general operation and its modes of operation were explained in detail, a steady-state mathematical model of the converter was derived, a design procedure of the converter was developed and demonstrated with a design example, and experimental results from a simple proof-of-concept prototype were presented in Section V.

The outstanding features of the proposed converter are that it has only four switches in its topology, it is bridgeless, its input currents are continuous, and it can be implemented with any control method used in standard three-phase, six-switch voltage source rectifiers. Its main drawbacks are that it has a significant low-frequency ripple and a DC bus voltage that increases as its load increases. The first drawback is not an issue if the converter is used in aerospace applications where three-phase 400 Hz AC voltage supplies are used or in applications where the converter's output is connected to a battery such as a battery charger or a telecom power system with battery backup. The second drawback is more

significant as it increases component stress and limits the load range of the converter to 2 kW – 3 kW if 1200 V devices are used, a load range that is the maximum on most other three-phase single-stage converters.

In essence, the proposed converter does away with issues caused by discontinuous input currents with high peaks such as high current stresses, turn-off losses, and noise that typically place limitations on three-phase single-stage converters, but places high voltage stress on its components. Nonetheless, the proposed converter has fewer semiconductors than any other topology of its kind and is thus the simplest and least expensive three-phase single-stage AC-DC converters with galvanic isolation in existence.

Chapter 5

5 Simplified Hybrid AC-DC Microgrid with a Novel Interlinking Converter

5.1 Introduction

A split DC bus converter can be used to simplify HMGs with IBA structure for ICT applications, since two conventional converters can be replaced by a split DC bus converter. Using split DC bus capacitor reduces the size and cost of HMGs.

In this chapter, a new, simpler, more flexible structure for an HMG is proposed. The proposed architecture, shown in Figure 5.2, requires fewer power electronic converters than the conventional structure shown in Figure 5.1 as it is based on a new multi-port IC (MP-IC) that interfaces an AC sub-grid to two DC sub-grids at the same time – one

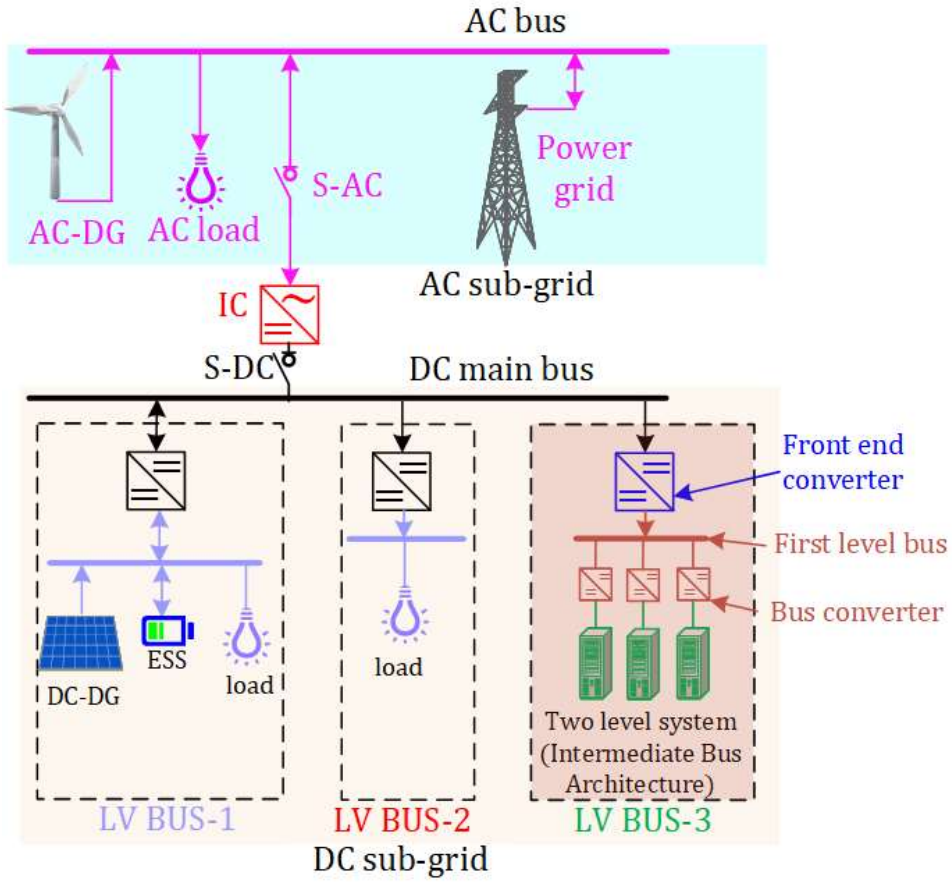


Figure 5.1. A typical HMG

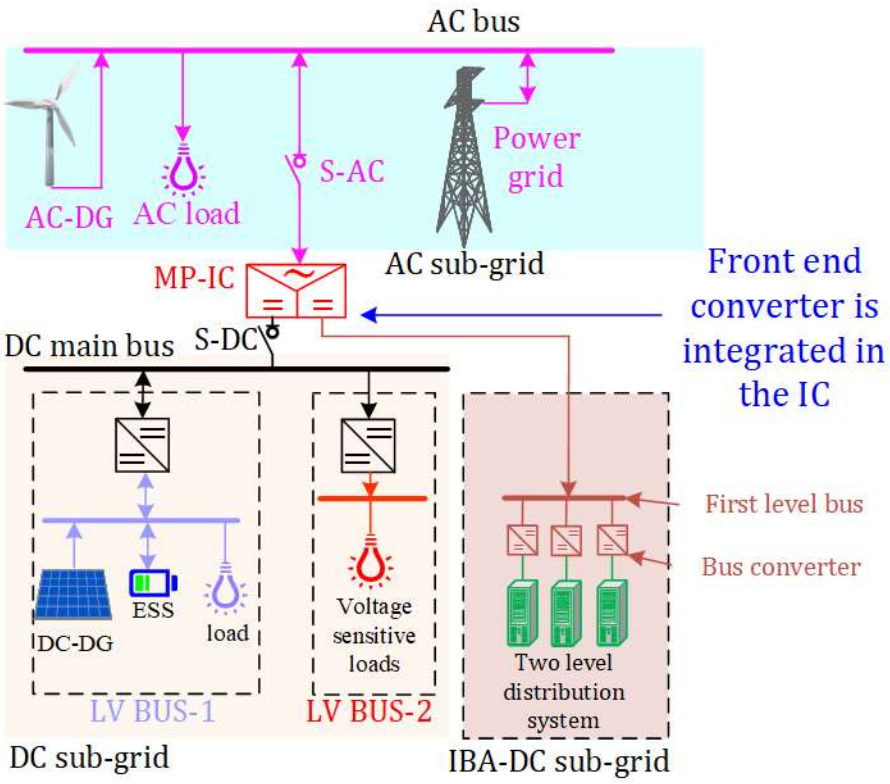


Figure 5.2. Simplified HMG

connected to a high-voltage DC main bus, the other connected to a low-voltage first-level DC bus. The IC can provide an output with galvanic isolation between the high-voltage and low-voltage DC systems so that it becomes possible to design DC load clusters with non-isolated DC-DC converters that reduce the overall cost of the system. Some of the outstanding features of the new IC are that it can be implemented with only six switches and that it can be operated as a bidirectional converter with any control method that is typically used in conventional AC-DC converters.

In the chapter, the basic principles related to the simplification of a typical HMG by using the new MP-IC are explained. The dynamics of the MP-IC are investigated using state equations and these state equations are compared to those of a conventional six-switch non-isolated converter. Experimental results from a simple proof-of-concept prototype are presented to confirm the feasibility of the proposed IC. Simulation results that show the effect of load variations in the IBA DC bus on the operation of the HMG are also presented as well.

5.2 Simplified HMG Structure and its components

In this section, it is explained how the new IC can simplify the architecture of the HMG in Figure 5.1, at the system level. The topology and operation of the proposed IC is then explained and its features are presented.

5.2.1 System-level simplification

In the HMG shown in Figure 5.1, a cluster of DC loads at LV BUS-3 is supplied by the IBA DC distribution system, which means that the intermediate bus can be supplied by a semi-regulated voltage, as explained in Section I. In such a HMG, it becomes possible to eliminate the front-end converter and integrate it into the IC without affecting the ability to control the IC. In the simplified HMG shown in Figure 5.2, the number of power electronic converters is reduced as the IC can supply the LV BUS-3 (IBA DC system) from both the AC and DC sub-grids; this increase the flexibility of the system design.

From the point of view of generation, storage, and load, the HMG shown in Figure 5.2 has the same structure as that in Figure 5.1, but the use of a MP-IC provides the following benefits:

- A front-end converter for the DC distribution system with an IBA is eliminated from the HMG structure.

- A DC distribution system with an IBA can supply voltage directly from the AC or the DC sub-grids. This means that if the AC or DC buses are out of service, the out-of-service bus can be isolated by a switch disconnector (S-AC or S-DC) and the DC distribution system with the IBA can be supplied from another bus. The availability of power delivered to the DC distribution system with the IBA thus increases.

- The power flow between the AC sub-grid and the main DC bus is the same as that of conventional ICs

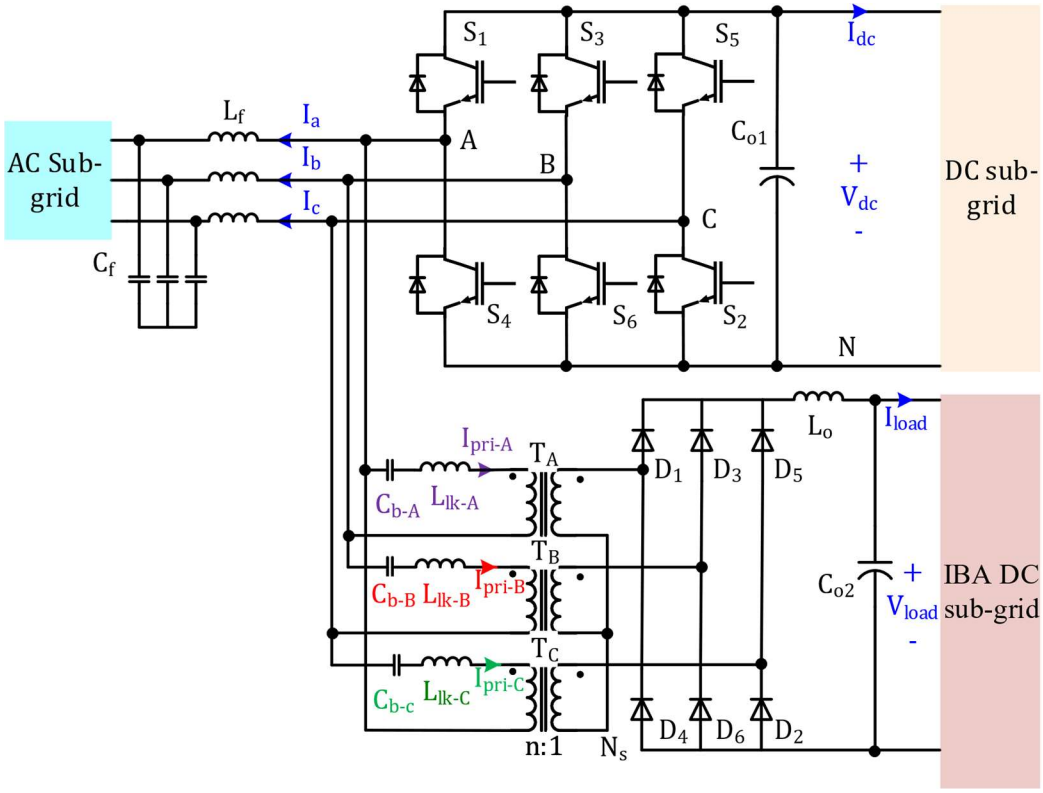
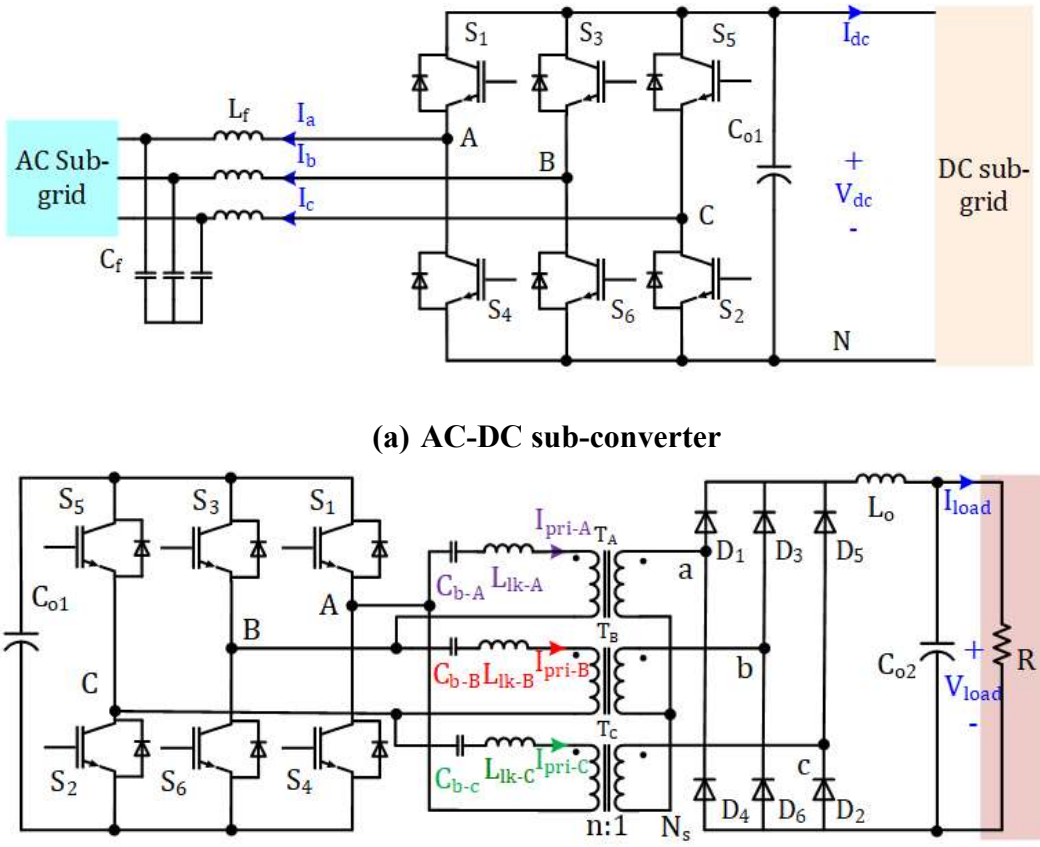


Figure 5.3. Proposed MP-IC

5.2.2 Proposed MP-IC

The proposed MP-IC that can be used in the simplified HMG shown in Figure 5.2 is shown in Figure 5.3. The proposed MP-IC consists of three input inductors L_f with internal resistance equal to R_f, three filter capacitors C_f, a six-switch three-phase inverter with switches S_1- S_6 and a capacitor C_{o1} in the DC main bus, three blocking capacitors C_{b-A} - C_{b-C}, three identical isolation transformers T_A - T_C with n:1 turns ratio and leakage inductance L_{lk}, six output rectifying diodes D_1-D_6 and an output filter consisting of an inductor L_o and a capacitor C_{o2} at the IBA DC sub-grid.

The proposed IC combines a bidirectional six-switch three-phase AC-DC sub-converter (BADSC) with a three-phase unidirectional full bridge DC-DC sub-converter (UDDSC) and these sub-converters share switches. The circuit diagram of each sub-converter is shown in Figure 5.4; it should be noted that the loads in the IBA DC sub-grid are modelled



(a) AC-DC sub-converter

(b) DC-DC sub-converter

Figure 5.4. Proposed MP-IC stages

as a resistor (R). The operation of the individual sub-converters is described first in this section, then the operation of the whole converter is explained.

5.2.2.1 Bidirectional AC-DC sub-converter (BADSC)

In essence, the bidirectional stage of the proposed MP-IC, which is shown in Figure 5.4(a), is a six-switch voltage source converter (VSC) that is connected between the AC sub-grid and the main DC bus. The power transfer at the BADSC happens at line frequency (i.e. 60 Hz). The BADSC operates as a conventional VSC and controls the active and reactive power exchange between the AC and DC sub-grids by applying a proper three-phase voltage at points A, B, and C. The voltages are generated based on three modulation signals that are generated by the control system; a set of typical modulation signal ($m_a, m_b,$ and m_c) is shown in Figure 5.5(a). The duty cycle of each upper switch in each

leg is determined by comparing the associated modulation signal with a double edge triangular carrier waveform, and the lower switch of each leg operates complementarily to that of the corresponding upper switch of the same leg, with an appropriate dead-time inserted to avoid any shoot-through.

5.2.2.2 Unidirectional DC-DC sub-converter (UDDSC)

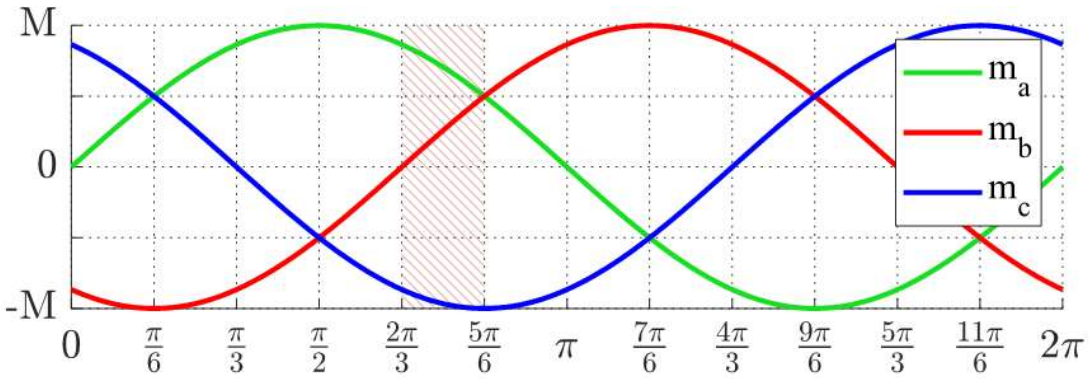
The unidirectional DC-DC (UDDSC) is shown in Figure 5.4(b). In essence, its structure is like that of a conventional three-phase full-bridge (3P-FB) DC-DC converter such as the one proposed in [106]. The only difference between the UDDSC and a conventional 3P-FB is the way in which the value of the converter duty cycle is obtained. In a conventional 3P-FB, the duty cycle of the switches is set by a dedicated controller with respect to the DC output voltage, but, in the UDDSC, the duty cycle of the switches is set by the control system of BADSC. Since the modulation signals variation is slow in comparison with switching frequency, the duty cycle of UDDSC can be assumed constant during each switching period. Based on this assumption, the modes of operation of the UDDSC can be explained with respect to the switching pattern, which is SPWM in this converter. Figure 5.5(b) shows the modulation signals for several switching cycles, along with the carrier signal, associated gating signals, the voltage across the transformer primary and the DC blocking capacitor for all transformers ($V_{AB}, V_{AC},$ and V_{CA}), in the region defined by shaded area of Figure 5.5(a) ($\frac{2\pi}{3} < \omega t < \frac{5\pi}{6}$),.

The six switch converter acts as a 3P-FB converter and applies three square-wave voltages with a DC component across point A and B (V_{AB}), B and C (V_{BC}), and C and A (V_{CA}). The DC and line frequency components of each square-wave is blocked by a series DC blocking capacitor ($C_{b-A}, C_{b-B},$ and C_{b-C}) and the high frequency AC component of the voltage is applied to the associated transformer primary winding. The AC component passes through the high-frequency isolation transformers and, after rectification, a low pass LC filter removes the switching frequency components from the output voltage. The output LC filter is designed to work in current continuous conduction mode to reduce current stress and to have a smoother current at the output of the UDDSC.

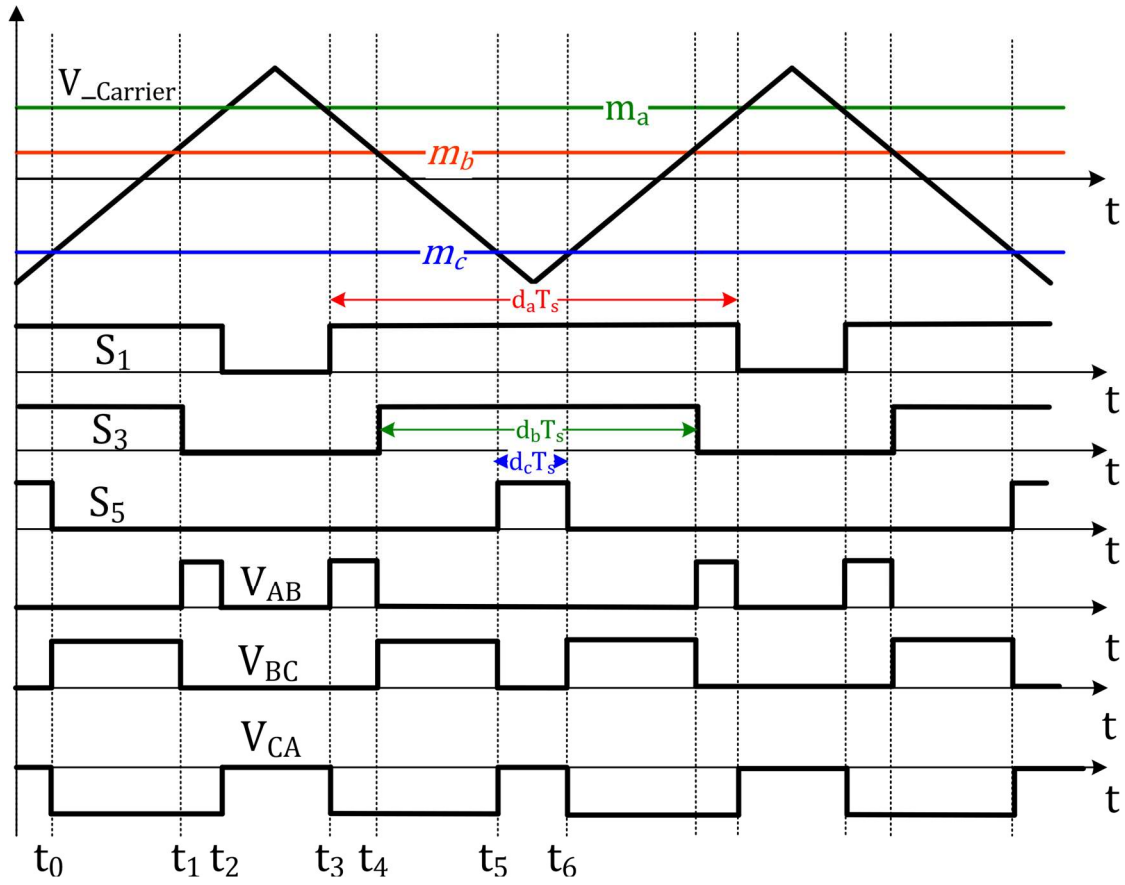
The converter modes of operation can be analyzed in ($\frac{2\pi}{3} < \omega t < \frac{5\pi}{6}$) time region. The modes of operation of the UDDSC with respect to the gate pulses shown in Figure 5.5(b) are explained for a switching cycle and an equivalent circuit for each mode shown in Figure 5.6.

The following assumptions will be used to explain the operation modes of the UDDSC:

- The output filter current (I_{Lo}) is continuous so that two diodes at the secondary always conduct.



(a) Line frequency



(b) Switching frequency modulation signals, switches status and inverter terminal voltages (V_{AB}, V_{BC}, V_{CA})

Figure 5.5. Typical modulation signals

- The secondary windings of the transformers are connected with a wye connection so that in each mode, I_{Lo} passes through two secondary windings and the reflected current passes through two primary windings.

- The polarity of the transformer primary voltage specifies the current direction in the transformer primary windings.

- V_{dc} is higher than the peak value of the phase-to-phase voltage.

- Since the phase-to-phase voltage is blocked by the DC blocking capacitors, at t_0, the relation between the DC blocking capacitor voltages are $V_{Cb-B(t0)} > V_{Cb-A(t0)} > 0 > V_{Cb-C(t0)}$ and $|V_{Cb-C(t0)}| > |V_{Cb-B(t0)}| > |V_{Cb-A(t0)}|$

Mode 1 ($t_0 < t < t_1$)

This mode begins when switch S_5 is turned off. During this mode, V_{AB} is equal to zero, V_{BC} is equal to $+V_{dc}$, and V_{CA} is equal to $-V_{dc}$. Writing the KVL equation for each transformer primary, V_{Pri-A} is equal to $(-V_{Cb-A})$, V_{Pri-B} is equal to $(V_{dc} - V_{Cb-B})$, and V_{Pri-C} is equal to $-(V_{dc} + V_{Cb-C})$. This means that the primary winding of T_B is connected to the highest positive voltage and the primary winding of T_C is connected to the highest negative voltage. Based on the polarities at the secondary side, the upper diodes associated with T_B (D_3) and the lower diodes associated with T_C (D_2) are conducting. At the primary side, I_{pri-B} is equal to I_{Lo}/n, and I_{pri-C} is equal to $-I_{Lo}$/n. Current I_{Lo}/n charges C_{b-B} and discharges C_{b-C}.

Mode 2 ($t_1 < t < t_2$)

This mode begins when switch S_3 is turned off. During this mode, V_{AB} is equal to $+V_{dc}$, V_{BC} is equal to 0, and V_{CA} is equal to $-V_{dc}$. Writing the KVL equation for each transformer primary, V_{Pri-A} is equal to $((V_{dc} - V_{Cb-A})$, V_{Pri-} is equal to $(-V_{Cb-B})$, and V_{Pri-C} is equal to $-(V_{dc} + V_{Cb-C})$. This means that the primary winding of T_A is connected to the highest positive voltage and the primary winding of T_B is connected to the highest negative voltage. Based on the polarities at the secondary side the upper diodes associated

with T_A (D_1) and the lower diodes associated with T_B (D_6) are conducting. At the primary side, I_{pri-A} is equal to I_{Lo}/n, and I_{pri-B} is equal to $-I_{Lo}$/n. Current I_{Lo}/n charges C_{b-A} and discharges C_{b-B}.

Mode 3 ($t_2 < t < t_3$)

This mode begins when switch S_1 is turned off. During this mode, $V_{AB} = V_{BC} = V_{CA} = 0$. Writing the KVL equation for each transformer primary, V_{Pri-A} is equal to $(-V_{Cb-A})$, V_{Pri-B} is equal to $(-V_{Cb-B})$, and V_{Pri-C} is equal to $(-V_{Cb-C})$. This means that the primary winding of T_C is connected to the highest positive voltage and the primary winding of T_B is connected to the highest negative voltage. Based on the polarities at the secondary side the upper diodes associated with T_C (D_5) and the lower diodes associated with T_B (D_6) are conducting. At the primary side, I_{pri-C} is equal to I_{Lo}/n, and I_{pri-B} is equal to $-I_{Lo}$/n. Current I_{Lo}/n charges C_{b-C} and discharges C_{b-B}.

Mode 4 ($t_3 < t < t_4$)

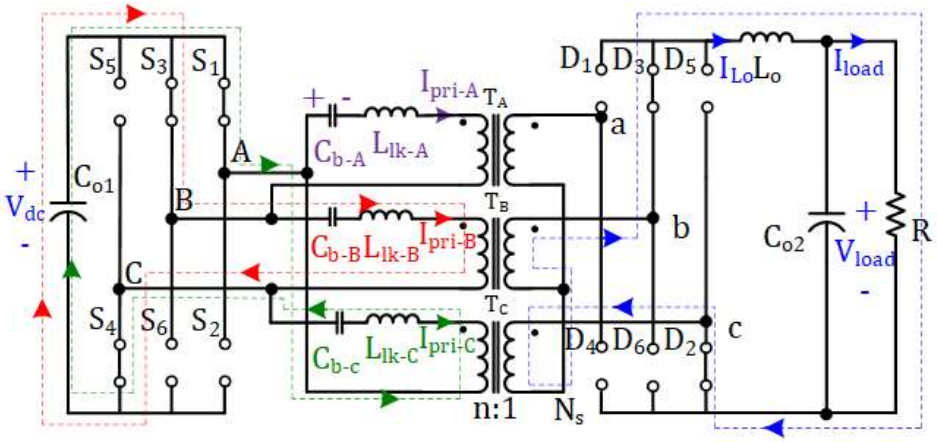
This mode begins when switch S_1 is turned off. It is the same as Mode 2.

Mode 5 ($t_4 < t < t_5$)

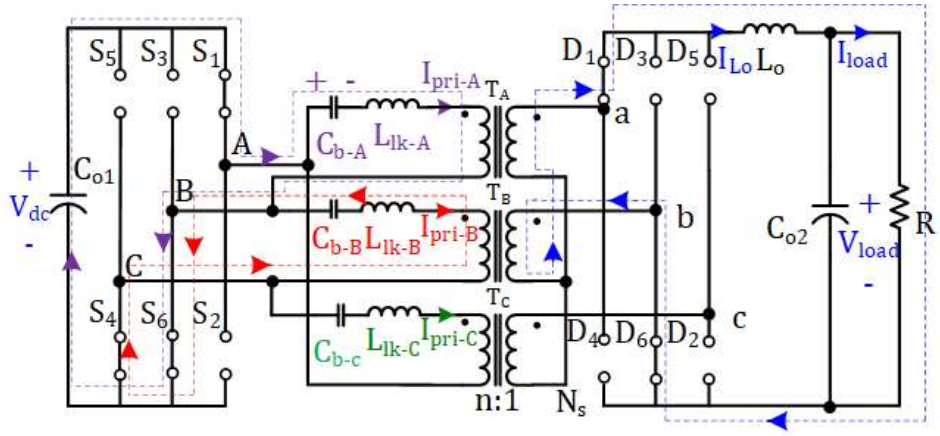
This mode begins when switch S_3 is turned off. It is the same as Mode 1.

Mode 6 ($t_5 < t < t_6$)

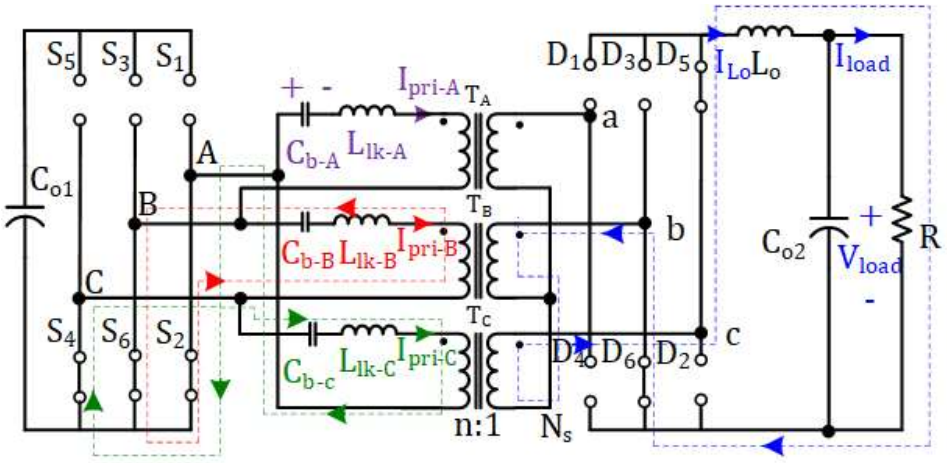
This mode begins when switch S_5 is turned off. It is the same as Mode 3.



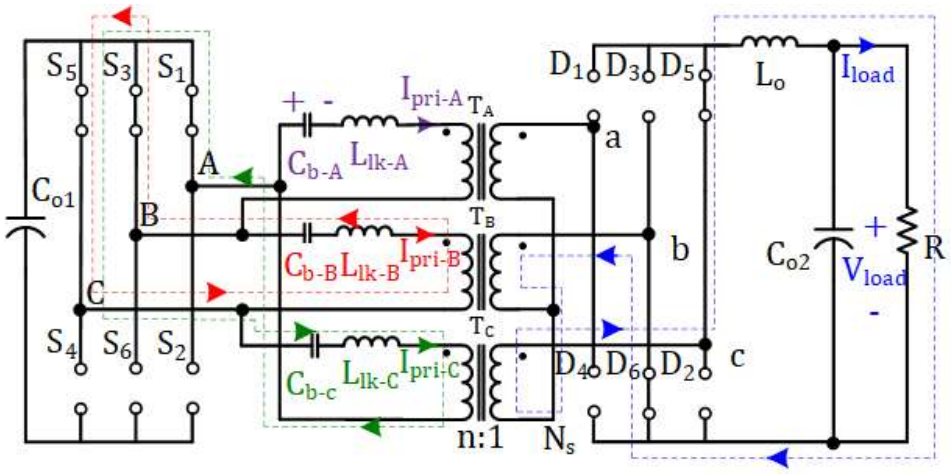
(a) Modes 1 & 5



(b) Modes 2 & 4



(c) Modes 3



(d) Modes 6

Figure 5.6. Modes of operation of UDDSC

5.3 MP-IC features

The proposed IC has the following features:

- The MP-IC can control the flow of power between the AC sub-grid and the main DC bus while providing an isolated semi-regulated voltage for a separate DC sub-grid with an intermediate bus architecture (IBA), at the same time. Although the isolated voltage is semi-regulated, this loose regulation is acceptable in the DC distribution system with an IBA [62].

- Any control method that can be used for a conventional three-phase, six-switch, bidirectional AC-DC converter can be used to operate the proposed MP-IC.

- The MP-IC uses only six active switches and can provide galvanic isolation to the low-voltage DC bus.

- The voltage-insensitive loads can be directly supplied from the AC or DC sub-grids by opening S-DC or S-AC, respectively, thus making the operation of these more reliable.

- Since the current of the DC-DC stage passes through the converter switches, the RMS current of the converter will be the sum of the currents of both stages, thus

switches with higher current ratings should be used in the converter. The cost of using switches with higher ratings is, however, offset by the elimination of a full converter.

5.4 MP-IC control and design

In this section, the control system for the BADSC of the MP-IC is explained and a design procedure for the MP-IC is developed.

5.4.1 BADSC control

In this subsection, the control system of BADSC is developed. Since power transfer in the BADSC happens through the low-frequency component of voltage and current, the control system of the MP-IC is developed based on a low frequency (i.e. 60 Hz) model of BADSC.

The control system of the proposed MP-IC is shown in Figure 5.7. As stated in section 5.2.2.1, power is transferred between AC sub-grid and the main DC bus at line frequency. Moreover, based on the modes of operation, the UDDSC current does not appear in the AC side of the MP-IC. As a result, the BADSC model (Figure 5.4(a)) can be used to model the power transfer between the AC sub-grid and main DC bus.

A mathematical model in the synchronous (dq) frame for the MP-IC can be developed with the same method that is proposed in [102]. The AC equation in the dq-frame can be expressed as

$$L_f \frac{di_d}{dt} + R_f I_d = L\omega_l I_q + \frac{V_{dc}}{2} m_d - e_d \qquad (5-1)$$

$$L_f \frac{di_q}{dt} + R_f I_q = -L\omega_l I_d + \frac{V_{dc}}{2} m_q - e_q \qquad (5-2)$$

where e_d and e_q are the AC sub-grid voltage components in the dq-frame. Since the voltage drop across the R_f is negligible, this term is eliminated from the equations in the next steps.

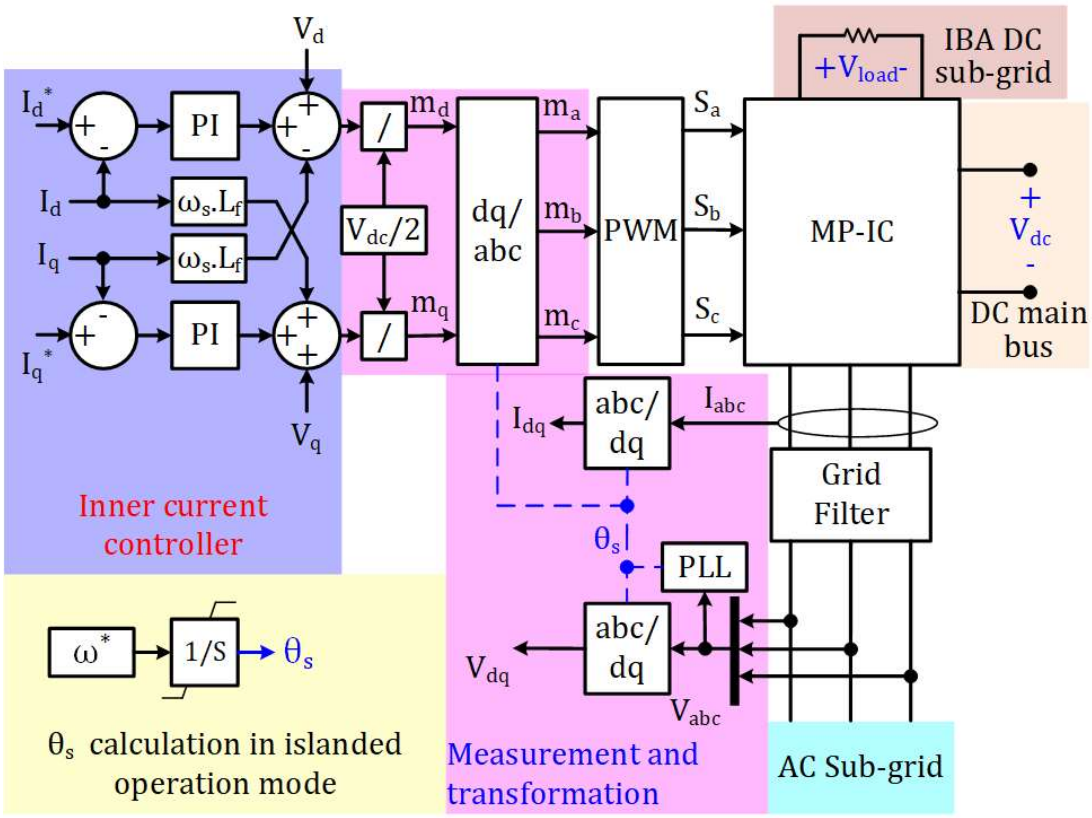


Figure 5.7. Proposed MP-IC control system

Equations (5-1) and (5-2) can be used to calculate the value of the modulation index in the steady state condition in the dq-frame (m_d and m_q), which can be expressed as

$$m_d = \frac{2}{V_{dc}}(u_d - L_f \omega_l I_q + e_d) \qquad (5-3)$$

$$m_q = \frac{2}{V_{dc}}(u_q + L_f \omega_l I_d + e_q) \qquad (5-4)$$

where u_d and u_q are the control inputs that are obtained from two PI controllers. The modulation index in ABC frame can be obtained by adding vectors m_d and m_q as follows:

$$M = \sqrt{m_q^2 + m_d^2} \qquad (5-5)$$

It can be seen from (5-1) to (5-4) that the BADSC operates in the same way as a conventional VSC because both have the same set of state equations. Consequently, the PI controllers can be designed in a conventional manner, as described in [27]-[28].

5.4.2 UDDSC modelling and design

The UDDSC acts as a voltage source for the IBA DC sub-grid. The design process of the UDDSC is to find proper values for the MP-IC components to maintain the IBA DC sub-grid voltage at a limited range, for all operation conditions of the BADSC stage.

Most of the parameters of the proposed IC are the same as those of the conventional three-phase, six-switch, non-isolated bidirectional AC-DC converter. The most critical parameter in the MP-IC is the transformer turns ratio (n), which differs from that of the conventional bidirectional AC-DC converter, as explained in this section of the thesis.

5.4.2.1 Transformer turns ratio (n):

In the proposed converter, power is transferred to the IBA DC sub-grid via high frequency switching components of the voltage at converter terminals and the low-frequency component of the voltage (i.e. 50 Hz or 60 Hz) is blocked with blocking capacitors. In this converter, the double Fourier series method [108] is used to decompose the inverter terminal voltages (V_{AB}, V_{BC}, V_{CA}) to their harmonic contents. After removing the low frequency components (line frequency and DC components), the RMS value of the transformers secondary voltages can then be calculated. The total RMS value of the voltage is equal to DC output voltage, since the output voltage is a DC value.

The inverter terminal voltages waveforms are shown in Figure 5.5(b). The harmonic contents of these waveforms can be expressed as

$$V_{AB} = V_{dc}\left(\frac{1}{2} + \frac{\sqrt{3}M}{2}cos\left(\omega_l t - \frac{\pi}{6}\right)\right) + \sum_{x=1}^{\infty}\sum_{y\in U_1}\frac{2\sqrt{3}}{\pi x}J_x\left(\frac{Mx\pi}{2}\right)sin\left(\frac{(x+y)\pi}{2}\right) \cos\left[x(\omega_c t + \theta_c) + y\left(\omega_l t - \frac{\pi}{6}\right)\right] + \sum_{x=1}^{\infty}\sum_{y\in U_2}\frac{2\sqrt{3}}{\pi x}J_x\left(\frac{Mx\pi}{2}\right)sin\left(\frac{(x+y)\pi}{2}\right) \cos\left[x(\omega_c t + \theta_c) + y\left(\omega_l t + \frac{\pi}{6}\right)\right] \quad (5-6)$$

where ω_l is the angular frequency of the phase voltage, ω_c is the angular frequency of the carrier signal, and J_x is the Bessel function of the first kind, $U_1 = \pm(3k-2)|\ k \epsilon N$, and $U_2 = \pm(3k-1)|\ k \epsilon N$; M is the modulation signal magnitude as shown in Figure 5.5(a). The harmonic contents of V_{BC} and V_{CA} waveforms are the same and only a $-\frac{2\pi}{3}$ and $\frac{2\pi}{3}$ radian phase shift should be added to (5), respectively.

The RMS value of the secondary side phase voltage of the T_A can be derived from (5) and is

$$V_{aNs} = \frac{V_{dc}}{n}\sqrt{\sum_{x=1}^{\infty}\sum_{y\in U_1\cup U_2}\frac{\sqrt{6}}{\pi x}J_x\left(\frac{Mx\pi}{2}\right)sin\left(\frac{(x+y)\pi}{2}\right)} = \frac{V_{dc}}{n}\lambda(M) \quad (5-7)$$

A limited number of harmonics can be used to calculate the value of $\lambda(M)$, since the magnitude of the harmonic contents inversely decrease with increasing number of harmonics. The value of $\lambda(M)$ versus M, shown in Figure 5.8, is calculated by using a finite number of harmonics (first to 20th).

With the RMS value of the transformer secondary voltage known, the output voltage can be calculated in the same way as it is calculated for a standard three-phase rectifier. The output DC voltage of the UDDSC can be expressed as [26]

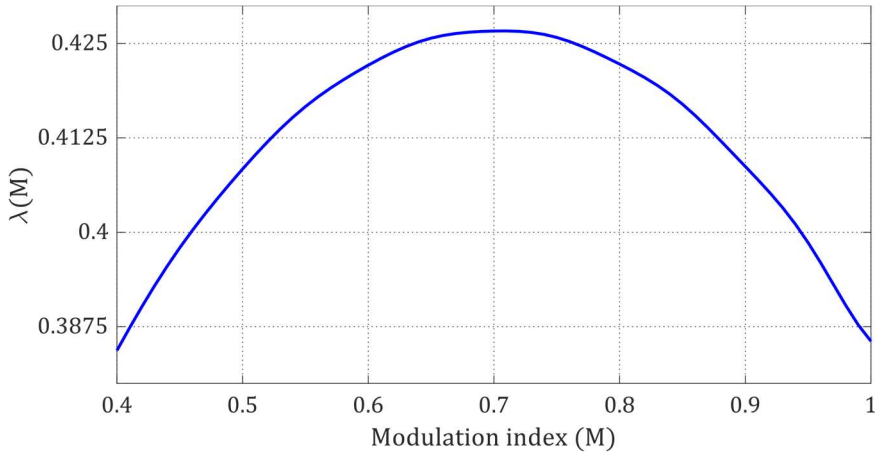


Figure 5.8. $\lambda(M)$ variations vs. modulation index (M)

$$V_{load} = \frac{3\sqrt{6}}{\pi} V_{aNs} - 2V_f = \frac{3\sqrt{6}V_{dc}}{n\pi}\lambda(M) - 2V_f \qquad (5-8)$$

where V_f is the forward voltage drop across the rectifier diodes. Rearranging (5-7), the value of n can be calculated as

$$n = \frac{3\sqrt{6}V_{dc}\lambda(M)}{\pi\left(V_{load} + 2V_f\right)} \qquad (5-9)$$

5.4.2.2 IBA DC sub-grid voltage variations:

In this part, IBA DC sub-grid voltage variations with respect to the value of the modulation index is considered. To do so, the variations of $\lambda(M)$ in (5-7) should be calculated. Since $\lambda(M)$ is a function of modulation index (M), the range of variations of M can be determined.

M is specified by the control system to control the current flow from/to the AC sub-grid. The value of M is set based on the inverter terminal voltages [102] and can be written as

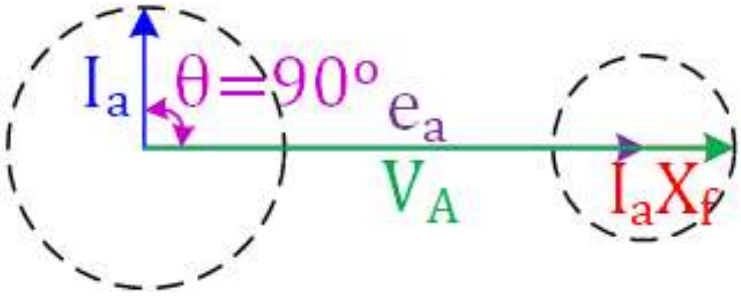
$$M = \frac{V_A}{2V_{dc}} \qquad (5-10)$$

where V_A is the phase to neutral voltage of the low frequency harmonic component of the inverter terminal voltage.

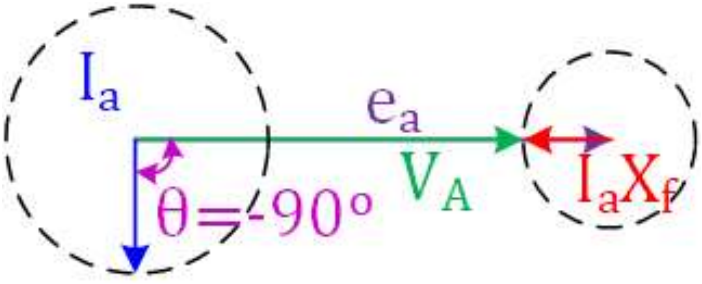
The value of V_A is set according to the phasor diagram of the MP-IC's AC side that is shown in Figure 5.9, where e_a denotes the peak value of the line-to-neutral voltage of the AC subgrid voltage, I_a is the converter phase current, and X_f is the input filter reactance at the line frequency.

As shown in the phasor diagram, the maximum value of V_A occurs when θ is equal to +90°, which means MP-IC is operated as a 1 p.u. pure capacitive load for the AC-sub-grid (Figure 5.9(a)). The minimum value of V_A occurs when θ is equal to -90°, which means that the MP-IC is operated as a pure inductive load for the AC-sub-grid (Figure 5.9(b)).

The converter terminal voltage (V_A) can be varied by I_aX_f to control the amplitude and phase of the current that flows from the MP-IC to the AC sub-grid. The term I_aX_f is typically limited to 0.05 p.u. [109] so that modulation index variations are limited to ±5% of M value when both the current components in the d and q axis are zero. The value of



(a) MP-IC is operated as a pure 1 p.u capacitive load for the AC sub-grid



(b) MP-IC is operated as a pure 1 p.u inductive load for the AC sub-grid

Figure 5.9. Phasor diagram of the AC side of the MP-IC

M at this point is defined as (M_0). Based on the value of M_0, the range of variations of $\lambda(M)$ can be found from Figure 5.8. According to Figure 5.8, the variation range of $\lambda(M)$ and consequently, the output voltage can be limited to $\pm 5\%$ in the worst case.

5.5 Simulation and experimental results

In this section, experimental results obtained from a scaled down prototype converter that show the feasibility of the proposed MP-IC are presented, as are simulation results that demonstrate the operation of proposed MP-IC as a part of an HMG.

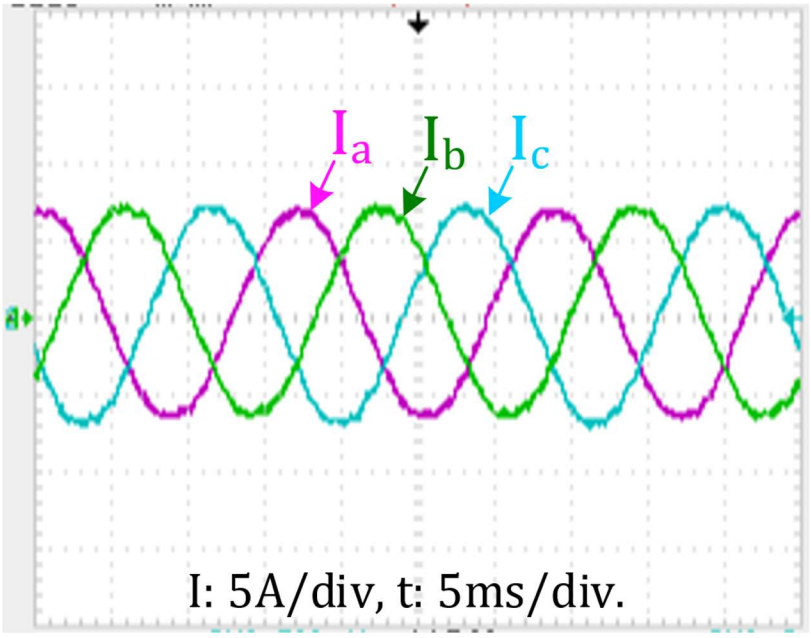
5.5.1 Experimental results

A simple proof-of-concept scaled-down prototype of the proposed converter was built to verify its feasibility. The prototype was built based on the following specifications: Line-to-line RMS voltage, $V_{LL} = 120V$, main DC bus output voltage $V_{dc} = 280V$, IBA DC sub-grid voltage $V_{load} = 48V$, maximum apparent power between the AC terminal and the main DC bus $S_{main} = 1kVA$, maximum IBA DC sub-grid load $P_{m-loa} = 250\,W$, and switching frequency $f_{sw} = 50\,kHz$. The devices used for the switches S_1-S_6 were IPx60R190P6 MOSFETs, and devices were used for the output rectifying diodes D_1-D_6 were DPG10I400PM. The input inductors L_f were $1.2\,mH$, the input filter capacitors C_f were $470\,nf$, the value of the blocking capacitors was $680\,nF$, and the transformer turns ratio was 5:1 for the scaled-down system. The values of L_o and C_{o2} were $2\,mH$ and $1\,mF$ respectively. The converter was implemented with the same control structure that is shown in Figure 5.7 and with double edge carrier conventional SPWM, using the slave DSP of a dSPACE 1103 (TM320F240).

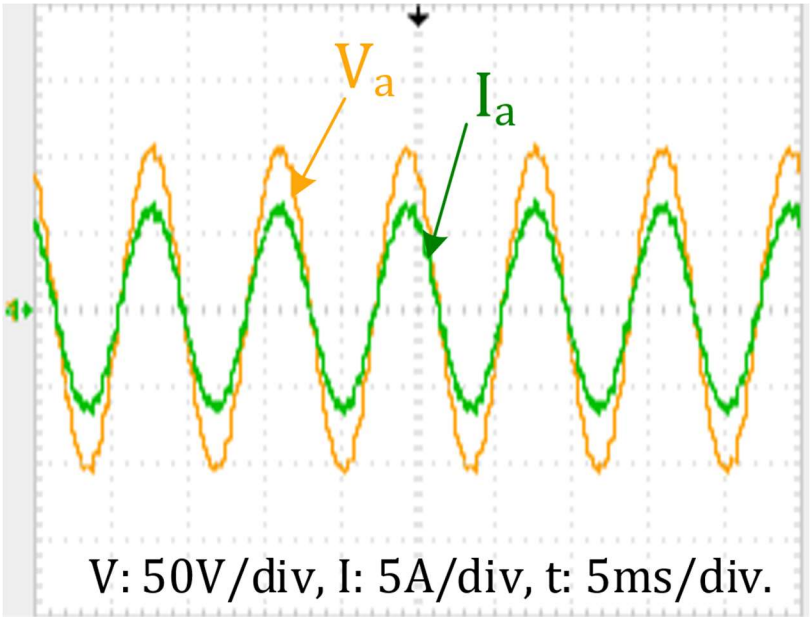
It was shown in Sections 5.4.1 that the state equations of the converter (and thus the dynamic performance) are the same as those of a typical three-phase, six-switch, non-isolated bidirectional AC-DC converter; thus, only steady-state results are presented here.

Figure 5.10 shows typical converter waveforms when the rated power is transferred from the main DC bus to the AC sub-grid and isolated DC bus. Figure 5.10(a) shows the three-phase AC currents. The inner current control loop in Figure 5.7 keeps the AC side currents sinusoidal. Figure 5.10(b) shows a typical phase (phase A) current and voltage. In this

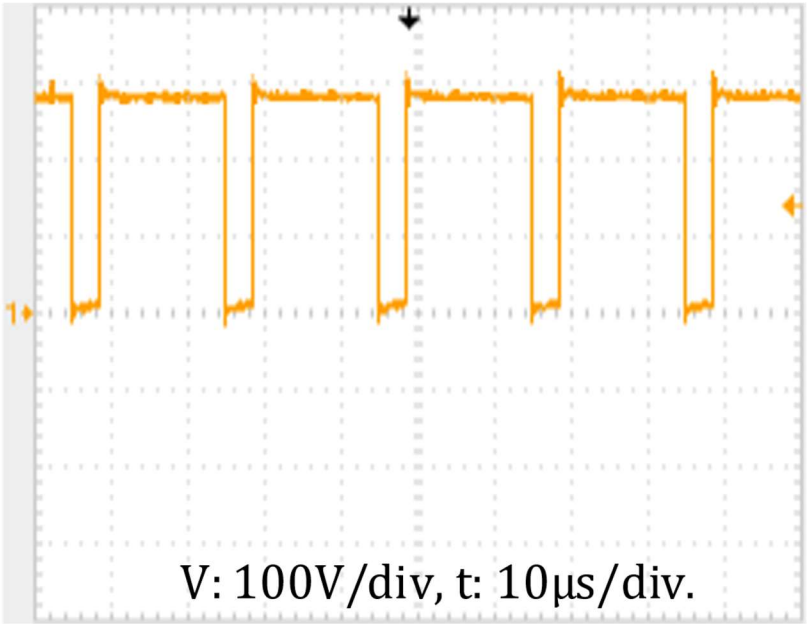
mode of operation, the power factor is set to one; thus, the phase voltage and current are in phase. Figure 5.10(c) shows the voltage across a typical switch voltage waveform, which is like any switch voltage waveform found in a bidirectional AC-DC converter. Figure 5.10(d) shows the output current on a line frequency scale. It can be seen that it is a smooth DC waveform.



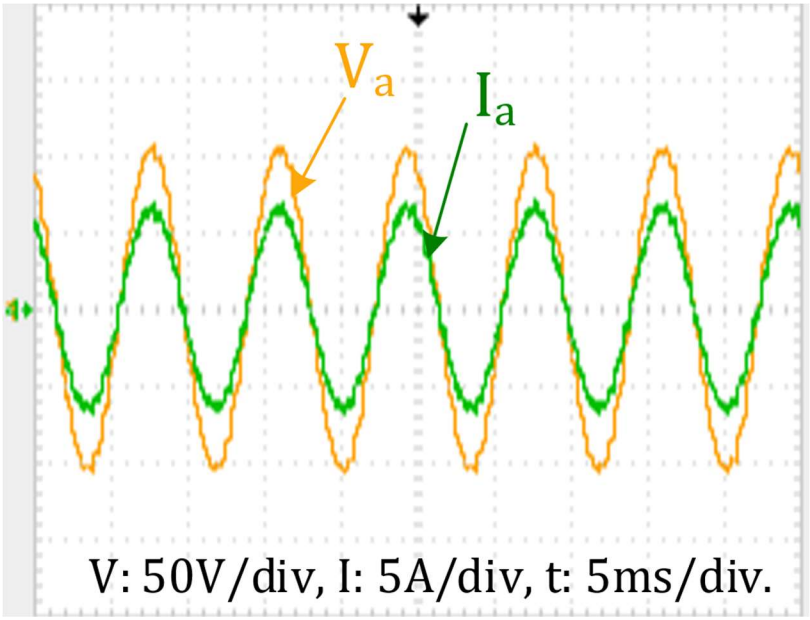
(a) The AC side currents ($I_a, I_b, and\ I_c$)



(b) A typical phase voltage and current (phase A)



(c) A switch voltage waveform



(d) the output current.

Figure 5.10. Scaled-down prototype waveforms

5.5.2 Simulation results

The simulation was performed by modeling the HMG in Figure 5.2 in PSIM software[110]. The components of the HMG are modeled as follows: The AC sub-grid power rating is 10 kW and 5kVar that can be supplied by either the power grid or the AC-DG (wind turbine) unit. The AC load is modelled as a 10 kW resistive load. The DC sub-grid rating is 10kW. The composite DC bus (LV-BUS 1) consists of a 10kW DC-DG (PV panels), a 10 kWh energy storage unit, and a 7 kW load. LV-BUS 2 is modeled as a 1kW load that models a simple DC load without an IBA, and the DC sub-grid with the intermediate bus architecture is modeled as a 2 kW load. Since the HMG operation strategy is outside the scope of this thesis, it is assumed that a high level supervisory system provides the command signal for the MP-IC depending on the operating conditions of the HMG.

The AC voltage is the standard North America utility voltage of 208V and the DC bus voltage is 380V, which is common in DC distribution system. The value of M_0 is thus 0.89 and has a $\pm 5\%$ variation, which is common in conventional six-switch AC-DC converters. The DC voltage of the distribution system with IBA is selected to be 48V, which is common in applications with IBA DC distribution systems such as data centers. The parameters of the proposed MP-IC that were used in the HMG simulation study are listed in Table 5.1.

The main objectives of the simulation study were to show MP-IC performance for two cases:

To study the effects of the variations of HMG operation condition on the IBA DC sub-grid voltage (Case #1).

To demonstrate that the operation of the HMG control system is independent of load variations in the IBA DC sub-grid – to show that the DC-DC sub-converter does not affect

Table 5.1: Parameters of the simulated system

Symbol	Item	Value
S_{m-main}	Rated power (AC to main DC bus)	10 kVA
P_{m-load}	Rated power (AC to isolated DC sub-grid)	2 kW
$f_{sw} = f_c$	Switching frequency (carrier frequency)	25 kHz
L_f	Input filter inductance	500 µH
C_f	Input filter capacitance	5 µF
C_{o1}	Main DC bus capacitance	300 µF
n	Transformer turns ratio	7.5
C_{o2}	isolated DC sub-grid filter capacitor	1 mf
L_o	Load DC bus filter inductor	1 mH

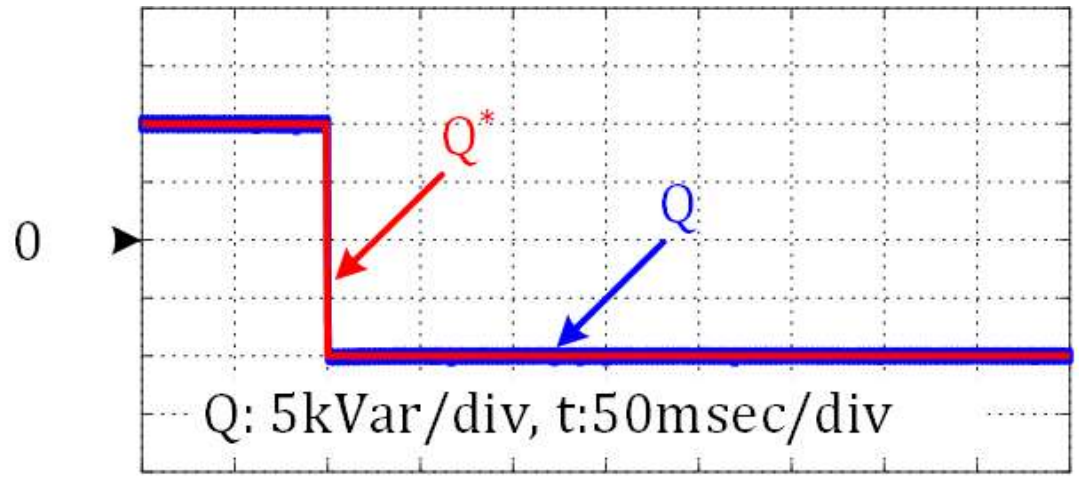
the operation of the AC-DC sub-converter, regardless of whether it is supplying or absorbing power from the main DC bus (Case #2).

In Case # 1, the value of M is varied from its minimum value to its maximum value and the IBA DC sub-grid voltage variations are observed. To do so, the MP-IC is operated as a 1 p.u. inductive load, based on the AC side phasor diagram (Figure 5.9), and is then switched to a 1 p.u. capacitive load. It should be noted that the magnitudes of I_d^* and I_q^* are calculated by using the following equations:

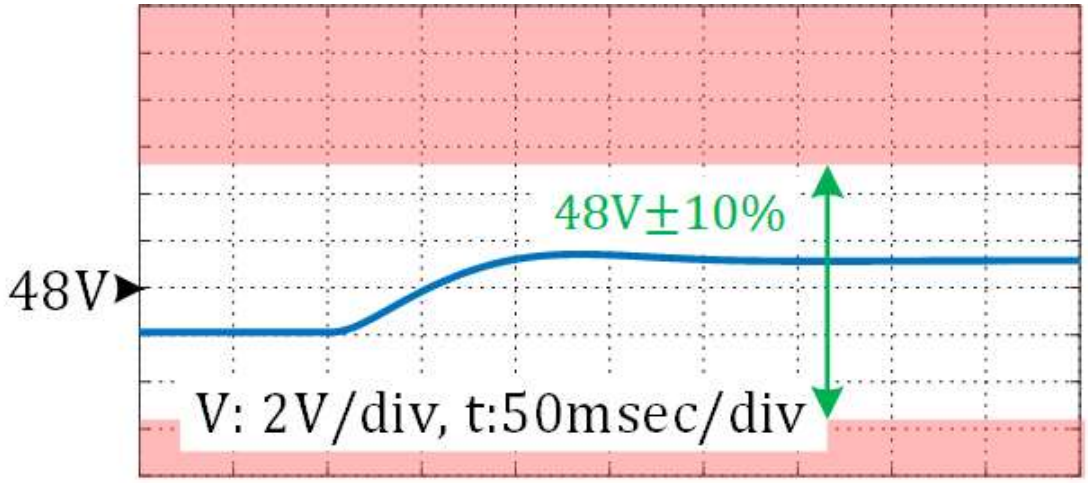
$$I_d^* = \frac{2(Q^*.V_q)}{3(V_d^2 + V_q^2)} \qquad (5-11)$$

$$I_q^* = \frac{-2(Q^*.V_d)}{3(V_d^2 + V_q^2)} \qquad (5-12)$$

As shown in Figure 5.11 the converter reactive power flow changes from 1 p.u. inductive to 1 p.u. capacitive because of the change in the value of IBA DC sub-grid voltage (V_{load}),



(a) Reactive power command and measured value



(b) IBA DC sub-grid voltage variations

Figure 5.11. IBA DC sub-grid voltage variations due to HMG operating point change

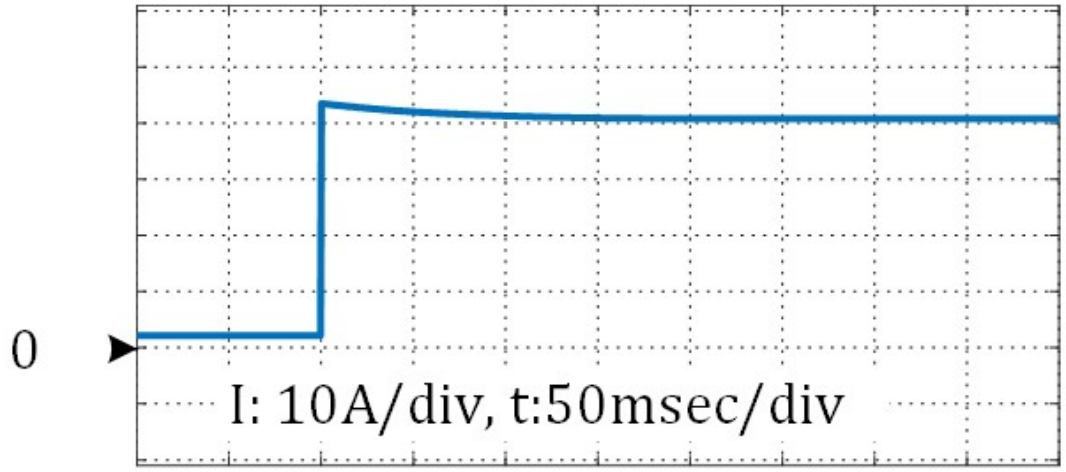
which is increased by almost 3%; this is less than the 5% limit mentioned in Section 5.4.2. It can be seen that the load voltage variations comply with voltage limitations placed on the semi-regulated converter that feeds the IBA DC distribution system (48V±10%), which means that DC-DC sub-converter can be the front-end converter of an IBA DC system such as a small data center.

In Case #2, the IBA DC sub-grid load is changed from 20% to 100% while the MP-IC transfers 0.5 p.u. active power from the AC sub-grid to the DC main bus and provides 0.5

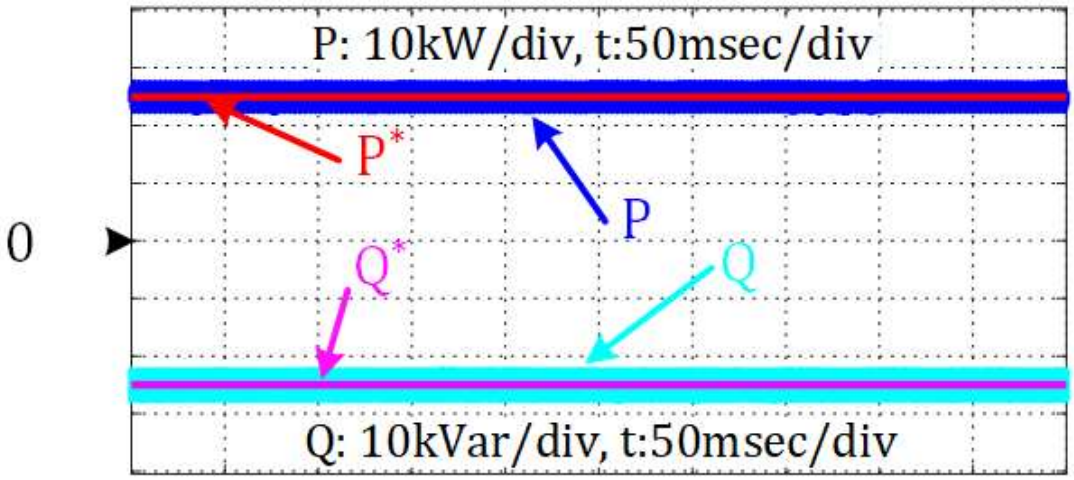
p.u. capacitive reactive power for AC sub-grid. The simulation results are shown in Figure 5.12 It can be seen that IBA DC sub-grid load variations affect neither the d-axis nor q-axis control loops performance, which means the load variations in an IBA DC system does not disturb the operation of the MP-IC from the point of view of the dynamics of the overall HMG.

5.6 Conclusion

This chapter proposed a method to simplify the architecture of hybrid AC-DC microgrids (HMGs) by using a novel multi-port interlinking converter (MP-IC). The simplified HMGs have fewer power electronic converters, are more flexible to design. The novel



(a) IBA DC sub-grid current



(b) Active and reactive power exchange with the AC sub-grid

Figure 5.12. The effect of IBA DC sub-grid load change on HMG operation

MP-IC works as an integrated bidirectional AC-DC converter and as a unidirectional DC-DC converter. The MP-IC is as used as an isolated DC power supply for a cluster of low-voltage loads in HMGs while interfacing their AC and DC sub-grids. The MP-IC has the same number of switches and the same dynamic behaviour as conventional non-isolated, single output bidirectional AC-DC converters behaviour as conventional non-isolated, single output bidirectional AC-DC converters.

In this chapter, the basic principles related to the simplification of a typical HMG by using the new MP-IC were explained. A mathematical model for the control system design and a design procedure for key components of the MP-IC was demonstrated. The models were validated through a simulation study of the MP-IC under different modes of operation. The feasibility of the proposed IC was verified by the experimental results from a simple proof-of-concept prototype.

It was confirmed through the simulation and experimental results that the performance of simplified HMG operation is the same as that of the conventional HMG since the proposed MP-IC works the same as conventional ICs. The only drawback of using the proposed converter is to have slightly more current in the converter switch because two converters use the same switch; however, the extra cost of this higher rated switch is offset by the elimination of a full isolated DC-DC converter from the HMG structure.

Chapter 6

6 Summary and Conclusion

6.1 Summary

AC-DC and DC-DC power electronic converters are extensively used for electrical power conversion in different applications such as renewable energy systems, utility applications, telecom equipment, and electric vehicles. The main objective of this thesis has been to investigate power converters with a split DC bus to reduce the stress on converter components or reduce the number of active switches in these converters. DC-DC converters, AC-DC converters, and converters for hybrid microgrids (HMGs) were examined in this thesis. The content of this thesis can be summarized as follows:

In Chapter 1, fundamental concepts related to the work performed for this thesis were reviewed and a literature review of relevant DC-DC converters, AC-DC converters, and converters for HMGs was done. The thesis objectives and outline were also stated as well.

In Chapter 2, a comparison between a three-level zero-voltage-zero-current-switching (ZVZCS) pulse-width modulated (PWM) DC-DC converter and a conventional zero-voltage-switching (ZVS) PWM full-bridge DC-DC converter was made. Both converters were implemented with four MOSFETs. The three-level ZVZCS-PWM converter that was used is an example of a split DC bus converter as it has two capacitors connected in series that are placed across the DC bus and the midpoint of these capacitors, which has a voltage that is half the DC bus voltage, is used as part of the converter circuit. This is a converter topology that has found use in high power, high voltage applications and is generally implemented with IGBT devices; it has never been used in lower power applications with MOSFET devices (< 1 kW). The ZVS-PWM full bridge converter is considered to be the standard DC-DC converter topology for DC-DC conversion applications that are > 500 W. In this chapter, the operation of both converters was reviewed, the design of the converters was explained, and experimental results obtained from proof-of-concept prototypes that were built with the same voltage and power specifications were presented. The experimental results were then used to compare the efficiency of both converters.

In Chapter 3, a comparison between a T-type DC-DC converter and a conventional ZVS-PWM full-bridge DC-DC converter was made. Both converters were implemented with four MOSFETs. The T-type converter that was used is an example of a split DC bus converter as it has two capacitors connected in series that are placed across the DC bus and the midpoint of these capacitors, which has a voltage that is half the DC bus voltage, is used as part of the converter circuit. Unlike the three-level ZVZCS-PWM converter, which can have all four of its switches exposed to a maximum peak voltage that is half the DC bus voltage, two of the T-type converter switches are exposed to the full DC bus voltage and the other two switches are exposed to a peak voltage that is half the DC bus voltage. The converter topology is used in high power, high voltage inverters and is generally implemented with IGBT devices. Although it was proposed in one paper as a DC-DC converter with MOSFET devices[75], its properties and characteristics for lower power applications relative to those of ZVS-PWM full-bridge converters. In this chapter, the operation of both converters was reviewed, the design of the converters was explained, and experimental results obtained from proof-of-concept prototypes that were built with the same voltage and power specifications were presented. The experimental results were then used to compare the efficiency of both converters.

In Chapter 4, a new split DC bus three-phase single-stage AC-DC converter with isolation is proposed. In the proposed converter the split DC bus structure is used to reduce the number of switches in a single-stage AC-DC converter. The proposed converter can perform AC-DC conversion with power factor correction (PFC), output voltage regulation, and galvanic isolation with only 4 active switches; it also does not have a diode bridge in its topology, which reduces conduction losses. Moreover, unlike many single-stage converters, the input current is continuous, which reduces the stress on the converter components and injected harmonic current to the grid. In this chapter, the operation of the proposed split DC bus AC-DC converter was explained, and an analysis of its steady-state characteristics was performed. The feasibility of the proposed converter was confirmed with experimental results obtained from a proof-of-concept prototype converter.

In Chapter 5, a new split DC bus three-port AC-DC-DC converter was proposed to simplify the structure of HMGs. In the proposed converter, the split DC bus structure is used to reduce the number of converters needed in HMGs by sharing switches between two converters: an AC-DC converter that operates as an interlinking converter between the AC and DC subgrids of the HMG and a DC-DC converter that operates as an isolated power supply for a two-level DC distribution system. The main converter control objective is to control the active and reactive power exchange to the AC subgrid. The DC-DC converter output is a semi-regulated voltage that complies with the voltage requirements for a first-level voltage of a two-level DC distribution system. This combination reduces the number of converters in an HMG without affecting HMG operation from the generation and load point of view. The feasibility of the proposed converter was verified by the experimental result that was obtained from a proof-of-concept prototype converter.

6.2 Conclusion

Based on the research that has been performed in this thesis, the following conclusion can be drawn:

- It shown in Chapter 2 that a three-level ZVZCS-PWM converter topology implemented with MOSFETs, which is a topology with a split DC voltage bus, has greater light-load efficiency than a standard ZVS-PWM full-bridge converter or a two-level ZVZCS-PWM full-bridge converter. For heavy-load operation, up to 900 W power, the three-level ZVZCS-PWM converter topology is just as efficient as a standard ZVS-PWM full-bridge converter, but less efficient than a two-level ZVZCS-PWM full-bridge converter.

- It was shown in Chapter 3 that the T-type converter implemented with MOSFETs, another type of split DC bus DC-DC converter, has greater light-load efficiency than a standard ZVS-PWM full-bridge converter, but less heavy-load efficiency.

- It was shown in Chapter 4 that a split DC bus voltage architecture can be used to reduce the number of switches in a three-phase single-stage AC-DC converter with

converter isolation. The proposed converter was shown to have a number of advantageous features and can be implemented with just four active switches.

- It was shown in Chapter 5 that a bidirectional AC-DC converter with a split DC bus architecture can be successfully used to reduce the number of converters in a HMG structure, thus reduced microgrid size and cost. The semi-regulated voltage that is fed to a two-level DC distribution system was shown to be compliant with standard industrial practices.

6.3 Contributions

The main contributions of the thesis are as follow:

- It was shown that a three-level ZVZCS-PWM DC-DC converter implemented with MOSFETs can have better light-load efficiency than a standard ZVS-PWM full-bridge converter or a two-level ZVS-PWM full-bridge converter. Although the three-level ZVZCS-PWM DC-DC converter is an established topology that is used for high-voltage, high-power applications with IGBTs, its operation for lower -voltage, lower-power applications with MOSFETs has never been examined until now. Given that light-load efficiency has become more of a concern in recent years due to the increased use of power electronic converters in society and the greater stress this places on the utility grid, this thesis has shown that a split-level DC bus converter such as a ZVZCS-PWM DC-DC converter is a possible converter option where a converter needs to operate with light-loads often.

- It was shown that a T-type DC-DC converter implemented with MOSFETs can have better light-load efficiency than a standard ZVS-PWM full-bridge converter. Although T-type converters are used for high-power DC-AC power converter and are implemented with IGBTs, the operation of the T-type DC-DC for lower-power applications with MOSFETs has never been examined until now. This thesis has shown that a T-type DC-DC converter is a possible converter option where a converter needs to operate with light-loads often.

- A new reduced switch, three-phase, single-stage AC-DC converter with a split DC bus architecture was proposed in this thesis. The proposed converter uses only four active switches, has continuous input current, can perform input power factor correction, has galvanic isolation between its AC and DC sides, and can be operated with conventional control methods. The proposed converter represents an advance on AC-DC converter technology as it is the only converter of its type that has all the above-mentioned features, especially so few active devices.

- A new multi port AC-DC-DC converter with a split DC bus architecture that can replace two separate converters in a hybrid AC-DC microgrid (HMG) was proposed to simplify HMG structures. This is the first converter of its type tht has been proposed in the literature.

6.4 Suggested Future Work

The following are suggestions for future work:

- Three-level DC-DC converters and T-type DC-DC converters are two types of converters that have a split DC voltage bus that were investigated in this thesis. Future work can be done on a detailed comparison of the efficiency of these converters when implemented with MOSFETs, for lower power applications.

- The converter proposed in Chapter 4 used a single-phase transformer. Future work can be done on examining the operation and characteristics of this converter when implemented with a three-phase transformer. This will allow the proposed converter to operate with higher power levels.

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