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BEHAVIOR OF BUSBAR DIFFERENTIAL RELAYS WITH AIR-GAP CORE CURRENT TRANSFORMERS

(Spine title: BEHAVIOR OF DIFFERENTIAL RELAYS WITH AIR-GAP CORE CT)

(Thesis Format: Monograph)

By

Babak Jamali-Firouzabadi

Graduate program in Engineering Science
Department of Electrical and Computer Engineering

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Engineering Science

Faculty of Graduate Studies
The University of Western Ontario
London, Ontario, Canada

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**THE UNIVERSITY OF WESTERN ONTARIO
FACULTY OF GRADUATE STUDIES**

CERTIFICATE OF EXAMINATION

Supervisor

Dr. T. S. Sidhu

Examiners

Dr. A. Yazdani

Dr. M. R. Kermani

Dr. A. Bassi

a thesis by

Babak Jamali-Firouzabadi

entitled:

**Behavior of Busbar Differential Relays with Air-gap Core
Current Transformers**

is accepted in partial fulfillment of the
requirements for the degree of
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Chair of the Thesis Examination Board

ABSTRACT

Protective relays normally estimate the magnitude and phase angle of current. Since the level of current is normally too high to permit a direct connection to the power system, a Current Transformer (CT) is used to scale down the current value. A CT should faithfully replicate waveform of the primary current. Power utilities normally use air-gap core and solid-core CTs. Air-gap core CTs are expensive and hard to maintain but they are able to reproduce the primary current without becoming saturated unlike solid-core CTs. Nowadays relay manufacturers claim that no matter what type of CT is used in the power grid, protective relays can intelligently sense a saturated waveform produced by a CT, and facilitates a correct decision, based on a unique algorithm. Therefore, continued use of the air-gap core CTs is being questioned.

To verify relay manufacturer's claim, behavior of protective relays when subjected to solid-core and air-gap core CT output waveforms need to be analyzed. Therefore, a mathematical model for both CT types is needed. Output waveform of a solid-core CT is already simulated by IEEE Power System Relaying Committee. In this thesis, a mathematical model of an air-gap core CT is developed and simulated on the Excel platform. Output waveform of the proposed model is then verified using the IEEE PSRC CT Simulator. Then, two commercially available busbar differential relays with CT saturation detection logic were subjected to the output waveforms of solid-core and air-gap core CTs.

After testing about hundred scenarios on each relay, it is concluded that first, there is no difference in the relays' performances for internal faults. Besides, for external faults, an air-gap core CT renders the trip output less sensitive to the relay setting. Further, the relay might be considerably slow in operation for an evolving fault, if a solid-core CT is involved.

Keywords: Instrument current transformer, air-gap core, remanence, saturation, differential protection, dynamic simulation, RTDS.

DEDICATION

I dedicate this work to my brother, Dr. Hassan Jamali.

“Wish You Were Here”

ACKNOWLEDGEMENTS

First, I would like to express my humble appreciation to Dr. Tarlochan S. Sidhu for his valuable guidance, fast feedback, motivation, and support throughout the course of this research. His broad knowledge and his logical way of thinking have been of great value to me.

I can never thank my lovely wife, Negar Mahmoudi, enough. Without her selfless love, understanding, patience, and constant encouragement, it would have been impossible for me to finish this work.

Special thanks are extended to my parents, my brother, and my sister for their endless love and affection showered upon me. They have supported me on how to pursue a higher level of learning ever since I was a child. The happy memory of my brother still provides a persistent inspiration for my journey in this life and I hope to continue, in my own small way, the noble mission to which he sacrificed his life. It is to him that I dedicate this work.

The chain of my gratitude would be definitely incomplete, if I forgot to thank my in-laws for their moral support.

During this work, I have collaborated with many colleagues for whom I have great regard, and I wish to extend my warmest thanks to all those who have helped me with my research work at the University of Western Ontario and Kinectrics Inc.

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LIST OF ABBREVIATIONS

AC	Alternative Current
ANSI	American National Standard Institute
COMTRADE	COMmon format for TRAnsient Data Exchange
CT	Current Transformer
DC	Direct Current
EMTP	Electro Magnetic Transient Program
EMF	Electro Magnetic Force
IED	Intelligent Electrical Device
IEEE	Institute of Electrical and Electronic Engineers
PSRC	Power System Relaying Committee
RMS	Root Mean Square
RTDS	Real Time Digital Simulator
A/D	Analogue to Digital
WIC	Workstation Interface Card
IRC	Inter-Rack Communication Card
MFLOPS	Millions of Floating Points Per Second
ASCII	American Standard Code for Information Interchange
pu	per unit

Chapter 1

1.0 INTRODUCTION

Protective relays require sensing the magnitude and the phase angle of current as well as voltage values for proper operation. Since these values are usually too high to permit a direct connection, instrument transformers are used to scale down the values. Protective relays can be purchased with different current ratings. Typical current ratings for the relays are 1 or 5 A, and they are usually able to tolerate currents higher than the rating current for a limited period of time. Therefore, instrument transformers should be connected to the power system on the primary side and to the protective relays on the secondary side. The primary side of these devices should be capable of handling high voltages and currents with the appropriate insulation. In addition, instrument transformers protect the protective relays, control circuits, and personnel from danger of high voltages and currents.

For various applications, the instrument transformers must be able to provide a representation of the actual current and voltage quantities in steady-state and transient conditions in terms of the following:

- Magnitude
- Frequency
- Waveform

Current Transformers (CT) are instrument transformers which are used to rescale the current. The current transformers are designed to be connected in series to the power system on the primary side. An error in the instrument transformer output can result in an operational delay or the unnecessary operation of the protective relays.

The use of a continuous steel solid-core with no intentional gap in the core is a common way of manufacturing a current transformer. High current levels, with full dc offset at the time of a power system fault, can saturate the steel core. This results in a corrupted output waveform from the current transformer and causes the protective relays to mal-operate. To overcome this deficiency and to minimize the problem, current transformers with an intentional gap in their steel core have been manufactured. The electrical characteristics of the air-gap core CTs have not been standardized, nor have the results of studies of the performance capabilities and characteristics been widely published.

1.1 Objective of the Research Work

Air-gap core CTs provide a number of advantages over solid-core CTs, primarily, their ability to not become saturated. This is one of the driving forces behind a user's decision to choose air-gap core CTs extensively in a power grid. However, air-gap core CTs are more expensive and, as such, their continued use is being questioned.

Nowadays, relay manufacturers claim that protective relays can intelligently sense a saturated waveform produced by a current transformer, and facilitates a correct decision, based on a unique algorithm. Moreover, as will be discussed in Section 3.4, the internal components of a typical microprocessor-based relay reduce the effect of CT saturation. These components are the relay's internal CT, analogue filter and analogue-to-digital converter. However, it is important to ensure that the saturation detection logic of a modern relay can intelligently react to a saturated waveform and help the relay to make the correct decision. In order to verify this, operational characteristics of protection relays must be reviewed when the relays are connected to a solid-core and an air-gap core CTs. Two commercial busbar differential relays were chosen for the verification.

To achieve this, the following steps are carried out in this research work:

- Establishing a computer model for air-gap core CT

- Simulating the air-gap core CT on the computer and extracting the CT output from the computer model in digital format
- Converting the extracted waveform to the COMTRADE format
- Converting the COMTRADE waveforms from digital to analogue
- Amplifying the analogue waveform and injecting it into the relays

Solid-core CTs have already been modeled by the IEEE to provide the output waveform [1]. The proposed model for the air-gap core CT is presented in Section 4.0. The waveforms are then extracted from the modeling software, and injected into the relays by using Real Time Digital Simulator (RTDS) and current amplifiers.

Objectives of this research work are enumerated as follows:

- to provide an effective and easy-to-execute model that can represent the output waveforms of an air-gap core current transformer.
- to validate the performance of the proposed model of an air-gap core current transformer.
- to study the operational differences of two commercial busbar differential relays, where the relays are connected to the solid-core and the air-gap core CT.

1.2 Outline of the Thesis

This thesis is organized into six chapters and two appendixes. In Chapter 1, the objectives of the research work are discussed. Chapter 2 is an introduction to current transformer with a discussion about CT saturation and the differences between solid-core and air-gap core CTs. Chapter 3 presents the differential protection concept.

In Chapter 4, a model for air-gap core CT is presented and validated. Also, air-gap core and solid-core current transformer waveforms are compared with each other. Chapter 5 presents a method for testing two commercial busbar differential relays to study the

operational performance of the relays if they are connected to solid-core and air-gap core current transformers. A summary of the research work and conclusions are given in Chapter 6.

The various books, journals, conference proceedings, standards and instruction manuals, referred to in this work, are listed in References chapter. The two appendixes describe the structures of the Real Time Digital Simulator (RTDS) and the COMTRADE format.

1.3 Summary

The research work is introduced. The background for the research work and the objectives of the work are clearly laid out. A brief overview of this thesis organization is also presented.

Chapter 2

2.0 INTRODUCTION TO A CURRENT TRANSFORMER (CT)

In general, there are two recognized types of current transformers, the wound-type and the through-type which are defined as follows:

The wound-type current transformer has two separate windings, primary and secondary, wound on an iron core. This CT is designed so that there are at least one turn on the primary side and several turns on the secondary side. The turn ratio of the windings defines the scale of the CT. For example a wound-type CT with a turn ratio of 50, reduces the 250 A line current to 5 A which is in the acceptable range for protective relays. The wound-type CT can have several turn ratios. They are constructed by connecting several secondary windings in series.

The through-type current transformer is constructed of a secondary winding mounted on a cylindrical iron core. The line current passes through the insulated core hole to provide flux in the core. In through-type current transformers, the turn ratio of the CT is defined by dividing one over the secondary turns.

The standard ratings and application guides deal with the steady-state sine wave behavior of a current transformer. The dilemma is that, despite the use of recommended rules to avoid transient saturation, saturation consistently occurs in certain critical relay applications and results in mal-operation of the protection system. The principle goal of this Chapter is to quantify the steady-state and transient condition errors of solid-core and air-gap core current transformers. This Chapter also discusses the IEEE PSRC solid-core CT saturation calculator.

2.1 Terminology

Three types of current transformers that are commonly used by utilities [2]:

- Solid-Core CT: This is a traditional type of CT with a solid-core. It has the potential for a high degree of core magnetization, if the primary current is removed (typically 60% to 70%). A large magnetizing inductance of, typically, 2-2000 Henry (H) is seen from the secondary side.
- Air-gap Core CT: This type of CT incorporates an air gap(s), in the order of 0.0001 to 0.0003 per unit of mean length of magnetic path, in the core material. The degree of magnetization, left on the core after removing the primary current, is very low in this type of CT. Typically, they have a modest magnetizing inductance of 0.5-5 H.
- Linearized CT: This type of CT has a large air gap incorporated in the core. There is no magnetization degree left after the primary current is removed, and the magnetizing inductance is low.

The focus in this research is solid-core and air-gap CTs.

2.2 CT Equivalent Circuit

A solid-core current transformer equivalent circuit is depicted in Figure 2-1 [3]. An ideal CT is one that operate with an ampere-turn balance of $i_p \times 1 = i_{ss} \times N$. An actual CT does not behave as an ideal transformer. The CT secondary voltage (V_m) is generated by the rate of the flux change in the core. The fundamental magnetizing voltage, which can also be applied to current transformers, is calculated by Equation(2.1):

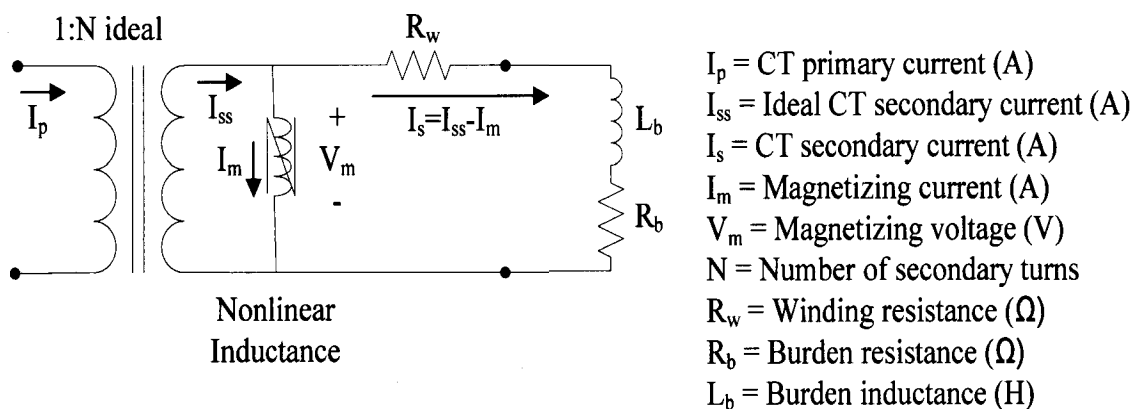


Figure 2-1 - CT Circuit Model

$$V_m = 4.44 B A n f, \quad (2.1)$$

where:

V_m = RMS voltage of the secondary winding (V)

B = flux density (T)

A = core cross section (m^2)

f = frequency (Hz)

n = number of secondary turns

To produce flux in the CT core, a magnetizing current (I_m) is calculated which can be expressed as Equation (2.2)

$$I_m = I_{ss} - I_s, \quad (2.2)$$

where I_{ss} is the primary current referred to the secondary side of the CT

Equation (2.1) along with (2.2), can be used for a steady-state and transient analysis. A more detailed equivalent circuit is shown in Figure 2-2.

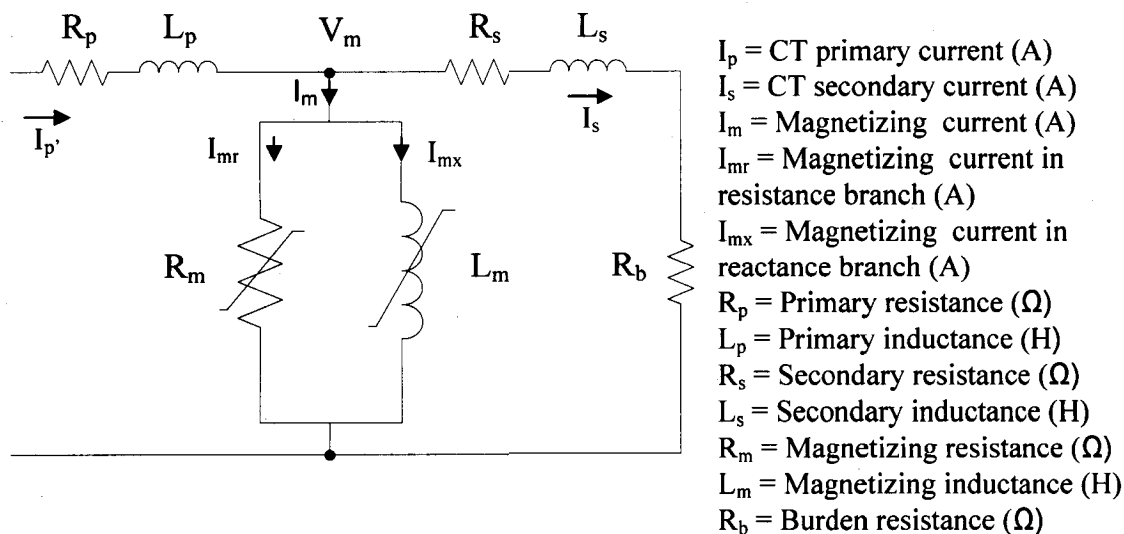


Figure 2-2 – Detailed CT Single Line Diagram

In Figure 2-2, the value of the CT parameters such as R_p , L_p , R_m and L_s are low and can be neglected in the transient modeling. The CT inter-winding capacitance (not shown in Figure 2-2) can also be neglected at the frequencies of interest in protection studies. By neglecting aforementioned parameters, Figure 2-2, can be simplified to Figure 2-3.

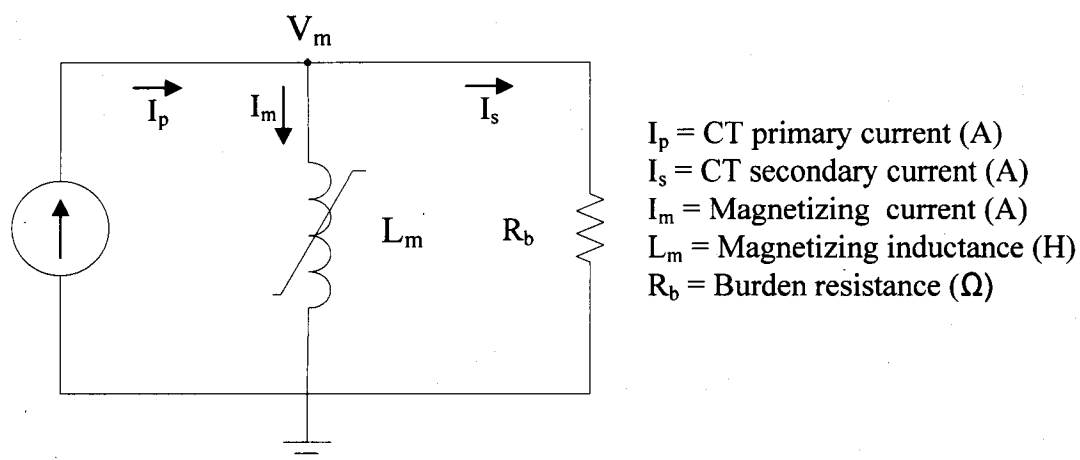


Figure 2-3 - CT Representation for Transient Analysis

In Figure 2-3, the CT time constant is defined as $T_2 = L_m/R_b$. The magnetic field strength (**H**) versus the flux density (**B**) characteristic of the core defines the magnitude of the magnetizing current (**I_m**). Since the magnetizing current (**I_m**), subtracted from the primary current is referred to the secondary side of the CT (**I_{ss}**) to produce the output current (**I_s**), steady-state error in the magnitude and the phase angle of the secondary current, which passes through protective relays is created. This error can result in the mal-operation of the protection system. The B-H characteristic curve of the core must be carefully selected to reduce this error. Figure 2-4 is a vector diagram of the currents and voltages on a 1:1 current transformer and reflects this error.

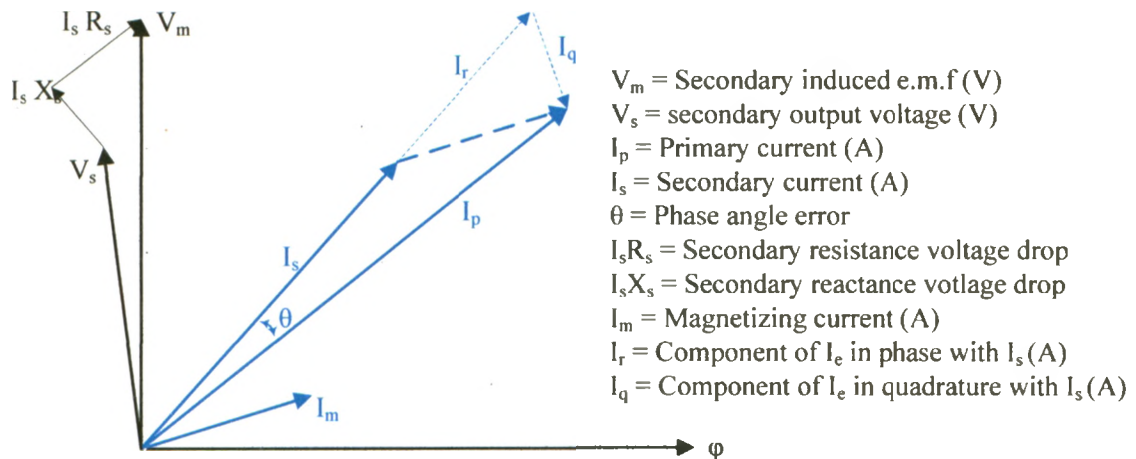


Figure 2-4 - Vector Diagram of a 1:1 Current Transformer

As seen in Figure 2-4, the higher the magnetizing current (**I_m**) or core loss, the larger the error between the primary and secondary currents of the CT (**I_p** and **I_s**).

2.3 B-H Characteristic of a CT

Ampere's law administers the production of a magnetic field by Equation(2.3).

$$I = \oint H \cdot dl, \quad (2.3)$$

where H is the magnetic field strength produced by current I . The unit of the magnetic field strength is expressed as ampere per meter. By applying Ampere's law to a current transformer, the magnetic field strength is equal to primary current, divided by the mean pass length of the magnetic core (l).

The relationship between the magnetic field strength (H) and the flux density (B) is governed by Equation(2.4).

$$B = \mu.H , \quad (2.4)$$

where μ is the magnetic permeability of the core material. The unit for the flux density is expressed as weber per square meter and the permeability has a unit of Henry per meter. The permeability of the free air is the constant number of $4\pi \cdot 10^{-7}$ H/m. The permeability of the ferromagnetic material is not constant as it is for the free air and is ususally represented by a curve.

2.4 Hysteresis Loop

A hysteresis loop shows the relationship between the magnetic field strength (H) and flux density (B) for ferromagnetic materials. An example of a hysteresis loop is denoted in Figure 2-5.

This loop is generated by measuring the flux density of a CT core, while the magnetic field strength is changed. A CT core which has never been magnetized, initially, is represented by the dashed line. At Point a, almost all of the magnetic domains are aligned and an additional increase in the magnetizing force increases the magnetic flux, negligibly. At this point, the material has reached the point of saturation.

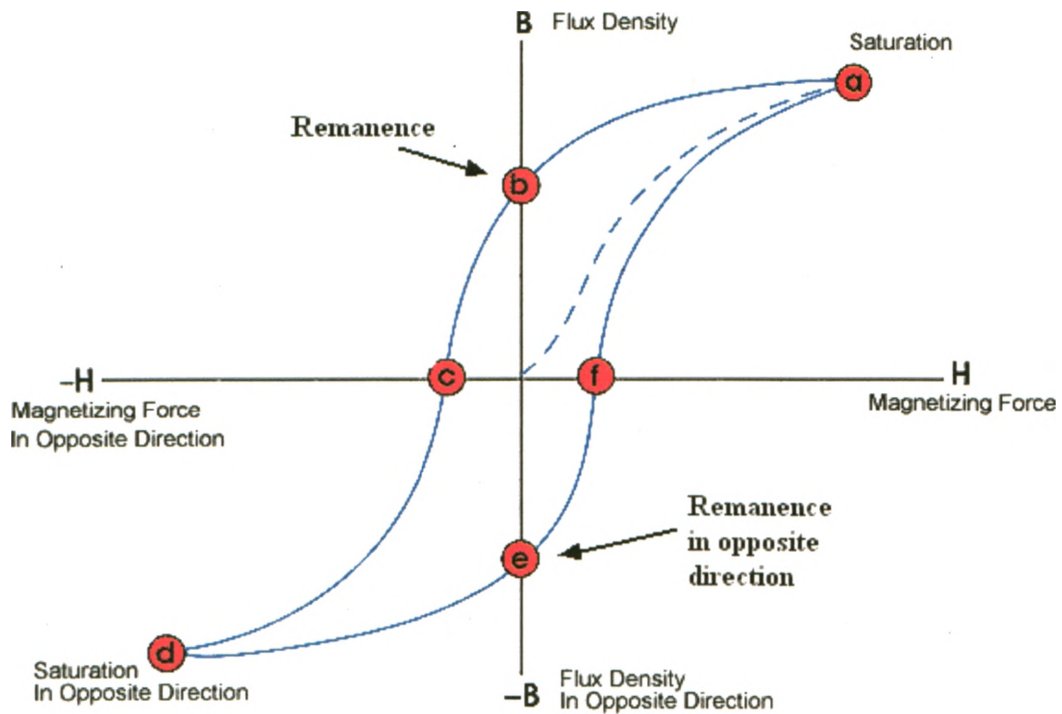


Figure 2-5 - Hysteresis Loop

When H returns to zero, the curve moves from Point a to Point b. At this point, it can be seen that some magnetic flux remains in the material, even though the magnetic field strength is zero. This is referred to as the remanence.

As the magnetic field strength is reversed, the CT core again becomes magnetically saturated in the opposite direction, Point d. Reducing H to zero brings the curve to Point e with the same remanence value as that achieved at Point b. Increasing H in the positive direction returns the flux density (B) to the same saturation Point a.

Air-gap core CTs have the advantage that they do not saturate as quickly as solid-core CTs [4]. This is best illustrated with in Figure 2-6, which shows part of the B-H characteristic of the two CTs. The first curve, A, is for a typical solid-core CT, whereas the second curve, B, is for the air-gap core CT. Point x and Point y refers to the remanent flux of solid-core and air-gap core CTs, respectively.

It is evident the remanent flux in the core can be effectively reduced by inserting gaps in the magnetic circuit of the core. Gaps in the order of 0.0001 to 0.0003 per unit of the mean length of the magnetic path can reduce the remanent flux to a value lower than 10%. A reduction of the remanence in the core provides a proportional increase in the amount of core available for flux excursions, improving the transient performance of the CT.

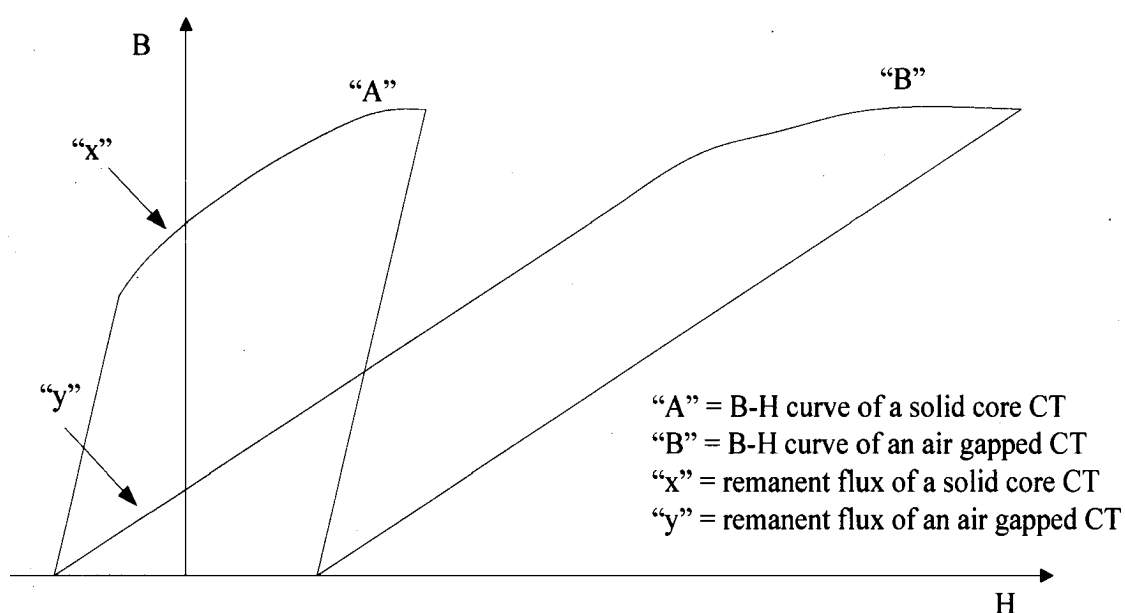


Figure 2-6 – Part of B-H Characteristic of Air-gap Core and Solid-core CTs

2.5 CT Secondary Voltage Rating

The impedance of the magnetizing branch is not linear and its approximate fundamental impedance varies with the voltage applied to the CT secondary. The value of this impedance is in the several hundred to the several thousand ohms range, until the saturation voltage level is reached. The ANSI knee point corresponds to the highest magnetizing impedance of the CT. Above the knee point, a small magnetizing voltage increase (V_m) causes a large magnetizing current (I_m) increase, which corresponds to a low X_m .

The CT secondary voltage rating varies for different standards. Three common definitions of the CT secondary voltage rating follows:

- **KneePoint Voltage:** IEEE C57.13 defines a “knee point” voltage as the CT secondary voltage rating. The knee point voltage is defined as the intersection of the V-I characteristic and a 45° line.
- **C Rating Voltage:** Section 6.4.1.2 of the IEEE C57.13-1978 defines a rating, called “C rating” as the CT secondary voltage. The “C rating” calls for less than a 10% error between the primary and secondary currents, when the secondary current of 100 A passes through a burden resistance of 1, 2, 4, or 8 Ω. This effectively specifies that the CT should be able to reproduce 100 V (100 A multiple by 1 Ω), 200 V, 400 V, or 800 V at the secondary terminals, when 100 A flow into the specified burdens.
- **Saturation Voltage:** The saturation voltage is defined as the intersection of a straight line drawn from the two sections of the CT V-I characteristic. These sections are the linear section and saturated section. Sometimes the saturation voltage is referred to as the IEC knee point voltage.

To take the dc offset into account in order to avoid all hints of saturation, a CT with the following secondary voltage rating is required:

$$V_{Rated} \geq (1 + X/R) I_f Z_b \quad (2.5)$$

where:

V_{Rated} = knee point voltage, saturation voltage, or C rating voltage (V)

I_f = maximum fault current per unit of the CT rating (pu)

Z_b = CT burden per unit of the standard burden (pu)

$X/R = X/R$ ratio of the primary fault circuit

2.6 Time-to-saturate

Time-to-saturate is the time that the CT replicates the primary current without introducing any error to the primary current waveform due to saturation. The time-to-saturate of a current transformer is a vital consideration in a CT application [3]. Some protections, such as breaker failure, require that reliable currents be present for a given period of time. Care must be taken in choosing the proper auxiliary transformers in these cases.

Several factors influence the time-to-saturate of a CT.

- *Degree of Fault Current Offset (dc offset):* The amount of the offset in the primary fault current is determined by the angle of incidence of the fault, as well as the X/R ratio of the system. This offset is, in fact, a decaying dc component which is superimposed on the ac current. The dc offset in the primary current causes a reduction in the amount of time needed for saturation.
- *Fault Current Magnitude:* The magnitude of the fault current is also a contributing factor to the increase of flux in the CT core. This, of course, can also cause the CT core to saturate sooner for higher fault currents.
- *Remanent Flux in the CT Core:* The remanent flux in the core either adds to or subtracts from the flux created by other means, depending on the polarities of the remanent flux and the fault current. If the fluxes have the same polarity, then the time-to-saturate is reduced. This is not so much of a consideration with air-gap core current transformers as it is with solid-core current transformers. A solid-core CT can have up to a 75% remanent flux, residing in the core [2].

- *Secondary Circuit Impedance:* The secondary circuit impedance (also called the burden) also impacts the time-to-saturate. Typically, the higher the burden, the faster the CT saturates. This is a critical consideration with regard to the proliferation of microprocessor-based protection and control equipment with very low burdens compared with traditional electromechanical devices. Also, the power factor of the burden should be considered in the performance of a CT with respect to the speed of saturation.
- *Saturation Voltage:* The quantity and quality of the iron in a CT core is a factor in determining the secondary impedance of a CT. The larger the core cross section, the more, flux is required to saturate the CT, and thus, the time-to-saturation is generally longer.
- *Turn Ratio:* A CT saturates when the flux density exceeds the saturation flux density level, and thus, by increasing the turn ratio of a CT (thereby reducing the flux), the saturation level of a CT can be increased.

A conservative estimate of the time-to-saturate is determined by Equation(2.6) [5]:

$$T_s = -\frac{X}{\omega R} \ln \left[1 - \frac{K_s - 1}{\left(\frac{X}{R}\right)} \right], \quad (2.6)$$

where:

T_s = time-to-saturate (s)

K_s = saturation factor

X = reactance of the primary system to the point of a fault (Ω)

R = resistance of the primary system to the point of a fault (Ω)

and

$$K_s = \frac{V_x}{V_{secondary}} = \frac{V_x}{I_s (R_s + R_B)}, \quad (2.7)$$

where:

V_x = saturation voltage (V)

I_s = secondary current (I_p / N)

R_s = resistance in the secondary circuit (Ω)

R_p = resistance of the burden (Ω)

Figure 2-7 offers an example of the saturation factor curves for the primary circuit time constant $T_1 = 20$ ms and current transformer time constants of $T_2 = 0.1, 0.3, 0.6, 1, 2,$ and 10 s. As shown, if the value of the saturation factor (K_s) exceeds the curve for particular T_2 , the CT does not saturate.

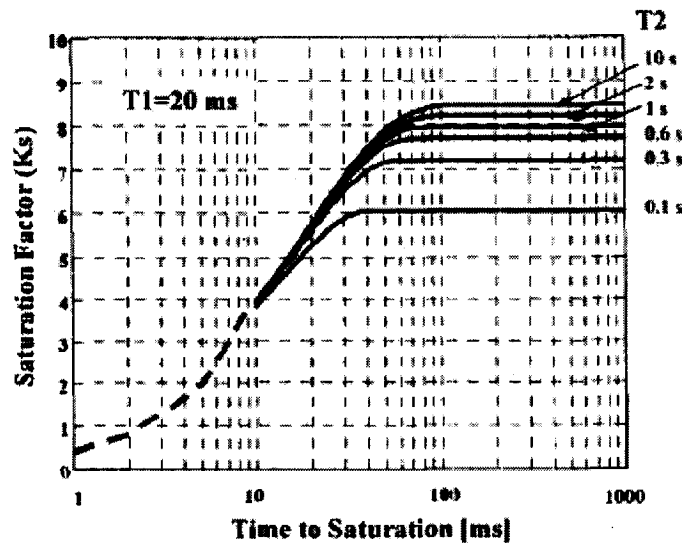


Figure 2-7 - Saturation Factor (K_s) and Time to Saturation for the Primary Circuit Time Constant ($T_1=20$ ms) and the Different Current Transformer Time Constant (T_2)

2.7 IEEE PSRC Solid-core CT Saturation Calculator

IEEE PSRC has generated spread sheet called, the CT Saturation Calculator, to provide a quick indication of not only whether or not a CT saturates in a particular application, but also an accurate indication of the actual waveform of the secondary current so that the degree of saturation as a function of time is apparent [1].

It has been stated that there are many papers on the subject of modeling the behavior of a iron-core current transformer used for protective relay purposes. However, one of the difficulties in using an elaborate model is in obtaining the parameters in a particular study case to implement that model easily, effectively, and accurately.

For case of the CT behavior, it turns out that if the excitation current waveform reaches the saturated region, part of the waveform, below the knee point region has a negligible effect on the overall solution. Therefore, modeling that part is not critical.

The IEEE PSRC method to calculate the secondary current of a solid-core CT is described in the following sections.

2.7.1 B-H characteristic

Figure 2-8 illustrates the B-H characteristic of a solid-core CT as a plot of the rms magnetizing voltage versus the rms magnetizing current on the log-log axes.

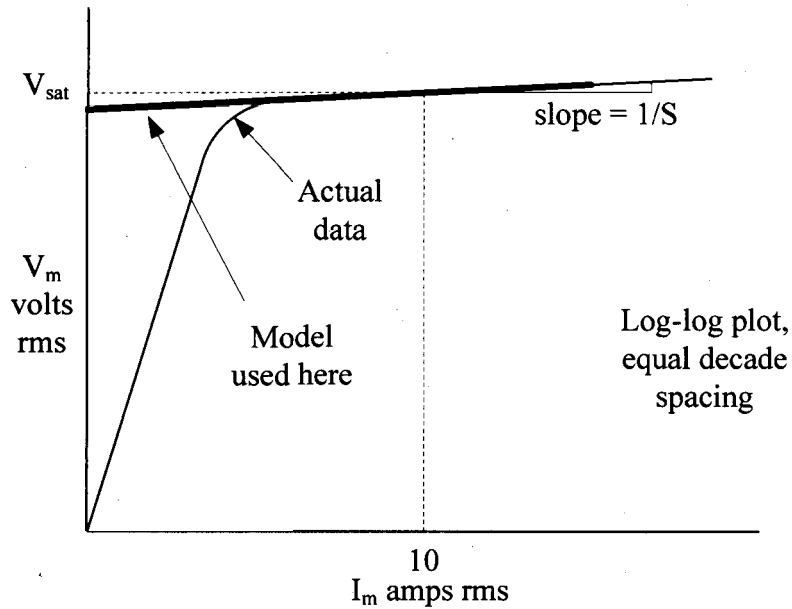


Figure 2-8 – B-H Characteristic of a solid-core CT

For the IEEE solid-core CT model, only two parameters need to be extracted from the characteristic curve in Figure 2-8: the inverse of the slope of the saturation section (S) and the rms saturation voltage (V_{sat}).

The straight line with a slope of $1/S$, which represents the saturation section of the characteristic, is not linear and can be mathematically defined by Equation(2.8).

$$V_m = V_i I_m^{1/S}, \quad (2.8)$$

where:

V_i = value of V_m for a magnetizing current equal to one ($I_m = 1, \log I_m = 0$).

2.7.2 Solution of circuit model

The circuit of Figure 2-1 is solved by writing Kirchhoff's Law around the right-hand loop such that in Equation(2.9)

$$v_m - (i_{ss} - i_m) \cdot (R_w + R_b) - L_b \cdot \frac{d}{dt}(i_{ss} - i_m) = 0. \quad (2.9)$$

The ideal CT secondary current (i_{ss}) can be expressed as Equation(2.10).

$$i_{ss}(t) = \frac{I_{peak}}{N} [Off \cdot e^{-t/\tau} - \cos(\omega t - \cos^{-1} Off)], \quad (2.10)$$

where:

I_{peak} = peak value of the Current (A)

N = CT Turns ratio

Off = magnitude of DC offset (per unit)

τ = system time constant

CTs present difficulties in manipulating the primary current if the magnitude of the primary current dc offset is high (**off** = 1), because it saturates the magnetic core. The magnitude of this offset is at its highest value, if the fault happens at the zero crossing of the voltage waveform.

The value of the magnetizing current (i_m) can be expressed as Equation(2.11)

$$\frac{di_m}{dt} = \frac{di_m}{d\lambda} \cdot \frac{d\lambda}{dt}, \quad (2.11)$$

where:

λ = instantaneous Flux Linkage (Weber-turns)

In order to find the magnetizing current, the instantaneous curve of λ versus i_m is needed.

It is postulated that the following formula can replace the curve [1]:

$$i_m = A \cdot \lambda^S, \quad (2.12)$$

where:

A = equation constant

Therefore, Equation(2.11) is written as Equation(2.13)

$$\frac{di_m}{d\lambda} = A \cdot S \cdot |\lambda|^{S-1} \quad (2.13)$$

Finally, with substitutions and manipulation, the differential equation is re-written as Equation(2.14)

$$\frac{d\lambda}{dt} \cdot [1 + L_b \cdot A \cdot S \cdot |\lambda|^{S-1}] = -(R_w + R_b) \cdot i_m + (R_w + R_b) \cdot i_{ss} + L_b \frac{di_{ss}}{dt}. \quad (2.14)$$

This first-order nonlinear differential equation is solved for $\lambda(t)$ by using standard numerical analysis techniques, such as trapezoidal integration. Then, with the magnetizing current (i_m) and the fault current (i_{ss}), the actual secondary current i_s can be found by Equation(2.15)

$$i_s = i_{ss} - i_m. \quad (2.15)$$

The next step is to determine the constant factor (A) of Equation(2.12) in terms of the known parameters.

2.7.3 Determination of constant "A"

By Faraday's law, flux linkage (λ), is related to the instantaneous magnetizing voltage (v_m) as follows:

$$v_m = \frac{d\lambda}{dt}. \quad (2.16)$$

By assuming a sinusoidal waveform for the magnetizing voltage (v_m), the flux linkage can be found by Equation(2.17):

$$v_m = \sqrt{2} V_m \cos(\omega t) \Rightarrow \lambda = \int v_m dt = \int \sqrt{2} V_m \cos(\omega t) dt = \sqrt{2} V_m \frac{1}{\omega} \sin(\omega t), \quad (2.17)$$

This implies that the flux linkage also has a sinusoidal waveform. The magnetizing current (i_m) has a non-sinusoidal waveform and can be expressed as Equation (2.18):

$$i_m = A \lambda^s = A \left[\frac{\sqrt{2} V_m}{\omega} \sin(\omega t) \right]^s = A \left[\frac{\sqrt{2} V_m}{\omega} \right]^s \sin^s(\omega t). \quad (2.18)$$

By definition, the *rms* value of the magnetizing current (i_m) represented by Equation(2.19):

$$i_{m \text{ rms}} = I_m = A \left[\frac{\sqrt{2} V_m}{\omega} \right]^s \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \sin^{2s}(\omega t) dt}. \quad (2.19)$$

By defining the ratio of the rms to the peak value of the magnetizing current as the RP in Equation(2.20):

$$RP = \frac{\text{rms}}{\text{peak}} = \frac{\sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_{\text{peak}}^2 \sin^{2s}(\omega t) dt}}{I_{\text{peak}}} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \sin^{2s}(\omega t) dt}, \quad (2.20)$$

the magnetizing current (i_m) can now be re-written as

$$I_m = A \left[\frac{\sqrt{2} V_m}{\omega} \right]^s \cdot RP. \quad (2.21)$$

As shown in Figure 2-8, the magnetizing voltage (V_m) is equal to the saturation voltage (V_s), if the magnetizing current (I_m) is equal to 10 A. Therefore, Equation(2.21) can be written as:

$$10 = A \left[\frac{\sqrt{2} V_{sat}}{\omega} \right]^s RP \Rightarrow A = \frac{10\omega^s}{(\sqrt{2} V_{sat})^s} \cdot \frac{1}{RP}. \quad (2.22)$$

Therefore, the fundamental i_m vs. λ relationship (Equation(2.12)) is expressed as:

$$i_m = \frac{10\omega^s}{(\sqrt{2} V_{sat})^s} \cdot \frac{1}{RP} \cdot |\lambda|^s. \quad (2.23)$$

2.8 Advantages and Disadvantages of Air-gap Core CTs

2.8.1 Advantages

There are several significant advantages of air-gap core CTs over conventional solid-core CTs, as follows [4].

- Current transformers that contain air gaps, provide a reduction in the remanent flux which results in an improved transient performance.
- A smaller core cross section is required to produce the same flux, generated by solid-core CTs. This physically smaller CT should not imply that it is to manufacture. In fact, the air-gap core CT is typically more expensive to manufacture due to the mechanical mounting of the core to prevent movement of the CT.

- Less core oversizing is required to avoid the implication of saturation.
- The open circuit voltage across the secondary terminals is less for air-gap core CTs.

2.8.2 Disadvantages

The disadvantages of the air-gap core CT are as follows:

- Air-gap core CT's require a higher magnetizing current which results in larger ratio and phase angle errors.
- When the core flux decays to its final value (remanence level) after a fault interruption, the energy stored in the magnetic circuit must be dissipated in the secondary circuit of the CT which results in a lengthy unidirectional discharge (approximately 1 sec). Since this change in the flux is greater than that for an air-gap core CT, the time to the flux in the CT secondary circuit is longer. In fact, this time can be so long that a high-speed reclosing can take place before the remanence level is reached.
- The Core is mechanically weaker due to the slots cut into it. This can be a factor during extremely high fault currents, where the forces in the iron can cause movement of the CT.
- It is difficult to keep the air gap consistently the same size due to mechanical forces and temperature variations. As a result, the CT parameters change over time. Typical cuts made in the core of the CT are in the order of 0.5 mm. Given the mechanical forces and expansion/contraction due to temperature, it is difficult to maintain the same gap size.

- There is some loss in the transformation of the dc component with an air-gap core CT.

2.9 Consequences of CT Saturation

A saturated CT that fails to deliver a true reproduction of the primary current can result in undesirable, and sometimes, desirable operation [1].

The current differential is most likely to mal-operate when the CT saturates. The partial or full saturation of one CT allows the other CTs to deliver the necessary operating current to the differential relay for a through fault condition, causing a false trip by not producing the expected balancing current.

When a CT provides a partial or a distorted current reproduction of the primary current to a protective device which has an inverse time current characteristic (e.g., overcurrent relay), an additional delay in tripping the power circuit may result. This delay in tripping can result in de-energizing a large portion of the distribution system due to the loss of the relay coordination, caused by the CT saturation.

2.10 Summary

Current transformers are a necessary component of any viable power system for both protection and metering applications. The main role of a current transformer is to replicate the primary current without introducing any error. In this Chapter, after an equivalent circuit of a current transformer was introduced, steady-state and transient errors were illustrated. Two types of current transformers were introduced and the advantages and disadvantages of using one over the other were discussed.

In order to come closer to primary objectives of this thesis, studying the behavior of busbar differential relays with air-gap core current transformer, the differential protection concept must be clarified. The next Chapter illustrates this concept.

Chapter 3

3.0 DIFFERENTIAL PROTECTION CONCEPT

Any relay, which has information on the sum of all the currents entering and exiting the zone of protection and operates on the difference between these currents, falls under the category of “differential” relaying.

Differential relaying is a typical form of closed-zone protection that can detect a fault within the protected zone with a high selectivity and security. Such relaying involves all currents entering and leaving a protection zone and comparing them. The zone of differential protection is precisely determined by the location of the current transformers as seen in Figure 3-1. When the net value of the currents exceeds the pre-set threshold, a fault must exist within the zone. Typically differential protection is applicable to all components of the power system: transmission lines, distribution feeders and cables, transformers, generators, motors, buses, capacitors, and reactors.

The other reason for applying the differential relaying method to any power system is its high sensitivity. The relay operates on the current difference instead of the through current in the power system. Thus, the relay has a much higher sensitivity than that of an overcurrent or distance relay that must be set above the load flow through the protected zone. This type of protection does not need to have any intentional time delay to coordinate with other protection relay. Thus, differential protection can provide relatively high-speed protection.

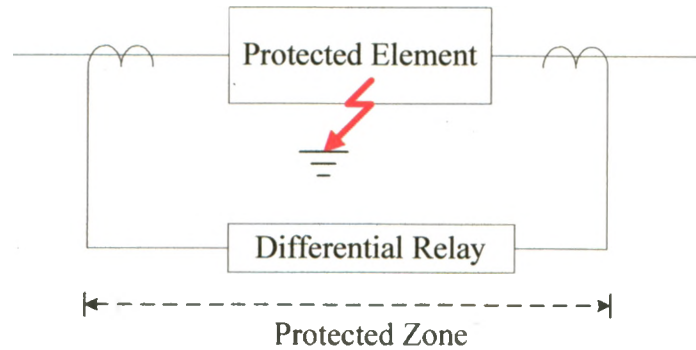


Figure 3-1 - Closed Zone Protection

Differential relaying has several advantages.

- It operates only for faults within the protected zone.
- It is sensitive to internal faults.
- It has a high stability to external faults.
- It is immune to power swings and load encroachments.
- It has simple and convenient settings.
- It does not require coordination with other relays.
- It can operate instantaneously.

Differential relaying also has following disadvantages.

- It is communication-dependent, when it is applied to a line, feeder, or cable protection.
- It has no back-up protection.

3.1 Principle of Differential Protection

Differential relays employ the circulating principle, along with either the high or low impedance principle to ensure stability in external fault conditions. The protected zone is clearly defined by the current transformers at each end of the zone. Faults, external to the protected zone, are not seen by the differential relay. As depicted in Figure 3-2, during normal or external fault conditions, no current flows into the relay, because the current

circulates within the circuit. When a fault occurs within the protected zone, fault currents from both directions are injected into the relay and enabling it to operate as illustrated in Figure 3-3. Since the relay does not respond to the faults outside its protected zone, the relay does not need to discriminate from other devices and can, therefore, be instantaneous.

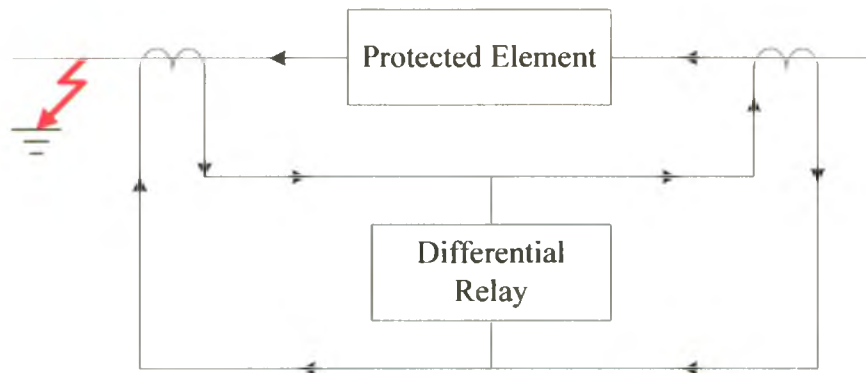


Figure 3-2 - Current Path during External Faults

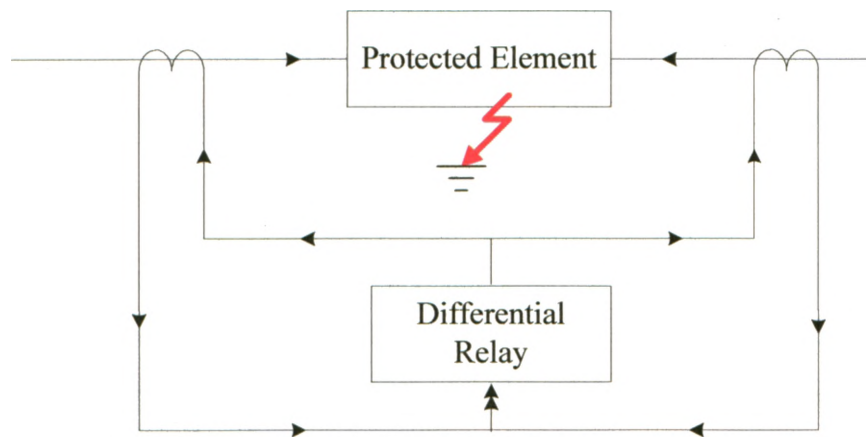


Figure 3-3 - Current Path during Internal Fault

Differential relays can mal-operate in undesirable circumstances such as CT saturation in external fault conditions, since the output from the saturated CT is reduced, resulting in a false differential current flowing through the relay. There are three categories of differential relays:

- overcurrent differential protection
- high-impedance differential protection
- percentage-restrained differential protection

The cost, reliability, sensitivity, and speed of each category should be considered in deciding what type of differential relay should be applied for a specific power system application.

3.1.1 Overcurrent differential protection

In this protection scheme, a time overcurrent relay is connected in parallel with all the current transformers. The overcurrent relay is then set above the maximum load current of all the feeders for security in the steady-state condition. This type of protection has been used for many decades.

3.1.2 High impedance differential protection

The criterion used in high impedance differential protection is very simple. The high impedance path, by a resistor, produces a voltage during an internal fault. By measuring the produced voltage value, the unit can determine if the fault is within the protected zone [6].

During external faults, even with severe saturation in some of the connected current transformers, the voltage does not rise above a certain level, because the other CTs provide a lower impedance path than that with the relay input impedance. This principle has been used for more than half a century because it is robust, secure, and fast. However, the technique is not free from disadvantages, including the following.

- The high impedance approach requires dedicated CTs which contribute to the overall cost.
- The approach can not be applied to re-configurable buses.

- Such an approach requires limiting varistors that are capable of absorbing significant energy during the busbar faults.

3.1.3 Percentage-restrained differential protection

The percentage-restrained characteristic operates on the ratio of the operating current (I_{op}) to the restrained current (I_{res}). The operating current is the phasor sum of the currents flowing into the zone of protection. Under normal conditions, these currents should sum to zero. The restrained current is the current flowing through the zone of protection. This provides the desirable feature of restraining the relay when high levels of currents are flowing through the zone. There are several ways to qualify the restrained current [7]:

- **Summation:** The relays using the summation restraint current have the polarities of each current input arranged such that they tend to be additive for an external fault and subtractive for an internal fault. By considering a simple two-restraint circuit with equal sources for each circuit, an external fault has the restraint current that is two times the current measured by each input of the relay. For an internal fault, the two currents cancel, resulting in a restraint current that is zero times the current measured by the relay.
- **Average:** The Relays with an average restraint current measure the magnitudes of the current in each input circuit and take the average. That is the sum of the magnitude of the individual currents divided by the number of input circuits. For a simple two-restraint circuit with equal sources for each circuit, an external fault has a have restraint current that is half the sum of the current, measured by each input of the relay. For an internal fault, the restraint current is also half the sum of the currents, measured by each circuit.
- **Maximum:** For relays using the maximum restraint current measure magnitudes of the current in each input circuit, the largest of these is the restraint current.

Figure 3-4 signifies the single line diagram of a motor differential relay, where the current polarity of the left current (I_L) and the right current (I_R) are shown in the polarity of an internal fault.

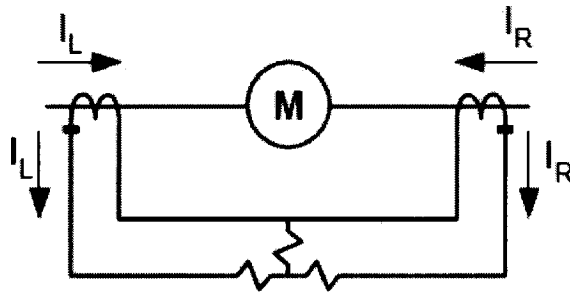


Figure 3-4 - Differential Protection

Based on the previous explanation for the operation (I_{op}) and restrained (I_{res}) current,

$$I_{op} = |I_L + I_R|, \quad (3.1)$$

$$I_{res} = |I_L| + |I_R|, \quad (3.2)$$

$$I_{res} = (|I_L| + |I_R|)/2, \quad (3.3)$$

And

$$I_{res} = \text{Max} (|I_L|, |I_R|). \quad (3.4)$$

Equation(3.2) expresses the summation restrained current, whereas Equation(3.3) expresses average restrained current, and Equation(3.4) expresses the maximum restrained current.

As portrayed in Figure 3-5, in a percentage differential relay, the magnitude of the sum of the currents, entering the zone of protection must exceed a predetermined percentage of the restrained current quantity, expressed as Equation(3.5).

$$I_{op} = k * I_{res}. \quad (3.5)$$

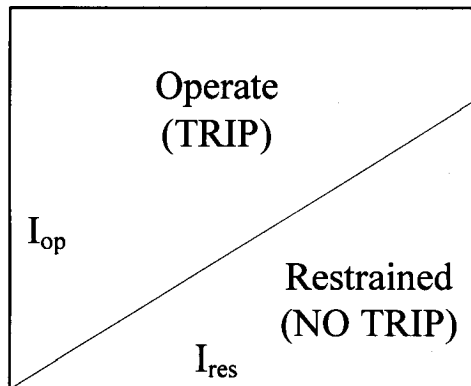


Figure 3-5 - Percentage Restraint Characteristic

The percentage-restraint characteristics are classified into two types:

- straight percentage
- variable percentage

The solid line in Figure 3-6 illustrates a straight percentage-restraint characteristic set at 50%. The minimum pickup line provides a cutoff of the characteristic at low levels, where the accuracy errors result in poor ratio measurements.

The dotted line in Figure 3-6 shows a dual-slope characteristic that provides the variable percentage restraint characteristic. The dotted line starts out as a straight percentage restraint up to the point of inflection where increases to a higher slope. The second slope crosses the y-axis in the negative region. Consequently, as the restraint current increases, the percentage of differential current required to cause a trip increases.

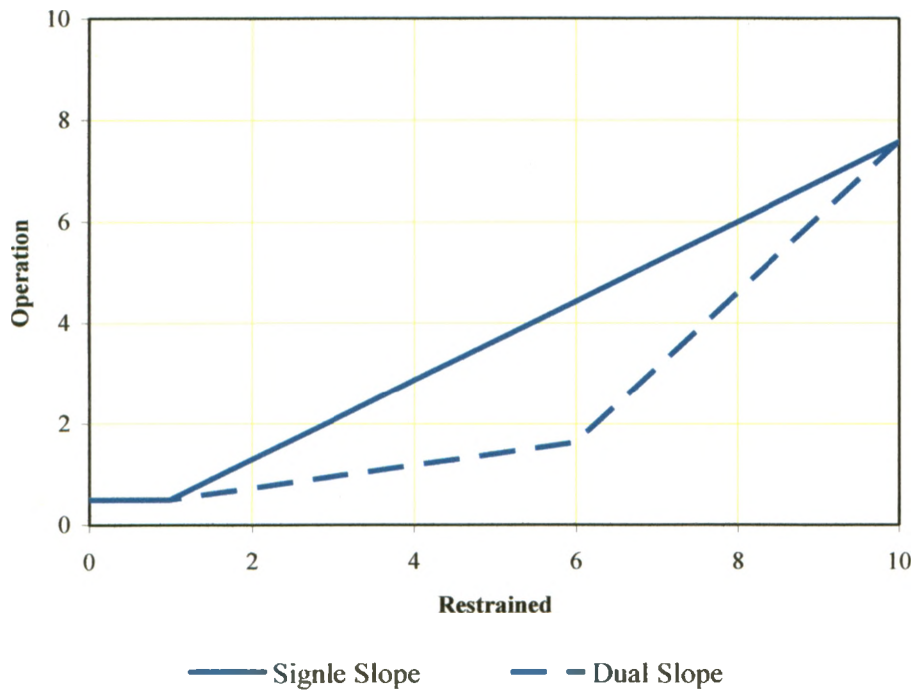


Figure 3-6 - Single and Dual Slope Differential Characteristic

3.2 Effect of the CT Saturation on Differential Protection

A solid-core CT saturates at a smaller current level and in less time than an air-gap core CT with the same voltage rating and with the same burden. It is accepted that the performance of a solid-core CT has a detrimental effect on the performance of the protective relays and, hence, air-gap core CTs are applied in most HV applications. With the flexibility of implementing relay algorithm in microprocessor-based equipment, there have been developments towards improving the response of the relays to corrupted current waveforms from the effect of the CT saturation (in the form of the saturation detection features). Consequently, there is the expectation that because of these improvements, the use of modern microprocessor-based relays can alleviate most of the concerns that are affixed to the use of solid-core CT's.

3.3 Electromechanical vs. Microprocessor-Based Technology

Since electro-mechanical differential relays are still in use, it is important to highlight the differences between the electro-mechanical and microprocessor-based differential protection [8].

Any electromechanical transformer protective device involves moving parts. The movement is caused by electrometrical forces and torques, which are proportional to the RMS values of the input signals. A microprocessor-based device, on the other hand, does not have any moving parts, and does not solely rely on the RMS values of the sensed signals. This is a major difference between electromechanical and microprocessor-based technologies. The microprocessor-based technology offers a selection of attributes of the input signals (e.g., fundamental frequency values, and other harmonics), electromechanical technology operates solely on the RMS values of the input signals.

The key differences in the settings are also due to the change in the principal of operation between the two technologies. Some of these differences have been analyzed and published in several papers as follows.

- Electromechanical technology offers only few selectable single slopes such as 15%, 25%, or 40%. Microprocessor-based technology offers a dual slope selection with a much higher resolution. The use of two slopes in microprocessor relays has become a common practice among the utilities. Lower slopes are used for through currents as high as 200% of the protection zone rated current. The steeper slopes are used for higher through current to better remedy the CT errors and partial CT saturation.
- The restraint current in electromechanical technology is proportional to the sum of all the input circuit currents, connected to the differential protection. Microprocessor-based relays offers variety of restraint possibilities, as mentioned before.

- Electromechanical technology uses a fixed harmonic spectrum for additional restraint during the CT saturation or transformer power up. Microprocessor-based technology offers a variety of choices in this area.

3.4 Microprocessor-based Relays and Saturated Current Waveforms

3.4.1 Introduction

Protective relays rely on rescaled current, produced by current transformers, as an input. The rescaled current should pass through several internal components of the relay. These internal components are the input CT, analogue filter, A/D converter and digital filter. Order of the mentioned components is shown in Figure 3-7.

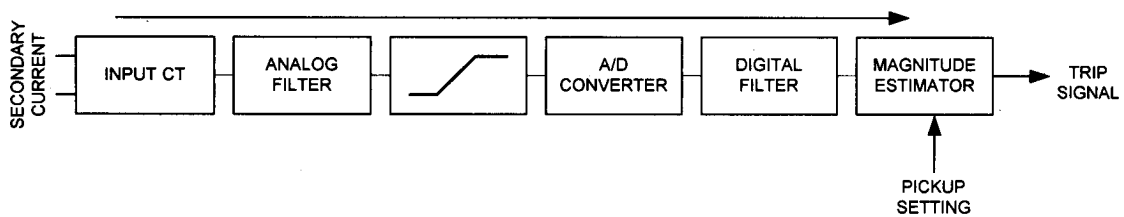


Figure 3-7 - Signal Processing Chain of a Typical Relay

Each component reduces effect of the saturated waveform on the relay's final decision [9]. This section explains and illustrates how internal components, of a typical microprocessor-based relay responds to a saturated waveform.

3.4.2 Impact of relay current transformer

Usually, the relay input CTs can saturate, adding to the complexity of the analysis, and to the scale of the problem. However, the saturation of the relay input CTs can be neglected for the following reasons:

- The secondary current is substantially reduced under severe saturation of the main CTs.

- The saturation of the main CT makes the secondary current symmetrical, eliminating the danger of exposing the relay input CT to decaying dc components.
- The secondary current has a form of short-lasting spikes. This limits the flux in the cores of the relay inputs of the CTs.

3.4.3 Impact of analogue filters

Analogue filters are implemented in order to prevent the aliasing of higher frequencies on the fundamental frequency signal. Typically, a second order filter is used with a cut-off frequency of about $1/3^{\text{rd}}$ of the sampling rate.

Analogue filters have a positive impact on the response of the relay to heavily saturated current waveforms. Due to its intended low-pass filtering response, the analogue filter reduces the peak values of its input signal and lengthens the duration of such spikes. In a way, the analogue filter smoothes out the waveform by shaving its peaks and moving the associated signal energy into the area of lower magnitude as illustrated in Figure 3-8. Given the fact that the peak magnitude of the spikes is well above the conversion level of the relay, and as such is not used by the relay, when the operating quantity is derived, the operation of shifting some signal energy from the peaks into the low magnitude area increases the operating signal, and improves the overall response of the relay.

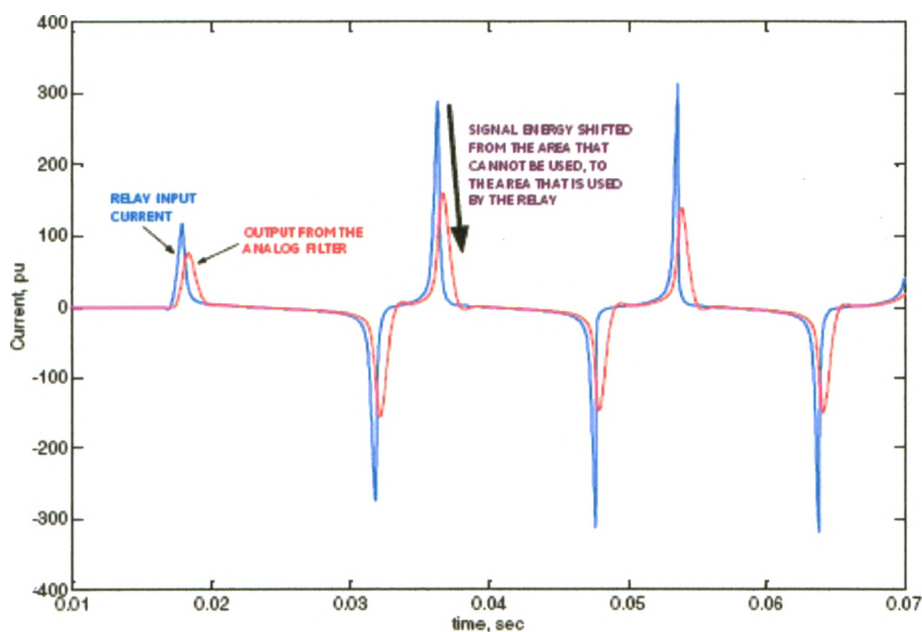


Figure 3-8 - Impact of a Linear Analogue Filter on the Saturation Current Waveform [9]

3.4.4 Impact of the A/D converter

The impact of the A/D converter is twofold. First, any converter has a limited conversion range, where signals above a certain level are clamped. The conversion range of today's relays is typically in the range of 10 to 50 times the rated secondary current. Figure 3-9 illustrates the impact of the A/D clamping on the signal processed by the relay.

The second aspect, related to the A/D conversion, is a limited sampling rate. Today's relays sample at rates varying from 8 to 128 samples per cycle. Industrial relays tend to sample at 8 to 16 times per cycle. Given the short duration of the signal pulses, produced by a heavily saturated CT, the location of the A/D samples on the waveform plays an important role. This results in different values of the operating signal for the protection function. In Figure 3-10, the samples line up in a way that three samples in each cycle catch the peaks of the signal.

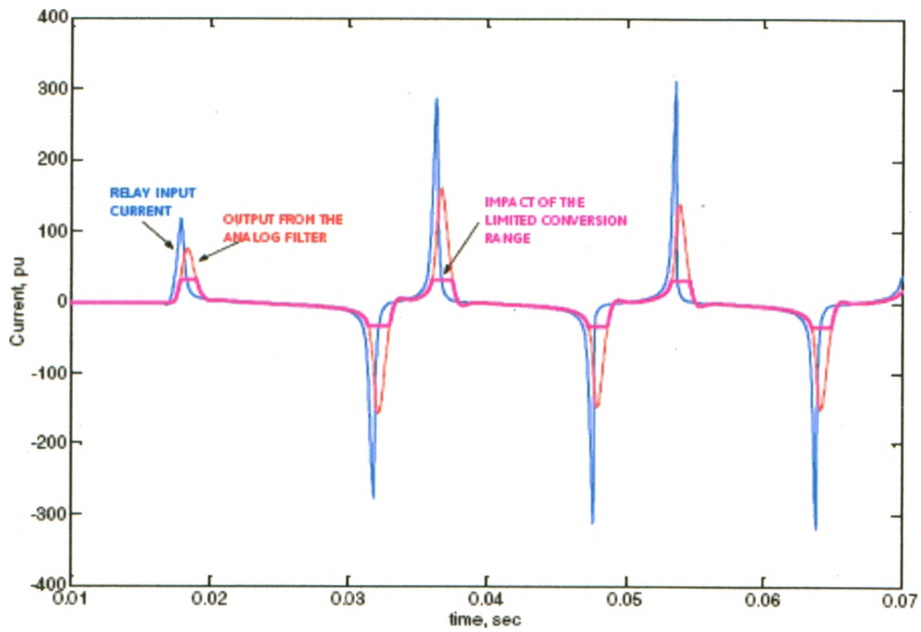


Figure 3-9 - Impact of A/D Converter – Clamping [9]

It is also obvious that the higher sampling rates provides more opportunities to “integrate” the short-lasting signal pulses and yield a higher operating signal.

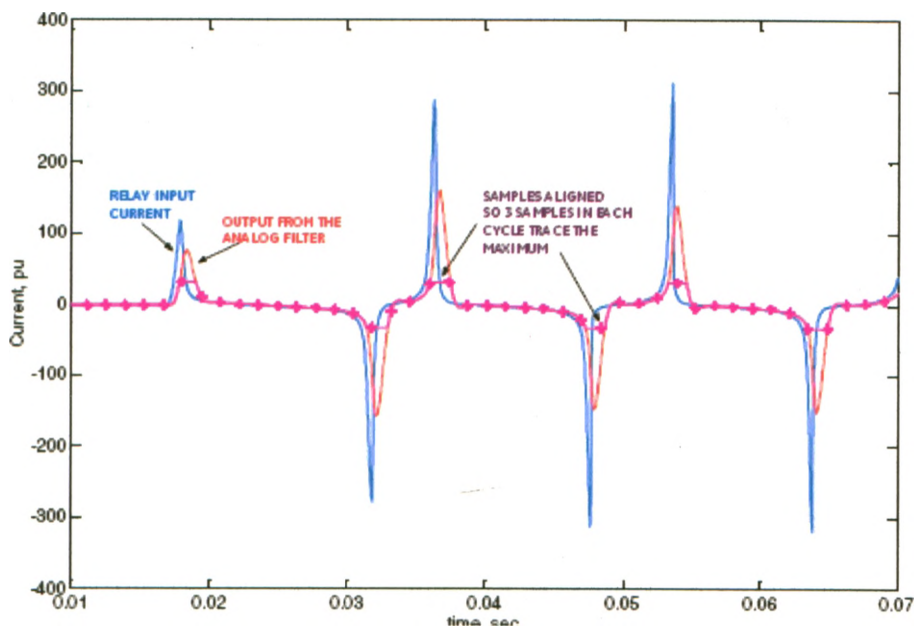


Figure 3-10 - Impact of A/D Converter (sampling) [9]

3.5 Summary

Differential protection, as its name implies, compares the currents entering and leaving the protected zone, and operates when the difference between these currents exceeds a pre-determined magnitude. This Chapter summarized the concept of differential protection and the effect of CT saturation on this type of protection. Also, the differences between new microprocessor-based relays and old electromechanical-based relays from the CT saturation perspective are described.

In the next Chapter, an algorithm for modeling air-gap core CTs is presented. Presented model is then validated by using a solid-core CT model, presented by the IEEE PSRC committee.

Chapter 4

4.0 AIR-GAP CORE CT MODELING

4.1 Introduction

In order to study the differential protection behavior with air-gap core CT, a mathematical model of an air-gap core CT is needed. This model should accurately indicate the actual waveform of its secondary current, especially in the event of CT saturation. This model should also indicate the degree of saturation as a function of time.

Typically, CT manufacturers usually do not disclose all the CT parameters needed for an elaborate mathematical model of an air-gap core CT. For example, the magnetizing current in the region below the B-H characteristic knee point (discussed in Section 2.5) is a complex combination of magnetizing, hysteresis, and eddy current components which are not usually disclosed by the CT manufacturer. Therefore, the model that is proposed in this thesis is simplified by ignoring the parameters that are hard to get and have negligible effect on the overall solution. Since the main discussion of this thesis is on the saturation effect of an air-gap core CT, part of the waveform in the below-knee-point region can be neglected with little effect on the accuracy. Because of neglecting part of the B-H characteristic, this model is not a good repetitive of the air-gap core CT secondary waveform under low current and low burden conditions.

An equivalent circuit used for modeling basis is discussed in Section 4.2. Section 4.3 introduces a novel algorithm for the air-gap core CT model. In Section 4.4 the method of calculating the model parameters is described. Section 4.5 is about the model's validation and Section 4.6 investigates the saturation characteristic of the modeled CT.

In this thesis, an Excel spreadsheet is generated as the modeling software. The spreadsheet functions are similar to those of the Electro Magnetic Transient Program (EMTP) in using trapezoidal integration to approximate the response of the equivalent circuit.

4.2 Theory

Figure 4-1 reflects the electrical equivalent circuit, chosen to develop the model for the air-gap core CT.

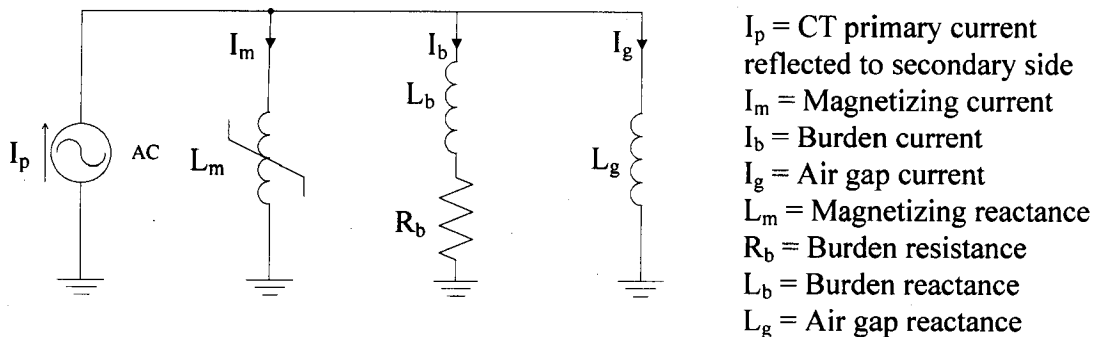


Figure 4-1 - Equivalent One Line Diagram Used for the Air-gap Core CT Simulation

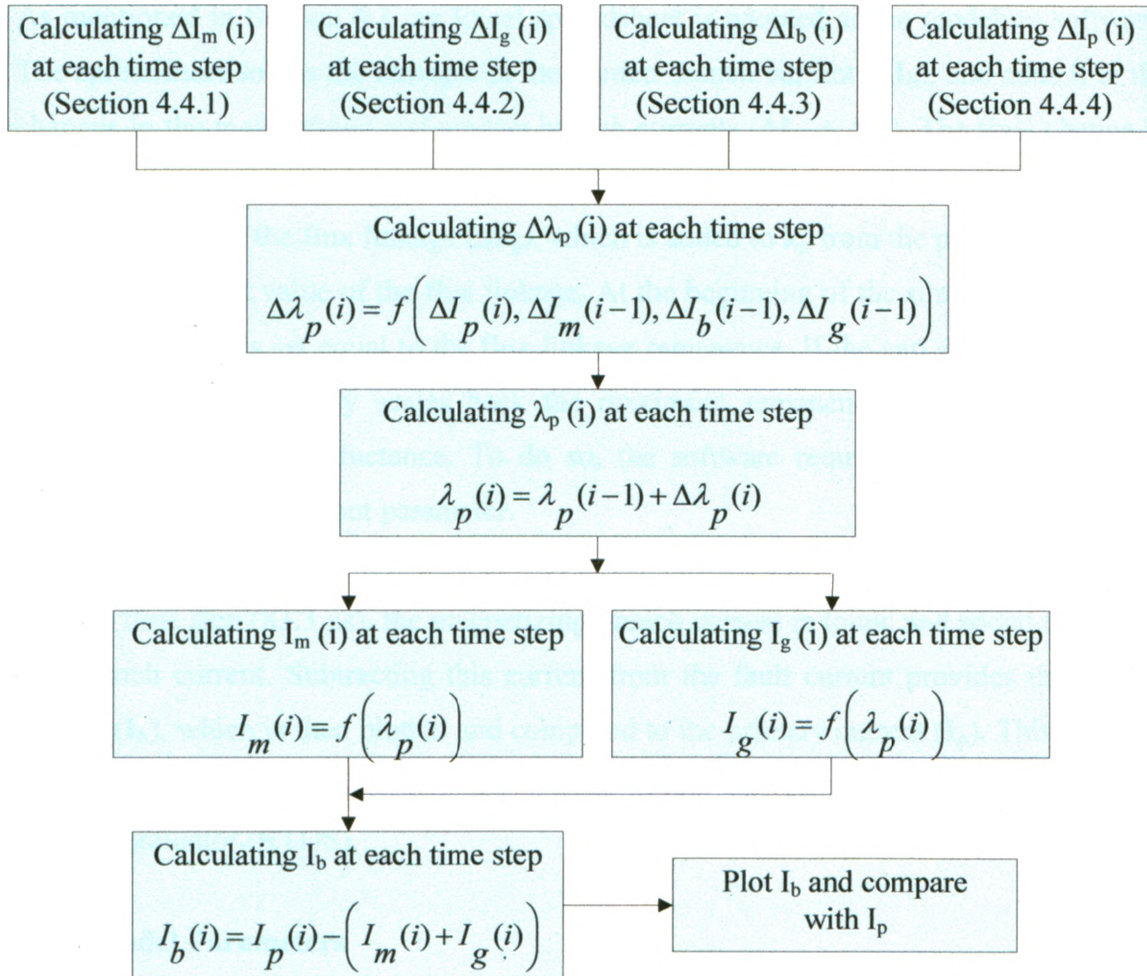
As stated by the Kirchhoff law, the current entering any junction is equal to the current leaving that junction. The results of applying Kirchhoff law to the equivalent circuit of Figure 4-1 are mathematically expressed as Equations(4.1) and (4.2).

$$I_p = I_m + I_g + I_b, \quad (4.1)$$

$$\Delta I_p = \Delta I_m + \Delta I_g + \Delta I_b. \quad (4.2)$$

4.3 Modeling Algorithm

Air-gap core CT modeling algorithm is portrayed in Figure 4-2.



Initial Condition:

Instantaneous flux linkage at time step zero ($i=0$) is equal to flux linkage remanence.

Parameter Definition:

I_p = Primary current reflected to secondary side

I_b = Burden Current

I_m = Magnetizing current

I_g = Air gap Current

λ_p = Instantaneous flux linkage

Figure 4-2 - Modeling Algorithm

As mentioned in Section 4.1, an Excel spreadsheet is adopted as the modeling software. The spreadsheet solves the changes in the burden branch current (ΔI_b), and adds it to the changes in the magnetizing and air-gap branch currents ($\Delta I_m + \Delta I_g$). The final change in the current must be set equal to the change in primary current (ΔI_p). The result is solved for the changes in the flux linkage ($\Delta \lambda_p$), which is added to λ_p from the previous time step to find the current value of the flux linkage. At the beginning of the simulation ($i=0$), the flux linkage (λ_p) is set equal to the flux linkage remanence. If the gap size increases, the spreadsheet automatically scales back the maximum remanence in proportion to the reduced magnetizing inductance. To do so, the software requires permeability of the unsaturated iron as an input parameter.

At each time step (83.3 μ s), the magnetizing branch current is found and added to the air-gap branch current. Subtracting this current from the fault current provides the burden current (I_b), which is then plotted and compared to the primary current (I_p). This sampled burden current is then applied to commercial busbar differential relays by the Real Time Digital Simulator (RTDS).

4.4 Model Parameters

The next four subsections describe the proposed method for calculating the parameters of the equivalent circuit air-gap core CT, as depicted in Equation(4.1).

4.4.1 *Defining the non-linear magnetizing current (I_m)*

The non-linear magnetizing branch (I_m) is calculated from the B-H characteristic of the CT.

The B-H characteristic of a CT is a plot of the rms magnetizing voltage in relation to the rms magnetizing current on the log-log axes, as shown in Figure 4-3.

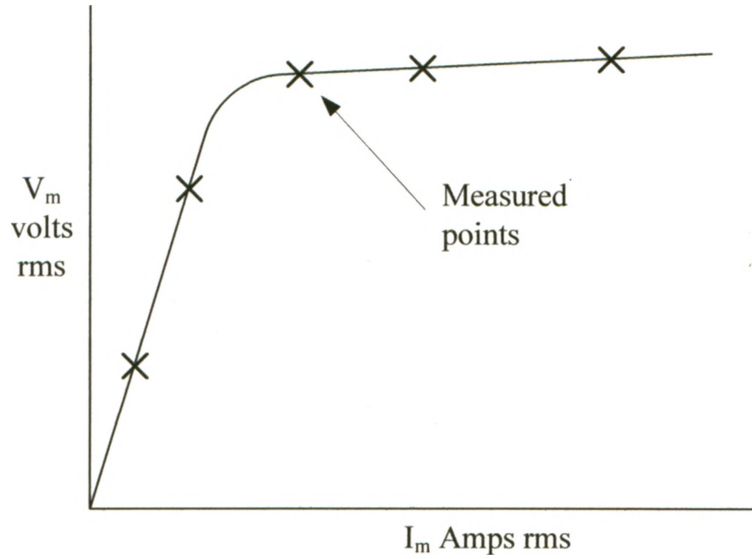


Figure 4-3 – B-H Characteristic of a CT

To formulate this characteristic, it should be considered as two parts. The first part simulates the linear section and the second part simulates the saturated section of the characteristic, as signified in Figure 4-4.

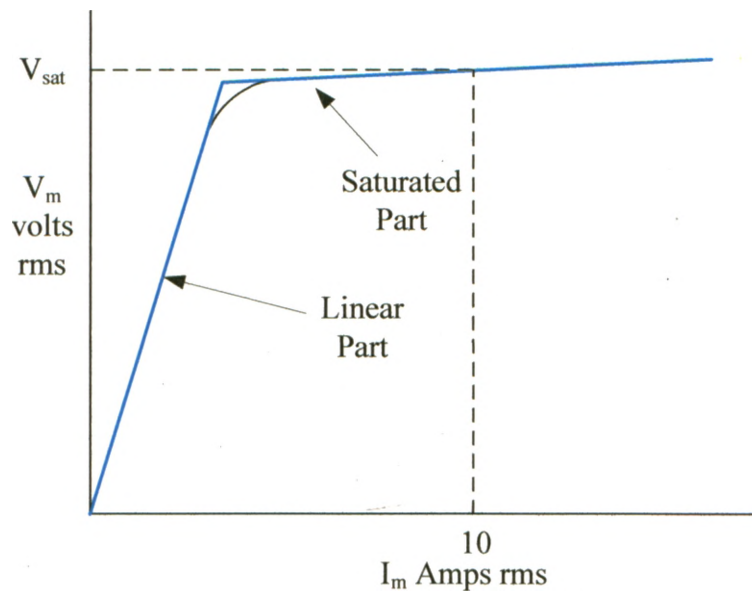


Figure 4-4 - CT B-H Characteristic Simulated as Two Parts

The saturation voltage (V_{sat}) is chosen at the point, where the magnetizing current is ten amps ($I_m = 10$), as defined by the IEEE standard PC37.110.D5 [5]. For example, a C400 CT has a saturation voltage of 400 volts rms for a magnetizing current of 10 amps [5].

The straight line in Figure 4-4, which approximates the saturation section, is not linear. It is a curve defined mathematically by Equation(4.3) as

$$\log V_m = \frac{1}{S} \log I_m + \log V_i, \quad (4.3)$$

where

$1/S$ = line slope

V_i = value of V_m for magnetizing current equal to one ($I_m = 1$, $\log I_m = 0$)

The data sheets supplied by the CT manufacturers indicated that 22 is a reasonable value for the inverse of the line slope ($S = 22$).

After the logarithmic factors are removed, Equation(4.3), can be expressed as Equation(4.4):

$$V_m = V_i I_m^{1/S}. \quad (4.4)$$

It is postulated that the current passing through the CT magnetized branch can be defined as:

$$I_m = i_0 \left(\frac{\lambda_p}{\lambda_0} \right)^S + \text{sign}(\Delta\lambda) i_h \Rightarrow \Delta I_m = \frac{i_0 S}{\lambda_0} \left(\frac{\lambda}{\lambda_0} \right)^{S-1} \Delta\lambda, \quad (4.5)$$

where

λ_p = primary flux (Weber-turns)

λ_0 = base flux linkage (Weber-turns)

i_0 = current scaling factor

i_h = hysteresis current (A)

S = inverse of the slope in the saturated part of the B-H characteristic

$\Delta\lambda$ = remanence difference at each time step (Weber-turns)

The base flux linkage (λ_0 in volts seconds peak) is found from $V_{sat}/2\pi f$ ¹. If the flux linkage is at the rated value, the current scaling factor (i_0) must be set to the peak value, corresponding to 10 A rms. Therefore, the peak value of the distorted magnetizing current is assigned as i_0 .

The sign function displaces the magnetizing current (I_m) to the right by an amount of i_h , when the flux linkage is increasing, and left by i_h when the flux linkage is decreasing. This offset approximates the core hysteresis. Although it is secondary in importance to this study, this term can be adjusted to keep the saturation curve symmetric with respect to the origin, when the core includes the flux remanence. This term is ignored at the high current levels.

4.4.2 Defining the air-gap branch current (I_g)

The second component of the magnetizing current I_g is extracted from Equation(4.6):

$$I_g = \frac{\lambda_p}{L_g}, \quad (4.6)$$

where

L_g = air gap inductance (H)

λ_p = instantaneous flux linkage (Weber-turns)

¹ Saturation voltage should be expressed as a peak (not rms) since the time domain analysis needs the instantaneous quantities.

The air gap inductance (L_g) is related to the reluctance of the air-gap core. Reluctance of the air-gap gap (\mathfrak{R}) is calculated by Equation(4.7)

$$\mathfrak{R} = \frac{l_g}{\mu_0 A_g}, \quad (4.7)$$

where

l_g = length of the air gap (m)

A_g = cross sectional area of the air gap (m²)

μ_0 = permeability of the free space (H/m)

The gap length (l_g) is commonly expressed in per unit (pu) of the core perimeter (typically 0.0002 to 0.0003 pu). Therefore, the average core radius is required to calculate reluctance of the air-gap core. CTs without an air gap are modeled by selecting the gap size arbitrarily, as a small value such as 0.000001 pu. This makes the gap inductance (L_g) large and the gapped branch current (I_g) negligible.

The change in the air-gap branch magnetizing current is then expressed as

$$\Delta I_g = \frac{\Delta \lambda_p}{L_g}. \quad (4.8)$$

4.4.3 Defining the burden branch current (I_b)

The third component of the magnetizing circuit is the CT burden current (I_b). That is calculated from Equation(4.9)

$$\lambda_p = L_b I_b + \int I_b R_b dt, \quad (4.9)$$

where

L_b = burden inductance (H)

R_b = burden resistance (can include resistance of the secondary winding of the CT) (Ω)

λ_p = instantaneous flux linkage (Weber-turns)

the numerical integration by using the trapezoidal rule [10] approximates Equation(4.9) to Equation(4.10):

$$\Delta\lambda_p = L_b \Delta I_b + \left(I_b + \frac{\Delta I_b}{2}\right)R_b \Delta t. \quad (4.10)$$

4.4.4 Defining the source current (I_p)

The source current (I_p) in Figure 4-1 models the fault current, as seen from the secondary winding side of the current transformer. The instantaneous value of this current is derived from Equation(4.11)

$$I_f = I_{f0} [A_0 e^{-(\omega t/\tau)} - \cos(\omega t - \theta_0)], \quad (4.11)$$

where

$$\omega = 2\pi f = 377 \text{ Rad/s}$$

τ = fault time constant (X/R)

A_0 = fault offset factor

The fault offset factor $-1 < A_0 < 1$ describes the point-on-wave for the fault and offset angle $\theta_0 = \text{ArcCos}(A_0)$. The faults at zero voltage going positive, peak voltage and, zero voltage going negative denote A_0 equal to 1, 0, and -1, respectively.

4.5 Model Validation

As mentioned in Section 1.0, the electrical characteristic of the air-gap core CT has not been standardized. Moreover, the air-gap core CT performance characteristic has never been widely published [4]. This section proposed a new model for the air-gap core CT

and the verification of the output waveform of the proposed model vs. that of the actual air-gap core CT is necessary. A validation test by employing an actual air-gap core CT requires the procurement of the CT and the engagement of a high current laboratory for about a week. These kinds of tests are costly and time consuming.

In this thesis, for validation purposes, a comparison between the waveform of the air-gap core CT model and the solid-core CT model, presented by the IEEE PSRC committee, is made. The length of the air gap (l_g) should be considered as 0.000001 pu of mean length of the magnetic path for the new air-gap core CT model to produce the same results as the IEEE PSRC model produces.

4.5.1 Comparison of the models

Waveform of the air-gap core CT model is compared with the IEEE PSRC CT model under various conditions by changing the fault current (I_f), the CT burden (R_b), and the CT remanence flux linkage (λ_{rem}). Figure 4-5 exhibits the first four cycles of the air-gap core CT model waveform and the IEEE PSRC waveform for a CT with $I_f = 70$ kA, $R_b = 2.5 \Omega$, and $\lambda_{rem} = 0.8$ pu.

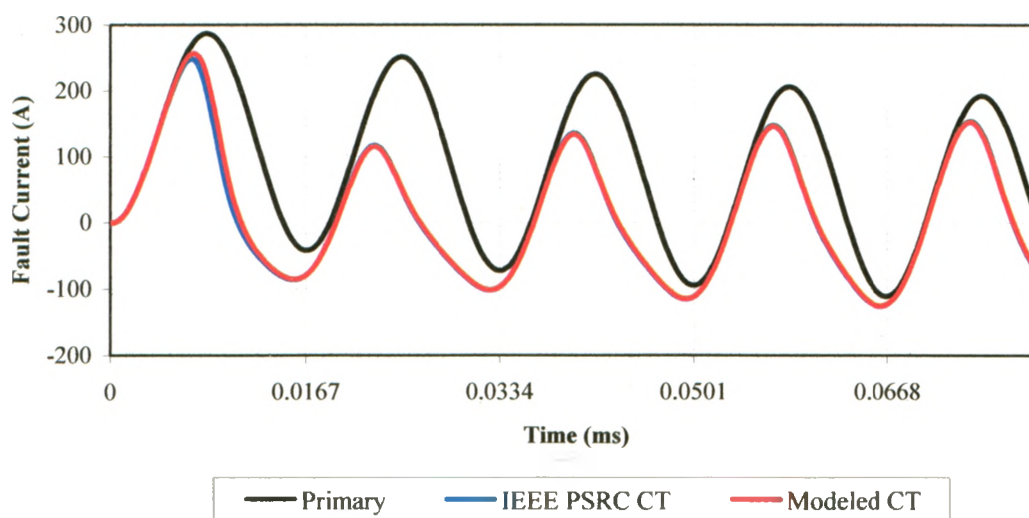


Figure 4-5 – Waveforms Comparison ($I_f = 70$ kA, $R_b = 2.5 \Omega$, and $\lambda_{rem} = 0.8$ pu)

As shown, both CTs saturate in the first cycle, and the level of saturation increases in the second and third cycles. As shown, the model waveform accurately replicates the IEEE PSRC model waveform. There is a small phase shift and magnitude difference between the waveforms which is discussed and quantified in Section 4.5.2.

Figure 4-6 compares the waveforms of the same CTs by applying a lower fault current (30 kA) to them.

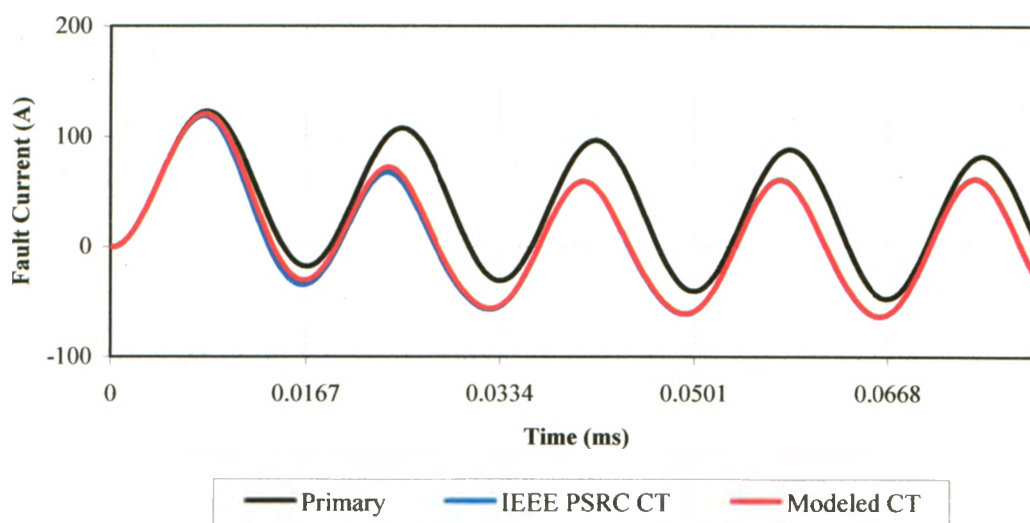


Figure 4-6 - Waveform Comparison ($I_f = 30 \text{ kA}$, $R_b = 2.5 \Omega$, and $\lambda_{rem} = 0.8 \text{ pu}$)

Since the fault current is reduced, the waveforms of the CTs in Figure 4-6 are not significantly distorted by the core saturation effect compared with those in Figure 4-5. In the first and second cycles, a small amount of phase shift and magnitude difference between the models is also noticeable.

4.5.2 Error Quantification

A comparison between the waveforms of the proposed model and the IEEE PSRC model for a solid-core CT indicates a small phase shift and magnitude difference between the models. These are quantified in Table 4.1 for various simulation configurations.

Table 4.1 – Phase Shift and Magnitude Error

Condition Number	Description	Phase Shift Error (ms)			Magnitude Error (% of the peak current)		
		First Cycle	Second Cycle	Third Cycle	First Cycle	Second Cycle	Third Cycle
1	If = 70 kA Rb = 5.0 Ω $\lambda_{rem} = 0.6$ pu	0.3	0.1	0.0	3.6%	2.3%	0.4%
2	If = 30 kA Rb = 5.0 Ω $\lambda_{rem} = 0.6$ pu	0.3	0.1	0.0	3.1	2.2	0.0%
3	If = 70 kA Rb = 2.5 Ω $\lambda_{rem} = 0.6$ pu	0.3	0.2	0.1	3.5%	2.1%	0.3%
4	If = 30 kA Rb = 2.5 Ω $\lambda_{rem} = 0.6$ pu	0.0	0.1	0.1	3.2	2.6	0.0%
5 No Saturation	If = 70 kA Rb = 0.5 Ω $\lambda_{rem} = 0.6$ pu	0.0	0.0	0.0	0.0%	0.0%	0.0%
6 No Saturation	If = 30 kA Rb = 0.5 Ω $\lambda_{rem} = 0.6$ pu	0.0	0.0	0.0	0.0%	0.0%	0.0%
7	If = 70 kA Rb = 5.0 Ω $\lambda_{rem} = 0.8$ pu	0.3	0.0	0.0	3.8%	2.3%	0.5%
8	If = 30 kA Rb = 5.0 Ω $\lambda_{rem} = 0.8$ pu	0.2	0.0	0.0	3.3	2.7	0.2%

Condition Number	Description	Phase Shift Error (ms)			Magnitude Error (% of the peak current)		
		First Cycle	Second Cycle	Third Cycle	First Cycle	Second Cycle	Third Cycle
9	If = 70 kA R _b = 2.5 Ω λ _{rem} = 0.8 pu	0.4	0.1	0.0	3.2%	2.0%	0.3%
10	If = 30 kA R _b = 2.5 Ω λ _{rem} = 0.8 pu	0.3	0.1	0.0	3.1	2.2	0.0%
11 No Saturation	If = 70 kA R _b = 0.5 Ω λ _{rem} = 0.8 pu	0.0	0.0	0.0	0.0%	0.0%	0.0%
12 No Saturation	If = 30 kA R _b = 0.5 Ω λ _{rem} = 0.8 pu	0.0	0.0	0.0	0.0%	0.0%	0.0%

As shown in Table 4.1, the maximum phase shift error is 0.4 ms, and maximum magnitude error is 3.8% of the peak current for the aforementioned simulation conditions. Although the errors are not critical, additional analysis is performed in Section 4.5.3.

4.5.3 Additional Analysis

As detailed in Section 3.4.1, protective relays estimate magnitude and phase angle of the signal in power system fundamental frequency (60 Hz), after digitizing the analogue input signal. The same exercise on the output waveforms of the proposed model and IEEE PSRC model can demonstrate importance of the phase shift and magnitude error, mentioned in Section 4.5.2.

Condition Number 7 of Table 4.1 has the maximum error between the output waveforms. This condition has a burden resistance (R_b) of 5.0 Ω, remanence flux linkage (λ_{rem}) of

0.8 pu, and fault current (I_f) of 70 kA. The output waveforms of both models were passed through a full cycle discrete Fourier algorithm in order to estimate the magnitude and phase angle of the signals in power frequency. Figure 4-7 shows magnitude and Figure 4-8 shows phase angle of both signals in power frequency.

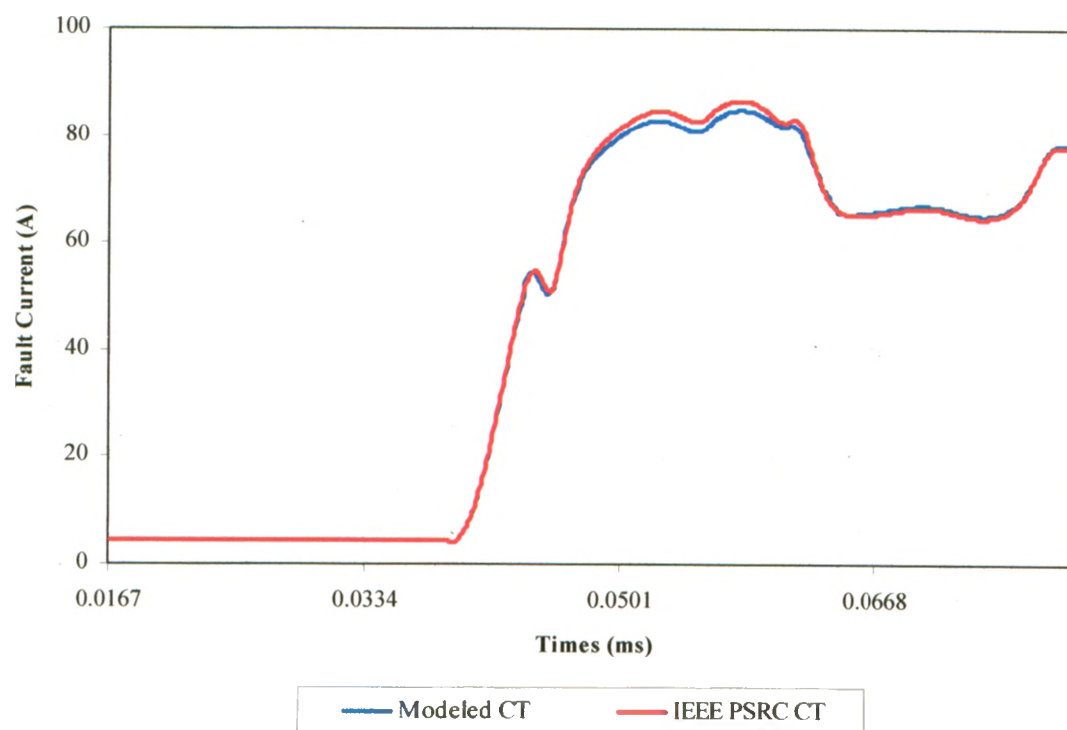


Figure 4-7 – Magnitude Estimation of the Output Signals Using District Fourier Algorithm

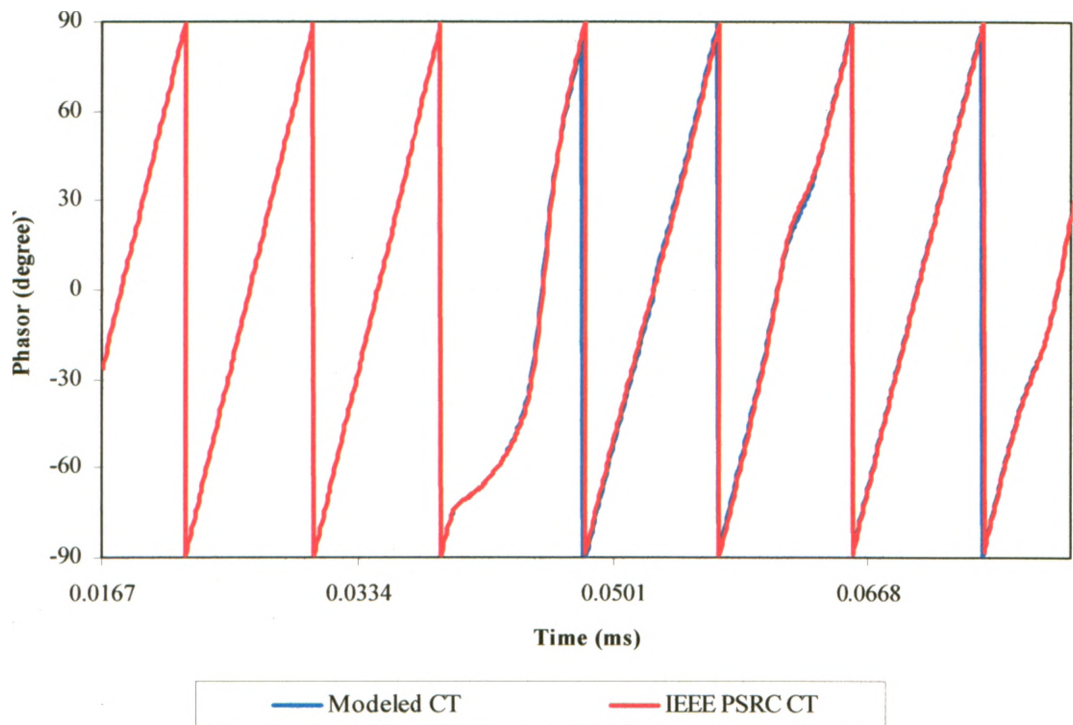


Figure 4-8 – Phase Angle Estimation of the Output Signals Using District Fourier Algorithm

As shown, a fault with condition of Test Number 7 of Table 4.1 is applied to both models after two cycles of pure sinusoidal current of 4.42 V. Some magnitude and phase angle differences appeared, 16 ms after applying the fault. Magnitude percentage difference and phase angle difference between the signals are shown in Figure 4-9 and Figure 4-10 respectively.

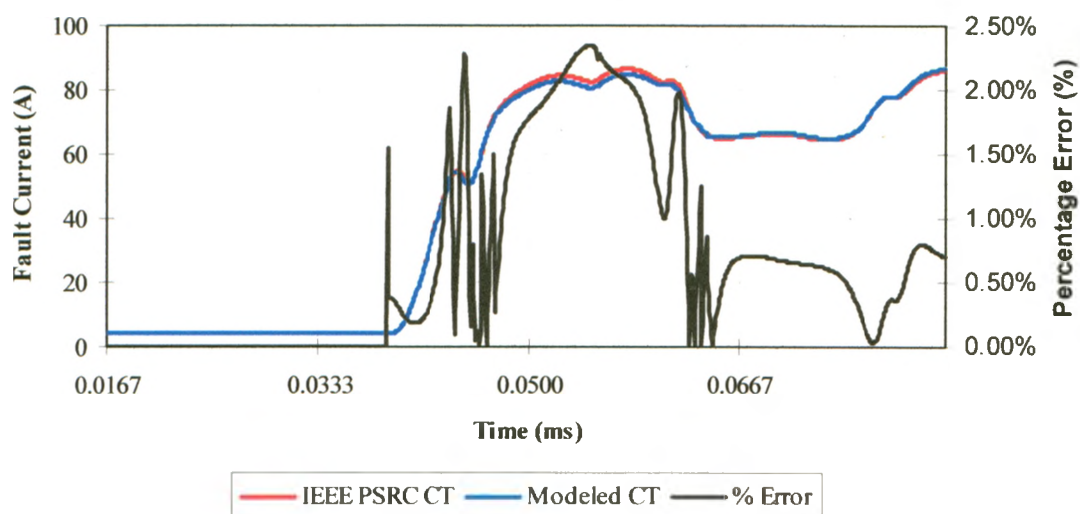


Figure 4-9 – Magnitude Difference of the Signals

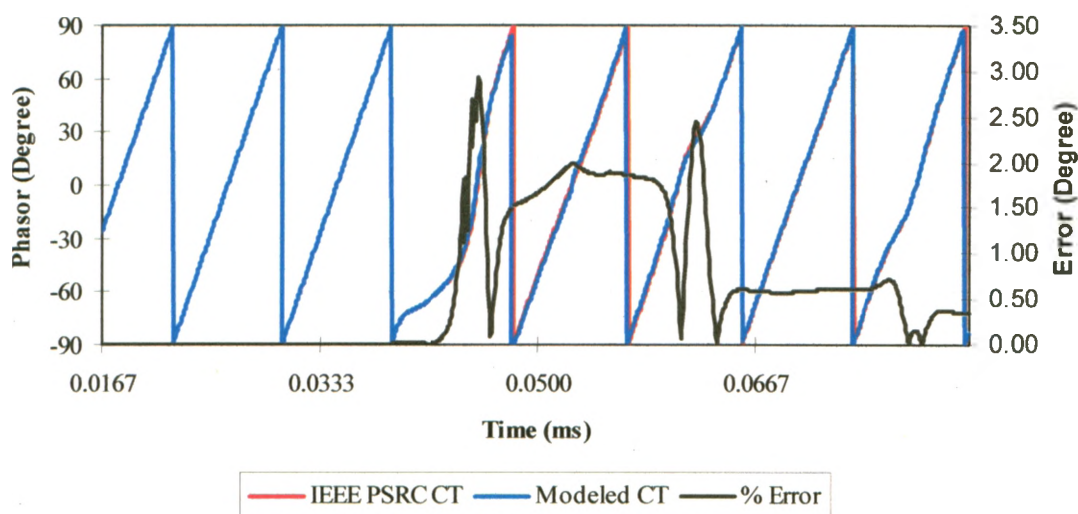


Figure 4-10 – Phase Angle Difference of the Signals

The maximum magnitude difference of 2.34% occurs 21 ms after the fault and the maximum phase angle error of 2.93° occurs 12 ms after the fault. These errors are less than the current transformer accuracy rating which calls for less than 10% error at any current from 1 to 20 times of secondary rated current.

4.6 Investigation of the Saturation Characteristic of a CT

Figure 4-11 and Figure 4-12 denote the sample results for the air-gap core and solid-core CTs with a burden resistance (R_b) of 2.5Ω , remanence flux linkage (λ_{rem}) of 0.6 pu, and fault current (I_f) of 70 kA. The black and red traces show the primary and CT output current, respectively, with the calculation parameters listed in Table 4.2.

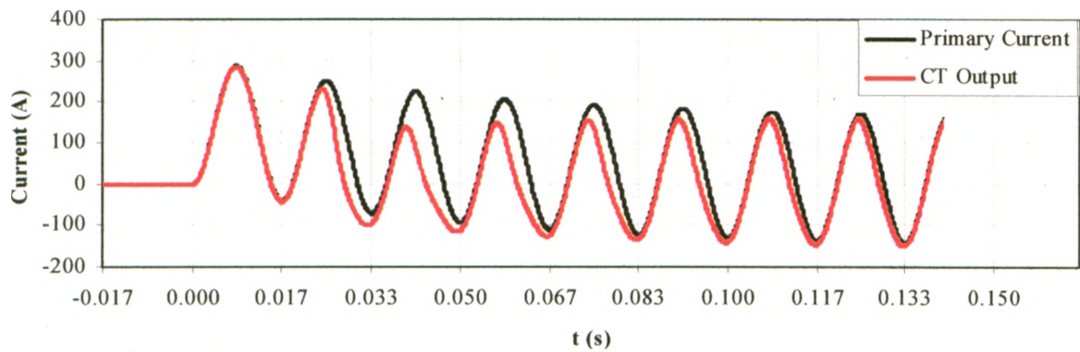


Figure 4-11 – Air Gap Core CT Waveform ($I_f = 70 \text{ kA}$, $R_b = 2.5 \Omega$, and $\lambda_{rem} = 0.6 \text{ pu}$)

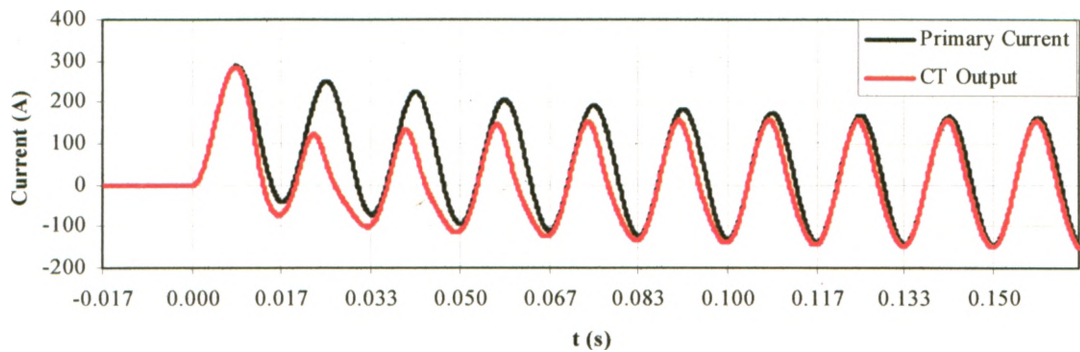


Figure 4-12 – Solid-core CT Waveform ($I_f = 70 \text{ kA}$, $R_b = 2.5 \Omega$, and $\lambda_{rem} = 0.6 \text{ pu}$)

Table 4.2 - CT Parameter Associated with Figure 4-11 and Figure 4-12

Parameters	Unit	Figure 4-11	Figure 4-12
S	-	22	22
V_s	V rms	3000	3000

Parameters	Unit	Figure 4-11	Figure 4-12
N	Turns	640	640
R _w	Ω	0.00	0.00
R _b	Ω	2.50	2.50
X _b	Ω	0.25	0.25
X/R	-	20	20
A ₀	-1 < off < 1	1	1
λ _{rem}	pu	0.60	0.60
μ _{core}	pu	3000	3000
r _{core}	mm	335	335
A _{core}	mm ²	6750	6750
S _{gap}	pu	0.0003	Solid-core
I _{hyst}	A peak	0.00	0.00
I _f	A rms	70E+03	70E+03
dt	s	8.3E-05	8.3E-05

Typically, protective relays make a tripping decision in the first one-and-a-half cycles. It is evident that the air-gap core CT does not saturate in this period of the time and helps the relay to make the proper decision. Also, the level of saturation is not as high as the one of the solid-core CT for the remaining cycles.

Figure 4-13 demonstrates waveform of the same air-gap core CT with higher burden. By comparing this figure with Figure 4-11 the level of saturation increases by increasing the burden resistance.

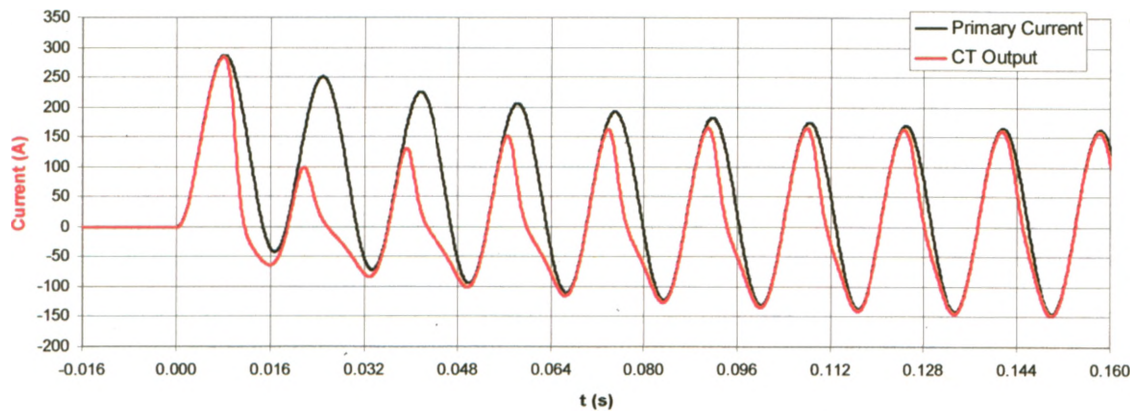


Figure 4-13 – Air-gap Core CT Waveform ($I_f = 70 \text{ kA}$, $R_p = 5.0 \Omega$, and $\lambda_{rem} = 0.6 \text{ pu}$)

Figure 4-14 reflects the effect of the burden on the first four cycles of the output waveform of the air-gap core CT.

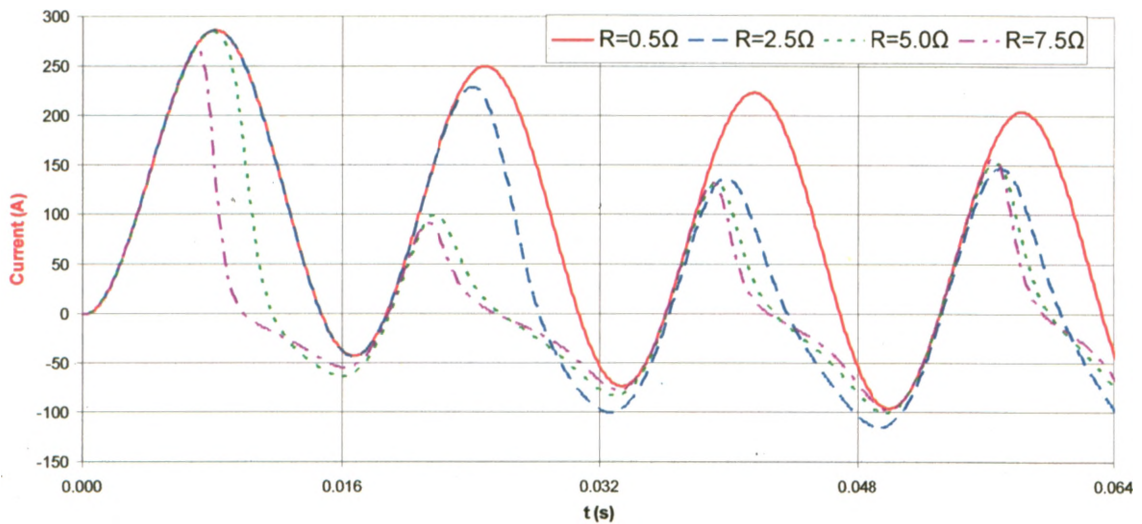


Figure 4-14 – Effect of the Burden on the Output Waveform of the Air-gap Core CT

This figure can be compared with Figure 4-15 which is prepared for the solid-core CT.

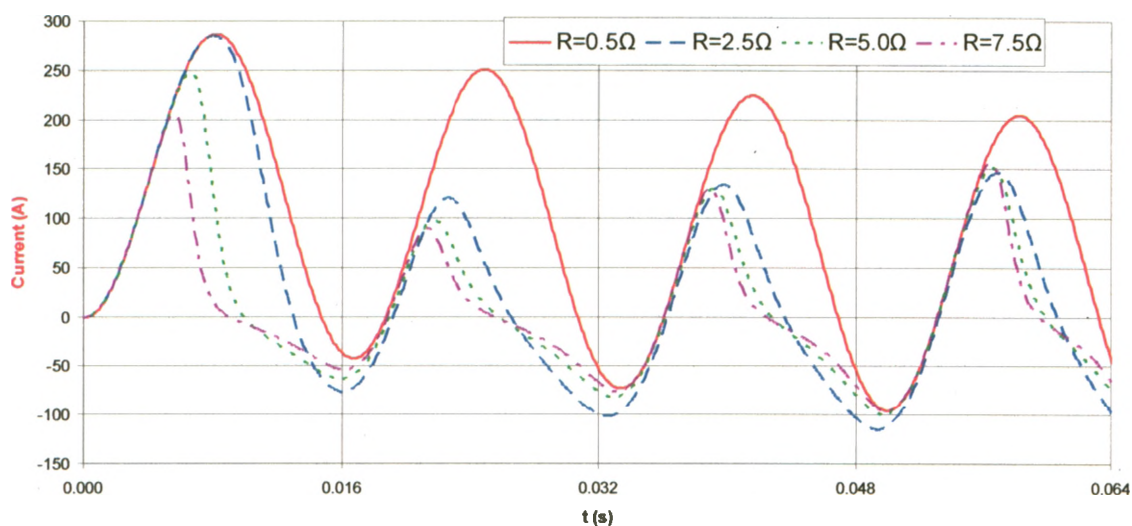


Figure 4-15 - Effect of the Burden on the Output Waveform of the Solid-core CT

4.7 Summary

Since electrical characteristics of the air-gap core CTs are not standardized, a novel model for the air-gap core CT is presented in this Chapter. This model can also produce the output waveform in a graphical format. This can be helped to visually study the level of saturation on the output current of the air-gap core CT. The proposed model is validated using the solid-core current transformer model, presented by the IEEE PSRC committee and the error between the output waveforms is quantified.

Then saturation characteristics of air-gap core and solid-core CT are investigated and the differences are studied with details in Section 4.6.

Chapter 5

5.0 TEST RESULTS

5.1 Introduction

Now that an air-gap core CT has been simulated and the CT secondary waveform is validated, the output waveform of the simulation can be re-configured to a common exchanging format. This format is understandable by the Real Time Digital Simulator (RTDS) and is injected into any protective relay. Two commercial busbar differential protection relays are chosen to study the operational differences, when the relays are connected to a solid-core and an air-gap core CT.

Section 5.2 describes the test setup, connection setup, and data representation. Section 5.3 presents scenarios that are tested on the two commercial differential relays to verify the performance differences of the two relays. Finally Sections 5.4 and 5.5 summarize the performance differences of Relay 1 and Relay 2, respectively.

5.2 Test setup

The setup of the RTDS power system model setup is illustrated in Figure 5-1. The direction of the current in this simulation is from left to right in a steady-state condition. In other words, the left-hand-side current transformer simulates the current entering the zone of protection, and the right-hand-side current transformer simulates the current leaving the zone of protection in a steady-state condition. Here, the input current to the zone of protection (I_{left}) is a clean sinusoidal waveform with no sign of saturation. The current leaving the zone of the protection (I_{right}) is obtained from either the solid-core or air-gap core CT simulator. This current can have different degrees of saturation, based on the parameters of the power system and the type of CT that is used. The IEEE PSRC

solid-core CT saturation calculator is used to simulate the current waveform of the solid-core CT and the air-gap core CT saturation calculator, introduced in Section 4.0, to simulate the waveform of the air-gap core CT.

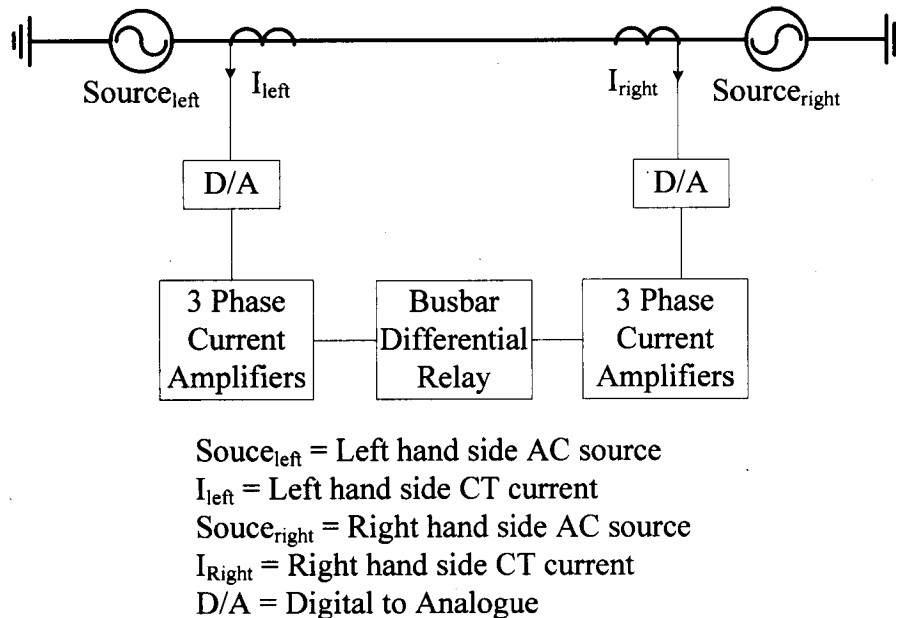


Figure 5-1 - Test Setup

5.2.1 Data representation

The COMTRADE format [11] is a common format for exchanging data files between computer and protective relays. This format is illustrated in Appendix A. In order to store current waveforms in the COMTRADE format, they are first extracted from the modeling spreadsheet and stored as Comma Separated Values (CSV). After this file is reformatted to COMTRADE, it is appropriate for the RTDS.

RTDS reads the COMTRADE files and provides a digital voltage waveform with the same shape. It is then transformed to analogue and injected into the amplifiers. To study operational differences of the two commercial differential relays when they are connected

to solid-core and air-gap core current transformers, the amplified current signals are then applied to the relays.

5.2.2 Connection to the relay

Usually, commercial relays have two ranges for the secondary analogue current inputs which are specified when the relay is ordered. These two current input values are 1 A or 5 A. The first commercial busbar differential protection relay, Relay 1, that was ordered for this study, has a secondary current input of 1 A; the second one, Relay 2, has a secondary current input of 5 A to test two typical secondary ranges.

Typically, busbar differential protection relays have inputs for a power system voltage connection. The voltage signal connection is not essential for this study. Although the aforementioned inputs are provided for the two chosen relays, none are used.

5.3 Tests

To study operation differences of the chosen relays, the following scenarios are simulated and tested on the relays.

- The dependability of the protection on the internal faults at low fault currents and high fault currents, with the right hand side current (I_{right}) in the saturation mode by using an air-gap core and solid-core CT simulator.
- The security of the protection for the external faults at low fault currents and at high fault currents with the right hand side current (I_{right}) in the saturation mode by using air-gap core and solid-core CT simulator.
- The dependability of the protection for an external fault evolving into an internal fault.

A number of cases are generated for these scenarios by changing the model parameters, listed in Table 5.1.

Table 5.1 – Model Parameters Change

Parameter	Change
Fault Current (I_f)	from 60 kA to 80 kA
X/R Ratio (X/R)	from 20 to 35
Burden Resistance (R_b)	from 5 Ω to 10 Ω
Burden Inductance (X_b)	0.1 * R_b

The other parameters, listed in Table 5.2, remain constant during the course of the tests:

Table 5.2 – Constant Model Parameters

Parameter	Change
B-H Characteristic Slope ($1/S$)	1/22 = 0.045
Saturation Voltage (V_s)	3000 V
CT Number of Turns (N)	640
Remanence Flux Linkage (λ_{rem})	0.75 pu
Core Permeability (μ_{core})	3000 pu
Core perimeter (r_{core})	335 mm
Core Cross Section Area (A_{core})	6750 mm ²
Gap Size (S_{gap})	0.003 pu

5.4 Testing of Relay 1

5.4.1 Differential characteristics

Relay 1 uses a dual-slope, dual-breakpoint operating characteristic to verify the location of the fault, and issue a tripping signal if the fault is in operation region, as demonstrated in Figure 5-2 [12].

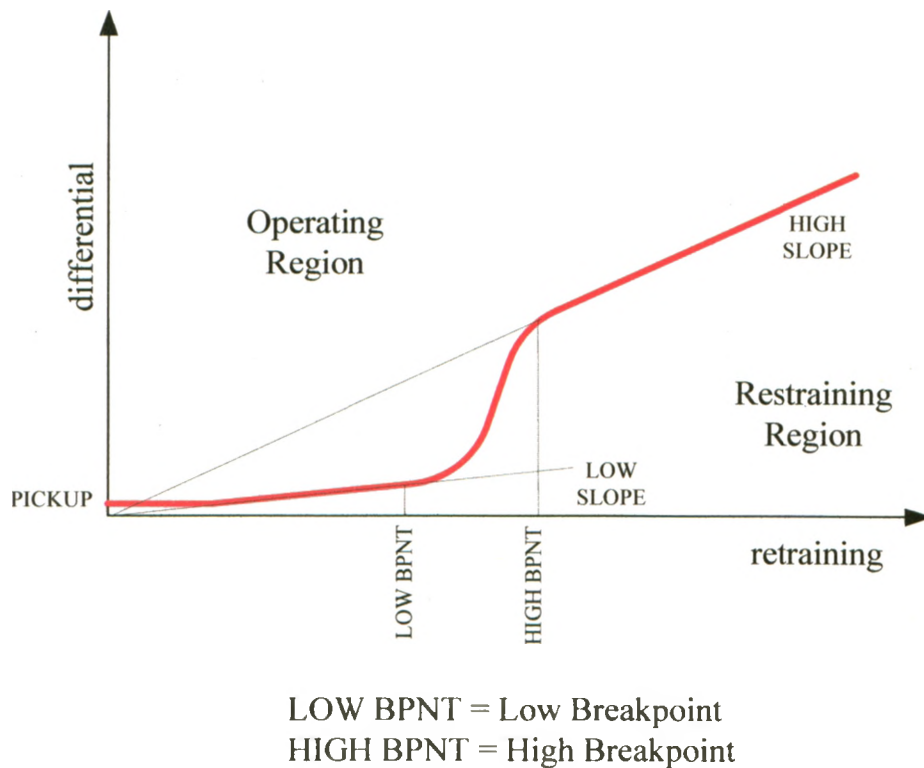


Figure 5-2 – Relay 1 Differential Operating Characteristic

The pickup setting is provided to cope with the spurious differential signals, when the bus carries a light load and there is no effective restraint current. The first breakpoint (**LOW BRNP**) is provided to specify the limit of the guaranteed linear operation of the CT in the most unfavorable conditions. These include high residual magnetism left in the magnetic cores. This point defines the upper limit for the application of the first slope. The second breakpoint (**HIGH BPNT**) is provided to specify the limits of operation of

the CT without substantial saturation. This point defines the lower limit for the application of the second slope.

The differential current is produced as a sum of the phasors of the input currents to a differential bus zone (Equation (3.1) of Section 3.1.3), and the restraint current is produced as a maximum of the magnitude of the phasors of the input currents to a differential bus zone (Equation (3.4) of Section 3.1.3).

5.4.2 Saturation detector

The saturation detector of Relay 1 takes advantage of the fact that any CT operates correctly for a short period of time even under strong primary currents that subsequently cause a severe saturation. As a result, the following is considered,

- In the case of an external fault, the differential current remains very low during the initial period of the linear operation of the CT, whereas the restraint signal develops rapidly. Once one or more CTs saturate, the differential current is built up.
- In case of an internal fault, both the differential and restraint currents increase simultaneously.

This creates characteristic patterns for the differential–restraint trajectory as depicted in Figure 5-3.

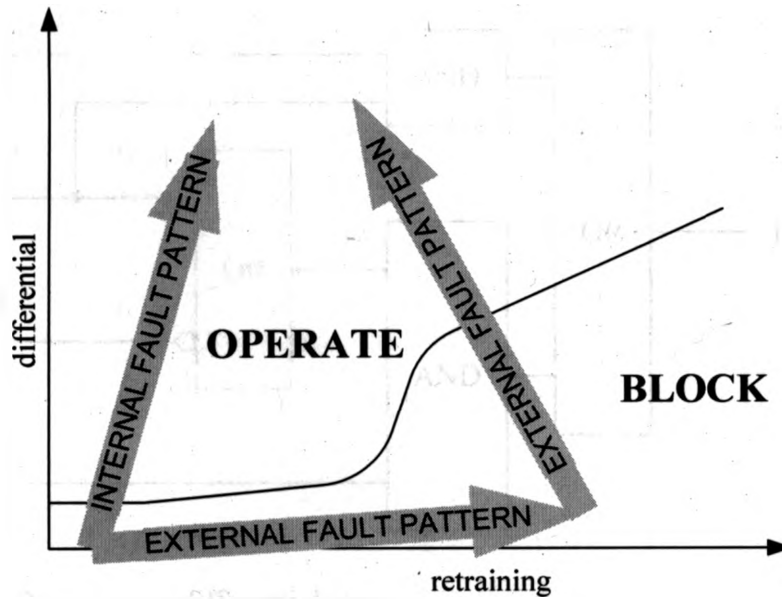
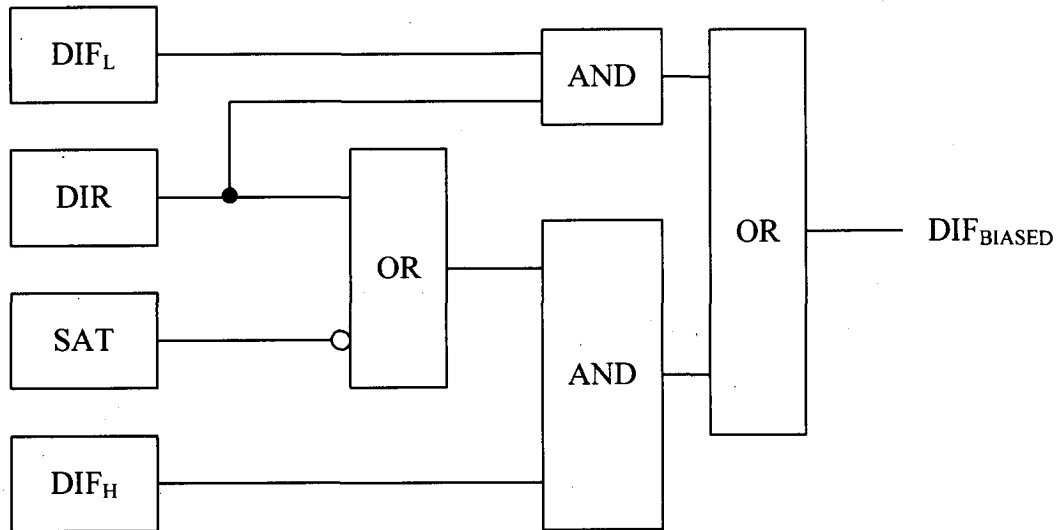


Figure 5-3 - CT Saturation Detection Patterns for Internal & External faults

The CT saturation condition is declared by the saturation detector, when the magnitude of the restraint signal becomes larger than the higher breakpoint and, at the same time, the differential current is below the first slope. The saturation detector is capable of detecting saturation, occurring approximately 2 ms into a fault.

The biased differential characteristic requires the output logic in Figure 5-4. For low differential signals, the biased differential element operates, when both the differential (**DIF_L**) and directional (**DIR**) functions pick up. For high differential signals, the biased differential element operates, when both the differential (**DIF_H**) and directional (**DIR**) functions pick up, or when the differential function (**DIF**) picks up, and the saturation function (**SAT**) does not detect any CT saturation. Typically the directional function is slower, so the relay gains speed by avoiding the use of this function when possible.



DIF_L = Low differential slope
 DIF_H = High differential slope
 SAT = Saturation detection logic
 DIR = Forward directional element
 DIF_{BIASED} = Biased bus differential pickup

Figure 5-4 - Output Logic of Biased Differential Protection

5.4.3 Relay setting

Bus Zone 1 Diff	Description	Setting
	Pickup	0.1 A
	Low Slope	30 %
	LOW BPNT	2
	High Slope	60 %
	HIGH BPNT	10

5.4.4 Test results of internal faults

The differential function operation time of Relay 1 due to an internal fault is measured the same for both the solid-core and air-gap core CTs. The recorded time is less than one

cycle (in the range of 8 to 12 ms), which is within the manufacturer's specification for Relay 1.

A number of internal fault scenarios are simulated by changing the fault current (I_f), X/R ratio (X/R), and burden impedance (R_b , $X_b = 0.1 \cdot R_b$) and injected the waveform to Relay 1. Table 5.3 summarizes result of these scenarios.

Table 5.3 – Differential Function Test Results of Relay 1 for Internal Fault Scenarios

Scenario Number	Description	Trip Time with Solid-core CT (ms)	Trip Time with Air-gapped Core CT (ms)
1	$I_f = 80\text{kA}$, X/R = 22, $R_b = 1\Omega$	8	8
2	$I_f = 80\text{kA}$, X/R = 22, $R_b = 3\Omega$	8	8
3	$I_f = 80\text{kA}$, X/R = 22, $R_b = 5\Omega$	8	8
4	$I_f = 60\text{kA}$, X/R = 32, $R_b = 3\Omega$	9	10
5	$I_f = 40\text{kA}$, X/R = 32, $R_b = 3\Omega$	10	10
6	$I_f = 40\text{kA}$, X/R = 22, $R_b = 3\Omega$	12	12

5.4.5 Test results of external faults

The Performance of the differential function due to an external fault depends on high breakpoint setting (**HIGH BNPT**). This setting controls the CT saturation detector element (**SAT**) which blocks the biased differential function of the relay to operate on the external faults. The pickup time of the CT saturation detector element, due to an external fault, is measured in the range of 4 to 12 ms for both the air-gap core and solid-core CTs. However, the biased differential function of the relay is incorrectly picked up after 13 to 40 ms for both CTs because of the saturation effect. However, the relay operation is blocked by the CT saturation detection logic (**SAT**).

Figure 5-5 shows the CT saturation detection logic (**SAT**) and biased differential function pickup (**BIASED PKP**) of the differential function for a 80 kA external fault with a solid-core CT. As shown, the biased differential function incorrectly operates after 14 ms. This incorrect operation does not operate the differential function because the CT saturation detection logic (**SAT**) picked up at 6 ms and blocked the operation of the differential function. In Figure 5-5, only the signals that change the state are indicated.

Figure 5-6 portrays CT saturation detection logic (**SAT**) and biased differential function pickup (**BIASED PKP**) of the differential function for a 80 kA external fault with an air-gap core CT. It is evident that the biased differential function incorrectly operates after 36 ms. This incorrect operation does not operate the differential function, because the CT saturation detection logic (**SAT**) picks up at 6 ms and blocks the operation of the differential function. In Figure 5-6, only the signals that changes the state are included.

Although there is no difference in the operation of the differential function between the solid-core and air-gap core CTs, the biased element pickup time differs for both cases. This confirms that the CT saturation detection logic does not need to be set very sensitive to saturation in the case of having an air-gap core CT in the power system.

Figure 5-7 show the CT saturation detection logic (**SAT**) and biased differential function pickup (**BIASED PKP**) of the differential function for a 60 kA external fault with a solid-core CT. The biased differential function incorrectly operates after 13 ms. This incorrect operation does not operate the differential function, because the CT saturation detection logic picks up 1 ms before that and blockes the operation of the differential function. In this figure, only the signals that change the state are given.

Figure 5-8 displays CT saturation detection logic (**SAT**) and biased differential function pickup (**BIASED PKP**) of the differential element for a 60 kA external fault with an air-gap core CT. it is evident that the biased operation incorrectly operates after 36 ms. In this case, the CT saturation detection logic picks up after 26 ms and blocks the

differential function operation. In Figure 5-8, only the signals that change the state are denoted.

Although there is no difference in the operation of the differential function between the solid-core and air-gap core CTs, the CT saturation detection logic behaves differently in the two cases.

5.4.6 Test results of evolving faults

In the case of an external fault with a CT saturation, the CT saturation detection logic (**SAT**) picks up quickly. This element blocks the differential function to trip even if the biased differential function picks up incorrectly. If the external fault evolves to an internal fault, the biased element should wait for the forward directional element (**DIR**) to pickup in order to trip the circuit due to a differential protection operation. The forward directional element (**DIR**) of Relay 1 is not a fast element, and results in a slow operation for the evolving fault.

Figure 5-9 shows Relay 1's event recorder for a 60 kA external fault with solid-core CT. This fault evolves into an internal fault 32 ms (two cycles). It should be noted that the operation of the differential function is blocked by the CT saturation detection logic (**SAT**) for the external fault. It takes about 43 ms for the forward directional element (**DIR**) to detect the internal fault and triggers the biased element of the differential function.

Figure 5-10 shows Relay 1's event recorder for a 60 kA external fault which evolves into an internal fault after 32 ms (two cycles). In this case the relay is connected to the air-gap core CT. As observed, the CT saturation detection logic (**SAT**) does not pickup. In this case, biased element does not need a forward directional element (**DIR**) confirmation to operate, and can trip the circuit as soon as the fault evolves. This confirms the fact that Relay 1 reacts fast (in the range of 20 to 26 ms) for the evolving faults if it is used with the air-gap core CT and reacts slower (in the range of 40 to 46 ms) if it is used with the solid-core CT.

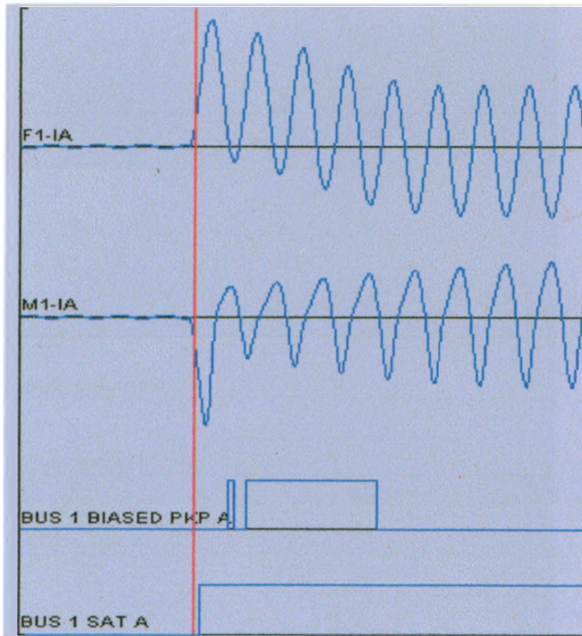


Figure 5-5 - Differential Element Pickup for a Solid-core CT (fault current: 80kA, X/R: 32, CT burden: 3 Ω , remanence: 75%)

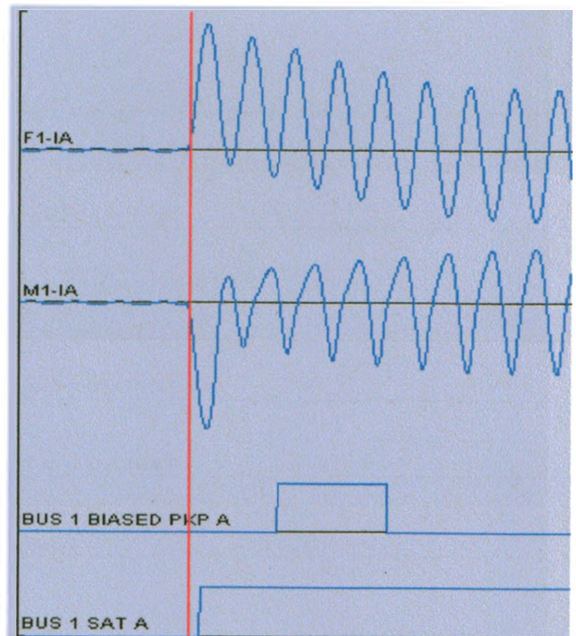


Figure 5-6 - Differential Element Pickup for an Air-gap Core CT (fault current: 80kA, X/R: 32, CT burden: 3 Ω)

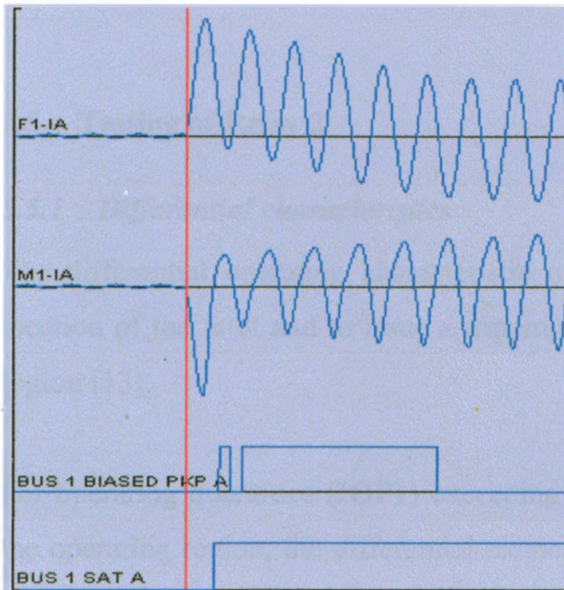


Figure 5-7 - Differential Element Pickup for a Solid-core CT (fault current: 60 kA, X/R: 35, CT burden: 3 Ω , remanence: 75%)

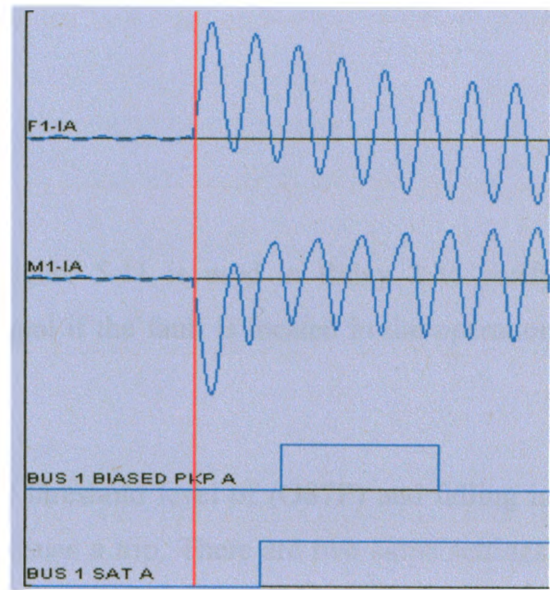


Figure 5-8 - Differential Element Pickup for an Air-gap Core CT (fault current: 60 kA, X/R: 35, CT burden: 3 Ω)

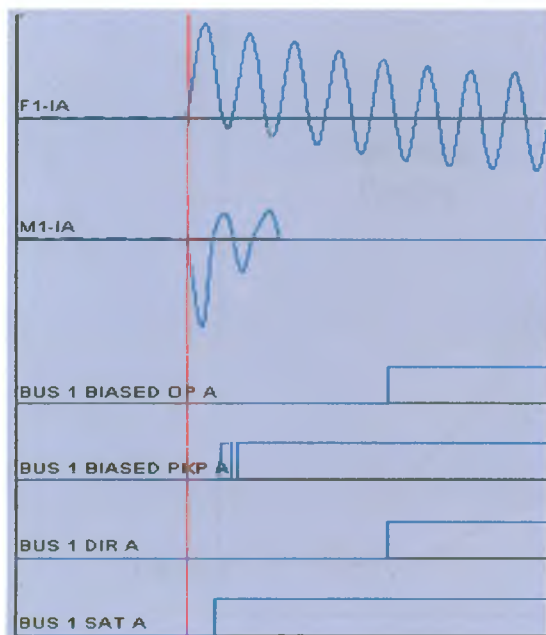


Figure 5-9 - Differential Element Pickup for a Solid-core CT (fault current: 60 kA, X/R: 35, CT burden: 3 Ω , remanence: 75%)

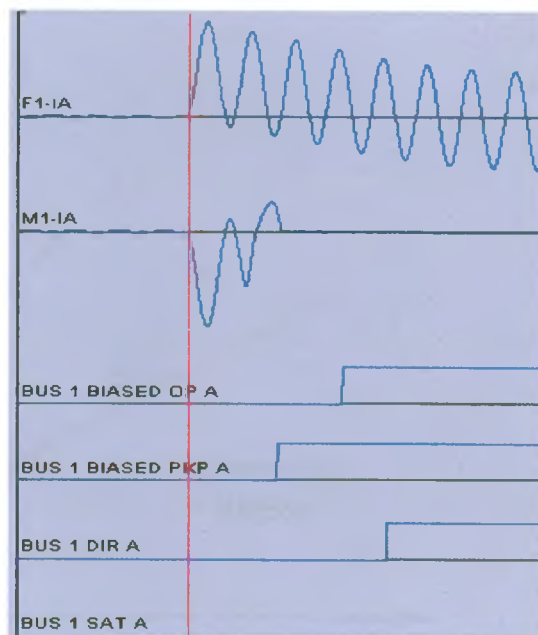


Figure 5-10 - Differential Element Pickup for an Air-gap Core CT (fault current: 60 kA, X/R: 35, CT burden: 3 Ω , gap size: 0.0003 pu)

5.5 Testing of Relay 2

5.5.1 Differential characteristics

The differential operating characteristic of Figure 5-11 is used in Relay 2 to verify location of the fault and to issue a tripping signal if the fault is located in the operation region [13].

For operating quantities (**IOPI**) exceeding the threshold level of (**O87P**) and falling in the operating region, the differential element issues a trip. There are two slope settings. Slope 1 (**SLP1**) is enabled for the internal faults, and slope 2 (**SLP2**) is enabled for the external faults. When the fault detection logic identifies an external fault condition, Relay 2 dynamically switches the slope of the differential characteristic from Slope 1 (**SLP1**) to Slope 2 (**SLP2**) to add security to the differential element of the relay.

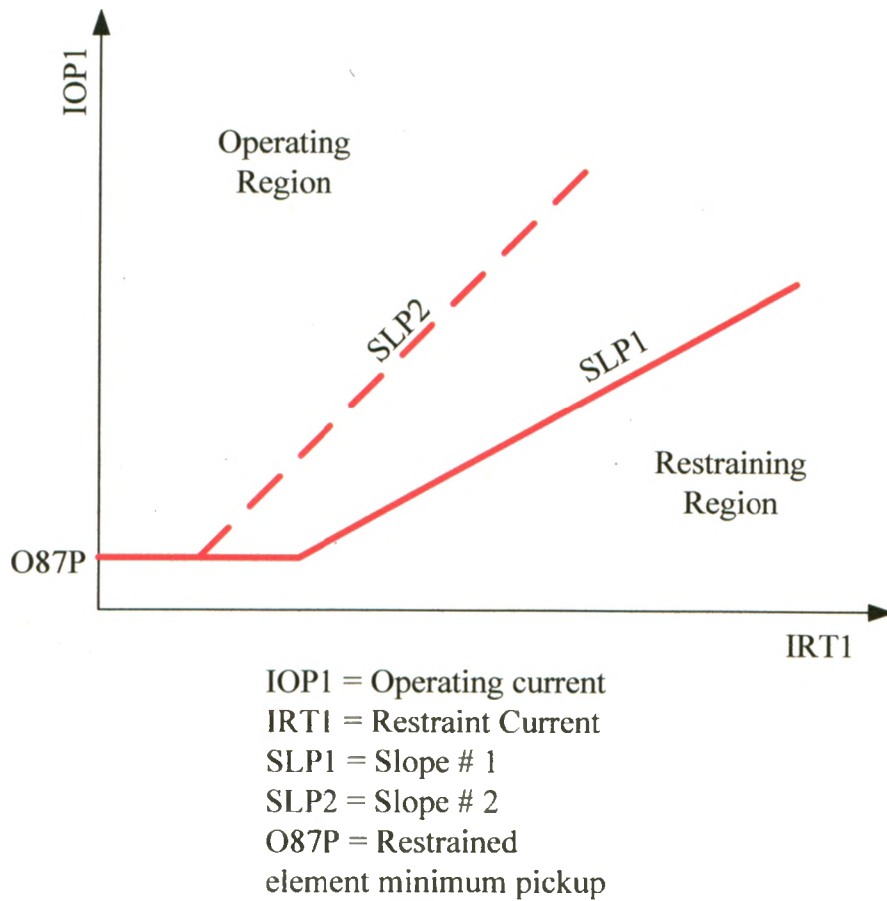


Figure 5-11 – Relay 2 Differential Operating Characteristic

The differential element calculates the restraint current and operating current quantities according to Equations (5.1) and (5.2).

$$I_{res} = |I_{left}| + |I_{right}|, \quad (5.1)$$

$$I_{op} = |I_{left} + I_{right}|, \quad (5.2)$$

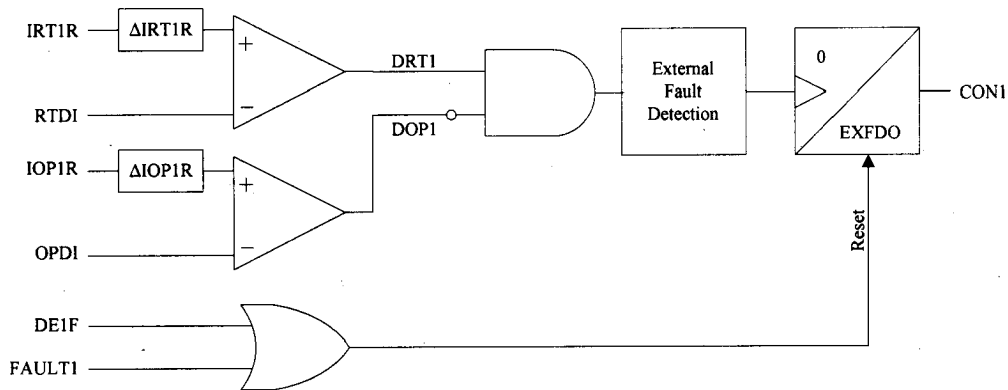
where

I_{left} = left-hand-side current according to Figure 5-1

I_{right} = right-hand-side current according to Figure 5-1

5.5.2 Saturation detection logic

Relay 2 takes advantage of the phenomenon of the fact that the operating and restraint current increase simultaneously for an internal fault, but only the restraint current increases for an external fault, if there is no CT saturation. By comparing the change in the operating current ($\Delta IOP1R$) to the change in the restraint current ($\Delta IRT1R$), the relay detects external fault conditions (**CON1**). Because CTs can saturate during the external faults, the relay asserts the external fault condition (**CON1**) for 60 cycles after an external fault, which blocks the differential function of the relay, is detected. Figure 5-12 denotes the logic for the external fault condition detection.



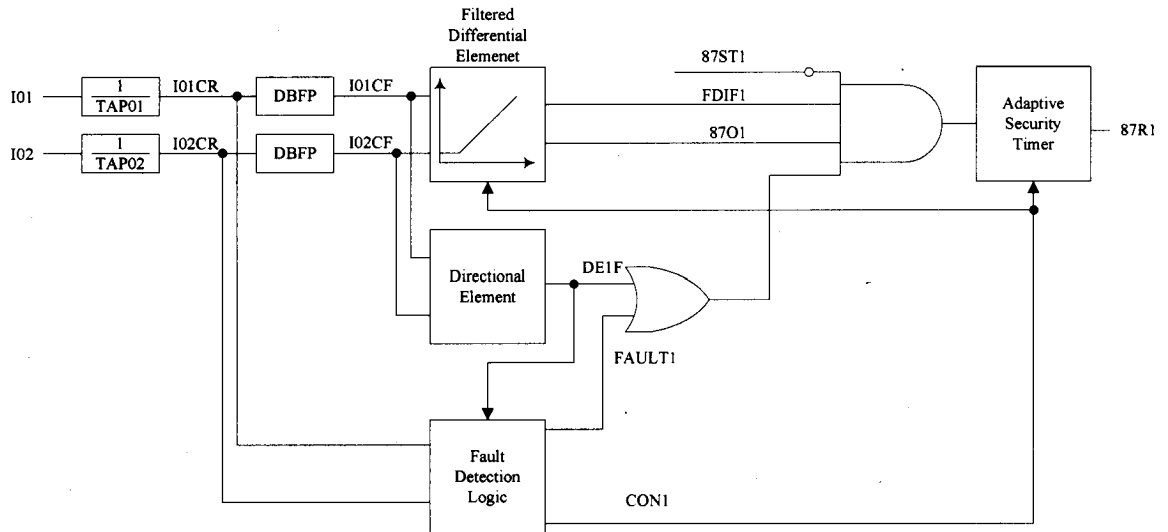
IRT1R = Restraint current
 $\Delta IRT1R$ = Change in restraint current
 IOP1R = Operating current
 $\Delta IOP1R$ = Change in operating current
 RTDI = Incr. restrained current threshold
 OPDI = Incr. operating current threshold

DE1F = Forward directional element pickup
 FAULT1 = Internal fault detection logic
 DRT1 = Incr. restraint current pickup
 DOP1 = Incr. operating current pickup
 CON1 = External fault condition
 EXFDO = Timer setting

Figure 5-12 – Relay 2 External Fault Detection Logic

Asserting the external fault condition (**CON1**) for 60 cycles can slow the Relay 2 operation for evolving faults. To prevent delayed tripping, **CON1** resets when either the forward directional element (**DE1F**) detects an evolving fault or the internal fault detection logic (**FAULT1**) confirms an internal fault condition.

Figure 5-13 is block diagram of the differential function for Relay 2.



I01 = Current in ampere for terminal 01
 I01CR = Current in per unit for terminal 01
 TAP01 = Tap value for terminal 01
 I01CF = Filtered per unit current value for terminal 01
 I02 = Current in ampere for terminal 02
 I02CR = Current in per unit for terminal 02
 TAP02 = Tap value for terminal 02
 I02CF = Filtered per unit current value for terminal 02
 DBFP = Digital band-pass filter

DEIF = Forward directional element pickup
 FAULT1 = Internal fault detection logic
 CON1 = External fault condition
 FDIF1 = Output of the differential calculation
 87ST1 = Sensitive differential element time out
 O87P = Differential element minimum pickup
 87O1 = Restraint differential operating current above O87P
 87R1 = Restraint differential element pickup

Figure 5-13 - Output Logic of Differential Protection

After the per unit conversion, the data follows two separate paths. One path is through a digital band-pass filter to the filtered differential element and the directional element; the other path leads the instantaneous values to the fault detection logic.

The filtered differential element uses the input currents from each terminal in the protection zone to calculate operate and restraint currents. The directional element compares the direction of the current at a reference terminal to the direction of current at all the other terminals in a protection zone to calculate the fault direction. Several elements combine in the fault detection logic to distinguish between the internal or

busbar fault condition (**FAULT1**), and external fault condition (**CON1**), described by Figure 5-12.

5.5.3 Relay setting

Bus Zone 1 Diff	Description	Setting
	Pickup (O87P)	0.1 A
	Low Slope (SLP1)	30 %
	High Slope (SLP2)	60 %
	Increased rate of restraint current threshold (RTD1)	2.0 pu
	Increased rate of operating current threshold (OPD1)	0.3 pu

The increased rate of the restraint current threshold (**RTD1**) and increased rate of operating current threshold (**OPD1**) are complicated settings, and the values are recommended by the manufacturer.

5.5.4 Test results of internal faults

The differential function operation time of Relay 2 due to an internal fault, is measured the same for both the solid-core and air-gap core CT. The recorded time is less than one cycle (in the range of 4 to 10 ms) which is within the manufacturer's specification for Relay 2.

A number of different internal fault scenarios are simulated by changing the fault current (I_f), X/R ratio (X/R) and burden impedance (R_b , $X_b = 0.1 \cdot R_b$), and are injected to Relay 2. Table 5.4 summarizes result of these scenarios.

Table 5.4 – Differential Function Test Results of Relay 2 for Internal Fault Scenarios

Scenario Number	Description	Trip Time with Solid-core CT (ms)	Trip Time with Air-gap Core CT (ms)
1	$I_f = 80\text{kA}$, $X/R = 22$, $R_b = 1\Omega$	4	5
2	$I_f = 80\text{kA}$, $X/R = 22$, $R_b = 3\Omega$	4	4
3	$I_f = 80\text{kA}$, $X/R = 22$, $R_b = 5\Omega$	4	4
4	$I_f = 60\text{kA}$, $X/R = 32$, $R_b = 3\Omega$	8	8
5	$I_f = 40\text{kA}$, $X/R = 32$, $R_b = 3\Omega$	10	10
6	$I_f = 40\text{kA}$, $X/R = 22$, $R_b = 3\Omega$	10	10

5.5.5 Test results of external faults

As mentioned before, CT saturation detection logic of Relay 2 relies on the declaration of an external fault. External fault declaration can be checked by monitoring the rate of change of the restraint current versus the rate of the change of the operating current. Since the CT saturation can occur only if there is an external fault, the relay then blocks the differential tripping circuit for a limited time. This time can be reset by the other elements, discussed in Section 5.5.2.

Figure 5-14 signifies word bit output of Relay 2 for a 60 kA fault current with a solid-core current transformer. The increment operating current pickup (**DOP1**) is set to high value, 0.4 ms before the increment restraint current pickup (**DRT1**). Although this is an external fault simulation, the configuration does not set the external fault condition (**CON1**) of the relay. Since the output of the differential calculation (**FDIF1**) is already high and the restrained differential operating current is above the differential element minimum pickup (**O87P**), the relay incorrectly issues a trip signal for an external fault.

Figure 5-15 shows the word bit output of Relay 2 for the same fault current (60 kA), but the relay is connected to an air-gap core current transformer. As expected, the increment restraint current pickup (**DRT1**) operates 1.2 ms before the increment operating current pickup (**DOP1**) at 8.0 ms. This configuration is sensed by the relay as an external fault and flags an external fault condition (**CON1**) at 8.0 ms. As mentioned before, **CON1** blocks the differential function operation of the relay for a limited time. Therefore, the relay correctly does not trip due to an external fault.

The results of the tests and several other external fault tests with different fault currents and X over R ratios confirm that using an air-gap core CT renders the differential function of Relay 2 less sensitive to the relay setting.

5.5.6 Test results of evolving faults

As indicated in Section 5.5.2, if the CT saturation detection logic of the relay detects an external fault, the relay blocks the differential function for a limited time (60 cycles). But, if the fault evolves into an internal fault, the relay can sense this situation by either the internal fault detection logic (**FAULT1**) or the forward directional element (**DE1F**), and release the differential function for the operation.

Figure 5-16 reflects the word bit outputs of Relay 2 for an 80 kA fault current with a solid-core current transformer. As expected, the increment restraint current pickup (**DRT1**) changed the state at 8.6 ms and set the external fault condition (**CON1**) to high position. This condition blocks the relay while the external fault exists. When the fault evolves into the zone of protection after 32 ms, the internal fault detection logic (**FAULT1**) recognizes the internal fault condition after 50.6 ms and trips the relay due to an internal fault.

Figure 5-17 exhibits the word bit outputs of Relay 2 for the same fault current (80 kA) but the relay is connected to an air-gap core CT. The same as the fault with the solid-core CT, the increment restrained current pickup (**DRT1**) changed the state at 7.6 ms, and sets the external fault condition (**CON1**) to high position. This blocks the differential function

for the period of the external fault. When the fault evolves into the zone of protection after 32 ms, the internal fault detection logic (**FAULT1**) recognizes the internal fault condition after 49.6 ms and trips the relay due to an internal fault.

The results on these tests and several other evolving fault tests with different fault current and X/R ratios confirm that there is no operational difference between solid-core and air-gap core CTs due to an evolving fault.

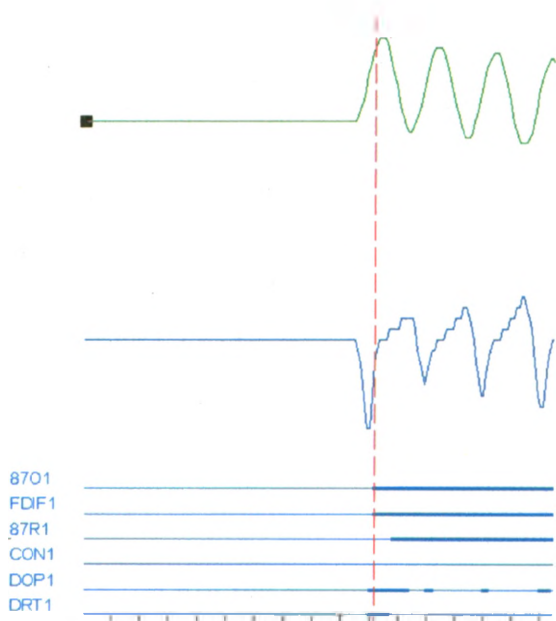


Figure 5-14 - Differential Word Bit Pickup for a Solid-core CT (fault current: 60kA, X/R: 35, CT burden: 10Ω, remanence: 75%)

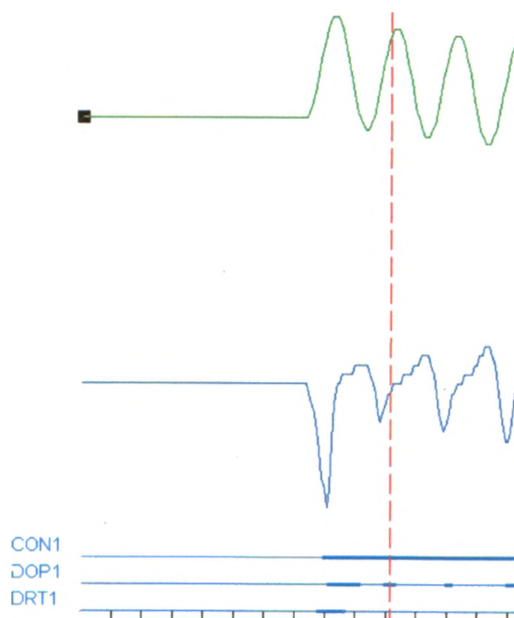


Figure 5-15 - Differential Word Bit pickup for an Air-gap Core CT (fault current: 60kA, X/R: 35, CT burden: 10Ω, gap size: 0.0003 pu)

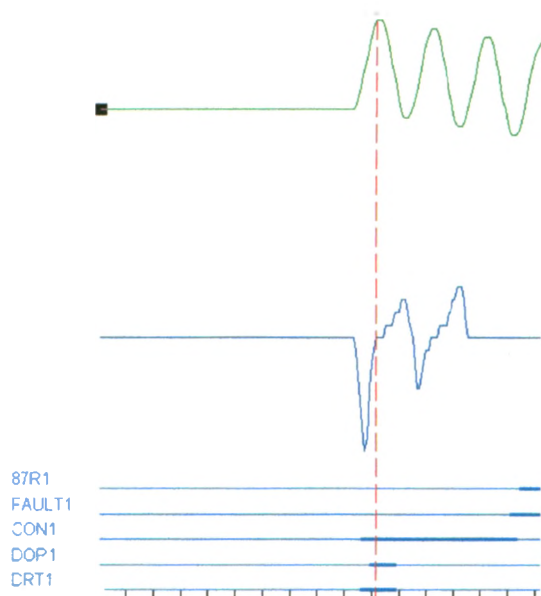


Figure 5-16 - Differential word Bit Pickup for a Solid-core CT (fault current: 80kA, X/R: 32, CT burden: 10 Ω , remanence: 75%)

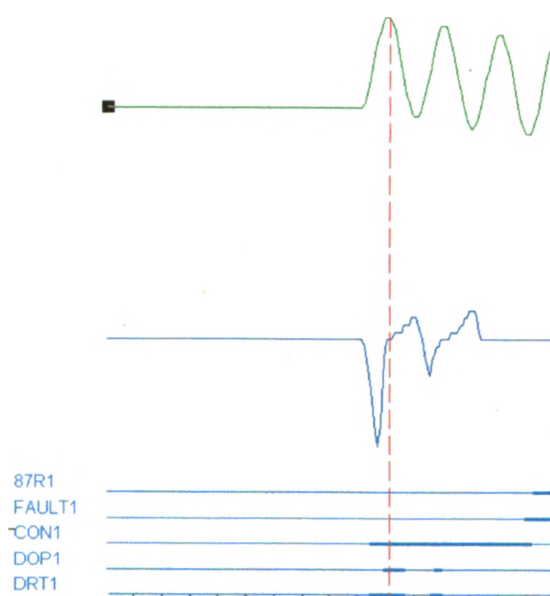


Figure 5-17 - Differential Word Bit Pickup for an Air-gap Core CT (fault current: 80kA, X/R: 32, CT burden: 10 Ω , gap size: 0.0003 pu)

5.6 Analysis of the Result

The differential function operation differences of the two busbar relays when they are connected to the air-gap core and solid-core CT are summarized in Table 5.5

Table 5.5 – Differential Function Operational Differences

Scenario	Differential Function Operational Differences	
	Relay 1	Relay 2
Internal fault	No difference in operation time	No difference in operation time

Scenario	Differential Function Operational Differences	
	Relay 1	Relay 2
External Fault	<p>No Difference in operation time</p> <p>CT saturation detection logic does not need to be set very sensitive for an air-gap core CT</p>	<p>No Difference in operation time</p> <p>Relay with connection to solid-core CT might mal-operate in some conditions</p>
Evolving Fault	<p>Relay with connection to air-gap core CT reacts about 20 ms faster than the relay connected to solid-core CT</p>	<p>No difference in operation time</p>

As tabulated, there are differences between differential function operation of Relay 1 and Relay 2. These differences are caused by dissimilar CT saturation detection algorithm of each relay. Generic differential relay algorithm is exhibited in Figure 5-18

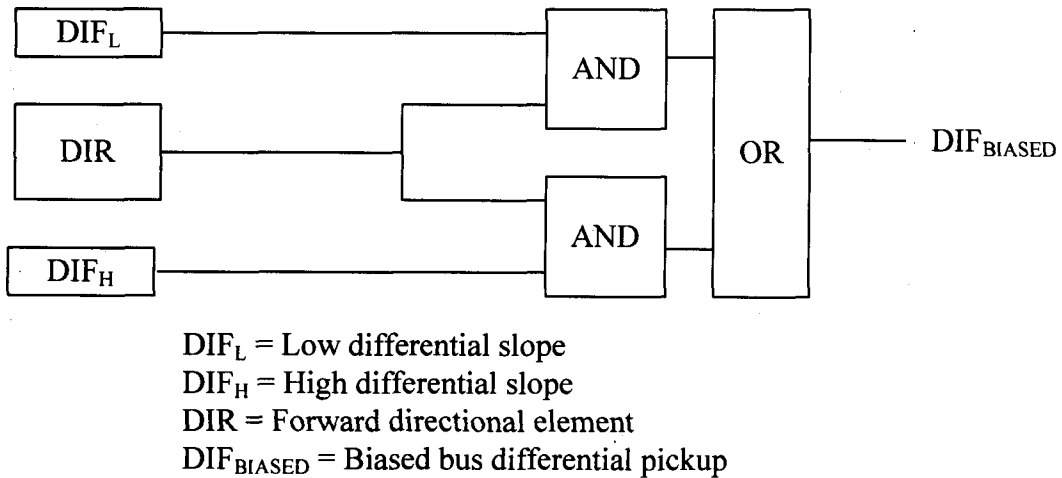


Figure 5-18 – Output Logic of Generic Biased Differential Protection

As shown, the logic does not include the CT saturation detection algorithm. Operational performance of the tested relays when they are connected to air-gap core or solid-core CTs are by far better than operational performance of generic differential function.

5.7 Summary

Solid-core and air-gap core CTs' output waveforms are transformed into the COMTRADE format. Two busbar differential protection relays are tested by using solid-core and air-gap core CTs. Real Time Digital Simulator (RTDS) is used to inject the COMTRADE files into the relays. Extensive testing shows that using an air-gap core CT makes the trip output less sensitive to the relay setting.

The out put logic of generic differential function does not include the CT saturation detection algorithm. Operational performance of the tested relays when they are connected to air-gap core or solid-core CTs are by far better than operational performance of generic differential function.

Chapter 6

6.0 SUMMARY AND CONCLUSIONS

Current transformers have been around for as long as power systems have existed. CTs are a necessary part of any viable power system for both protection and metering applications. Current transformers form the basis for providing a manageable size of secondary current to reflect the high current magnitudes found in power system operation and even the higher currents found under abnormal, or fault conditions. Many types of current transformers are available on the market. The two that this thesis focuses on are solid-core current transformers and air-gap core current transformers. Solid-core current transformers do not replicate the system current for a high magnitude fault current because of core saturation. Air-gap core CTs are introduced to the market because of their ability to reproduce the system current even in high fault currents. The core of this type of current transformer consists of an air gap which prevents CT saturation in high fault currents. Also, air-gap core CTs provide a number of advantages over solid-core CTs. However, air-gap core CTs are somewhat more expensive.

Nowadays, Intelligent Electrical Devices (IEDs) are being used as protective relays. Relay manufacturers can cleverly program the IEDs in order to sense a saturated waveform, produced by a current transformer. Then the relay is conducive to a correct tripping decision, based on its unique saturation detection algorithm. Moreover, IEDs internal components can also reduce the effect of CT saturation. Consequently, extensive usage of air-gap core current transformers are being questioned.

This thesis proposes an easy to use, mathematical, model of an air-gap core current transformer to compare the performance of microprocessor-based busbar differential relays when the input current is produced by solid-core and air-gap core CTs.

An introduction to current transformer basic modeling and differential protection concept are presented in the second and third chapters of this thesis, respectively. In Chapter four a novel model for air-gap core CT is presented and validated. The CT model is validated by considering no air-gap in the proposed model and comparing the output waveform of the model with that of the solid-core CT model, presented by the IEEE PSRC committee. The waveform comparison between the proposed model and an actual air-gap core CT is recommended as a future work. This comparison requires availability an air-gap core CT and its testing in a laboratory.

The performance of two commercial busbar differential protection relays, where the current is supplied by solid-core and air-gap core CT are documented in Chapter five. This is achieved by converting waveform data to the COMTRADE format and injecting them to the relay using Real Time Digital Simulator (RTDS) and amplifiers.

Extensive testing of the two commercial busbar differential protection relays shows the following:

- There is no difference in the relays' performances for internal faults.
- For an external fault, an air-gap core CT renders the trip output less sensitive to the relay setting.
- The relay might be considerably slow in operation for an evolving fault, if a solid-core CT is involved.

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Appendixes

APPENDIXES

Appendix A) Real Time Digital Simulator (RTDS)

The traditional way of performing transient testing involves simulators, consisting of scaled-down power system components. They are connected to each other in the same way that they are connected in a real power system. This simulation technique forms the basis of both the Transient Network Analyzer (TNA) for ac systems and the HVDC analogue simulator.

The second method of simulation is based on the detailed computational models of power system components by using well-known transient modeling software. To interactively test a physical protective relay, the software must operate in real time. This implies that an event in the power system, which lasts for one second, must be simulated on the simulator for only one second. Typically, digital simulations on a PC run 10 or 100 times slower than in real time, and do not maintain a fixed sample rate.

Recently the advantages of digital signal processing by using fast computers have a significant effect on digital simulation technology. However, as the size of the system increases, the number of calculations which must be performed increases, and a single CPU requires excessive time to compute the results. An alternative method divides the complexity of the calculation into several modules that can be solved in parallel. In this approach, adding more CPUs to the equipment can accommodate the difficulty of solving the represented power system without affecting the real time capability of the digital simulation. The approach has been investigated and implemented at the Manitoba HVDC Research Center results, designated as the Real Time Digital Simulator (RTDS).

The RTDS is a combination of specialized computer hardware and software, designed specifically for the solution of power system electromagnetic transients [14].

RTDS Hardware

The RTDS is organized into individual racks of tightly coupled digital signal processors, connected to one another by a common backplane. Each rack is identical and contains three distinct types of cards: the Processor Card, Workstation Interface Card (WIC), and Inter-Rack Communication Card (IRC) [14].

Processor Cards have a computing speed of several hundred Millions of Floating Point Operations Per Second (MFLOPS). A number of processing cards are located in each rack. Since the processing cards are identical, their function in any simulation is defined by the software. This flexibility provides increased processing power for component models with more complicated algorithms.

The Workstation Interface enables communication between the graphical interface software and the RTDS racks. An Ethernet controller in the WIC is able to interpret the data packets intended for its use, and respond to the originating workstation. Incoming data is re-directed by the WIC, and sent on the interconnecting backplane to particular processor cards. In this way, control actions such as fault application or set point adjustment can be dynamically conducted on the workstation.

The Inter-Rack Communication Card exchanges the data between the processors residing on separate racks. Each IRC includes a number of transmitter/receiver channels, allowing direct communication among several racks.

Because one of the principle applications of any real time simulator is physical equipment testing, a generated digital real time signal is converted to an analogue signal by using an accurate 1-bit digital to analogue card. This signal can be amplified to the desired level and applied to the relay being tested.

RTDS Software

RTDS software contains two distinct levels: the Graphical User Interface (GUI) and the Compiler [14].

The Graphical User Interface plays the role in the interaction between the user and RTDS. This interaction is performed by using a sophisticated, graphical-driven program called PSCAD. The GUI consists of two parts: Draft and Run Time. The Draft module is a pre-processing module, adopted to assemble the power system circuits and enter the associated parameters. Rather than creating text-based files, the describing interconnection of the power system, all the power system components are available in the PSCAD library as icons. The user drags and drops the modules into the Draft Module. All the actions are mouse driven and can be performed with minimal effort. The operation of the RTDS is accomplished by using the Run Time module to start and control the Draft Module. The Run Time Module also allows the user to monitor the specified parameters by using graphical icons for meters and plotted output.

The RTDS Compiler Module plays the role of an interactor between the Graphical User Interface software and the digital signal processing codes which run on the RTDS. The compiler takes the system layout and converts it into understandable codes for the RTDS. In addition, the Compiler Module creates a text file, indicating the terminal for each output so that the user can easily access these outputs.

Appendix B) Common Format for Transient Data Exchange

Electrical power utilities record fault data for post-fault analysis. In order to store the voltage and current waveforms in computers, these waveforms should be digitized. The digitized waveform can then be analyzed or exchanged between devices such as computer, relay, event recorder, etc. COMTRADE is a standard format for the exchange of fault or transient data for use with various devices, since this data is derived from a variety of sources. There are several possible sources of transient data for exchange, including digital fault recorders, digital protective relays, and transient simulation programs.

Each event has three types of files associated with it, which must be stored as ASCII files and carries a different class of information. The mentioned three files are header, configuration, and data files.

Header File: The header file is created by the originator of the fault data. The header file is intended to be used by the analyzer of the data, and file includes any information in any desired format.

Configuration File: This file must have its data in a specific format, because it is intended to be read by a computer program. The information in the configuration file is needed by a computer program in order to properly interpret the transient data. This file includes items such as the sample rate, number of channels, line frequency, and input channel information.

Data File: This file contains the value of each sample of each input channel. The stored data can be either zero-based or have a zero offset. The zero-based data changes from a negative number to a positive number. All the zero-offset numbers are positive with a positive number designated to represent zero. The scaling factors, specified in the configuration file, define how to convert the data vales to engineering units.

In addition to data representing analogue inputs, the input that represents digital (on/off) signals can also be recorded and stored in the configuration file. The state of a digital input is represented as the binary format in the data file.