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A Three-Phase Single-Stage AC-DC ZVZCS PWM Full-Bridge Converter

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by

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Abstract

It is standard practice to use two separate power converters to convert an ac input voltage to a desired and isolated dc output voltage. A front-end ac-dc converter is used to convert the input ac voltage into an intermediate dc voltage which is then fed into a dc-dc converter with transformer isolation. The front-end converter also performs input power factor correction (PFC) to shape the input currents to be sinusoidal and in phase with the input voltages to maximize the use of the available source power.

Conventional two-stage power conversion, however, requires two power converters and there has been considerable interest to try to integrate the PFC and dc-dc conversion functions in a single power converter to reduce cost and complexity. Although many of these single-stage converters have been proposed for low power, single-phase applications, there have been relatively few higher power three-phase converters that have been proposed. This is due to the challenges faced when trying to perform PFC and dc-dc conversion for a wider load range.

A new three-phase, single-stage ac-dc full-bridge converter is proposed in this thesis. The outstanding features of the new converter are that it is relatively simple and it can perform PFC using standard phase-shift pulse width modulation (PWM). In the thesis, derivation of the converter is discussed and its general operation is reviewed. The modes of operation of the converter are explained in detail and analyzed and the results of the analysis are used to develop guidelines for its design. The feasibility of the proposed converter is confirmed with experimental results that were obtained from a prototype and are presented in this thesis.

KEY WORDS: Three-Phase Ac-Dc Rectifiers, Power Factor Correction, Zero Voltage Zero Current Switching.

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Acronyms

Ac	*Alternate current*
BDVM	*Boundary Discontinuous Voltage Mode*
BJT	*Bipolar Junction Transistor*
C	*Collector*
CVM	*Continuous Voltage Mode*
Dc	*Direct current*
D	*Drain*
DVM	*Discontinuous Voltage Mode*
E	*Emitter*
G	*Gate*
IGBT	*Insulated Gate Bipolar Transistor*
L-C	*Inductive-Capacitive*
MOSFET	*Metal Oxide Semiconductor Field Effect Transistor*
PFC	*Power Factor Correction*
PWM	*Pulse Width Modulation*
rms	*root mean square*
S	*Source*
tf	*Transformer*
ZCS	*Zero Current Switching*
ZVS	*Zero Voltage Switching*
ZVZCS	*Zero Voltage Zero Current Switching*

Nomenclature

C	*Input capacitor of single-phase equivalent circuit with L-C filter*
C_a	*Input capacitor of phase-a*
C_b	*Input capacitor of phase-b*
C_{BDVM}	*Input capacitor at boundary discontinuous voltage mode*
C_c	*Input capacitor of phase-c*
C_o	*Output filter capacitor*
C_{sw}	*Switch capacitance between drain/collector and source/emitter*
C_x	*Auxiliary Capacitor*
D	*Duty ratio*
$D1$	*Rectifier diode in dc-dc PWM full-bridge converter*
D_1	*Normalized discharging time of C*
$D2$	*Rectifier diode in dc-dc PWM full-bridge converter*
D_b	*Diode in three-phase single switch buck converter*
D_c	*Auxiliary circuit charging diode*
D_d	*Auxiliary circuit discharging diode*
E_1	*Energy fed to load by* C_x
E_2	*Energy given to discharge* L_{lk} *by* C_x
E_a	*Energy input by Phase-a for* $\frac{\pi}{6}$
E_b	*Energy input by Phase-b for* $\frac{\pi}{6}$
E_c	*Energy input by Phase-c for* $\frac{\pi}{6}$
E_{C_x}	*Energy stored in* C_x
E_{in}	*Total input energy*
E_{out}	*Output Energy*
f_l	*Line frequecny*
f_r	*Dominant harmonic frequency (sideband)*
f_s	*Switching frequency*
$I_{a,pk}$	*Phase-a peak current*
I_a	*Phase-a current*

I_C	*Current through C*
I_{C_a}	*Current through* C_a
$I_{c_{fr}}$	*Harmonic current in C*
I_{C_x}	*Current through* C_x
I_d	*Current through switch body diode*
I_{in}	*Input current in equivalent single-phase circuit*
$IL_{a,ave}$	*Average Input Line Current*
I_{L_a}	*Current in* L_a
$I_{l_{fr}}$	*Harmonic current in L*
$I_{L_{lk}}$	*Current in* L_{lk}
I_{L_o}	*Average* L_o *current*
I_{mag}	*Maganetizing current*
I_o	*Load current*
I_{pri}	*Transformer primary current*
I_{S1}	*Current in* S_1
I_{S2}	*Current in* S_2
I_{S3}	*Current in* S_3
I_{S4}	*Current in* S_4
i_{T-}	*Transient switch current from on/off or off/on*
$I_{t_{fr}}$	*Total harmonic current of frequency* f_r
K	*Circuit parameter*
K_{BDVM}	*K at boundary discontinuous voltage mode*
L	*input inductor in equivalent single-phase circuit*
L_a	*Input filter indcutor-phase-a*
L_b	*Input filter indcutor-phase-b*
L_c	*Input filter indcutor-phase-c*
$L_{lk,min}$	*Minimum leakage inductance*
L_{lk}	*Leakage inductor*
L_o	*Output filter indcutor*
n	*Transformer turns ratio*
$N1$	*Number of primary turns*
$N2$	*Number of secondary turns*

P_{T-}	*Power loss during the switch transition*
R	*Resistive load*
R_a	*Input resistance, phase-a*
$rads$	*Radians*
R_b	*Input resistance, phase-b*
R_c	*Input resistance, phase-c*
$R_{ds,on}$	*Drain-Source resistance*
R_{in}	*Input resistance, equivalent single-phase circuit*
t	*time*
TC	*Time constant*
T_s	*Switching period*
V	*dc output to ac input voltage ratio*
V_a	*Instantaneous phase-a voltage*
V_b	*Instantaneous phase-b voltage*
V_{BDVM}	*Voltage at boundary discontiunous voltage mode*
$V_{bus,ave}$	*Average bus voltage*
$V_{bus,pk}$	*Peak bus voltage*
V_{bus}	*Instantaneous bus voltage*
$V_{C,pk}$	*Peak voltage across C*
V_C	*Input Capacitor Voltage*
V_c	*Instantaneous phase-c Voltage*
$V_{C_a,avg}$	*Average voltage across* C_a
$V_{C_a,pk}$	*Peak voltage across* C_a
V_{C_a}	*Instantaneous voltage across* C_a
$V_{C_x,min}$	*Minimum voltage of* C_x
$V_{C_x,pk}$	*Peak voltage of* C_x
V_{C_x}	*Instantaneous voltage of* C_x
V_d	*Source Voltage*
V_{fb}	*Instantaneous full-bridge input voltage*
V_{g1}	*Gate voltage pulse,* S_1
V_{g2}	*Gate voltage pulse,* S_2
V_{g3}	*Gate voltage pulse,* S_3

V_{g4}	*Gate voltage pulse,* S_4
V_{gs}	*Gate-Source voltage*
V_{in}	*Input voltage to equivalent single-phase circuit*
V_l	*Line-to-line peak Voltage*
$v_{ll,rms}$	*line-to-line rms volateg*
$V_{L_{lk}}$	*Voltage across* L_{lk}
V_o	*Output voltage*
$V_{p,ave}$	*Average tf primary voltage*
V_p	*tf primary voltage*
$V_{ph,pk}$	*Peak phase voltage*
V_{pk}	*Peak Phase voltage-equivalent single-phase circuit*
V_{pri}	*Tf primary voltage*
$V_{rec,ave}$	*Average secondary rectifier voltage*
V_{rec}	*secondary rectifier voltage*
$V_{s,ave}$	*Tf secondary side average voltage*
V_s	*Transformer Secondary Voltage*
V_{S1}	*Switch 1- High side MOSFET*
V_{S1}	*Switch 2- Low side IGBT*
V_{S1}	*Switch 3- High side IGBT*
V_{S1}	*Switch 4- Low side MOSFET*
V_{Sw1}	*Voltage of* S_1
V_{Sw2}	*Voltage of* S_2
$V_{sw,pk}$	*Peak switch voltage*
V_{sw}	*Instantaneous switch voltage*
$\boldsymbol{v}_{T-}$	*Transient switch voltage from on/off or off/on*
V_{th}	*Gate-Source threshold voltage*
Y	*Star Connection*
η	*Efficiency*
ω_l	*line frequency in rad/s*

Chapter 1

Introduction

1.1 Introduction to Power Electronics

Power electronics is the field of electrical engineering related to the use of semiconductor devices to convert power from the form available from a source to that required by a load. A block diagram of a typical power electronic system is shown in Figure 1.1 ([1]). The power source may be a dc source or a single-phase/three-phase ac source with line frequency of 50 to 60 Hz or 400Hz; it may be an electric battery, a solar panel, an electric generator or a commercial power supply. The source feeds the input of the power converter or processor, which converts the input power to the required form for a load. The load may be dc or ac, single-phase or three-phase, and may or may not need transformer isolation from the power source.

The power converter can be an ac/dc converter, a dc/dc converter, a dc/ac inverter or an ac/ac converter depending on the application. Feedback control is used to ensure that the required output voltage and/or current are provided to the load. This is done by sensing the output voltages and currents and feeding the information into the controller so that the controller can send information to the power processor, which makes the necessary adjustments.

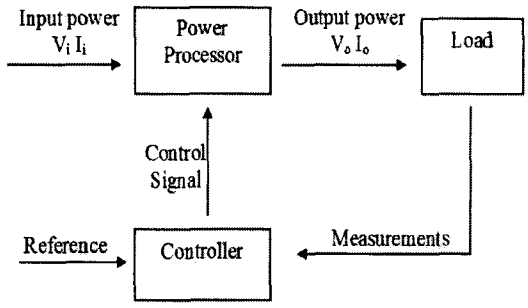


Figure 1.1: Block diagram of a power electronics system.

1.2 Semiconductor Devices

The semiconductor devices that are typically used in a power converter are diodes, MOSFETs and IGBTs. Devices such as thyristors are used in very high power converters and will not be discussed here. Diodes are uncontrolled switches as they are on and conduct current when they are forward-biased and are off when they are reverse-biased. Current cannot be interrupted in a diode and some action external to the diode must be taken to divert current away from it and make it reverse biased.

MOSFETs and IGBTs are controllable switches and can be turned on and off by feeding a control signal to their gate then removing it. The basic characteristics of each device are discussed in further detail below.

1.2.1 MOSFETs

A MOSFET is a metal oxide semiconductor field effect transistor and is typically depicted as shown in Figure 1.2. It has three terminals - a gate, a drain, and a source. The switch is on when current is fed to the gate and its gate-source capacitance is charged to a threshold voltage V_{th}, which creates a field that opens the drain-source channel and allows current to flow from drain to source. Current does not have to

be continuously fed to the gate to keep the device on; the device is on as long as the voltage across the gate-source capacitance V_{gs} is greater than V_{th} and the field that keeps the channel open exists.

The MOSFET has three main regions of operation: triode, saturated, and cut-off. Since controllable semiconductor devices in almost all power electronics applications function as switches that are either fully on or fully off, a MOSFET in a power converter operates either in the triode region (fully on) or in the cut-off region (fully off). When a MOSFET is on, however, it is not an ideal switch as it has some resistance $R_{ds,on}$ between its drain and source, which contributes to energy loss when current flows through the device.

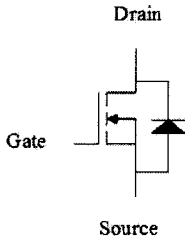


Figure 1.2: Power MOSFET symbol.

Since MOSFETs are turned on and off due to the generation and removal of an electric field, they can be turned on and off very quickly and are the fastest semiconductor devices in terms of switching. They are the devices of choice in applications such as low power applications as their fast switching characteristics allows them to be implemented in converters that operate with high switching frequencies ($> 100kHz$) to reduce the size of their passive elements (inductors, capacitors, transformers). They are not suitable for higher power applications due to their $R_{ds,on}$ and the conduction losses created by this parameter.

1.2.2 IGBTs

An IGBT is an insulated gate bipolar transistor and gets its name from the fact that it has the characteristics of both BJTs and MOSFETs. It is typically depicted as shown in Figure 1.3. It has three terminals - a gate, a collector and an emitter. The term "gate" comes from the MOSFET part of the device while the terms "collector" and "emitter" comes from the BJT part of the device.

A BJT is a bipolar junction transistor and is a minority-carrier device. This means that unlike a MOSFET, which is turned on by generating an electric field that can be very quickly removed, the BJT is turned on by feeding a continuous current to its base (the "gate" of the device). The advantage that the BJT has over the MOSFET is that is has a fixed voltage drop across its collector-emitter terminals when the device is on, whereas the MOSFET has a variable voltage drop because it depends on the product of the current flowing through the device and its $R_{ds,on}$. The BJT is therefore better suited for high power applications than the MOSFET because its lower voltage drop results in lower conduction losses.

The BJT, however, turns on and off very slowly because it is a minority-carrier device that depends on the presence of a continuous base current. It cannot match the switching speed of a MOSFET as it is easier to generate and remove an electric field than it is to inject and remove electrons. In order to improve the switching times of the BJT, its base was made into a MOSFET gate and thus the IGBT with its insulated gate was created. Although the IGBT turns on and off more quickly than a BJT, its switching speed cannot match that of a MOSFET, which can operate with switching speeds in the MHz range. The IGBT, however, still has the voltage drop characteristics of the BJT and is thus preferred over the MOSFET in higher

power applications.

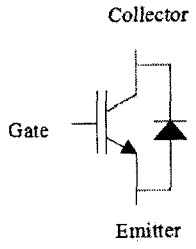


Figure 1.3: IGBT symbol.

1.3 Switching Characteristics

The switching of a MOSFET or an IGBT is not ideal. An ideal switch would turn on and off instantaneously and there would be no overlap between the voltage across a device and the current through it, and, therefore, no power loss as the power lost due to switching is related to product of the two. In reality, however, such overlaps do exist whenever the device is in a switching transition, going from on to off or vice versa. An example of the overlap of voltage and current that can be encountered by a device is shown in Figure 1.4 ([1]).

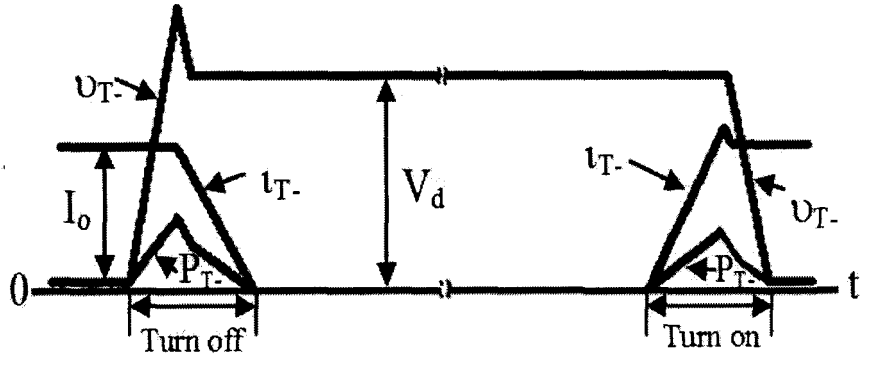


Figure 1.4: Non-ideal switching characteristics of a semiconductor device.

The switching losses generated by a MOSFET or an IGBT is related to its switching frequency - the faster it is turned on and off, the more switching losses will be generated. Switching losses, however, can be reduced if either the voltage or the current is made to be zero during the time that a switching transition takes place so that there is no voltage and current overlap and thus no power lost. Techniques for ensuring that this occurs can be classified as either zero-voltage switching (ZVS) techniques or zero-current switching (ZCS) techniques; these two types of techniques are generally referred to as soft-switching techniques while hard-switching refers to the case when such techniques are not used. Both ZVS and ZCS are briefly reviewed here.

ZVS techniques are techniques that force the voltage across a switch to be zero just before it is turned on or off and keep this voltage zero while a switching transition occurs. Both MOSFETs and IGBTs have anti-parallel diodes that are built into the "body" of each device that allows current to flow from source to drain in a MOSFET and from emitter to collector in an IGBT. A ZVS turn-on in MOSFETs and IGBTs is therefore done by forcing current through the body-diode of the devices just before they are turned on. This clamps the voltage across the device to a single diode drop (which is a negligible voltage) during a switching transition so that turn-on switching losses are greatly reduced. A ZVS turn-off is achieved by slowing down the rate of voltage rise across a switch when it is turned off by adding some capacitance across the switch; this limits the overlap between voltage and current.

ZCS techniques are techniques that force the current through a switch to be zero just before it is turned on or off and keep this current zero while a switching transition occurs. A ZCS turn-off is achieved by diverting current away from the

switch into the rest of the power converter before the switch is turned off. This is typically done by providing a path of negative voltage potential to the switch or by imposing a negative voltage somewhere in the current path. A ZCS turn on can be done by adding an inductor in series with the switch that slows down the rate of current rise when the switch is turned on; this limits the overlap in voltage and current.

Since MOSFETs are used in low current, high switching frequency applications and have a significant drain-source capacitance, they are usually implemented with some ZVS technique. The drain-source capacitance is often sufficient to ensure that the device can be turned-off with ZVS and negative current is used to discharge this capacitance and flow into the body-diode so that the device can turn on with ZVS. Since IGBTs are used in high current applications and have a slower turn-off due to their being minority-carrier devices, they are usually implemented with ZCS. They have smaller collector-emitter capacitances than MOSFETs and it is the turn-off losses that must be dealt with.

1.4 Two-Stage Ac-Dc Power Conversion

The main type of power electronics converters that will be the focus of this thesis are power converters that convert a three-phase ac input voltage into a stepped down and transformer isolated dc output voltage. This is typically done using two switch-mode converters (as opposed to completely passive converters made up of diodes and no active switches). As shown in the block diagram in Figure 1.5, an ac-dc converter or rectifier is used to convert the ac input voltage into an intermediate dc bus voltage and is then fed to a second converter that converts it into the desired, isolated, dc

voltage.

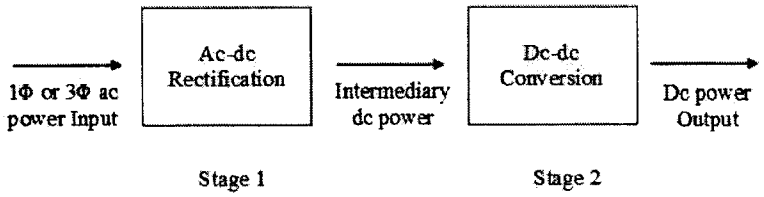


Figure 1.5: Block diagram of Two-Stage ac-dc converters.

An example of a two-stage ac-dc converter is shown in Figure 1.6. The ac-dc converter is typically a six-switch converter that performs input power factor correction (PFC) while it is performing ac-dc power conversion. Input PFC shapes the input line currents so that they are sinusoidal and in phase with the line voltages to maximize the use of available power from the source. Input PFC is now a standard feature in ac-dc converters as consumer demands and the resulting proliferation of electric equipment has resulted in the need to satisfy stringent regulatory limits on the harmonics that can be injected into the ac mains. The dc-dc converter is typically a four-switch full-bridge converter for higher power applications where a three-phase source instead of a single-phase source is used.

In this section of the thesis, the operation of the full-bridge and alternatives to the six-switch converter are reviewed.

1.4.1 Full-Bridge Converter Operation

A dc-dc full-bridge converter is shown in Figure 1.7. It can be seen that the converter consists of four switches, a transformer, two output diodes, an inductor and a capacitor; the load is represented as a resistor. The converter works as follows:

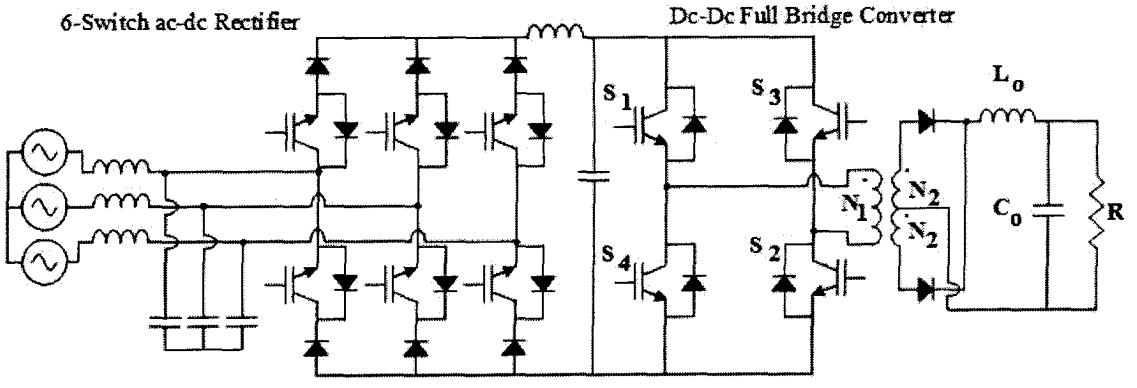


Figure 1.6: Three-phase ac-dc six switch two-stage full-bridge converter.

Voltage is impressed across the primary of the transformer winding whenever a diagonally opposite pair of switches are on (S_1 and S_2 or S_3 and S_4); the polarity of the voltage depends on the pair of switches that is on. No voltage is impressed across the transformer primary whenever current flows through two top switches (or their body-diodes) or two bottom switches (or their body diodes).

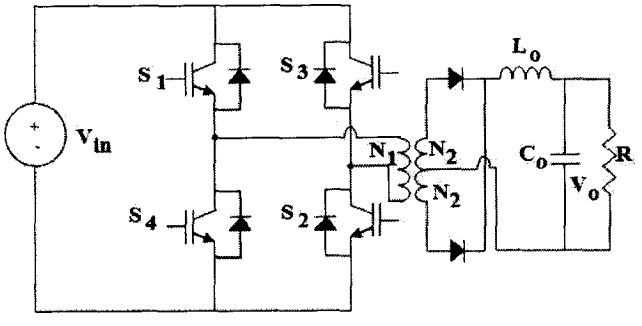


Figure 1.7: Dc-dc full-bridge converter.

The converter can be said to be in an energy-transfer mode whenever a voltage is impressed across the transformer primary and appears at the secondary, and to be in a freewheeling mode when there is no voltage across either transformer winding and current just flows ("freewheels") throughout the converter. Since the voltage across

the transformer is a symmetrical ac square voltage with zero voltage sections, two diodes are needed at the secondary to rectify this voltage and a low-pass inductor-capacitor (L-C) filter is needed to smooth out the voltage and make it almost purely dc.

Starting from a state when S_1 and S_2 are on, the typical sequence of operation during a half switching cycle is as follows:

- S_1 and S_2 are on and conduct current;
- S_2 is turned off and the current in the transformer primary flows through the anti-parallel body-diode of S_3 (which allows S_3 to turn on with ZVS);
- S_1 is turned off and current in the transformer primary flows through the body-diode of S_3 and S_4 (which allows S_4 to turn on with ZVS):
- Current in S_3 and S_4 eventually reverses direction so that it flows through the switches instead of the body-diodes

The next half switching cycle begins when S_3 is turned off and current starts flowing in the body diode of S_2. If a switch is considered to be on regardless of current flowing through the switch itself or through its body-diode, then the switching sequence over a full switching cycle is as follows:

- S_1-S_2 on (energy-transfer mode/transformer voltage $+ve$ polarity)
- S_1-S_3 on (freewheeling mode/transformer voltage zero)
- S_3-S_4 on (energy-transfer mode/transformer voltage $-ve$ polarity)
- S_2-S_4 on (freewheeling mode/transformer voltage zero)

The signal voltage pulses that are fed to the gates of each switch (gating signals) are high for 50% of the switching cycle (switch on) and low during the rest of the cycle (switch off). The gating signal of any switch is complementary to that of the switch in the same leg so that two switches in the same leg (i.e. S_1 and S_4 or S_3 and S_2) are never on simultaneously, which would result in a short circuit. Typical dc-dc full-bridge waveforms are demonstrated in Figure 1.8.

The output dc voltage level can be controlled by controlling the width of the positive and negative voltage pulses relative to the zero voltage portions of the transformer. This can be done by shifting the gating signal pulses of the switches in one leg, relative to those of the switches in the other leg. If S_1 and S_2 are always on simultaneously and S_3 and S_4 are always on simultaneously, then the converter will always be in an energy-transfer mode and the output voltage will be at its maximum possible value. If S_1 and S_2 are never on simultaneously and S_3 and S_4 are never on simultaneously, then the converter will never be in an energy-transfer mode and the output voltage will be zero. This method of controlling the output dc voltage is called phase shift pulse width modulation (phase shift PWM) and is considered to be the standard method of controlling a dc-dc full-bridge converter.

1.4.2 Ac-Dc Front-End Converters

The three-phase six-switch ac-dc rectifier converter that is the front-end converter of the two-stage converter shown in Figure 1.6 is considered to be the standard converter in this setting (either with low pass L-C filter, as shown in Figure 1.6 or with just a C filter). This converter, however, is expensive as it requires six active switches along with associated gate drive and control circuitry and requires sophisticated con-

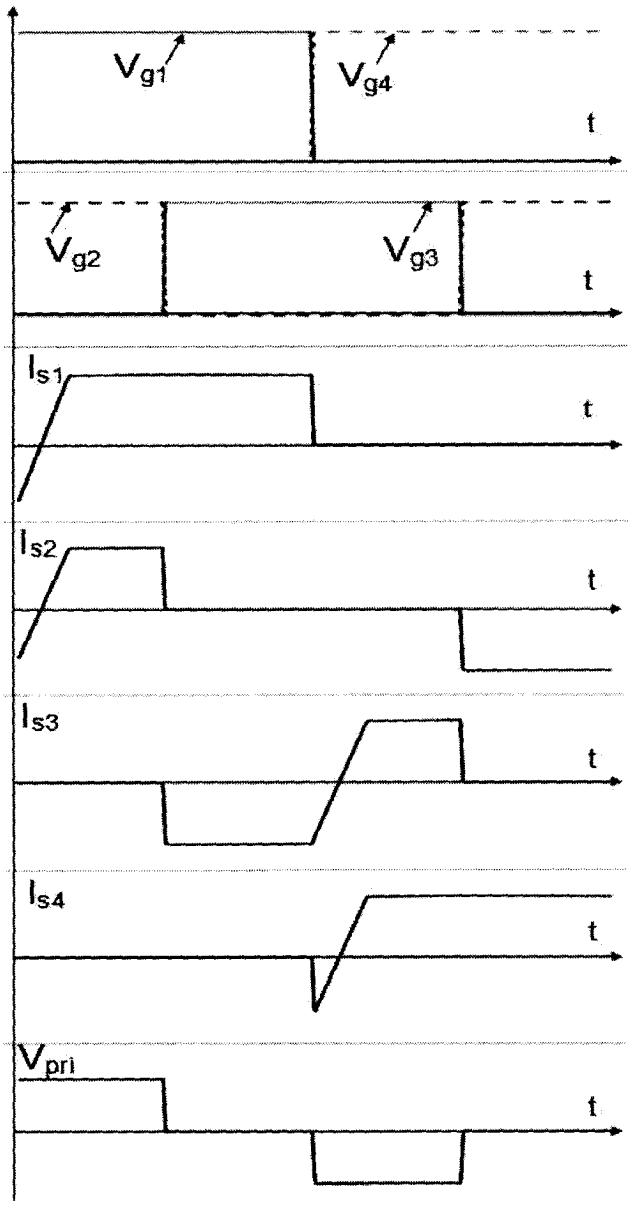


Figure 1.8: Typical dc-dc full-bridge waveforms.

trol methods to perform input PFC. Power electronics researchers, therefore, have been motivated to find simpler and cheaper alternatives to the standard six-switch converter.

One approach to three-phase ac-dc conversion is to use three separate single-

phase boost PFC converter modules as shown in Figure 1.9 [2]. Each module in Figure 1.9 is a two-stage converter consisting of PFC boost converter followed by a dc-dc converter to get the desired bus voltage. The main advantage is that existing single-phase modules can be used, which are popular and widely available and do not require knowledge of sophisticated three-phase control. The main disadvantages are the need to synchronize the operation of each individual module to the others and the presence of triplen harmonics (these are odd multiples of the 3rd harmonic, 3rd, 9th, 15th etc.) due to parametric variations in the modules.

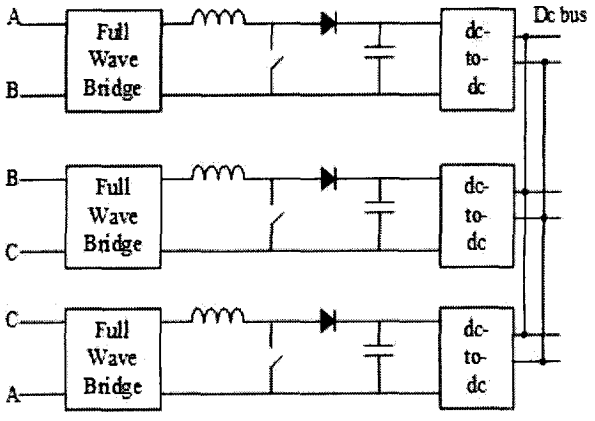


Figure 1.9: Three-phase ac-dc converter using three single-phase modules.

Another approach is to use reduced switch rectifiers that contain only three or four switches [2] instead of six as the front-end ac-dc converter. An example of such a rectifier is shown in Figure 1.10. Although the number of switches has been reduced, the overall two-stage converter still requires seven or eight switches and the control methods needed to perform PFC and ac-dc conversion remain very sophisticated.

A third approach is to use a three-phase single-switch ac-dc rectifier as the

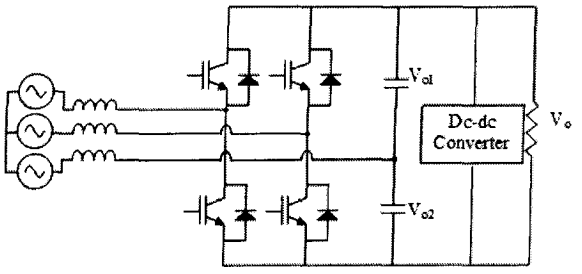


Figure 1.10: Three-phase ac-dc converter with four switches.

front-end converter [3]-[4]. This approach is most suitable for applications of about $2kW - 6kW$ power, which is just above the range where single-phase converters are more attractive than three-phase converters. There are two types of three-phase single switch rectifiers: the boost (step-up) converter [4] and the buck (step-down) converter [3]-[4]; the boost converter is shown in Figure 1.11. Its operation is as follows: When the boost converter switch is turned on, current in each line inductor rises to a peak value proportional to the voltage applied in that switch cycle. When the switch is off, currents in those inductors fall to zero as energy is transferred to the output capacitor. As a result, each input line current is discontinuous and is bounded by a sinusoidal envelope so that it is essentially a sinusoid with high frequency components that can be filtered out with some additional filtering. A typical line current waveform for a half line cycle is shown in Figure 1.12.

Figure 1.13 shows the three-phase single-switch buck converter. It operates in similar manner to boost converter, but, in this case, it is the voltages across input capacitors (C_a, C_b and C_c) that must be discontinuous so that they are essentially sinusoidal in nature. Since these voltages are sinusoidal and the input voltages are sinusoidal, the input inductor currents will also be sinusoidal, but unlike those of the boost converter, they will be continuous.

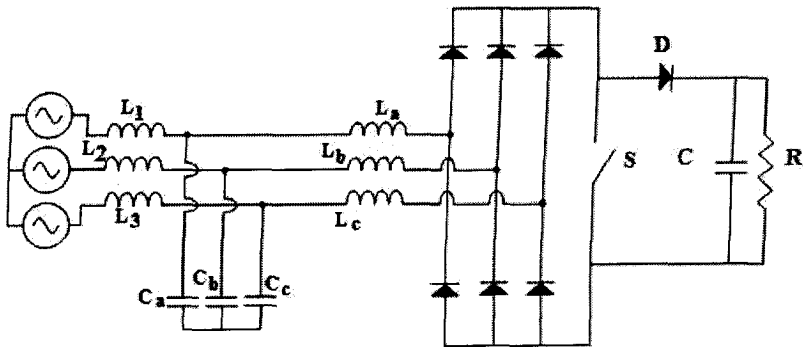


Figure 1.11: Three-phase ac-dc single-switch PFC front-end boost converter.

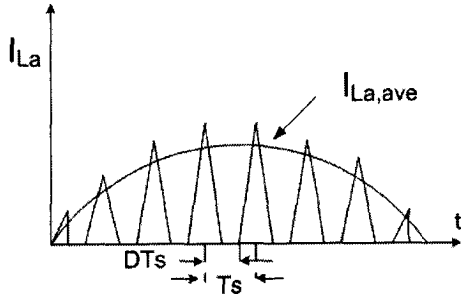


Figure 1.12: Input line current waveform of a three-phase ac-dc single-switch boost converter (half-line cycle).

Both types of single switch, three-phase converters are very attractive because they are simple. They are, however, limited in power because all the power being converted must be processed by a single active switch.

1.5 Three-Phase Single-Stage Ac-Dc Converters

Regardless of whichever of the above-mentioned ac-dc rectifier converters is used as the front-end converter of a two-stage ac-dc converter with ac-dc front-end and dc-dc full-bridge stages, two separate switch-mode converters need to be implemented. In

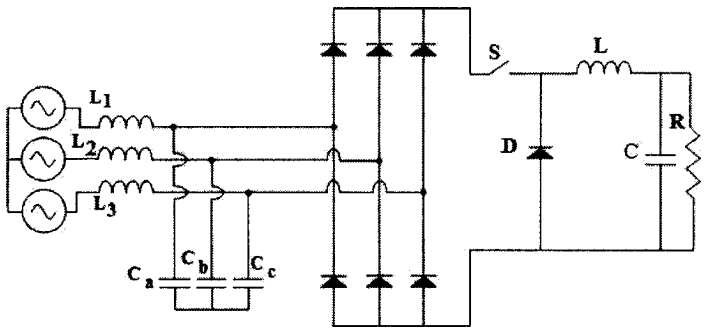


Figure 1.13: Three-phase ac-dc single-switch PFC front-end buck converter.

order to reduce the cost and complexity associated with implementing two switch-mode converters, power electronics researchers have tried to combine the PFC function of the ac-dc front-end converter with the dc-dc conversion function of the full-bridge converter in a single converter [5]-[13]. Power converters of this type are referred to as single-stage converters in the power electronics literature. Several examples of three-phase, single-stage converters are shown in Figure 1.14.

There has been considerable research on low power, single-phase, single-stage ac converters, but there has been relatively little research on three-phase, single-stage converters. This is because of the challenges involved in simultaneously performing both PFC and dc-dc conversion over a much wider load range than what the low power single-stage converters encounter. The few three-phase single-stage converters that have been proposed have at least one of the following drawbacks:

- The converter uses a three single-phase full-bridge modular approach [13] (i.e. Figure 1.14(a)). This is expensive and it is not easy to synchronize the operation of all three converters to produce sinusoidal input currents.

- The input currents are distorted and contain a significant amount of low fre-

quency harmonics [6] (i.e. Figure 1.14(b)) as the converter has difficulty performing PFC and dc-dc conversion simultaneously; thus compromising the quality of the input waveforms and power factor.

- The input currents must become zero during each switching cycle (discontinuous input currents) in order for input PFC to be achieved. Converters shown in Figures 1.14(a) - 1.14(d) ([6], [14]) incorporate the principles of the three-phase single-switch boost converter (which was originally proposed in [5]) into their topologies. Although an excellent input power factor may be achieved, the peak current stress of the semiconductor devices is very high. Moreover, additional and significant filtering is required to attenuate the large amount of high frequency noise fed back to the line.

- The converter must be controlled using very sophisticated techniques. This is especially true of multilevel converters shown in Figure 1.14(c) ([8], [10]) where the need to balance the voltages on the split capacitors at the dc bus is critical.

1.6 Thesis Objectives

The main objectives of this thesis are as follows:

1. To propose a new three-phase, ac-dc, single-stage, PWM converter that can operate with an excellent input power factor i.e., the the line current harmonics are well below the standard specification and that does not have the disadvantages of the above-mentioned three-phase single-stage converters.

2. To analyze its steady-state operation and to determine its steady-state characteristics.

3. To develop guidelines and a procedure for designing the proposed converter so that it can operate properly.

4. To confirm its feasibility with results obtained from a working, experimental prototype.

   The above objectives were achieved and will be elaborated in the chapters to come.

1.7 Thesis Outline

The thesis is comprised of the following six chapters. Following is a briefing of each chapter following;

Chapter 2: The derivation of the proposed three-phase, single-stage, ac-dc converter is discussed in detail in this chapter. Since the proposed single-stage converter is based on the combination of a single-switch three-phase buck converter with a dc-dc zero-voltage-zero-current switched (ZVZCS) full-bridge converter, the basic operation of both these converters and their modes of operation are explained. It is then shown how these two converters can be combined to form the proposed three-phase single-stage converter.

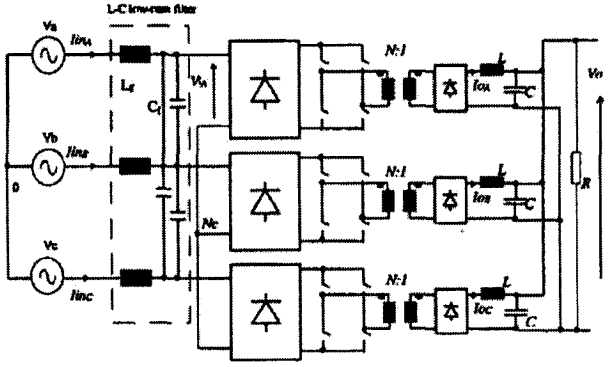
Chapter 3: The proposed three-phase single-stage ac-dc converter is introduced in this chapter and its operation is discussed. The modes of operation that the converter goes through are explained in detail, the key equations that define its

operation during these modes are derived and the attractive features of the new converter are stated.

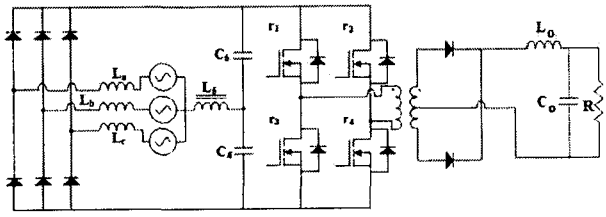
Chapter 4: A steady-state analysis of the proposed converter is performed in this chapter. The purpose of the analysis is to derive expressions and determine relations of key converter parameters to understand the steady-state characteristics of the converter and to help establish a procedure for its design, which will be done in Chapter 5.

Chapter 5: The design of the converter is discussed in this chapter. An example is given to demonstrate how the most important converter parameters can be selected using the results of the analysis performed in Chapters 3 and 4. The results of the design process will be used in the implementation of an experimental prototype converter that will confirm the feasibility of the converter.

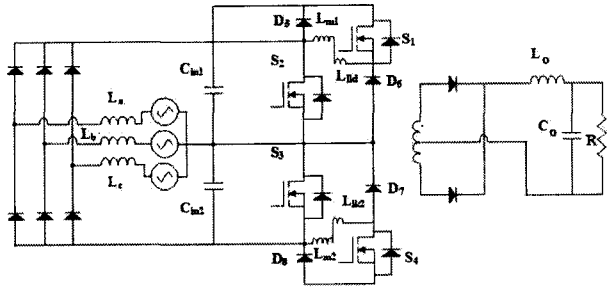
Chapter 6: In this chapter, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work performed in thesis are presented, and the main contributions of the thesis are stated. The chapter concludes by suggesting potential future research that can be done based on the thesis work.



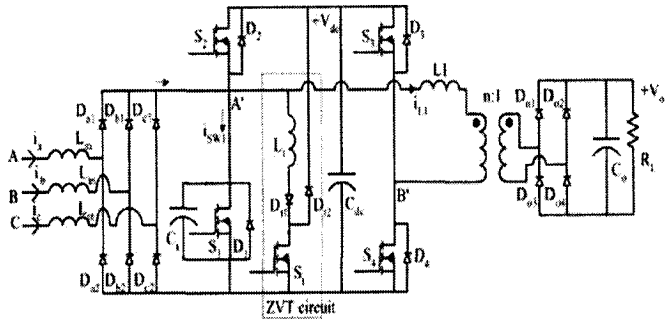
(a) Converter with three single-phase modules ([13])



(b) Compromising between voltage regulation and PFC ([6])



(c) A multi-level converter ([10])



(d) A front-end boost converter technique is used for PFC ([14])

Figure 1.14: Examples of three-phase, single-stage converters.

Chapter 2

Fundamental Principles

2.1 Introduction

The derivation of the proposed three-phase, single-stage, ac-dc converter is discussed in detail in this chapter. Since the proposed single-stage converter is based on the combination of a single-switch three-phase buck converter with a dc-dc zero-voltage-zero-current switched (ZVZCS) full-bridge converter, the basic operation of both these converters and their modes of operation are explained in this chapter. It is then showed how these two converters can be combined to form the proposed three-phase single-stage converter.

2.2 Fundamental Principles - Ac-Dc Three-Phase Single-Switch Buck Converter

Before presenting and discussing the proposed three-phase, single-stage converter, the general fundamental principles behind its derivation and operation will be discussed first in this chapter. Consider the two-stage, three-phase ac-dc converter shown in

Figure 2.1. This converter has a single-switch buck (step down) ac-dc front-end rectifier as the front-end, followed by a dc-dc full-bridge converter. The objective in deriving a new three-phase, ac-dc single-stage converter is to combine these two converters into one to form the proposed single-stage converter. In order to understand how this can be done, the operation of the ac-dc single switch front-end converter is reviewed first in detail in this section. The converter is shown with a resistive load in Figure 2.2.

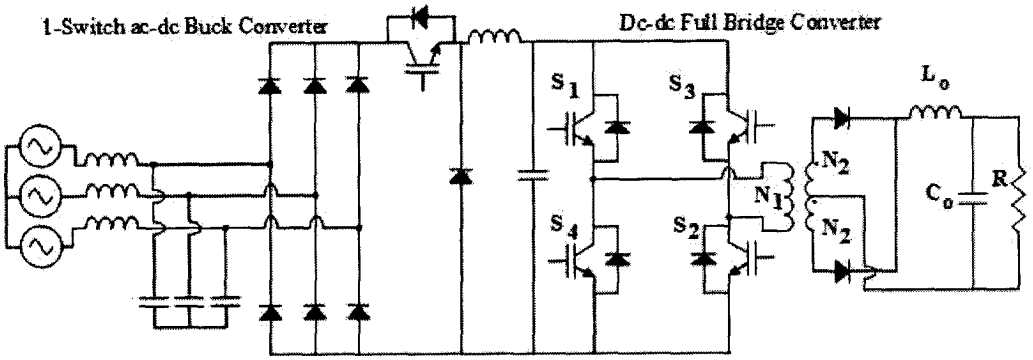


Figure 2.1: Ac-dc converter with single-switch buck rectifier and dc-dc full-bridge converter.

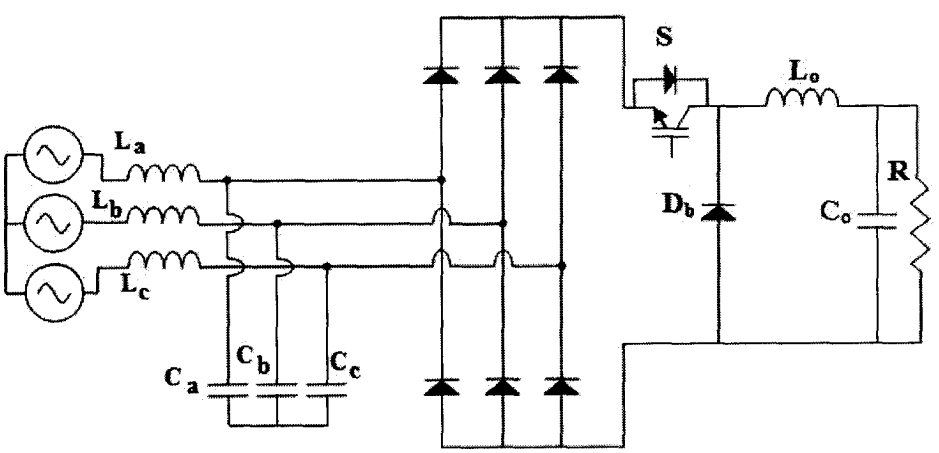


Figure 2.2: Three-phase ac-dc single-switch PFC buck converter.

The converter consists of three input inductors, three input capacitors, a three-phase diode rectifier and a standard buck converter section comprised of a switch, a diode, and a low pass L-C filter. During a typical switching cycle (which is a small fraction of the input ac line cycle), the converter goes through the following modes of operation, as shown in Figure 2.3:

Mode 1 ($t_0 < t < t_1$) *Figure 2.3(a)*

At $t = t_0$, the switch, S, is turned on. The input capacitors C_a, C_b, and C_c begin to discharge as current flows through the diode rectifier bridge to the output converter section. The diode, D_b, is reverse biased during this mode as the rectifier output voltage (which is the rectification of the input capacitor voltage) is placed across it. By the end of this mode, the input capacitors are fully discharged.

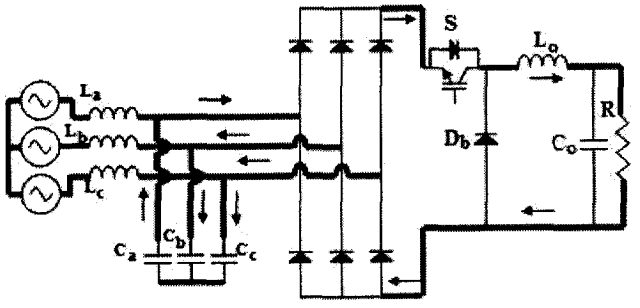
Mode 2 ($t_1 < t < t_2$) *Figure 2.3(b)*

The input capacitors remain discharged during this mode and only the line currents flow through the diode bridge rectifier to the output section. Since the input capacitors have no voltage across them, the voltage across the diode bridge rectifier output is zero, which makes D_b forward biased. The current that D_b conducts is the difference between the current flowing from the input section of the converter and the current flowing through output inductor L_o. The mode ends at $t = t_2$ when S is turned off.

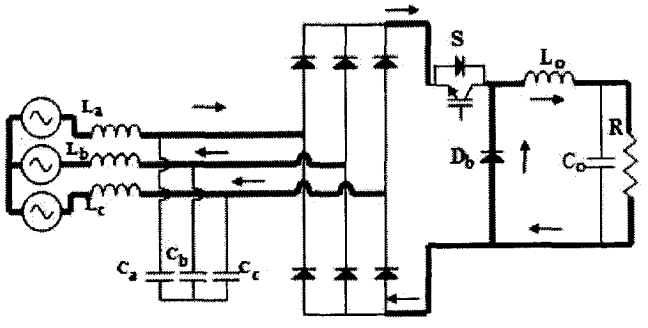
Mode 3 ($t_2 < t < t_3$) *Figure 2.3(c)*

After S is turned off, the path of current flow from the input section to the output section of the converter is broken; therefore the line currents begin to

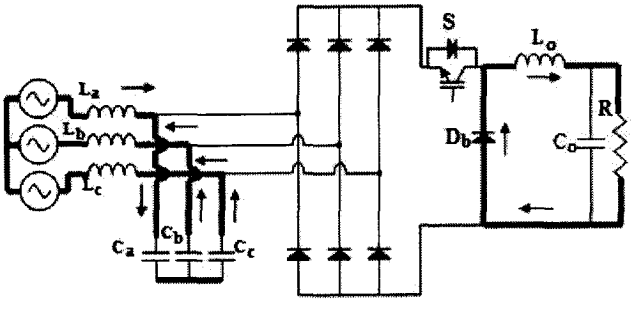
charge the input capacitors. All the current in L_o flows through D_b and the converter is in a freewheeling mode of operation, much like that found in a standard dc-dc buck converter. At $t = t_3$, S is turned on again to start the next switching cycle.



(a) Mode 1 ($t_0 < t < t_1$)



(b) Mode 2 ($t_1 < t < t_2$)



(c) Mode 3 ($t_2 < t < t_3$)

Figure 2.3: Steady state modes of the three-phase single-switch buck converter.

The input inductor currents can be sinusoidal and in phase with the input line

voltages as long as the input capacitors voltages can be fully discharged after Mode 1 for all switching cycles throughout the line cycle. If there is a significant number of switching cycles during which the input capacitors cannot be fully discharged, then the input capacitor voltages will not look like the voltage waveform shown in Figure 2.4, which is essentially sinusoidal, but will contain low frequency harmonic components. These components will cause the input inductor currents to become distorted, which will lead to a reduction in input power factor.

2.3 Fundamental Principles - Dc-Dc Zero-Voltage-Zero-Current Switching (ZVZCS) Full-Bridge Converter

A conventional dc-dc full-bridge converter, like the one shown as the second converter stage of the two-stage ac-dc converter in Figure 2.1, is considered to be a buck converter, but with transformer isolation. It would be, therefore, possible to replace the switch of the front-end ac-dc rectifier in Figure 2.2 with a full-bridge converter so that the two converters stages can be made into one, as shown in Figure 2.5. There is however, a catch. A path for the transformer primary-side current must be provided when the converter exits a freewheeling mode of operation.

It should be noted that the switches in one leg of the full-bridge converter are MOSFETs and the switches in the other leg are IGBTs. This is because the switches in one leg operate with ZVS and those of the other leg operate with ZCS. MOSFETs are preferred devices for ZVS operation and IGBTs are the favorable devices for ZCS functioning.

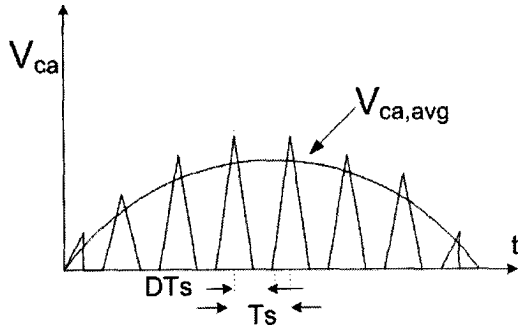


Figure 2.4: Input capacitor voltage of a three-phase, single-switch, ac-dc buck converter (half-line cycle).

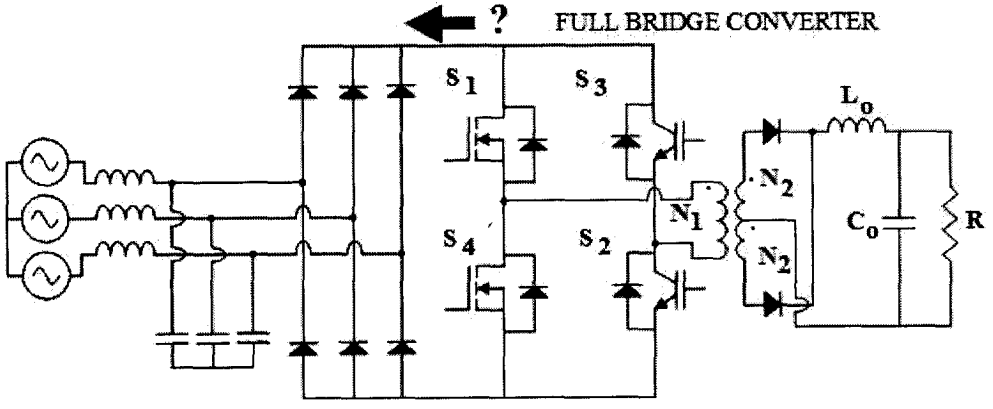


Figure 2.5: Three-phase single-stage ac-dc converter with conventional full-bridge.

Consider the operation of a dc-dc full-bridge converter, assuming that switches S_1 and S_2 are on (section 1.4.1). There is voltage from the dc bus capacitor that is impressed across the transformer primary and energy is being transferred from the primary to the secondary and the output. When switch S_1 is turned off, the current that was flowing in this switch is transferred to the anti-parallel diode of S_4 and this switch can be turned on with zero-voltage switching. The converter operates in a freewheeling mode with current circulating through S_2 and S_4 in the primary-side of the converter. When S_2 is turned off, current flows through the anti-parallel diodes of S_3 and S_4 and through the dc bus capacitor that is connected across the full-

bridge input. It is important to note that a typical full-bridge converter has modes of operation where primary current flows in the reverse direction out of the converter and back into the source.

If a full-bridge converter is to replace the switch in the buck front-end rectifier, then there must be little if any of this reverse current. This can be done if the full-bridge converter is a zero-voltage-zero-current switching (ZVZCS) converter (as the ones proposed in [15] - [18]). A ZVZCS converter has the property that most of the transformer primary current that circulates in the converter when it is in a freewheeling mode can be extinguished so that there is little "backwards" current that flows through the anti-parallel diodes of the switches when the converter exits a freewheeling mode of operation. The elimination of the reverse current means that the dc bus capacitor can be removed so that the converter shown in Figure 2.5 can become reality. Another option is to keep the reverse current and use it to feed an auxiliary power supply, as has been suggested for the two-switch forward converter in [12], but this is cumbersome and impractical for many applications.

An example of a ZVZCS dc-dc full-bridge converter is shown in Figure 2.6. The converter is almost the same as a conventional dc-dc full-bridge converter except that a small passive auxiliary circuit consisting of capacitor C_x, and diodes D_c and D_d has been added. The purpose of this circuit is to impress a counter voltage across the transformer primary whenever the converter is in a freewheeling mode to extinguish the circulating current that flows in the converter during that time.

Equivalent circuit diagrams showing the flow of current in the converter during a half switching cycle are shown in Figure 2.7 and typical converter waveforms are

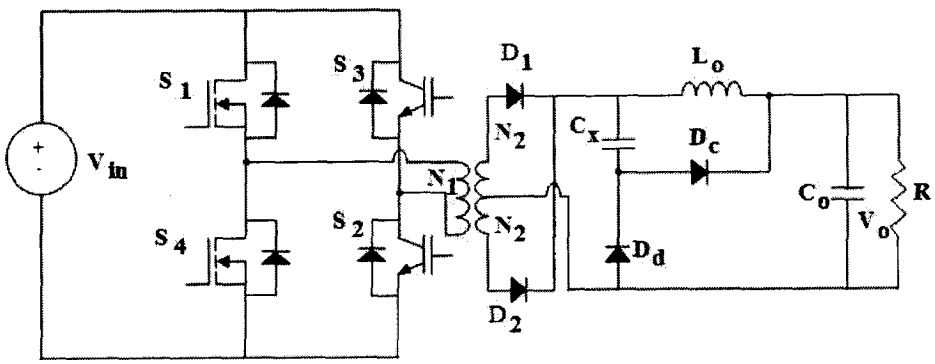


Figure 2.6: Dc-dc PWM ZVZCS full-bridge converter.

shown in Figure 2.8. Prior to $t = t_0$, switch S_1 of the full-bridge is on, switches S_2, S_3 and S_4 are off, and there is no current in the primary side of the full-bridge transformer. On the secondary side, the auxiliary circuit (C_x, D_d, and D_c) does not conduct current and current from the output inductor L_o is freewheeling though the two diodes D_1 and D_2, connected to the secondary winding of the transformer. The converter's modes of operation are as follows:

Mode 1 ($t_0 < t < t_1$) *Figure 2.7(a)*

Mode 1 starts at $t = t_0$ when S_2 is turned on. Current from the dc source flows through switches S_1, S_2 and voltage is impressed across the primary winding of the transformer. Voltage appears across the secondary winding and C_x begins to be charged through diode D_c; there is an interaction between C_x and the transformer's leakage inductance that limits the current charging this capacitor. Current from the output inductor L_o also flows through the load; and the primary current is the sum of the reflected currents through L_o and C_x. Mode 1 ends when D_c stops conducting and V_{C_x} is at its peak. The converter is in an energy transfer mode during Mode 1.

Mode 2 ($t_1 < t < t_2$) *Figure 2.7(b)*

Mode 2 is identical to Mode 1 except that no current flows through C_x. The transformer primary current is equal to the reflected current flowing through L_o during this mode.

Mode 3 ($t_2 < t < t_3$) *Figure 2.7(c)*

Switch S_1 is turned off at $t = t_2$. The current that was flowing through S_1 charges and discharges the capacitances across S_1 and S_4 respectively. These capacitances (shown only in the Figure 2.7(c) diagram for emphasis) are placed across these switches to limit the rise in voltage across them when they are turned off, as they carry the full transformer primary current during this switching transition. As the voltage across the transformer primary decreases from V_{in} to zero, the voltage at the secondary also decreases and settles at V_{C_x}, which is constant during this mode. The mode ends when the capacitances across S_1 and S_4 have been fully charged and discharged respectively.

Mode 4 ($t_3 < t < t_4$) *Figure 2.7(d)*

At $t = t_3$, current starts flowing in the anti-parallel body diode of S_4. Once this happens, S_4 can be turned on with ZVS at any time during this mode because the voltage across this switch is clamped to almost zero. Current circulates through S_2 and S_4 and the voltage impressed across the transformer primary is zero; the converter is in a freewheeling mode with no power being transferred from the dc source to the load. On the secondary side of the transformer, C_x starts to discharge through D_d at $t = t_3$, and V_{C_x} begins to decrease. Although the primary voltage of the transformer is zero, the voltage on the secondary

side is due to C_x. This creates a difference between the voltages of the two windings of the transformer that appears across the primary leakage inductance as a counter voltage. In essence, this counter voltage is like a dc source that appears in the path of the primary current that causes the primary current to decrease. *This is the mechanism by which the transformer primary current can be extinguished.*

Mode 5 ($t_4 < t < t_5$) *Figure 2.7(e)*

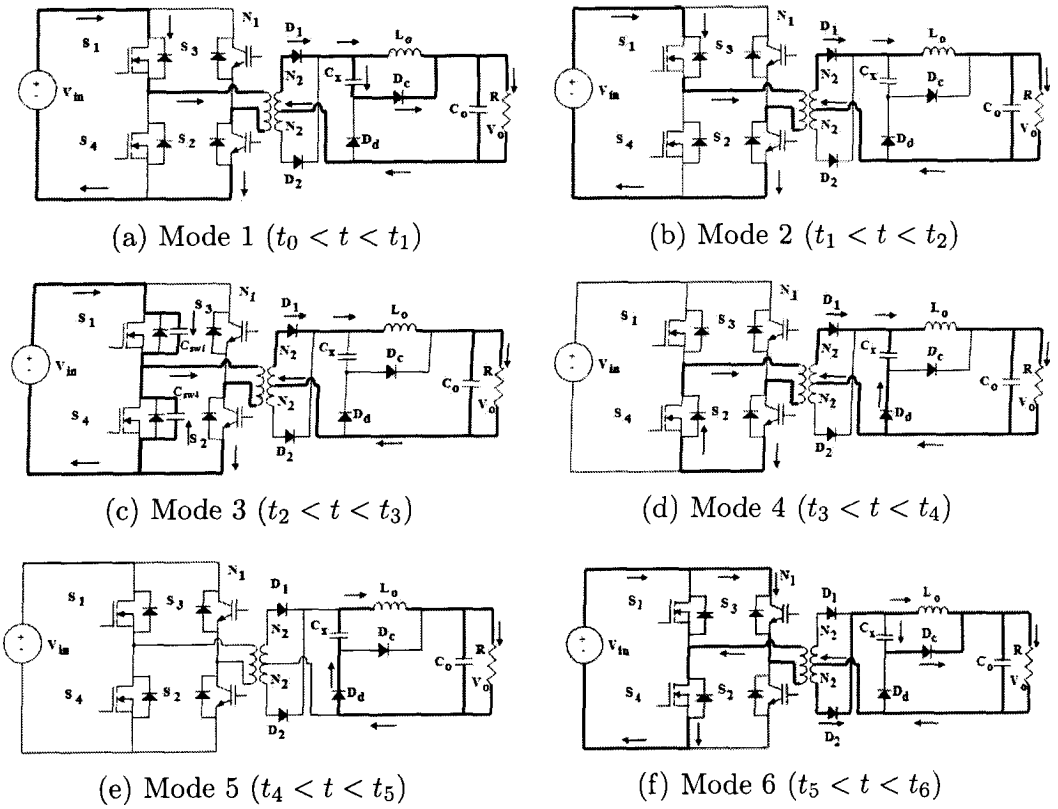
At $t = t_4$, there is no current flowing in the primary side of the transformer as it has been completely extinguished. On the secondary side, C_x continues to discharge via D_d until V_{C_x} becomes zero. Load current will now start to freewheel through the rectifier diodes D_1 and D_2 on the secondary side.

Mode 6 ($t_5 < t < t_6$) *Figure 2.7(f)*

At $t = t_5$, S_2 is turned off with ZCS as there is no current flowing in the transformer primary. After S_2 is completely off, S_3 is turned on with ZCS as well, since the leakage inductance of the transformer limits the rise of current in the switch. Current flows through S_3 and S_4 during this mode and the converter is in an energy transfer mode as another half-cycle begins.

The ZVZCS dc-dc full-bridge converter has the following characteristics, which should be noted:

- The converter can operate with the same phase shift PWM control method as the standard dc-dc PWM full-bridge converter. The output voltage is controlled



(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)

(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

(e) Mode 5 ($t_4 < t < t_5$)

(f) Mode 6 ($t_5 < t < t_6$)

Figure 2.7: Modes of operation of dc-dc ZVZCS full bridge PWM converter.

by phase-shifting the gating signals of the switches in one leg relative to those of the switches in the other.

- The switches in the leading converter leg operate with ZVS and those in lagging leg operate with ZCS. The leading leg is the leg whose switches turn on first during a half switching cycle and the lagging leg is the leg whose switches turn on second. In the modal sequence explained above, the leg with S_1 and S_4 is the leading leg and the leg with S_2 and S_3 is the lagging leg.

- Since the transformer primary current is extinguished when the converter is in a freewheeling mode, when there is no energy transfer taking place, energy losses caused by the current circulating in the primary during this time are eliminated.

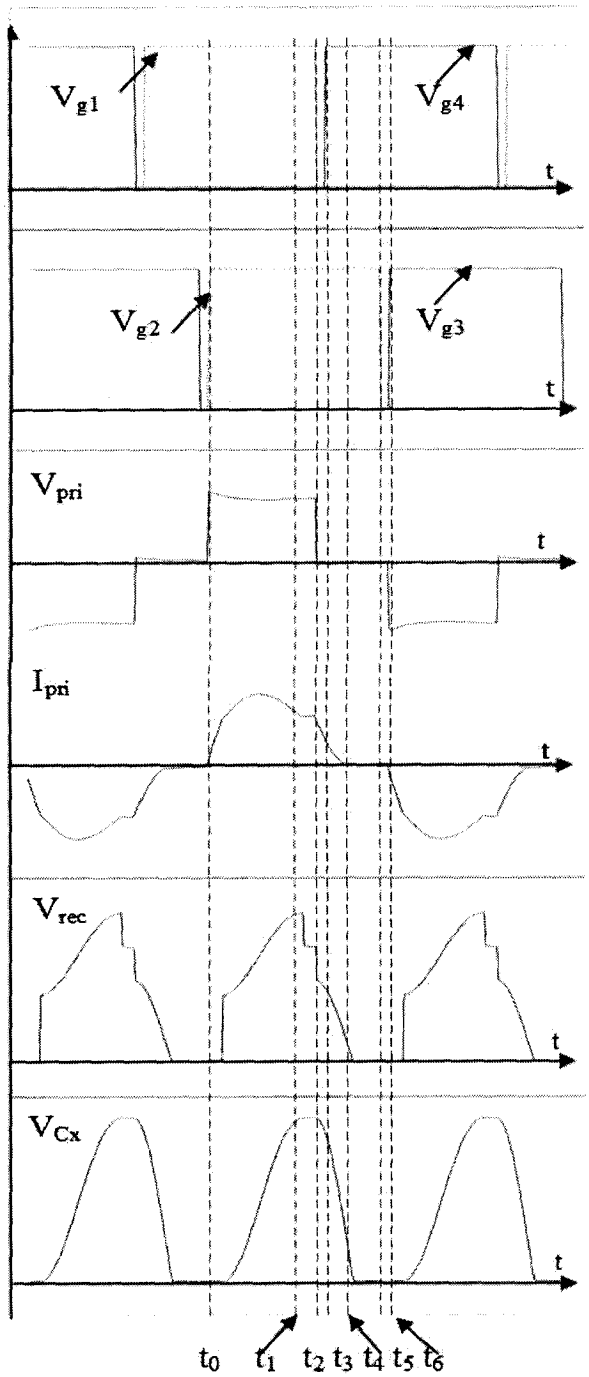


Figure 2.8: Steady state waveforms of dc-dc ZVZCS full bridge PWM converter.

2.4 Conclusion

In order to derive a three-phase single-stage ac-dc converter, the ac-dc front-end and the dc-dc full-bridge converters of a two-stage ac-dc converter must be combined. It was proposed that this be done by combining a three-phase, single switch, ac-dc buck converter with a dc-dc full-bridge converter and have the full-bridge converter act like the buck switch.

The conventional dc-dc full-bridge converter, however, is not suitable for this purpose because it has reverse current flowing through the anti-parallel diodes of its switches to the dc source whenever it exits a freewheeling mode of operation. Such a path cannot exist in a single-stage converter because there is no dc source across the input of the full-bridge section. A converter that does not have this issue is the zero-voltage-zero-current switching (ZVZCS) and it is this converter that will be combined with the ac-dc single switch buck converter to form the new three-phase, single-switch converter.

In this chapter, the operation of both the three-phase, single switch, ac-dc buck converter and that of a dc-dc zero-voltage-zero-current switched (ZVZCS) full-bridge converter were explained. This was done in preparation of the proposed three-phase single-stage converter, which will be presented in the next chapter of this thesis.

Chapter 3

A New Three-Phase Single-Stage Ac-Dc Converter

3.1 Introduction

In this chapter, the proposed three-phase single-stage ac-dc converter is introduced and its operation is discussed. The modes of operation that the converter goes through are explained in detail, the key equations that define its operation during these modes are derived, and the attractive features of the new converter are stated.

3.2 General Operating Principles

The converter shown in Figure 3.1 is the proposed single-stage ac-dc converter. It is basically a three-phase diode bridge rectifier with a three-phase L-C filter attached to a ZVZCS full-bridge converter with the full-bridge converter acting as the buck switch in a three-phase, single-switch buck rectifier. The ZVZCS full-bridge is almost the same as the conventional full-bridge converter except that it also has a passive circuit

that consists of a capacitor and two diodes that helps extinguish the transformer primary current.

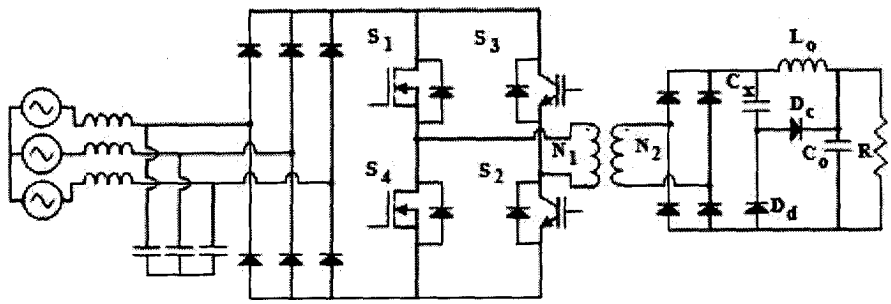


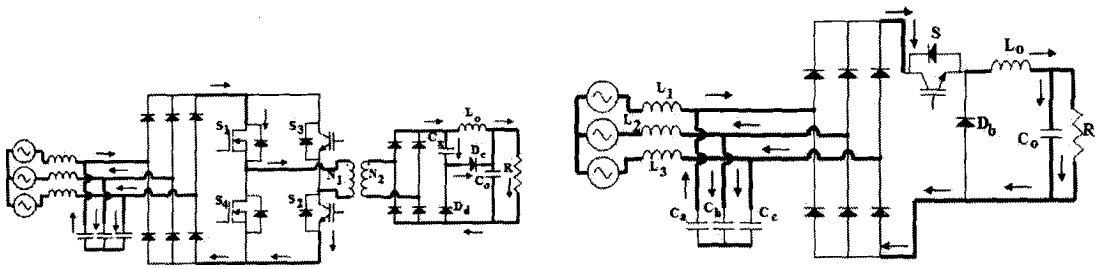
Figure 3.1: Proposed three-phase single-stage ac-dc converter with ZVZCS full-bridge.

The most important thing to note is that the full-bridge acts like the switch in the three-phase, single switch, ac-dc buck converter discussed in chapter 2. It can be seen in Figure 3.2 how the functioning of the full-bridge is analogous with the buck converter. When a diagonal pair of switches in the full-bridge is on it is considered as a power transfer mode and this is equivalent to the switch being on in the buck converter. This can be explained by the flow of currents of the converters as depicted in Figure 3.2(a).

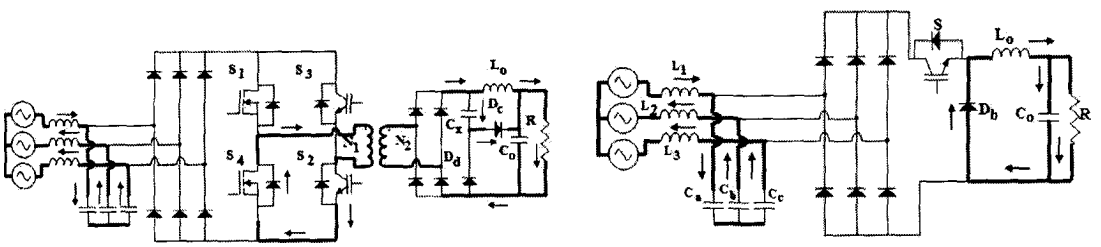
A mode of operation when no energy is transfer from input to output in the full-bridge can be considered a freewheeling mode and it's analogous to the switch in a buck converter being off. Input capacitors are charging with line currents and the freewheeling of the dc current is observable in both converters. Therefore the full-bridge section of the proposed converter can act as a buck switch because it is a ZVZCS converter that does not send reverse current back to the dc bus.

It should be noted that switches S_1 and S_4 are as being implemented with

MOSFETs in Figure 3.1 and switches S_2 and S_3 are shown as being implemented with IGBTs. This is because switches S_1 and S_4 operate with ZVS and switches S_2 and S_3 operate with ZCS. This will be explained in more detail in this thesis.



(a) Power Transfer Mode



(b) Freewheeling Mode

Figure 3.2: Comparison of the proposed converter to a three-phase single switch buck converter.

3.3 Modes of Operation

The proposed converter goes through six significant modes of operation at steady state during a half switching cycle. The modes are explained with the circuit diagrams shown in Figure 3.3 and the waveforms shown in Figure 3.4. The following assumptions are made for simplicity.

- The switching cycle where $V_a = V_{ph,pk}$ (peak phase voltage), $V_b = V_c = -V_{ph,pk}/2$ is considered.

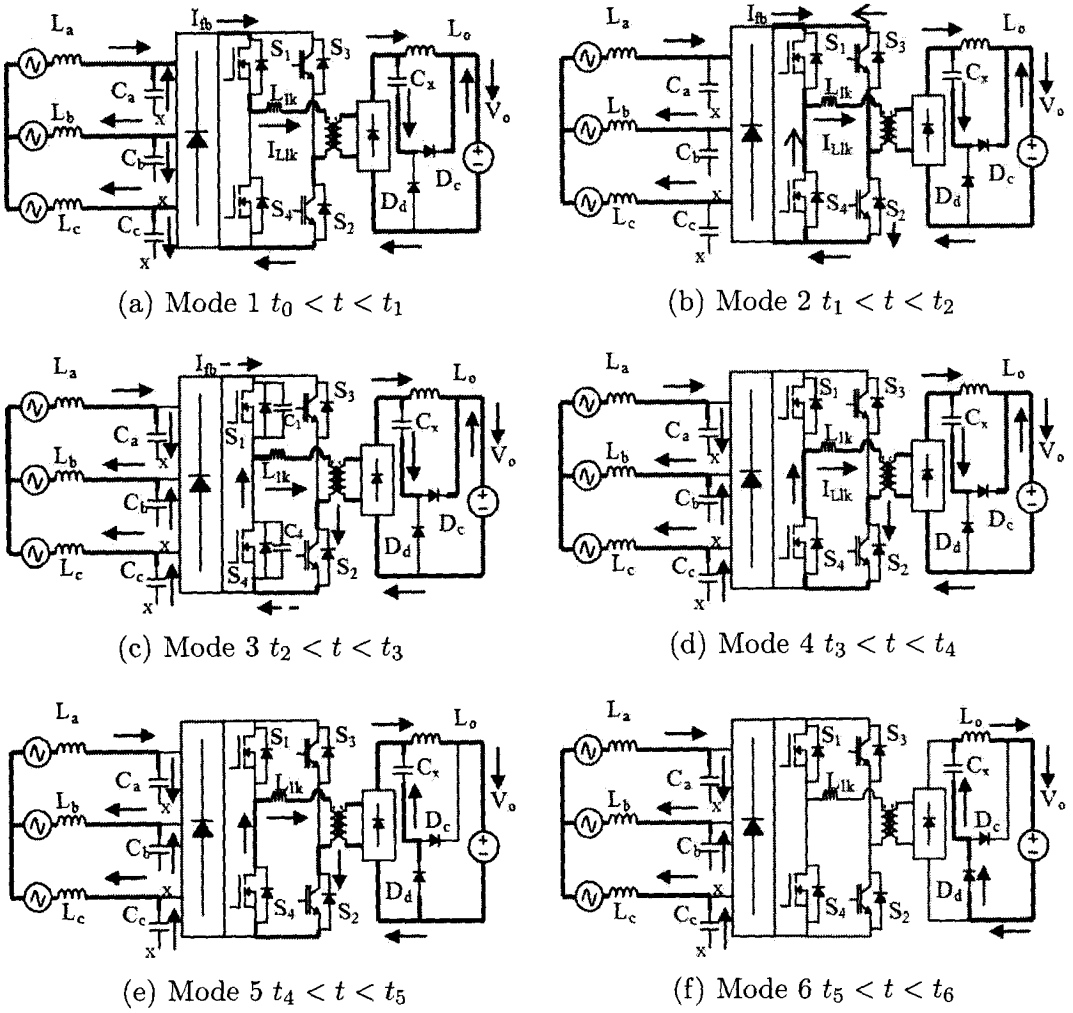
- When equations are stated for input side, only phase-a is considered from which phases b and c relationships can be derived easily.
- The line frequency is lower with respect to the switching frequency; therefore, line currents and voltages are constants during the switching cycle.
- The magnetizing current in the transformer is negligible.
- The output capacitor and resistive load are combined, and it is shown as a voltage source.
- The current in the output filter L_o is ripple free.

*Mode*1$(t_0 < t < t_1)$ *Figure: 3.3(a)*

Before $t = t_0$, S_1 is on and all other switches are off, the input capacitors are being charged, the auxiliary circuit capacitor C_x is at its minimum voltage $V_{C_{x,min}}$ and there is no current flowing in the full-bridge. At $t = t_o$, S_2 is turned on with ZCS and current I_{fb}, starts flowing into the full-bridge. This current is the result of the discharging of the input capacitors through the switches and the transformer primary $I_{L_{lk}}$. The transformer secondary current also charges the auxiliary circuit capacitor, C_x through diode D_c during this mode.

The input capacitors discharge during Mode 1 from its initial value $V_{C_{a0}}$ until V_{C_a} reaches zero at $t = t_1$. The difference between the current in the leakage inductor L_{lk} and line current gives the time varying current injected by input capacitor C_a. The discharging of input capacitor C_a can be expressed as

$$I_{L_{lk}} - I_a = C_a \frac{dV_{C_a}}{dt} \tag{3.1}$$



(a) Mode 1 $t_0 < t < t_1$

(b) Mode 2 $t_1 < t < t_2$

(c) Mode 3 $t_2 < t < t_3$

(d) Mode 4 $t_3 < t < t_4$

(e) Mode 5 $t_4 < t < t_5$

(f) Mode 6 $t_5 < t < t_6$

Figure 3.3: Modes of converter operation.

V_{Ca} is zero by the end of this mode. L_{lk} interacts with the input capacitors, and if the voltage across it is $V_{L_{lk}}$ then the voltage-current relationship of L_{lk} is given by

$$V_{L_{lk}} = L_{lk}\frac{dI_{L_{lk}}}{dt} \tag{3.2}$$

The voltages that are impressed across the dc bus of the full bridge and across

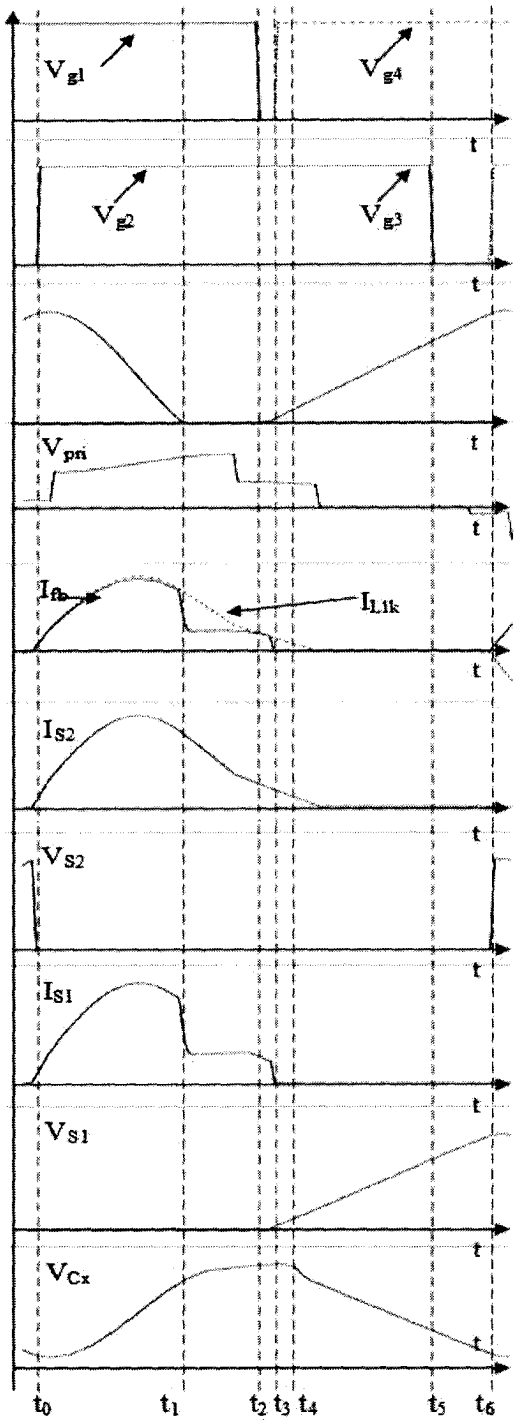


Figure 3.4: Proposed converter typical waveforms.

the primary winding are V_{fb} and V_p respectively where V_{fb} is the triangular dc input voltage to the full-bridge. The difference between V_{fb} and V_p is $V_{L_{lk}}$ according to Kirchoff's law and given in equation (3.3).

$$V_{fb} - V_p = L_{lk}\frac{dI_{L_{lk}}}{dt} \tag{3.3}$$

The voltage across the bus at $t = t_0$ is the line-line input capacitor voltage. Therefore, the dc bus voltage is $\sqrt{3}$ times capacitor voltage and equation (3.3) can be rewritten as

$$\sqrt{3}V_{C_a} - V_p = L_{lk}\frac{dI_{L_{lk}}}{dt} \tag{3.4}$$

The relationship between the transformer primary voltage V_p and the secondary voltage V_s in terms of voltage is

$$V_p = \frac{V_s}{n} \tag{3.5}$$

where n, is the ratio between secondary turns to primary turns of the transformer. V_s is made up of the voltage drop across auxiliary capacitor C_x and output voltage V_o. Equation (3.4) can be arranged to give V_p in terms of variable V_{C_x} and the known values V_o and n.

$$V_p = \frac{V_{C_x} - V_o}{n} \tag{3.6}$$

When equation (3.4) and equation (3.5) are combined together and V_p is removed, a relationship between the key variables V_{C_a}, V_{C_x} and $I_{L_{lk}}$ can be

obtained as

$$\sqrt{3}V_{C_a} - \left(\frac{V_{C_x} - V_o}{n}\right) = L_{lk}\frac{dI_{L_{lk}}}{dt} \tag{3.7}$$

The boundary condition for $I_{L_{lk}}$ is

$$I_{L_{lk0}} = 0.$$

On the transformer secondary side, C_x is charged by a current that is the difference of the reflected transformer primary current (secondary current) and load current I_{L_o} as given by the following.

$$I_{C_x} = C_x\frac{dV_{C_x}}{dt} \tag{3.8}$$

$$\frac{I_{L_{lk}}}{n} - I_{L_o} = C_x\frac{dV_{C_x}}{dt} \tag{3.9}$$

Let the value of V_{C_x} at $t = t_1$ be $V_{C_{x1}}$. All the above relationships yield to three variables V_{C_a}, V_{C_x} and $I_{L_{lk}}$, and three equations (3.1), (3.7) and (3.9). Combining and simplifying these equations gives the following differential equation for V_{C_a}.

$$-C_aC_xL_{lk}n\frac{d^3V_{C_a}}{dt^3} + (\sqrt{3}nC_x - \frac{C_a}{n})\frac{dV_{C_a}}{dt} - \frac{I_a}{n} + I_{L_o} = 0 \tag{3.10}$$

The boundary condition for V_{C_a} is

$$V_{C_{a1}} = 0.$$

Mode 2 ($t_1 < t < t_2$) *Figure: 3.3(b)*

At $t = t_1$, the input capacitors are all fully discharged and the dc bus voltage is zero while capacitor C_x continues to be charged. Since the input capacitors no longer provide current to the full-bridge, I_{fb}, is constant and equal to line current I_a.

There is a difference between the current flowing out of the diode bridge I_{fb}, and that flowing in the transformer primary $I_{L_{lk}}$, which is the greater current. As a result, the body diodes of switches S_3 and S_4 start to conduct to make up this difference in current. During this mode, the transformer primary current drops due to the presence of C_x in the secondary, which impresses a counter voltage across the secondary that is reflected in the primary and that reduces the current $I_{L_{lk}}$. Sometime during this mode, the transformer primary current has dropped to a level matching that provided from the input bridge so that the body diodes of S_3 and S_4 no longer need to conduct. Capacitor C_x continues to charge. The mode ends at $t = t_2$ when S_1 is turned off.

The input capacitor voltages are zero during Mode 2

$$V_{C_a} = 0; \quad \forall\, t \in (t_1, t_2) \tag{3.11}$$

For the body diodes of S_3 and S_4 to conduct in the forward direction, their respective switch capacitances must be discharged first. For simplicity, it is assumed that the discharging of the capacitors happens at the start of Mode 2 (during a short time of Δt) by a constant current. Since the transformer, primary current cannot change suddenly, the body diodes start to conduct im-

mediately after the switch capacitors are discharged and I_d is equal to the same current. This phenomenon can be expressed as,

$$I_d = C_{sw}\frac{dV_{sw}}{dt} \tag{3.12}$$

where I_d denotes the current conducted by the each body diode of switches S_3 and S_4, C_{sw} is the switch capacitance and V_{sw} is the voltage across a switch. Assuming linear discharge of the switch capacitors, equation (3.12) becomes

$$I_d = C_{sw}\frac{\Delta V_{sw}}{\Delta t} \tag{3.13}$$

$$I_d = C_{sw}\frac{V_{fb} - 0}{\Delta t} \tag{3.14}$$

$$I_d = C_{sw}\frac{V_{fb0}}{\Delta t} = 1.73\frac{C_{sw}V_{C_{a0}}}{\Delta t} \tag{3.15}$$

The current in the transformer primary at $t = t_1$ is made up of the line current I_a and the currents coming from body diodes. $I_{L_{lk}}$ at $t = t_1$ is

$$I_{L_{lk1}} = I_a + 2I_d \tag{3.16}$$

Substituting equation (3.15) into equation (3.16) gives

$$I_{L_{lk1}} = I_a + 3\frac{\left(V_{C_{a0}}C_{sw}\right)}{\Delta t} \tag{3.17}$$

V_{fb} is zero during the mode but V_{C_x} is non-zero (i.e. during this mode, both

V_s and V_p are non-zero as well). However V_{fb}, the input to full-bridge is zero. Thus, there should be a counter voltage across the leakage inductor (according to Kirchoff's law). The presence of counter voltage across the L_{lk} diminishes the primary current as stated in equation (3.18)

$$-\frac{V_{C_x}}{n} = L_{lk}\frac{dI_{L_{lk}}}{dt} \tag{3.18}$$

C_x continues to charge as shown by equation (3.8) and equation (3.9), and reaches $V_{C_{x2}}$ at $t = t_2$. Simplifying equation (3.9) and equation (3.18) gives the following differential equation for $I_{L_{lk}}$.

$$nC_xL_{lk}\frac{d^2I_{L_{lk}}}{dt^2} + \frac{I_{L_{lk}}}{n} - I_{L_o} = 0 \tag{3.19}$$

$I_{L_{lk2}} = I_a$ at $t = t_2$.

Mode 3 ($t_2 < t < t_3$) *Figure: 3.3(c)*

At $t = t_2$, the capacitors across S_1 and S_4 begin to charge and discharge respectively within a short duration. The line currents start to charge the input capacitors. The current flowing in the full-bridge continues to decrease due to the presence of the counter voltage across the transformer primary. Since the full-bridge current drops below that coming from the input inductors, current starts to flow through the input capacitors and they begin to charge; C_x, is charged via D_c. During this mode, the switch capacitor of S_4 is fully discharged and its body diode starts to conduct.

Since the input capacitors are charged by the line currents,

$$I_{C_a} = C_a \frac{dV_{C_a}}{dt} \tag{3.20}$$

$$I_a = C_a \frac{dV_{C_a}}{dt} \tag{3.21}$$

Solving equation (3.21) gives

$$V_{C_a} = \frac{I_a}{C_a} t \tag{3.22}$$

and the initial condition for V_{C_a} is $V_{C_{a0}} = 0$. The primary current continues to decrease as shown by equation (3.18), and C_x continues to charge as shown by equation (3.9) and reaches $V_{C_{x3}}$ at $t = t_3$. The differential equation that expresses $I_{L_{lk}}$ for this mode is the same as equation (3.19). At $t = t_3$, $I_{L_{lk}}(t = t_3) = I_{L_{lk3}}$.

Mode 4 ($t_3 < t < t_4$) *Figure: 3.3(d)*

At $t = t_3$, S_4 is tuned on with ZVS. The transformer primary current freewheels through the two bottom switches and decrease due to the counter voltage impressed by C_x. Since there is no current coming out of the input diode bridge, all the input inductors' currents are flowing through the input capacitors and continues to charge them.

The mode ends when diode D_d begins to conduct and help discharge C_x. This is because the transformer primary current continued to fall due to the counter

voltage impressed on the transformer by C_x and the current coming out of the transformer secondary is less than the output inductor current. D_d conducts the difference of these two currents. D_c is turned off softly.

The input capacitors continue to charge according to equation (3.22) and V_{C_a} reaches a value of $V_{C_{a4}}$. The primary current continues to decrease as explained in equation (3.18) and equals the reflected load current nI_{L_o}. C_x charges and reaches its peak voltage $V_{C_{x,pk}}$ at $t = t_4$. Equation (3.19) continues to define this mode. At $t = t_4$, $I_{L_{lk}} = nI_{L_o}$.

Mode 5 ($t_4 < t < t_5$) *Figure: 3.3(e)*

At $t = t_5$, there is no current flowing in the transformer primary as it has been extinguished by the reflected counter voltage. This allows S_2 to be turned off with ZCS. It should be noted that in a practical circuit, there may be some very small amount of magnetizing current $I_{mag}(t_5)$, from the transformer in S_2 when it is turned off so that the turn-off may be almost but not completely ZCS and some additional snubbing may be needed for this switch and for S3. The input capacitors continue to be charged and C_x discharges via D_d.

The transformer primary current continues to decrease with an initial value of nI_{L_o} and reaches zero. C_a charges up according to equation (3.22) and reaches $V_{C_{a5}}$ by $t = t_5$. Equation (3.19) continues to define this mode. At $t = t_5$, $I_{L_{lk}}(t = t_5) = 0$.

Mode 6 ($t_5 < t < t_6$) *Figure: 3.3(f)*

At $t = t_5$, the primary current is zero and C_x continues to discharge as the entire

load current flows through it. While this is happening, the input capacitors continue to charge. At $t = t_6$, S_3 is turned on with ZCS and current start to flow through S_3 and S_4, which was turned on earlier after t_4. The converter will then go through the same modes of operation as described above for the remaining half cycle.

The input capacitor C_a reaches its peak voltage at $t = t_6$. The converter is in steady-state therefore the voltage of C_a at the end of the half switching cycle is same as the value it had at the start i.e., at $t = t_0$. Input capacitors will start to discharge again at $t = t_6$, which is the start of the next half cycle.

$$V_{C_a}(t = t_6) = \frac{I_a}{C_a}(1 - D)\frac{T_s}{2} = V_{C_{a,pk}} \tag{3.23}$$

There is no current in the primary winding during Mode 6. C_x discharges with a constant current I_{L_o} as given below

$$-I_{L_o} = C_x \frac{dV_{C_x}}{dt} \tag{3.24}$$

Equation (3.24) is solved to give

$$V_{C_x} = -\frac{I_{L_o}}{C_x} t \tag{3.25}$$

where at $t = t_6$, $V_{C_{x6}} = V_{C_{x,min}}$

3.4 Converter Features

The proposed converter has the following features:

- The converter can operate with standard phase-shift PWM control and be implemented with any standard, commercially available, phase-shift PWM control IC without a need for input current sensing.
- The input currents are continuous (i.e., they will never become zero during a switching cycle) so that the input current does not have a very large ripple as it would if they were discontinuous and thus the need for additional input filtering is avoided.
- Since the input currents are continuous, the semiconductor peak current stresses are not excessive. The peak voltage stresses are comparable to those found in a three-phase ac-dc boost converter.
- The converter operates with fewer conduction losses as it does not have the circulating current that conventional PWM full-bridge converters have when they are in a freewheeling mode of operation.
- The converter is inexpensive. It only has four active switches and does not need additional hardware to perform input power factor correction.
- The converter is very simple, which makes the converter especially attractive to practising switch-mode power supply design engineers who may lack knowledge of the complex theory and hardware needed to control a three-phase rectifier.

3.5 Conclusion

In this chapter, the proposed three-phase single-stage ac-dc converter was introduced, and its operation was discussed. The modes of operation that the converter goes through were explained in detail, the key equations that define its operation during these modes were derived and the attractive features of the new converter were stated. The modal equations that were derived in this chapter will be used later in this thesis to analyze and design the proposed converter.

Chapter 4

Converter Analysis

4.1 Introduction

A steady-state analysis of the proposed converter is performed in this chapter. A steady-state is where the components' currents and voltages at the end of the switching cycle are same as the started values. The purpose of the analysis is to derive expressions and determine relations of key converter parameters to understand the steady-state characteristics of the converter and to help establish a procedure for its design, which will be done in the next chapter.

4.2 Input Capacitor Relations

4.2.1 Relation Between Input Capacitor Value and Peak Switch Voltage

The input capacitors voltages of the proposed converter must be discontinuous (Figure 2.4) for the converter in order for the input inductors line currents to be sinusoidal and

in phase with the input phase voltages so that the converter can operate with a very good power factor. If the voltage-current equation for discharging input capacitors is considered

$$I_{C_a} = -C_a \frac{dV_{C_a}}{dt} \tag{4.1}$$

or

$$\frac{dV_{C_a}}{dt} = -\frac{I_{C_a}}{C_a} \tag{4.2}$$

where charging of V_{C_a} is expressed as

$$I_{C_a} = C_a \frac{dV_{C_a}}{dt} \tag{4.3}$$

$$I_{a,pk} = C_a \left(\frac{V_{C_{a,pk}} - 0}{(1-D)\frac{T_s}{2}} \right) \tag{4.4}$$

It is clear that lowering the capacitor value will increase the rate of change in the voltage. In other words, smaller values of C_a ($C_a = C_b = C_c$) make it more likely that the input capacitors operate in discontinuous voltage mode (DVM) throughout the line cycle.

C_a, however, cannot be too small as it determines the peak voltage that is impressed across the input of the full-bridge, and thus the peak voltage stress of the switches. Unlike the dc bus voltage of a conventional dc-dc full-bridge that has a dc source connected across the dc bus at the input of the full-bridge, the dc bus voltage of the proposed converter is not a constant dc voltage because it has no bus capacitor.

In fact, it is a train of triangular pulses as shown in Figure 4.1. The maximum peak dc bus voltage, $V_{bus,pk}$, is the maximum peak voltage stress of the converter switches.

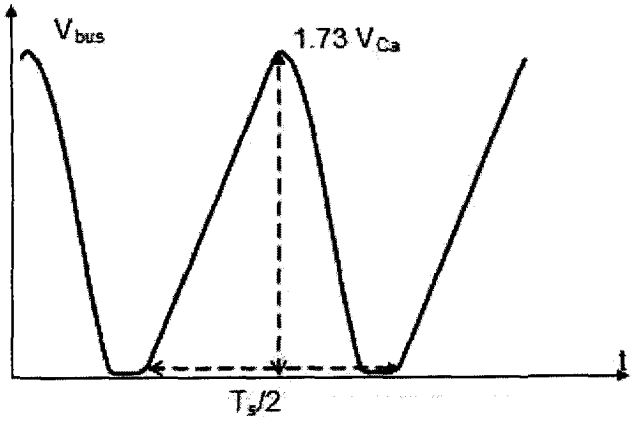


Figure 4.1: Bus voltage of the proposed converter when input capacitors in DVM.

C_a charges at a constant rate using entire line current during a freewheeling mode of operation. When the line current rises, the peak voltage to which C_a charges also increases; therefore, the maximum voltage across C_a will result during the switching cycles in which line current is maximum (i.e., I_a equals, $I_{a,pk}$). This can be expressed as

$$V_{C_{a,pk}} = \frac{I_{a,pk}(1-D)\frac{T_s}{2}}{C_a} \tag{4.5}$$

The value of C_a and thus $V_{C_{a,pk}}$ determines the maximum peak voltage that appears across the dc bus (the input of the full-bridge). This relationship can be written as

$$V_{bus,pk} = \sqrt{3}V_{C_{a,pk}} \simeq 1.73V_{C_{a,pk}} \tag{4.6}$$

with the $\sqrt{3}$ factor coming into play since V_{C_a} is a line-neutral or phase voltage and $V_{bus,pk}$ is the peak line-to-line voltage. Equation (4.6) can be rewritten by sub-

stituting equation (4.5) into equation (4.6), with $V_{bus,pk}$ being the maximum peak voltage stress of the switches.

$$V_{bus,pk} = \sqrt{3}\left(\frac{I_{a,pk}(1-D)\frac{T_s}{2}}{C_a}\right) \tag{4.7}$$

The conflicting criteria of having an excellent input power factor and not having excessive switch peak voltage stress must be considered when implementing the proposed converter. It is possible that the input currents may not be perfectly sinusoidal, but they must meet the appropriate standards for input line current harmonic content if it is to be used in an industrial application.

4.2.2 Relation Between Input Capacitor Value and Output Dc Voltage

The value of C_a also affects the output dc voltage since C_a affects the shape of the dc bus voltage waveform and the dc bus voltage is dependent on the average value of this waveform. In a standard dc-dc full-bridge converter, the ratio of output voltage V_o to dc bus voltage or input voltage V_{in} is directly proportional to the product of the turns ratio n and the duty ratio D. This can be expressed as.

$$\frac{V_o}{V_{in}} = nD \tag{4.8}$$

$$V_o = nDV_{bus,ave} \tag{4.9}$$

where $V_{bus,ave}$ is the average bus voltage. It is assumed without loss of generality that V_{in} in equation (4.8) can be replaced by $V_{bus,ave}$ to obtain equation (4.9),

which yields V_o in terms of $V_{bus,ave}$, n and D. Equation (4.10) shows how V_{C_a} is related to D and V_o.

$$D = \frac{V_o}{\left(\sqrt{3}n\frac{V_{C_{a,pk}}}{2}\right)} \tag{4.10}$$

4.2.3 Relation Between Input Capacitors C_a, C_b, C_c and Duty Ratio D

The main focus of the analysis is to establish a relationship between D and C_a. This analysis is based on the study done for a single-phase, single switch, ac-dc buck converter ([25]) and has been developed further to analyze the proposed converter.

4.2.3.1 Equivalent Single-Phase Circuit

The analysis is based on the use of a simplified equivalent circuit to determine an equivalent resistance value (ratio of input voltage to input current) to determine equations for output energy (energy supplied to load resistor for a certain period of time) and input energy (based on the sum of the three-phase products of phase voltage and line current), that can then be used to determine the ratio of output voltage to input voltage for particular values of D and C_a.

The simplified equivalent circuit is shown in Figure 4.2 and consists of a dc voltage source (V_{in}) representing a phase voltage for a given switching cycle), an input L-C filter and a conventional full-bridge converter. The analysis will proceed by finding the input resistance for this circuit in terms of certain key parameters, which will then be converted to the input resistance per phase for the proposed

three-phase ac-dc converter. For the sake of simplicity, the following assumptions have been made:

- The converter is ideal and thus lossless.
- The converter operates under steady-state conditions.
- The analysis does not take the secondary ZVZCS auxiliary circuit into account since it is based on an examination of input and output energy, which is not affected by the auxiliary circuit. Therefore this auxiliary circuit is neglected.
- The switching cycle when $V_a = V_{ph,pk}, V_b = V_c = -V_{ph,pk}/2$ is considered.
- The line frequency ($f_l = 60Hz$) is very low compared to the switching frequency. Therefore input ac voltages and currents can be considered as constants during a given switching cycle.
- The input inductor (L) in Figure 4.2 is equal to the per phase inductance in the proposed converter and the input capacitor (C) is equal to 2/3 times the input capacitor used in the three-phase converter (C_a). This is because C in equivalent circuit is between the phase and the neutral whereas C_a, C_b and C_c in the proposed converter are in a Y-connection [14].
- The input capacitor voltages are discontinuous throughout the entire line cycle.
- The output inductor current I_{L_o} is continuous.
- Switch S_1 is on while the other switches are off prior to start of Mode 1.

It should be noted that the secondary side auxiliary circuit that forces the transformer primary current to zero in the freewheeling mode of operation and thus

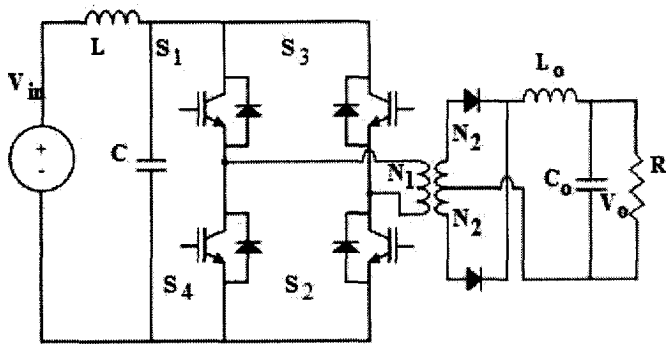
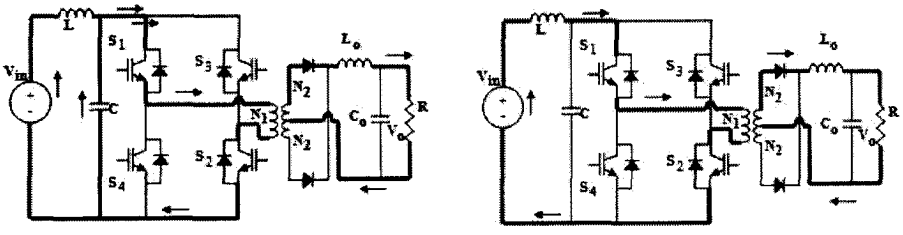


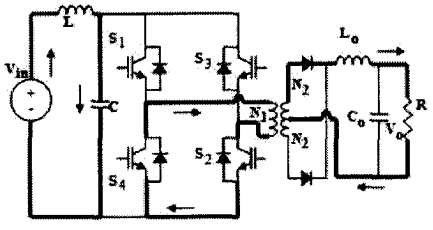
Figure 4.2: Dc-dc full bridge converter with L-C filter.

keeps any current from flowing into C when the converter is exiting a freewheeling mode of operation is not shown. It will be assumed for the equivalent circuit that the full-bridge circuit is like a buck switch and there is no reverse current entering C. What is of interest is how the input L-C section of the equivalent circuit behaves.

The significant modes of operation that the converter in Figure 4.2 goes through during a half switching cycle are shown in the circuit diagrams of Figure 4.3.



(a) Mode 1 (b) Mode 2



(c) Mode 3

Figure 4.3: Steady state modes of operation of the single-phase equivalent circuit.

4.2.4 Converter Input Resistance

4.2.4.1 Equivalent Input Resistance of the Simplified Equivalent Circuit

The first step in the analysis is to determine a mathematical expression for the equivalent input resistor R_{in} of the converter. R_{in} is not an actual resistance, but is defined as the ratio of input voltage to input current; it can be derived as follows.

Similar to equation (4.3) and equation (4.4), equations relating input current and input capacitor voltage can be expressed as

$$I_C = C\frac{dV_C}{dt} \tag{4.11}$$

$$I_{in} = C\left(\frac{V_{C,pk} - 0}{(1-D)\frac{T_s}{2}}\right) \tag{4.12}$$

where I_{in} is the input current from the source and $V_{C,pk}$ is the peak voltage across C. Equation (4.12) can be rearranged as

$$V_{C,pk} = \frac{I_{in}}{C}(1-D)\frac{T_s}{2} \tag{4.13}$$

to give an expression for $V_{C,pk}$. At steady state, over a half switching cycle, the average voltage across L is zero. Therefore, the average voltage across C is equal to V_{in} and the following expression can be obtained by considering the triangular waveform of the voltage across C,V_C

$$V_{in} = \frac{\left(\frac{V_{C,pk}}{2}\left(D_1\frac{T_s}{2} + \frac{T_s}{2}(1-D)\right)\right)}{\frac{T_s}{2}} \tag{4.14}$$

Or

$$V_{in} = \frac{V_{C,pk}}{2}(1 + D_1 - D) \tag{4.15}$$

where D_1 is the normalized discharging time of C, the time taken by C to discharge completely. During steady state operation, the average voltage across L_o is zero; therefore, the average voltage at the output of the secondary side rectifier diodes ($V_{rec,ave}$) is the same as V_o.

$$V_o = V_{rec,ave} = V_{s,ave} = nV_{p,ave} \tag{4.16}$$

In equation (4.16), $V_{s,ave}$, and $V_{p,ave}$ are the average values of absolute value waveforms of transformer secondary and the primary winding voltages respectively (note that V_s and V_p are actually square ac waveforms, but the negative portions have been "flipped" positive). $V_{p,ave}$ can be expressed as

$$V_{p,ave} = \frac{\left(\frac{V_{C,pk}}{2} D_1 \frac{T_s}{2}\right)}{\frac{T_s}{2}} \tag{4.17}$$

$$V_{p,ave} = \frac{V_{C,pk}}{2} D_1 \tag{4.18}$$

From equation (4.18) and equation (4.16), the following relation is obtained

$$V_o = n\frac{V_{C,pk}}{2} D_1 \tag{4.19}$$

An expression for the normalized discharge time D_1 can be derived from equation (4.15) and equation (4.19)

$$\frac{V_o}{V_{in}} = \frac{nD_1}{1 - D + D_1} \tag{4.20}$$

$$D_1 = \frac{V_o(1 - D)}{nV_{in} - V_o} \tag{4.21}$$

R_{in} can be obtained by ratio between V_{in} and I_{in} using equation (4.13), equation (4.19), and equation (4.48)

$$R_{in} = \frac{(1 - D + D_1)(1 - D)T_s}{4C} \tag{4.22}$$

By substituting equation (4.21) into equation (4.22) gives

$$R_{in} = \frac{nV_{in}(1 - D)^2 T_s}{4C(nV_{in} - V_o)} \tag{4.23}$$

4.2.4.2 Equivalent Input Resistances of the Proposed Three-Phase Converter

Equation (4.23) is the equivalent input resistance for the simplified converter. The next step in the analysis is to find the equivalent input resistances of the proposed three-phase converter, which is shown in Figure 4.4. Since it has been assumed that V_a is equal to the positive peak phase voltage and V_b and V_c are equal to the half of the negative peak phase voltage-a. $\frac{\pi}{6}$ ac line interval $\left[\frac{\pi}{3}, \frac{\pi}{2}\right]$ is considered for the purposes of integration without loss of generality.

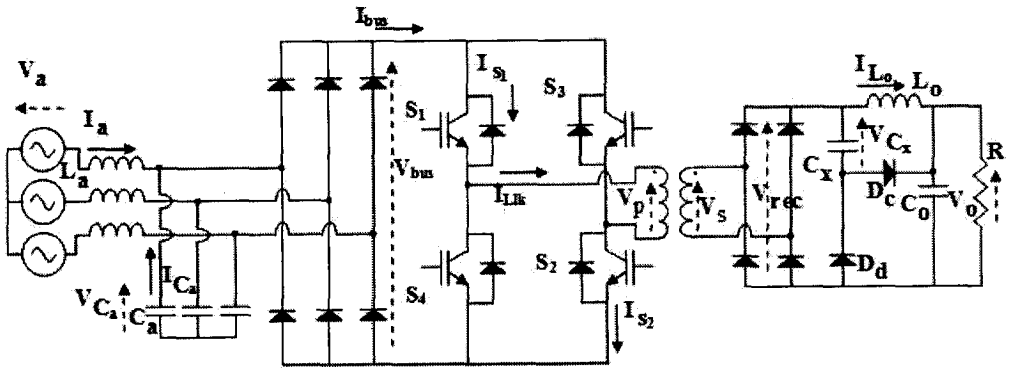


Figure 4.4: Proposed converter.

The balanced three phase voltages $V_a(t), V_b(t) and V_c(t)$ during a period $\theta = \omega_l t = \left[\frac{\pi}{3}, \frac{\pi}{2}\right]$ can be given as,

$$V_a(t) = V_{pk} sin\left(\omega_l t\right) \tag{4.24}$$

$$V_b(t) = V_{pk} sin\left(\omega_l t - \frac{2\pi}{3}\right) \tag{4.25}$$

$$V_c(t) = V_{pk} sin\left(\omega_l t - \frac{4\pi}{3}\right) \tag{4.26}$$

In equation (4.24)-equation (4.26), V_{pk} is the peak phase voltage; ω_l is the line angular velocity. The instantaneous input resistance per phase can be found based on equation (4.23). The V_{in} of equation (4.23) is replaced by the relevant instantaneous phase voltage.

$$R_a(t) = \frac{nT_s}{4C}(1-D)^2 \left(\frac{V_{pk} sin\left(\omega_l t\right)}{nV_{pk} sin(\omega_l t) - V_o}\right) \tag{4.27}$$

$$R_b(t) = \frac{nT_s}{4C}(1-D)^2 \left(\frac{V_{pk} sin\left(\omega_l t - \frac{2\pi}{3}\right)}{nV_{pk} sin(\omega_l t - \frac{2\pi}{3}) - V_o} \right) \tag{4.28}$$

$$R_c(t) = \frac{nT_s}{4C}(1-D)^2 \left(\frac{V_{pk} sin\left(\omega_l t - \frac{4\pi}{3}\right)}{nV_{pk} sin(\omega_l t - \frac{4\pi}{3}) - V_o} \right) \tag{4.29}$$

$R_a(t)$, $R_b(t)$ and $R_c(t)$ refer to the phase resistances. By Ohm's law, currents $I_a(t)$, $I_b(t)$ and $I_c(t)$ can be found by the ratio between voltage to resistance in each phase.

$$I_a(t) = \frac{\left(nV_{pk} sin(\omega_l t) - V_o\right)}{\frac{nT_s(1-D)^2}{4C}} \tag{4.30}$$

$$I_b(t) = \frac{\left(nV_{pk} sin\left(\omega_l t - \frac{2\pi}{3}\right) - V_o\right)}{\frac{nT_s(1-D)^2}{4C}} \tag{4.31}$$

$$I_c(t) = \frac{\left(nV_{pk} sin\left(\omega_l t - \frac{4\pi}{3}\right) - V_o\right)}{\frac{nT_s(1-D)^2}{4C}} \tag{4.32}$$

The input instantaneous power per phase can be found by the multiplication of instantaneous voltage and current terms.

4.2.4.3 Energy Relations

By integrating the power of each input phase over the specified time period of $\frac{\pi}{6}$ rad, the input energy per phase is derived. The first step in the integration process is to

obtain the energy given by phase-a into the converter, E_a;

$$E_a(t) = \int_{t_1}^{t_2} v_a(t) i_a(t) dt \tag{4.33}$$

$$E_a(\theta) = \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} v_a(\theta) i_a(\theta) d\theta \tag{4.34}$$

$$E_a(\omega_l t) = \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} V_{pk} sin(\omega_l t) \left(\frac{\left(nV_{pk} sin(\omega_l t) - V_o\right)}{\left(\frac{nT_s(1-D)^2}{4C}\right)} \right) d(\omega_l t) \tag{4.35}$$

$$E_a(\omega_l t) = \left(\frac{4C}{nT_s(1-D)^2}\right) \int_{\frac{\pi}{3}}^{\frac{\pi}{2}} \left(nV_{pk}{}^2 sin^2(\omega_l t) - V_o V_{pk} sin(\omega_l t) \right) d\omega_l t \tag{4.36}$$

Equation (4.36) can be solved to give

$$E_a = \left(\frac{4C}{nT_s(1-D)^2}\right) \left(\frac{nV_{pk}{}^2}{2} \left(\frac{\pi}{6} + \frac{\sqrt{3}}{4} \right) - \frac{V_{pk} V_o}{2} \right) \tag{4.37}$$

The details of this integration are shown in Appendix1 A.1.1 Input Energy. In a similar manner, expressions for E_b and E_c, which are the energy inputs of phases b and c respectively, can be determined from equation (4.25), equation (4.31) and equation (4.26), equation (4.32) to be

$$E_b = \left(\frac{4C}{nT_s(1-D)^2}\right) \left(\frac{nV_{pk}{}^2}{2} \left(\frac{\pi}{6} \right) + V_{pk} V_o \left(\sqrt{3} - 1 \right) \right) \tag{4.38}$$

$$E_c = \left(\frac{4C}{nT_s(1-D)^2}\right)\left(\frac{nV_{pk}{}^2}{2}\left(\frac{\pi}{6}-\frac{\sqrt{3}}{4}\right)+V_o\left(1-\frac{\sqrt{3}}{2}\right)\right) \tag{4.39}$$

The total energy input to the converter by the three-phases for period of $\frac{\pi}{6}$ rad, is obtained by the summation of equation (4.37)-equation (4.39).

$$E_{in} = \frac{\pi C V_{pk}{}^2}{T_s(1-D)^2} \tag{4.40}$$

where E_{in} denotes total instantaneous input energy. The energy supplied to the load R during the same duration $\frac{\pi}{6}$ rad is

$$E_{out} = \frac{\pi}{6}.\frac{V_o{}^2}{R} \tag{4.41}$$

If η is the efficiency of the converter, then the relationship between input and output energies is

$$E_{out} = \eta E_{in} \tag{4.42}$$

E_{out} is the same as E_{in} for a lossless converter with 100% efficiency.

4.2.5 Output to Input Voltage Ratio

The ratio of output dc voltage to input ac voltage in the proposed converter can be found by dividing equation (4.41) by equation (4.40).

$$\left(\frac{V_o}{V_{in}}\right)^2 = \frac{6\eta RC}{T_s(1-D)^2} \tag{4.43}$$

Let V be the output to input voltage ratio when the input is taken as peak line-line voltage and $V_{ll,pk} = V_1$. Equation (4.43) can be expressed as

$$\left(\frac{V_o}{V_1}\right)^2 = \frac{2\eta RC}{T_s(1-D)^2} \tag{4.44}$$

Or

$$V = \frac{V_o}{V_1} = \sqrt{\frac{2\eta RC}{T_s(1-D)^2}} \tag{4.45}$$

If a parameter K is defined as,

$$K = \frac{T_s}{2RC} \tag{4.46}$$

then equation (4.45) can be written as

$$V = \left(\frac{1}{(1-D)}\right)\sqrt{\frac{\eta}{K}} \tag{4.47}$$

It is important to note that the C, referred in the above equations is the input capacitor value of the equivalent single-phase circuit, where it is fixed across the dc voltage source. To find the input capacitor value C_a ($C_a = C_b = C_c$) of the proposed circuit, C should be multiplied by a factor 3/2, because the input capacitors in the proposed converter are in a Y-arrangement.

Equation (4.47) is a critical equation as it links the output to the input voltage conversion ratio, the duty ratio and the input capacitor (by parameter K). Equation (4.47) can be plotted as shown in Figure 4.5 using a MATLAB program, which is presented in Appendix A.1.2. Figure 4.5 can be used to find the K (or C_a) that should

be used, in order for the converter to operate with discontinuous input capacitor voltages for a chosen D and V.

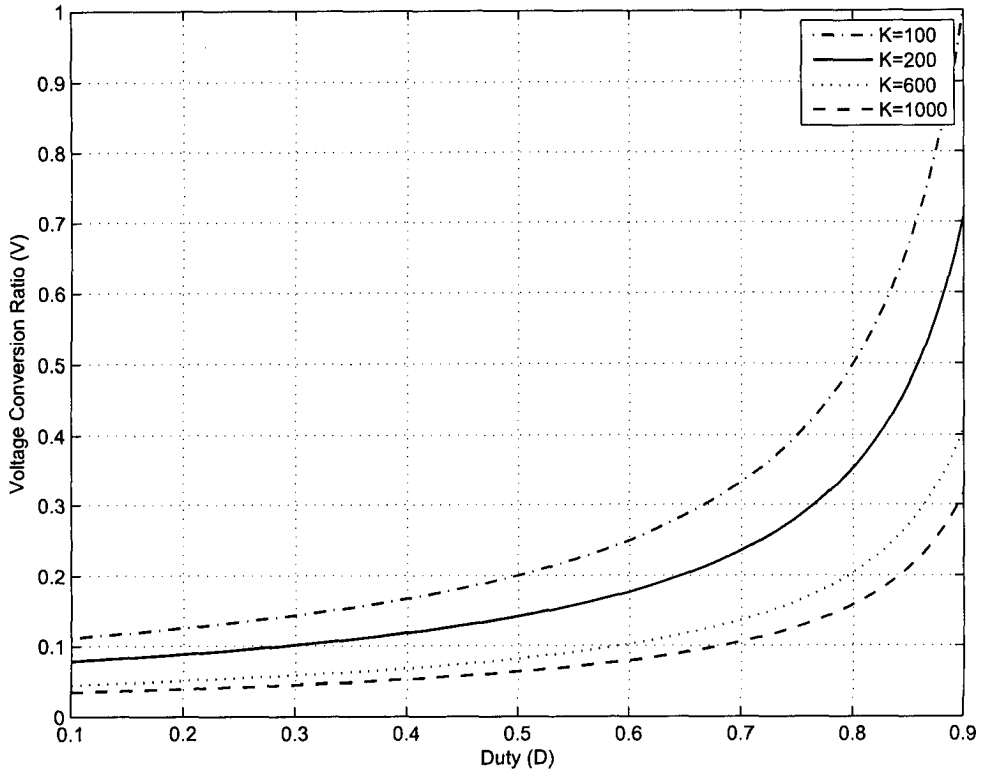


Figure 4.5: V vs. D for selected K values.

In order to ensure the lowest peak voltage stress for the converter switches while keeping the input capacitors' voltages discontinuous, the value of C_a should be selected so that when the phase-a voltage is at its peak, V_{C_a} drops to zero just at the end of an energy transfer mode then immediately rises when the converter enters a freewheeling mode. V_{C_a} becomes zero at $t = D\frac{T_s}{2}$, which corresponds to the end of an energy transfer mode in the half switching cycle. At $t = D\frac{T_s}{2}$, the converter enters a freewheeling mode and C_a starts being charged. In other words, at the peak of the phase-a voltage, V_{C_a} is at the boundary between being discontinuous and being continuous, and the converter can be said to be operating in boundary

discontinuous voltage mode (BDVM) - boundary conditions at a phase voltage peak, but discontinuous at all other times - under these conditions.

In order to plot the graphs to find the value of C_a under these conditions, the analysis needs to be developed further. For this purpose, equation (4.48) is reproduced below

$$\frac{V_o}{V_{in}} = \frac{nD_1}{1 - D + D_1} \tag{4.48}$$

During the interval $0 < t < D\frac{T_s}{2}$ the capacitors discharge when converter is in an energy transfer mode. If capacitor C_a is selected so that $D_1 = D$, then its voltage touches zero at $D\frac{T_s}{2}$ when the phase-a voltage is at its peak and the converter is in BDVM. The dc-dc voltage conversion ratio for the equivalent single phase circuit operating at BDVM is

$$D = D_1 \Rightarrow \frac{V_o}{V_{in}} = nD \tag{4.49}$$

V_{in} in equation (4.49) is replaced by V_1 to get the voltage conversion ratio for three-phase converter

$$V_{BDVM} = \frac{V_o}{V_{ll,pk}} = \frac{V_o}{V_1} = nD \tag{4.50}$$

where V_{BDVM} is the voltage conversion ratio at BDVM. D can be found from equation (4.50). Equation (4.46) can be rearranged to express K as a function of D

and V as

$$K = \left(\frac{1}{V^2(1-D)^2} \right) \tag{4.51}$$

If D in equation (4.51) is replaced by equation (4.50), boundary condition K_{BDVM} which is the parameter K at the boundary point of operation is found as a function of V_{BDVM}, as shown in equation (4.52).

$$K_{BDVM} = \left(\frac{1}{{V_{BDVM}}^2(1-\frac{V_{BDVM}}{n})^2} \right) \tag{4.52}$$

Figure 4.6) shows the plot of equation (4.52) is plotted using MATLAB (Appendix A.1.3 to indicate the three operating regions (DVM, BDVM and CVM) in which the input capacitors can operate.

D can be expressed in terms of V_{BDVM} by using equation (4.50); therefore K_{BDVM} can be written as a function of D by replacing V_{BDVM} from equation (4.51) which results in

$$K_{BDVM} = \left(\frac{1}{n^2D^2(1-D)^2} \right) \tag{4.53}$$

Equation (4.53) is plotted using MATLAB (Appendix A.1.4 Figure 4.7) assuming n is a constant. Figure 4.7 is a graph of K_{BDVM} vs. D.

Assume D is a constant in equation (4.53) and the input capacitors operate in BDVM at maximum load, parameter K_{BDVM} can be expressed as a function of n by rearranging equation (4.53) as follows

$$K_{BDVM} = \left(\frac{1}{D^2(1-D)^2} \right) \cdot \frac{1}{n^2} \tag{4.54}$$

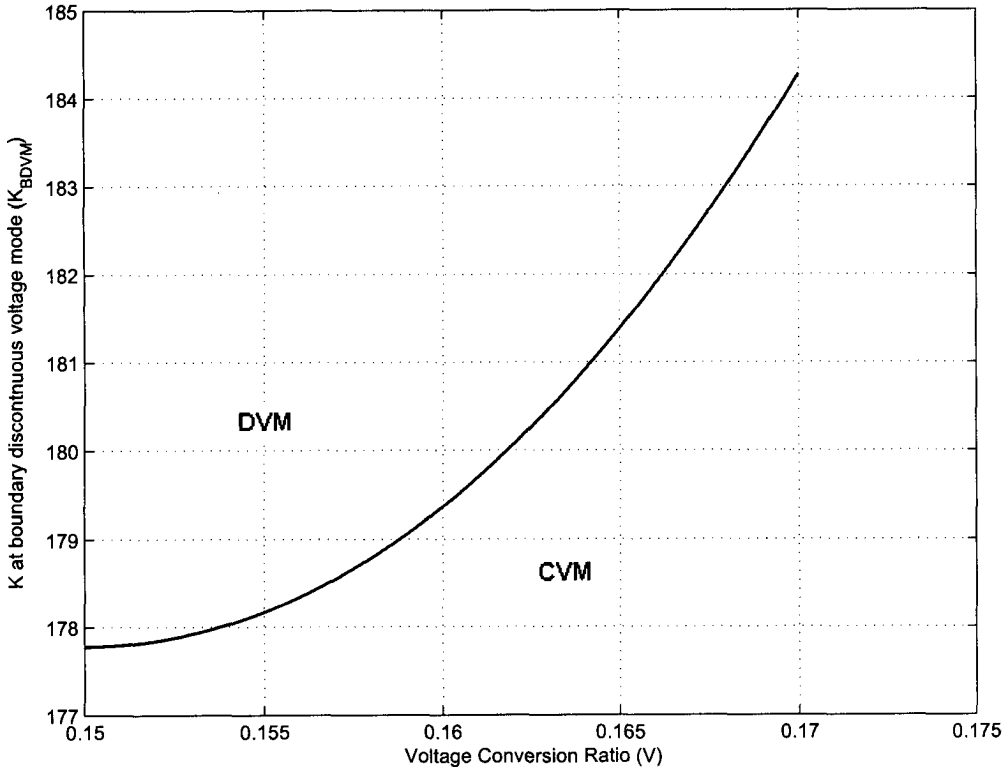


Figure 4.6: The curve of K_{BDVM} vs. V_{BDVM}.

Equation (4.54) can be plotted using a MATLAB program (Appendix A.1.5) and the result is shown in Figure 4.8.

4.3 Input Inductors (L_a, L_b and L_c)

Figure 4.9 shows a per phase equivalent circuit of L-C filter section which is helpful to find the relationship between C_a, L_a and line current harmonics ([26]). L_a and C_a refer to the input filter components of phase-a that is used to filter out undesired harmonics. Let f_r be the dominant harmonic frequency (sidebands) related to the

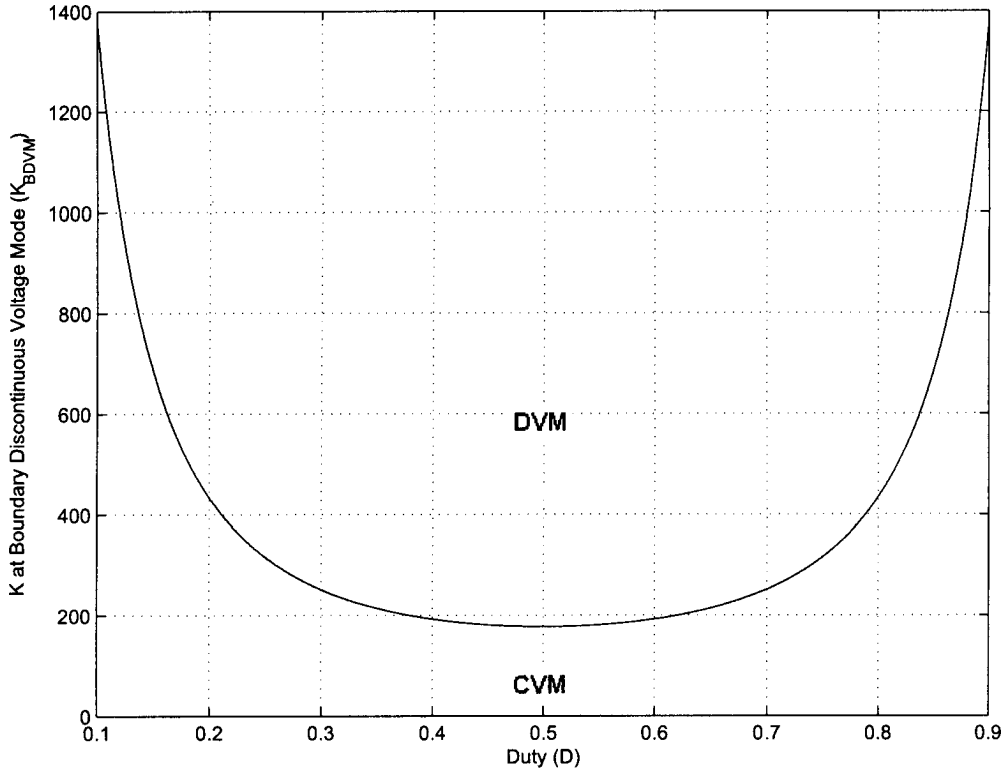


Figure 4.7: K_{BDVM} vs. D–K_{BDVM} for BDVM operation for the selected duty range.

switching frequency f_s. Then f_r can be written as

$$f_r = 2f_s \pm f_l \tag{4.55}$$

The total harmonic current of frequency f_r is denoted by $I_{t_{f_r}}$ where the currents through L_a and C_a are respectively $I_{l_{f_r}}$ and $I_{c_{f_r}}$. $I_{l_{f_r}}$ is the allowed harmonic flow into the line. By considering the current division rule through impedances, $I_{l_{f_r}}$ is written as,

$$I_{l_{f_r}} = I_{t_{f_r}} \left(\frac{\frac{1}{2\pi f_r C_a}}{2\pi f_r L_a - \frac{1}{2\pi f_r C_a}} \right) \tag{4.56}$$

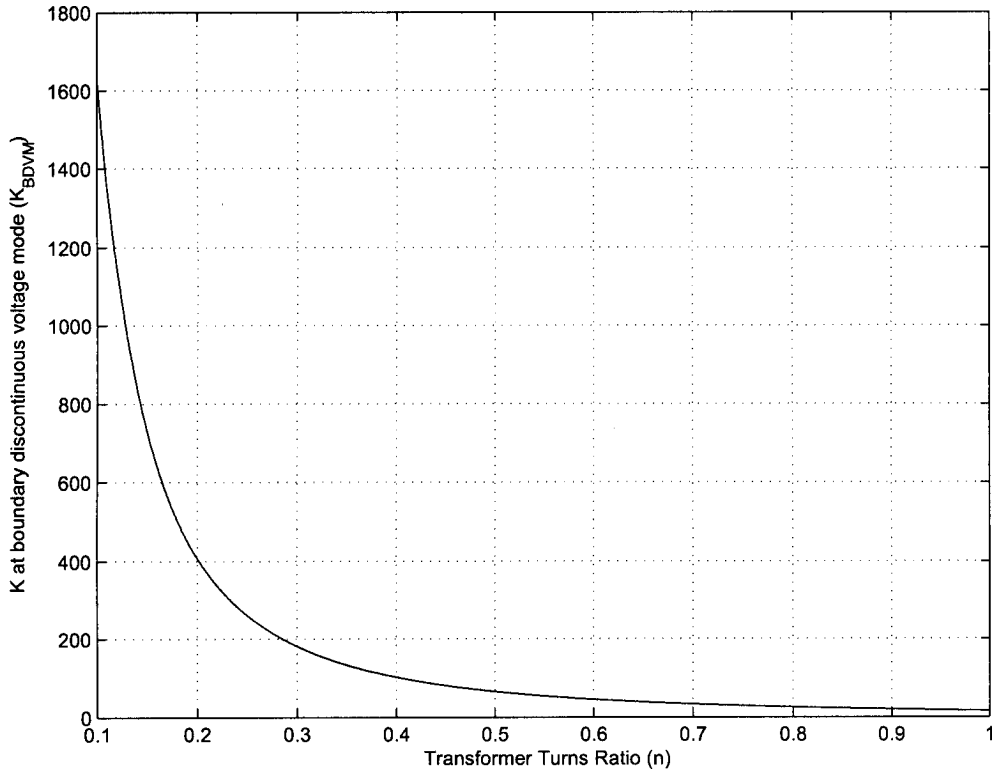


Figure 4.8: K_{BDVM} vs. n for BDVM operation.

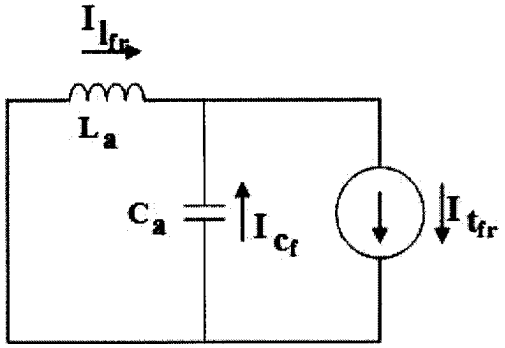


Figure 4.9: Single-phase equivalent input filter diagram.

If $I_{l_{fr}}$ is 20% of the total harmonics generated, then the relationship between the input filter components and harmonic content becomes

$$L_a C_a = \left(\frac{1}{2\pi f_r}\right)^2 \left(1 + \frac{I_{t_{fr}}}{0.2 I_{t_{fr}}}\right) \tag{4.57}$$

From equation (4.55), it can be seen that f_r is increased by increasing f_s. An increase in fr reduces the size of L_a according to equation (4.57), but this filter eliminates only the high frequency components. The low harmonics frequencies of f_l such as the 5th and 7th will only be attenuated but not eliminated.

4.4 Transformer Leakage Inductance (L_{lk})

The transformer leakage inductance L_{lk} is an important parameter in the operation of the converter as it prevents the premature charging of the input capacitors after they have been discharged, when the converter enters an energy transfer mode. Premature input capacitor charging makes it more likely that the capacitor voltages will not be discontinuous, which would result in low frequency harmonic components appearing in the input currents and distorting them.

Sometime during Mode 1 of operation (Section 3.4), the dc bus voltage V_{bus} of the converter (Figure 4.1) falls below the voltage impressed on the transformer primary side. The bus voltage keeps on decreasing and the difference between V_{bus} and the transformer primary voltage V_p which is negative, is applied across L_{lk}. Therefore the primary current starts to drop as a result of the building counter voltage across L_{lk}. If this current drops below the phase-a input inductor current I_a, then the difference in these currents will begin to charge the input capacitors. L_{lk} must be large enough to slow down the drop in primary current to keep it above I_a and also to slow down the rate of discharge of C_a during Mode 1 to avoid the premature charging of C_a.

During Mode 1, C_a interacts with L_{lk}. If L_{lk} is selected so that time constant

(TC) of resonance is closer to the duration of energy transfer, C_a will then discharge until S_1 is switched off. In other words, the value of C_a is brought closer to BDVM by controlling its rate of discharge, by increasing L_{lk}. TC is given by

$$TC = \sqrt{L_{lk}C_a} \tag{4.58}$$

In order to slow down the rate of discharge of C_a, TC should be selected closer to the period of energy transfer of the converter as

$$TC \geq D \cdot \frac{T_s}{2} \tag{4.59}$$

By considering equation (4.49), D in equation (4.59) can be replaced by V_{BDVM} and n as shown below,

$$TC \geq \frac{V_{BDVM}}{n} \cdot \frac{T_s}{2} \tag{4.60}$$

When equation (4.58) and equation (4.60) are put together, the following relationship among the variables, C_a, L_{lk}, n, V_{BDVM} and T_s is derived,

$$\sqrt{L_{lk}C_a} \geq \frac{V_{BDVM}}{n} \cdot \frac{T_s}{2} \tag{4.61}$$

Equation (4.61) can be rearranged as

$$L_{lk} \geq \left(\frac{V_{BDVM}}{n}\right)^2 \left(\frac{T_s}{2}\right)^2 \cdot \frac{1}{C_a} \tag{4.62}$$

Equation (4.62) can be plotted using MATLAB (Appendix A.1.6), as shown in Figure 4.10. The curves in this graph show the minimum values of L_{lk}, for the different turns ratios which should keep C_a from prematurely charging.

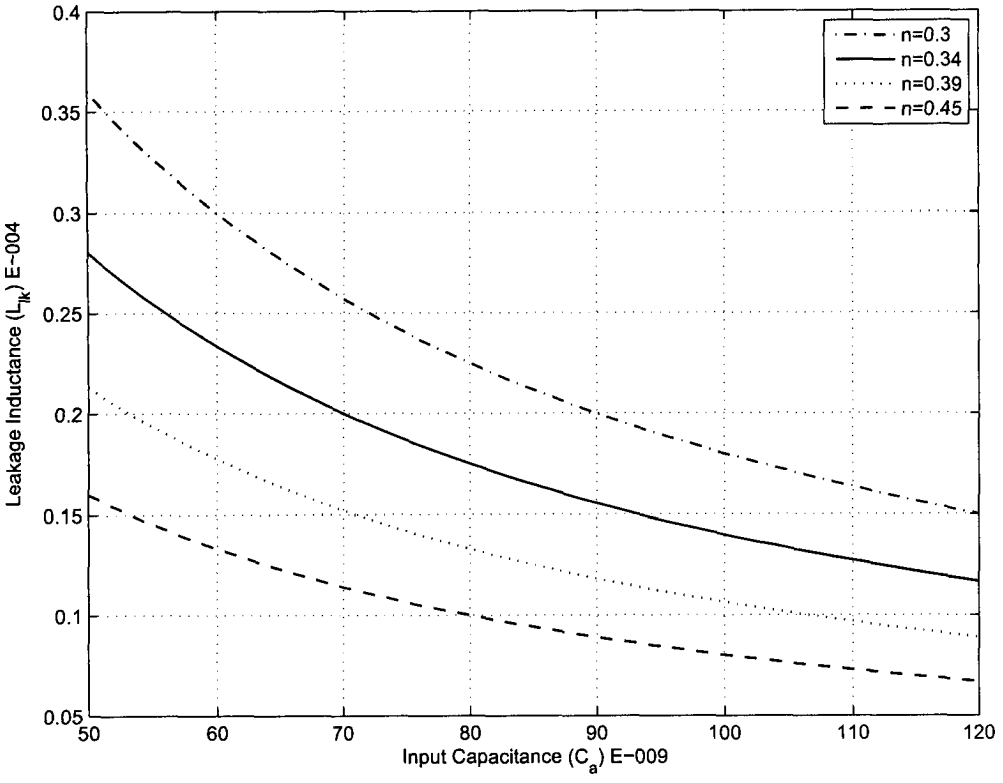


Figure 4.10: Curves of L_{lk} vs. C_a for different values of n.

4.5 Auxiliary Capacitor (C_x)

The main function of C_x is to extinguish the primary current in the transformer. In a typical dc-dc ZVZCS converter, the current begins to be extinguished after the full-bridge enters a freewheeling mode because V_{bus} is a dc source and is fixed. However V_{bus} in the proposed converter, is made of triangular pulses and is not fixed (Figure 4.1). Due to the nature of the converter, the primary current will start dropping as soon as V_{bus} equals the primary voltage and the primary current begins to be extinguished before full-bridge enters the freewheeling mode. Although it is the reflected counter voltage impressed by C_x that causes the primary current to extinguish, there is no net energy reduction in C_x until $t = t_4$ as V_{C_x} increases (Figure 3.4). At $t = t_4$, the primary current has reduced to a level which equals the

load current reflected to the primary side of the transformer. From that point on, until $t = \frac{T_s}{2}$, energy stored in C_x reduces as it simultaneously supplies energy to discharge L_{lk} and feeds the load till $t = \frac{T_s}{2}$.

The change in energy stored in C_x from its maximum to its minimum can be written as

$$E_{C_x} = 0.5C_x \left({V_{C_{x,pk}}}^2 - V_{C_{x,min}}^2 \right) \tag{4.63}$$

Let the energy fed to the load be E_1. If it is assumed that the load (R) is fed with constant current I_{L_o} during the period ($\frac{T_s}{2} - t_4$), then the energy absorbed by R is

$$E_1 = \left(R.{I_{L_o}}^2 \right) \left(\frac{T_s}{2} - t_4 \right) \tag{4.64}$$

The energy needed to discharge L_{lk}, E_2, can be written as

$$E_2 = \left(\frac{1}{2} L_{lk} \left(n.{I_{L_0}}^2 \right) - 0 \right) = \frac{1}{2}.L_{lk} \left(n.{I_{L_0}}^2 \right) \tag{4.65}$$

C_x can be expressed as follows, using equation (4.63), equation (4.64) and equation (4.65),

$$\frac{1}{2} C_x \left({V_{C_{x,pk}}}^2 - {V_{C_{x,min}}}^2 \right) = \frac{1}{2}.L_{lk} \left(n.{I_{L_0}}^2 \right) + \left(R.{I_{L_0}}^2 \right) \left(\frac{T_s}{2} - t_4 \right) \tag{4.66}$$

$$C_x = 2 \cdot \frac{\left(\frac{1}{2}.L_{lk} \left(n.{I_{L_0}}^2 \right) + \left(R.{I_{L_0}}^2 \right) \left(\frac{T_s}{2} - t_4 \right) \right)}{\left({V_{C_{x,pk}}}^2 - {V_{C_{x,min}}}^2 \right)} \tag{4.67}$$

By applying the values for $V_{C_{x,pk}}$ and $V_{C_{x,min}}$, C_x can be evaluated using equation (4.67).

4.6 Conclusion

A steady-state analysis of the proposed converter was performed in this chapter. Expressions and relations for key converter parameters such as duty ratio, input capacitor value, output to input voltage conversion ratio, transformer leakage inductance, auxiliary circuit capacitance were determined. The purpose of the analysis was to understand the steady-state characteristics of the converter and to help establish a procedure for its design, which will be done in the next chapter of this thesis.

Chapter 5

Converter Design and Experimental Results

5.1 Introduction

The design of the converter is discussed in this chapter. An example is given to demonstrate how the most important converter parameters can be selected using the results of the analysis performed in Chapters 3 and 4. The results of the design process will be used in the implementation of an experimental prototype converter that will confirm the feasibility of the converter.

5.2 Design Example

The proposed converter is to be designed according to the following specifications:

- Input three-phase voltage: 208 $V_{ll,rms}$
- Line frequency: $f_l = 60$ Hz

- Output voltage: $V_o = 48\ V_{dc}$
- Output power: 1.92 kW
- Switching frequency: $f_s = 50$ kHz

For the converter design, the key parameters that will be considered are as follows:

- Converter duty ratio D
- Transformer turns ratio n
- Input capacitor $C_a = C_b = C_c$
- Input inductor $L_a = L_b = L_c$
- Transformer leakage inductance L_{lk}
- Auxiliary circuit capacitor C_x
- Peak switch voltage stress $V_{sw,pk}$

Once these key parameters have been determined, the design for the rest of the converter is very similar to that of a standard ac-dc converter and a standard dc-dc full-bridge converter. This design will not be presented here as it can be found in any standard power electronics textbook [1].

The design of the proposed converter is an iterative process as many of the key converter parameters are related to one another. One way to tackle this problem is to write a computer program based on the modal equations derived in Chapter 3,

to "simulate" certain key voltages and currents such as the voltage across the input capacitors and the voltage across C_x so that a range of suitable operating points can be established. Once such a range has been determined, then a more detailed search can be made within this region to determine the values of the key parameters that will be implemented in a prototype.

What this "simulation" process involves is to select initial parameter values, go through the various modes of converter operation over a period of time by performing a time sweep (i.e., $t = 1$ ns, $t = 2$ ns, $t = 3$ ns, etc.), then see if the parameters values come back to their initial values at the end of the period (as they should if the converter is operating under steady-state conditions). Due to symmetries in the three-phase ac input voltage, the period under consideration need not be the entire line cycle, but can be 30 or $\frac{\pi}{6}$ rad. If the parameter values at the end of the period are not the same as those at the start, then the converter is not in a steady-state operating condition and the initial values have to be adjusted until they are. It is only when the parameter values at the end of the switching period match those at the start that the converter can be said to be operating under steady-state conditions and the operating point under consideration is valid. If this process is repeated for a number of operating points, then a range of appropriate points can be determined.

5.2.1 Transformer Turns Ratio n and Duty Ratio D

The most parameters that need to be determined are those for n and D as the range of appropriate operating points is narrowed down considerably once values for these parameters have been determined. Assuming that the output inductor current I_{L_o} is

continuous, the relationship between n and D is

$$n = \frac{\frac{V_o}{V_{bus,ave}}}{D} \tag{5.1}$$

where V_o is the output dc voltage and $V_{bus,ave}$ is the average value of the dc bus voltage, which is not fixed dc, but is a train of triangular pulses.

In order for enough average bus voltage to be generated so that the converter can produce the required output dc voltage, the input capacitors must be allowed to charge for a sufficient amount of time. Since the capacitors do not charge when the converter is in an energy transfer mode (for a length of time of $t = D\frac{T_s}{2}$), but do when the converter is in a freewheeling mode of operation (for a length of time of $t = (1 - D)\frac{T_s}{2}$), there are limitations on the values of D.

If D is too large, then the input capacitors will not be given enough time to charge so that the average dc bus voltage will be not sufficient to produce the desired output voltage. If D is too small, then the input capacitors may be sufficiently charged, but they may not be given enough time to discharge as the duration of the energy transfer modes will be too small so that they will not have discontinuous voltages, as shown in Figure 5.1, which would worsen the input power factor. An appropriate value is n is one that allows for a suitable range of values of D to exist.

The value of n should be the smallest value possible that satisfies the duty ratio criteria so that the current that is reflected from the secondary side of the converter to the primary is minimized. The auxiliary capacitor C_x on the transformer secondary side extinguishes the primary current when the converter is in a freewheeling mode and if n is too large, then the transformer primary is much larger and there is large amount is current need to be extinguished. A larger n requires a larger C_x and also

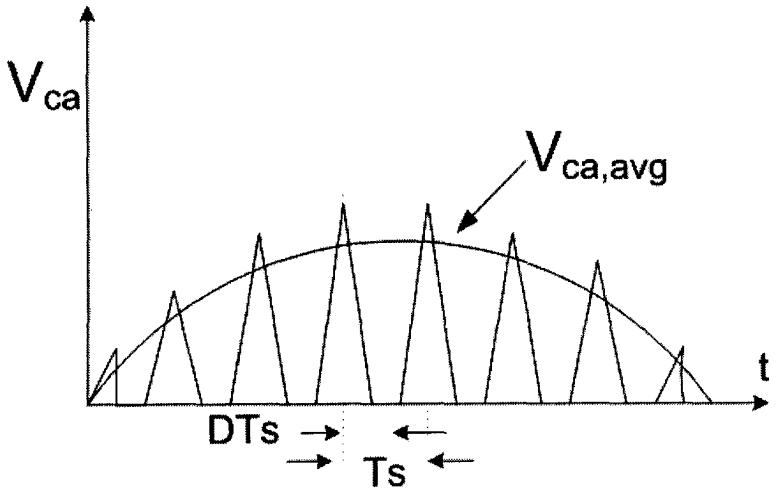


Figure 5.1: Triangular input capacitor voltage and sinusoidal envelope.

increases the time that the converter should be allowed to freewheel, (i.e., the time needed to eliminate the primary current). Therefore, increase in n would increase the conduction losses and decrease the time available for the energy transfer modes to exist.

By using a computer program as described above, it was determined that $n = 0.3$ and $D = 0.55$ for full-load conditions were the most suitable values for these parameters, given the converter specifications.

5.2.2 Input Capacitors (C_a, C_b, and C_c) and Peak Switch Voltage Stress $V_{sw,pk}$

The key requirement for the converter to operate with an excellent power factor is that the value of the input capacitors ($C_a = C_b = C_c$) must be such that the voltages across them will be discontinuous. If C_a is too large, then the voltages will not be discontinuous during significant portions of the line cycle as the capacitors will not

be able to fully discharge within a switching cycle.

If C_a is too small, then the peak input capacitor voltage will become excessive, which will result in an excessive peak bus voltage being impressed across the full-bridge switches. Moreover, the input capacitor voltage will discharge too quickly right after the converter enters an energy transfer mode so that not enough energy will be transferred to the output. As a result, the converter will not be able to produce the desired output dc voltage.

From the given specifications that the converter is to be designed, the output to input voltage conversion ratio is

$$V = \frac{V_o}{V_l} = \frac{48}{208\sqrt{2}} = 0.163 \tag{5.2}$$

where $V_l = 294.16V$ is the line-to-line peak voltage and V_o is $48V$. With the switching frequency being $f_s = 50kHz$ and $n = 0.3$ and $D = 0.55$ being determined beforehand, a value for C_a can be found indirectly through K from the curves in Figure 4.8. As stated in Section 4.2, the value of C_a should be such that the converter operates with DBDM when the phase-a voltage is at its peak value and the curves in this graph have been generated for this condition. From Figure 4.7 with $V = 0.163$ from equation (5.2) and $D = 0.55$, K_{BDVM}, the value of K at BDVM operation, is $K_{BDVM} = 200$. Since $K = \frac{T_s}{2RC}$, as stated in Section 4.2.3, C, which is the single-phase equivalent circuit input capacitor at the BDVM is

$$C = C_{BDVM} = \frac{1}{2f_s R K_{BDVM}} = \frac{1}{2 \times 50000 \times 1.2 \times 200} = 42nF \tag{5.3}$$

and C_a which is the Y-connected phase a input capacitor for the three-phase converter is

$$C_a = \frac{3}{2}(C_{BDVM}) = \frac{3}{4}\frac{1}{3 \times 50000 \times 1.2 \times 200} = 62nF \tag{5.4}$$

It should be noted that C (Figure 4.2) is between the phase and the neutral, but C_a, C_b, and C_c (proposed converter) are in Y-connection [14]. This is the reason for multiplying by the $\frac{3}{2}$ factor to arrive at the value of C_a as shown by equation (5.4).

According to equation (4.5), the maximum voltage across C_a is

$$V_{C_{a,pk}} = \frac{8(1-0.55)\frac{20\times10^{-6}}{2}}{60 \times 10^{-9}} = 600V \tag{5.5}$$

The peak switch voltage stress across the converter switches can determined from equation (4.7) to be

$$V_{bus,pk} = V_{sw,pk} = \sqrt{3} * \frac{7.9(1-0.55)\frac{20\times10^{-6}}{2}}{60 \times 10^{-9}} = 1026V \tag{5.6}$$

5.2.3 Input Inductors (L_a, L_b and L_c)

Once a value for C_a has been determined, a value for $L_a = L_b = L_c$ can be obtained from equation (4.57), According to equation (4.55), the dominant frequency is

$$f_r = 2 \times 50000 - 60 = 99940Hz \tag{5.7}$$

It should be considered that since the full-bridge converter has two energy transfer modes in a single switching cycle, the operating frequency that appears to

the input side is twice that of the switching frequency. Therefore $2f_{sw}$ is applied to equation (5.7) to derive the value of input inductors. If the harmonics at the dominant switching frequency that are allowed to the line are to allowed to be 20% of the harmonics created by the converter, as per equation (4.57) then the input inductor value is

$$L_a = \frac{\frac{1}{(2\pi * 99940)}^2 \left(1 + \frac{1}{0.2}\right)}{60 * 10^{-9}} = 255\mu H \tag{5.8}$$

5.2.4 Transformer Leakage inductance (L_{lk})

As explained in Section 4.3, too small a value of L_{lk} may result in the premature charging of the input capacitors during an energy transfer mode, which would ultimately affect the input power factor. A sufficiently large value of L_{lk} will keep the primary current from dropping below the line current during an energy transfer mode so that the input capacitors will not begin to get charged until a freewheeling mode has started. The minimum value of L_{lk} can be determined from figure 4.10, when $n = 0.3$ and $C_a = 60\ nF$,

$$L_{lk,min} = 30\mu H \tag{5.9}$$

5.2.5 Auxiliary Capacitor (C_x)

The value of C_x can be found from equation (4.67). If the maximum and minimum voltages across C_x are chosen to be $30V$ and $20V$ respectively then the minimum

value of C_x is,

$$C_x = 2\frac{\left(\frac{1}{2} \times 25 \times 10^{-6}(0.3 \times 40^2) + (1.2 \times 40)^2) \times \left(\frac{20\times10^{-6}}{2} - 5 \times 10^{-6}\right)\right)}{(30^2 - 20^2)} = 38\mu F \tag{5.10}$$

5.3 Experimental Results

An experimental prototype of the proposed converter, shown in Figure 3.1, was implemented according to the following specifications:

- Input three-phase voltage: 208 $V_{ll,rms}$
- Line frequency: $f_l = 60$ Hz
- Output voltage: $V_o = 48$ V_{dc}
- Output power: 1.92 kW
- Switching frequency: $f_s = 50$ kHz

The semiconductor components that were used were IXFN32N120-ND for S_1 and S_4, IXDH20N120-ND for S_3 and S_2, and RHRP1560 diodes for the secondary side rectifier and auxiliary circuit D_c and D_d. 36MT160 three-phase bridge module was used between the three-phase L-C filter and full-bridge as the bridge rectifier.

The inductor and capacitor values that were used for the input filter were $C_a = C_b = C_c = 60$ nF, $L_a = L_b = L_c = 255$ μH

The transformer had a turns ratio of $n = 3 : 10$ and a leakage inductance of $L_{lk} = 30\ \mu$H

The auxiliary capacitor used was a parallel combination of two capacitors, each having a value of 25 μF.

The output filter inductor was 460 μH and the filter capacitor was 1500 μF.

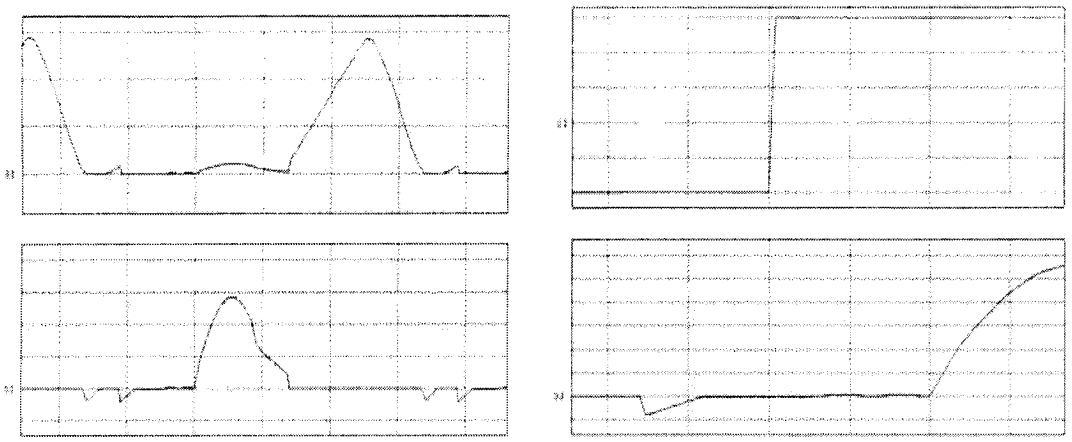
Switches S_1 and S_4 will be referred to as the ZVS switches because they happened to be in the leading leg of every half switching cycle. It was the switches in this leg that turned on first; they turned on and off with ZVS. Switches S_3 and S_2 will be referred to as the ZCS switches because they happened to be in the lagging leg of every half switching cycle. Each switch in this leg turned on after the respective leading leg switch was turned on. S_3 and S_2 turned on and off with ZCS, turning off after the transformer primary current has been extinguished during one of the converter's freewheeling modes of operation and turning on when there is no current in the transformer primary.

It should be noted that the experimental waveform will be compared to waveform obtained with PSIM, well-known, commercially available power electronics simulation software.

5.3.1 ZVS Leg Switching Waveforms

Figures 5.2-5.3 show typical switching waveforms of a switch in the ZVS leg. It can be seen that the switch is turned on with ZVS as it is turned on while its current is negative. This indicates that current is flowing through the body diode of the switch

when it turns on. This means that the voltage across the switch is clamped to the voltage drop of the diode, which is negligible.

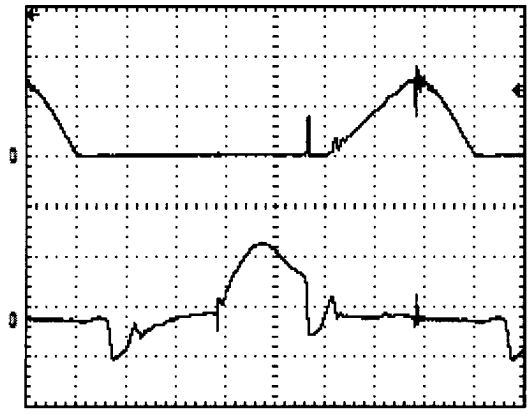


(a) (b)

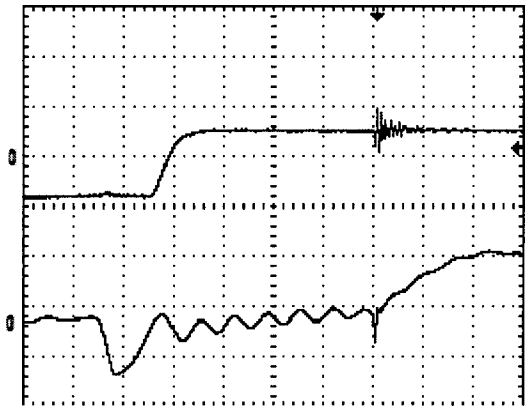
Figure 5.2: Simulation results of typical (a) ZVS switch voltage (top) and switch current (bottom) [V: 250V/div, I: 10A/div, t: 5μs/div], (b) Gate pulse (top) and switch current (bottom) [V: 5V/div, I: 10A/div, t: 1μs/div].

5.3.2 ZCS Leg Switching Waveforms

Figures 5.4 and 5.5 depict typical switching waveforms of a switch in the ZCS leg. It can be seen that the current in the switch is zero before its gating signal is removed, which shows that the switch turns off with ZCS and that the current rises gradually after the switch is turned on (gating signal goes high), which shows that it turns on with ZCS.



(a)

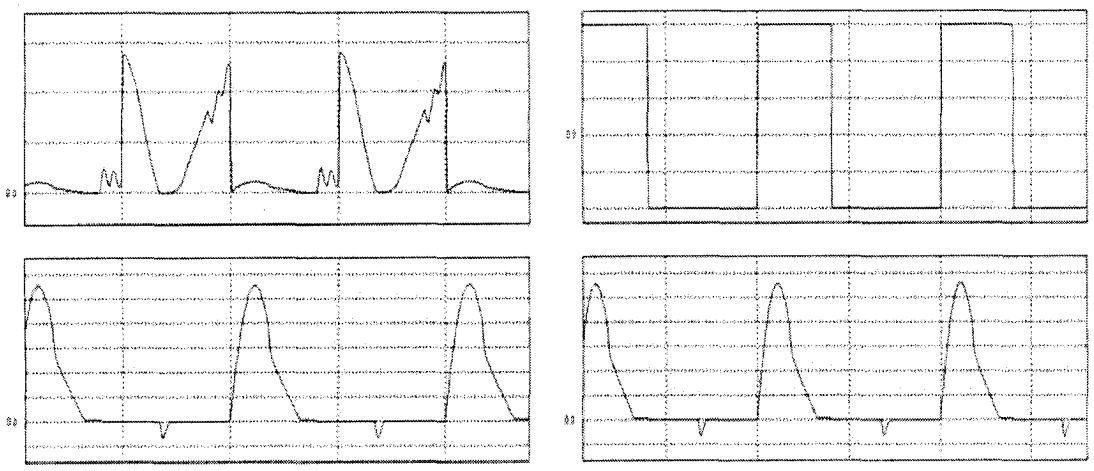


(b)

Figure 5.3: Experimental results of (a) ZVS switch voltage (top) and switch current (bottom) [V: 500V/div, I: 25A/div, t: 2.5μs/div], (b) Gate pulse (top) and switch current (bottom) [V: 25V/div, I: 25A/div, t: 1μs/div].

5.3.3 Input Voltage and Current Waveforms

Figures 5.6 (a) and (b) show typical input phase voltage and line current waveforms. It can be seen that the input current is almost sinusoidal i.e., the harmonics of the line currents are attenuated to meet the standard, where the standard does not require to inject perfectly sinusoidal line currents to the system. From those results it is visible that the current is in-phase with the voltage and almost sinusoidal in shape.



(a) (b)

Figure 5.4: Simulated waveforms of (a) ZCS switch voltage (top) and switch current (bottom) [V: 250V/div, I: 5A/div, t: 5μs/div]. (b) Gate pulse (top) and switch current (bottom) [V: 5V/div, I: 10A/div, t: 5μs/div].

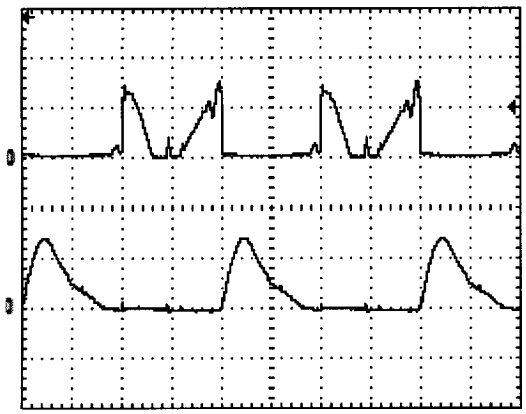
5.3.4 Input Capacitor Voltage Waveforms

Figures 5.8 and 5.7 show typical waveforms of the voltage across capacitor C_a. Figure 5.8 shows the waveform over a couple of line cycles and Figure 5.7 shows the same voltage over a couple of switching cycles.

It can be seen that voltage across the input inductor is discontinuous in every switching cycles, which is the key condition that must be met for the converter to operate with an excellent input power factor.

5.4 Conclusion

The design of the converter was discussed in this chapter. An example was given to demonstrate how the most important converter parameters can be selected using the results of the analysis performed in Chapters 3 and 4. The results of the design



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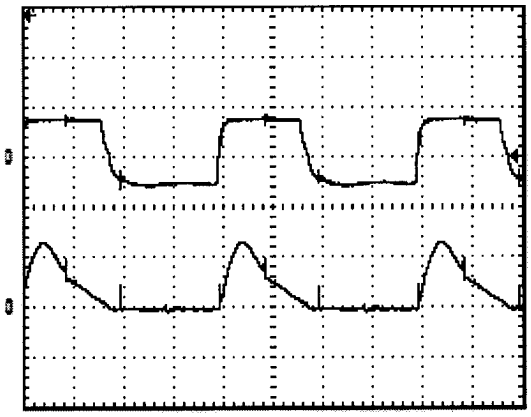
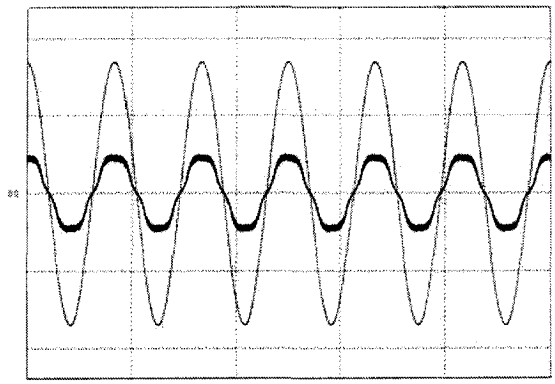


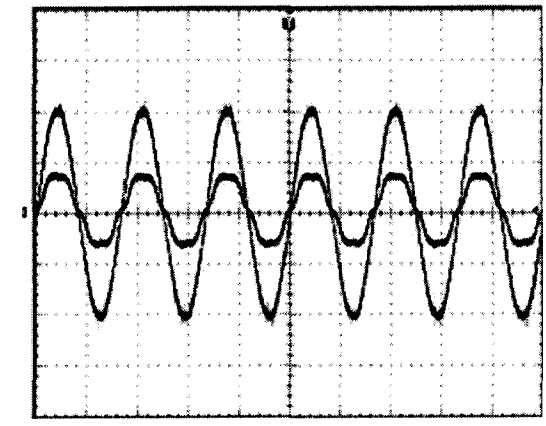
(b)

Figure 5.5: Experimental waveforms of(a) ZCS switch voltage (top) and switch current (bottom) [V: 500V/div, I: 25A/div, t: 5μs/div]. (b) Gate pulse (top) and switch current (bottom) [V: 25V/div, I: 10A/div, t: 5μs/div].

process were used in the implementation of an experimental prototype converter that confirmed the feasibility of the converter.

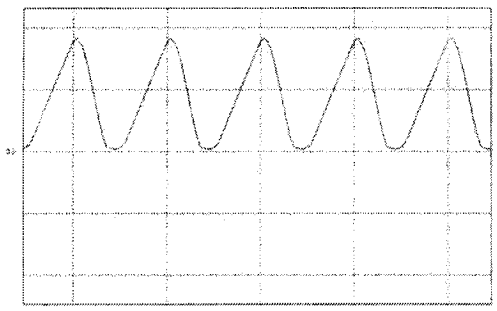


(a)

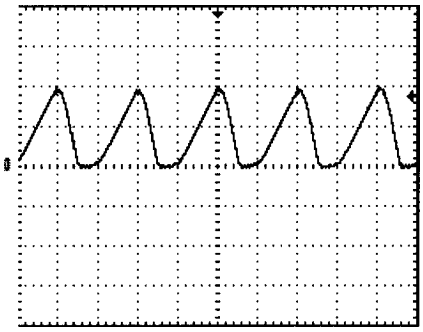


(b)

Figure 5.6: (a) Simulation of input phase voltage and input line current [V: 100V/div, I: 20A/div, t: 8ms/div]. , (b) Experimental input phase voltage and input line current [V: 75V/div, I: 10A/div, t: 8ms/div]].

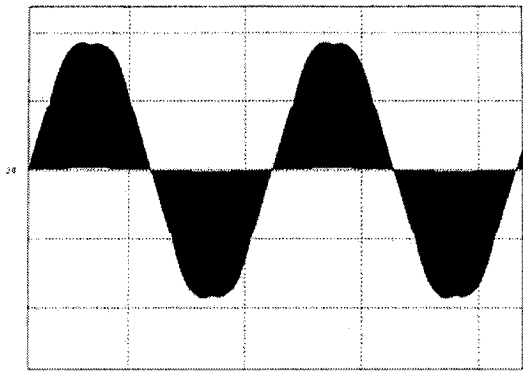


(a)

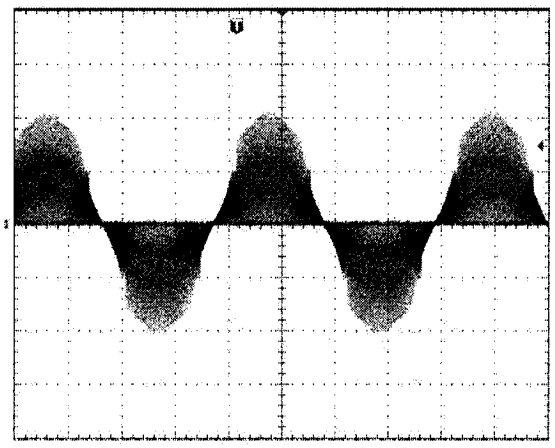


(b)

Figure 5.7: (a) Simulated voltage waveform of input capacitor C_a (b) Experimental input capacitor voltage across C_a [V: 200V/div, t=5ms/div].



(a)



(b)

Figure 5.8: (a) Simulation results of the input capacitor voltage measured across C_a (b) Experimental results of the input capacitor voltage measured across C_a [V: 200V/div, t=4ms/div]].

Chapter 6

Conclusion

6.1 Introduction

In this chapter, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work performed in thesis are presented and the main contributions of the thesis are stated. The chapter concludes by suggesting potential future research that can be done based on the thesis work.

6.2 Summary

The objective of this thesis was to propose, analyze, design, implement and experimentally confirm the operation of a new three-phase, ac-dc, single-stage, high power factor, ZVZCS full-bridge PWM converter, which does not have the drawbacks of previously proposed circuits three-phase ac-dc converters. In this thesis, a background study of the three-phase ac-dc converters was carried out, the derivation of the proposed converter was presented and the general operating principles of the converter were reviewed.

The converter's steady-state operation was discussed in detail and analyzed. Relationships between key converter parameters were determined, and graphs of steady-state characteristics were plotted using MATLAB programs. The analysis and characteristics graphs were used as part of the design procedure to select the values of key converter parameters. An experimental prototype of the proposed three-phase single-stage converter was built and its functionality was confirmed with simulation and experimental results obtained from a prototype.

6.3 Conclusion

The following conclusions can be made based on the results of this thesis:

1. It is possible to combine a three-phase, single switch ac-dc buck converter with a dc-dc ZVZCS full-bridge converter to get a feasible three-phase, single-stage, ac-dc converter.

2. The converter can operate with a very good input power factor as long as the input capacitor voltages are discontinuous throughout the entire line cycle.

3. The smaller the value of the input capacitors, the better the input power factor will be over a wider range of operating conditions, but the larger the maximum peak voltage across the converter switches will be. Although these stresses can be made to be comparable to those found in a converter with an ac-dc boost PFC front-end, a trade-off may have to be made between peak switch voltage stress and input power factor.

4. The leakage inductance of the transformer, L_{lk}, has a significant impact on the converter's input power factor. If this parameter is too small, then the input

capacitors may start to recharge while the converter is in an energy transfer mode, which may result in the input capacitors not being able to properly discharge. It is the proper discharging of these capacitors that allows the converter to operate with a very good power factor.

5. The size of the input capacitors has an effect on the converters ability to produce the required output dc voltage. These capacitors must be able to store a sufficient amount of energy when the converter is in a freewheeling mode of operation so that it can be transferred to the load when the converter is in an energy transfer mode of operation. If the input capacitors are too small, an insufficient amount of energy to do this may be stored.

6.4 Contributions

The principal contributions of this thesis are as follows:

1. A new three-phase, ac-dc, single-stage, ZVZCS full-bridge PWM converter that can operate with an excellent input power factor was proposed and its operation was explained.

2. The steady-state operation of the new converter was analyzed and its characteristics were determined.

3. Guidelines for the design of the converter were given, a procedure for its design was derived and demonstrated with an example.

4. The feasibility and the properties of the new converter were confirmed by simulation and by experimental results obtained from a prototype.

6.5 Proposal for Future Work

The following suggestions are made for future work:

1. The switches in the ZCS leg of the converter turn off with almost zero current. It has been assumed throughout this thesis that the magnetizing current of the transformer can be ignored. In fact, there is a small amount of magnetizing current in the transformer that flows through the ZCS switches at the time that they turn off. This current represents a reverse current that would normally flow back to a bulk capacitor connected across the dc bus. The proposed converter, however, has no such capacitor across its dc bus, and this reverse current was absorbed by small, passive resistor-capacitor-diode snubber circuit connected across the dc bus. This snubber circuit, however, create converter losses as they dissipate energy. For future work, the dissipative snubber can be replaced by suitable non-dissipative snubber to improve the efficiency of the converter.

2. The lack of a primary-side dc bus capacitor in the proposed converter means that it cannot be used in applications as a stand alone converter if hold-up is required. Hold-up time is defined as time the converter can produced the required output dc voltage after a power failure in the ac input line has occurred. In a standard two-stage converter, energy from the dc bus capacitor can be used to supply the load at the required voltage for a certain short amount of specified time - the hold-up time - until power from the input line returns. For future work, some means to introduce energy storage at the dc bus to allow the converter to work over a duration of hold-up time in case of a short ac power failure can be investigated.

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Appendix A

Matlab Codes

A.1 Codes for Programs in Chapter 4

A.1.1 Equations Solutions-4.42

```
%Chapter 4
%Section 4.2.4.3 Energy Relations
%Obj:Solve the Energy integrals
%to find the energy supplied by phase a, Ea
%
%Vl is the peak phase voltage
%Vo is the output voltage
%n is the transformer turns ratio
%Ea, Eb, Ec are phase input energies during a pi/6 rad period
%yita is efficiency & R is load
%Ein, Eout are total enery in & out respectively
%
```

```
clear all;
clc;
syms x a1 n V1 Vo  Ein Eout yita R;
Ea=int(V1*sin(x)*a1*(n*V1*sin(x)-Vo),x,pi/3,pi/2);
%
%to find the energy supplied by phase b
syms x a1 V1 Vo n;
Eb=int(V1*sin(x-2*pi/3)*a1*(n*V1*sin(x-2*pi/3)...
    -Vo),x,pi/3,pi/2);
%
%to find the energy supplied by phase c
syms x a1 V1 Vo n;
Ec=int(V1*sin(x-4*pi/3)*a1*(n*V1*sin(x-4*pi/3)...
    -Vo),x,pi/3,pi/2);
%
Ein=Ea+Eb+Ec;
syms x a1 V1 Vo;
Eout=(Vo^2)*R*(pi/6);
%
Eout=yita*Ein;
syms Ca D Ts;
a1=(4*Ca)/(n*Ts*(1-D)^2);
```

A.1.2 Figure 4.5

```
%Chapter 4
%Figure 4.5
%Obj:Relationship between, V, D, and Circuit parameter K

clc;
clear all;

fs=50000; % Switching Frequency
Ts=1/fs;  % Switching Period
Vo=48;    % Output Voltage
Io=40;    % Output Current
V1=208*sqrt(2); % Line to line peak voltage
V=Vo/V1; % Output to input voltage Ratio
eta = 1; % Considering 100% Efficiency
%D is the duty ratio
%K is the circuit parameter

K=[100 200 600 1000]; % Defining values for K
D=linspace(0.1,0.9,100);
for i=1:length(D)
    for j=1:length(K)
        str=sprintf('Vol-(1/(1-(%f)))*(sqrt(1/(%f)))=0'...
            ,D(i),K(j));
        a=solve(str);
```

```
        V(i,j)=double(a);
    end
end

V_K1 = zeros(1,length(D));
V_K2 = zeros(1,length(D));
V_K3 = zeros(1,length(D));
V_K4 = zeros(1,length(D));

for l=1: length(D)

  V_K1(l) = V(1,1);
  V_K2(l) = V(1,2);
  V_K3(l) = V(1,3);
  V_K4(l) = V(1,4);

end

plot(D,V_K1,'-.',D,V_K2,'-',D,V_K3,':',D,V_K4,'--',...
    'color','k','linewidth',1);
legend('K=100','K=200','K=600','K=1000');
xlabel('Duty (D)');
ylabel('Voltage Conversion Ratio (V)');
grid on;
print(gcf, '-depsc2', 'fig_45.eps');
print(gcf, '-dpng', 'fig_45.png');
```

A.1.3 Figure 4.6

```
%Chapter 4
%Figure 4.6
%Obj:plot K_boundary vs. Voltage conversion ratio
%
clear all
clc;
fs=50E+003;                    %Switch frequency
Ts=1/fs;
V1=(208)*sqrt(2);              %Line-line peak voltage
Vo=48;                         %output voltage-regulated
R=1.2;                         %Full load
D=0.55;                        %Duy at full load
Vb=linspace(0.15,0.17,1000); % Probable ouput(V0)/input(Vin)
yita=1.0 ; %Assume effciency of converter is 100%
n=30/100;  %Transformer turns ratio (assume constant at 0.3)

Kboun_Vb = zeros(1,length(Vb));
    for i=1:length(Vb)
        Kboun_Vb(i)=1/((Vb(1,i))^2*(1-((Vb(1,i))/n))^2);
     end
plot(Vb,Kboun_Vb,'linewidth',1.3,'color','k');
grid on;
xlabel('Voltage Conversion Ratio (V)');
ylabel('K at boundary discontnuous voltage mode (K_{BDVM})');
```

```
mTextBox = uicontrol('style','text');
set(mTextBox,'String','DVM','fontsize',12,'fontweight',...
    'BOLD','Position',[200 250 40 20],...
    'BackgroundColor','white');

mTextBox1 = uicontrol('style','text');
set(mTextBox1,'String','CVM','fontsize',12,'fontweight',...
    'BOLD','Position',[400 150 40 20],...
    'BackgroundColor','white');

print(gcf, '-depsc2', 'fig_46.eps');
print(gcf, '-dpng', 'fig_46.png');
```

A.1.4 Figure 4.7

```
%Chapter 4
%Figure 4.7
%plot K_boundary vs. Duty
%
clear all
clc;
fs=50E+003;                 %Set switch frequency
Ts=1/fs;
V1=(208)*sqrt(2);           %line-to-line peak input voltage
Vo=48;                      %output dc voltage
R=1.2;                      %full load
D=linspace(0.1,0.9,1000); %duty ratio
yita=1.0;                   %assume effciency of converter is 100%
n=30/100;                   %transformer turns ratio
fl=60;                      %line freq
F=fs-fl;                    %dominant harmonics, base frequency

    for i=1:length(D)
        Kboun_D(1,i)=(1*yita)/(n^2*D(1,i)^2*(1-D(1,i))^2);
     end
plot(D,Kboun_D,'color','k');
grid on;
xlabel('Duty (D)');
ylabel('K at Boundary Discontinuous Voltage Mode (K_{BDVM})');
```

```
mTextBox = uicontrol('style','text');
set(mTextBox,'String','DVM','fontsize',12,'fontweight',...
    'BOLD','Position',[375 250 40 20],'BackgroundColor','white');

mTextBox1 = uicontrol('style','text');
set(mTextBox1,'String','CVM','fontsize',12,'fontweight',...
    'BOLD','Position',[375 75 40 20],'BackgroundColor','white');

print(gcf, '-depsc2', 'fig_47.eps');
print(gcf, '-dpng', 'fig_47.png');

Duty=input('Input D value  for full load = ');
Kboun_D=input('Input K value  for the selected duty(load)= ');
V=n*Duty;
Ca_b=3/(4*R*fs*Kboun_D);
La_b=(1/(2*pi*F)^2)*(1+100/20)*(1/Ca_b);
```

A.1.5 Figure 4.8

```
%Chapter 4
%Figure 4.8
%OBJ:plot K vs. n AT BDVM operation
%
clear all;
clc;
V1=(208)*sqrt(2); %Line-to-line peak input voltage
Vo=48;            %Output dc voltage
Vb=Vo/V1;         %Required voltage conversion ratio at BDVM
D=0.55;           %Duty at full load
N=Vb/D;           %Turns ratio to get required Vb, at BDVM
R=1.2;            %Full load
fs=50000;         %Switching frequency
n=linspace(0.1,1,1000); %transformer turns ratio
yita=1.0;         %Assume effciency of converter is 100%
    for i=1:length(n)
        Kboun(1,i)=(1/(D^2*(1-D)^2))*(1/n(1,i)^2);
     end
plot(n,Kboun,'color','k');
grid on;
xlabel('Transformer Turns Ratio (n)');
ylabel('K at boundary discontinuous voltage mode (K_{BDVM})');
%print(gcf, '-depsc2', 'fig_48.eps');
print(gcf, '-dpng', 'fig_48.png');
```

```
%
Kboun=input('Input K value  for the selected n = ');
Ca_BDVM=3/(4*R*fs*Kboun);
fl=60;                  %line freq
F=fs-fl;                %dominant harmonics, base frequency
La_BDVM=(1/(2*pi*F)^2)*(1+100/20)*(1/Ca_BDVM);
```

A.1.6 Figure 4.10

```
%Chapter 4
%Figure 4.10
%Obj:Relationship between, Llk-Ca, turns ratio, Duty

clc;
clear all;
fs=50000;
Ts=1/fs;
Vo=48;
Io=40;
Vin=208*sqrt(2);
Mv=Vo/Vin;
Ca=linspace(50,120,50);
n= [0.3 0.34 0.39 0.45];
const=(3/2)*Ts^2*10^12/pi^2;
L_lk1 = zeros(1,length(Ca));
L_lk2 = zeros(1,length(Ca));
L_lk3 = zeros(1,length(Ca));
L_lk4 = zeros(1,length(Ca));

for i=1:length(Ca)
    for j=1:length(n)
        str=sprintf(...
            'Ll-%f*(%f)^2*1/(%f)^2*1/(%f)=0',...
```

```
            const,Mv,n(j),Ca(i));
        a=solve(str);
        Llk(i,j)=double(a);
    end
end

for l=1: length(Ca)
  L_lk1(l) = Llk(l,1);
  L_lk2(l) = Llk(l,2);
  L_lk3(l) = Llk(l,3);
  L_lk4(l) = Llk(l,4);
end

plot(Ca,L_lk1,'-.',Ca,L_lk2,'-',Ca,L_lk3,...
    ':',Ca,L_lk4,'--','color','k','linewidth',1);
legend('n=0.3','n=0.34','n=0.39','n=0.45');
xlabel('Input Capacitance (C_a) E-009');
ylabel('Leakage Inductance (L_{lk}) E-004');
grid on;
print(gcf, '-depsc2', 'fig_410.eps');
print(gcf, '-dpng', 'fig_410.png');
```