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A Novel AC-DC Interleaved ZCS-PWM Boost Converter

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Abstract

AC-DC converters with input power factor correction (PFC) that consist of two or more interleaved boost converter modules are popular in industry. PFC is a must in today's AC-DC converters as their input current must meet harmonic standards set by regulatory agencies. With interleaving, the input current of each module can make to be discontinuous and the size of their input inductors since interleaving can reduce the high ripple in each module and produce a net input current with a ripple that is comparable to that achieved with a single boost converter module with a large input inductor.

In high- frequency converters, so as to achieve low harmonic, fast dynamic response, low size, and high-power density the frequency should be increased. The drawback of increasing the switching frequency is increasing the switching losses. This is reason that why soft-switching methods should be used. The focus of the thesis is on zero current switching (ZCS) methods for insulated gate bipolar transistor (IGBT) converters. The auxiliary switch in the proposed converter is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS and eliminate the switching losses. In addition, the auxiliary circuit is designed in a way that it can be activated only when the converter is operating with heavier loads and not used when the converter is operating with light load to maximize the overall efficiency.

The operation of the novel converter will then be explained and the mathematical analysis in steady-state will be derived. Based on the results of the analysis, general design guidelines will be provided. Finally, the design procedure will be confirmed by experimental results obtained from the proof of concept prototype.

Keywords

Power conversion, AC-DC converter, Interleaved boost converter, Zero-current switching, Soft- switching

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Acronyms

AC	Alternative Current
DC	Direct Current
EMI	Electromagnetic Interference
DCM	Discontinuous Current Mode
CCM	Continuous Current Mode
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
RMS	Root Mean Square
PWM	Pulse Width Modulation
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
THD	Total Harmonic Distortion
PFC	Power Factor Correction

Abbreviations

V_{in}	Input AC Voltage
V_o	Output DC Voltage
I_{in}	Input Current
I_o	Output Current
V_{rec}	Rectified AC Voltage
V_{dc}	DC Voltage
D	Duty Cycle
f_{sw}	Switching Frequency
t	Time
C_O	Output Capacitor
R_o	Output Resistive Load
L_1	Input Inductor 1
L_2	Input Inductor 2
L_{r1}	Resonant Inductor 1
L_{r2}	Resonant Inductor 2
C_r	Resonant Capacitor
S_1	Main Switch 1
S_2	Main Switch 2
S_a	Auxiliary Switch
D_1	Main Boost Diode 1
D_2	Main Boost Diode 2
D_{a1}	Auxiliary Diode 1
D_{a2}	Auxiliary Diode 2
D_{a3}	Auxiliary Blocking Diode 3
D_{a4}	Auxiliary Clamping Diode 4
V	Volt
A	Ampere
μ	Micro
k	Kilo
H	Henry
F	Farad

Chapter 1

1 Introduction

1.1 General Introduction

Power electronics is a field of power engineering that converts and controls input power to the desired output power by using semiconductor devices. The power source can be DC sources such as solar cells, batteries, and fuel cells, or AC sources like different kinds of electric generators. The power source can be single-phase or three-phase based on the application and its frequency is 50 or 60 Hz according to the region in which it operates. For instance, in North America, the frequency should be 60 Hz while in Europe it is 50 Hz. The load can be AC or DC, with or without isolation, single-phase or three-phase. Thus, power electronics converters are classified into:

- DC to DC
- DC to AC
- AC to DC
- AC to AC

A new interleaved boost AC-DC converter is proposed in this thesis. Its modes of operation will be analyzed and relevant mathematical equations for each mode of operation will be derived. The results of the mathematical equations derived for the proposed interleaved converter in the steady-state condition will be used to design the converter. The characteristic curves for the key components of the proposed converter will be presented by using MATLAB simulations based on the derived equations. Then, the value of each component can be determined by using the circuit simulator PSIM in order to satisfy the

key design objectives. Finally, the feasibility of the converter will be confirmed with results obtained from an experimental prototype.

1.2 Semiconductor Devices

In many cases, power converters, which are used to convert the available input power source to the desired output load, consist of passive elements such as inductors and capacitors, controllers to regulate the output voltage and semiconductor devices such as transistors and diodes. The semiconductors are one of the most important parts of any converter and can be classified into uncontrollable and controllable devices.

The diode is an uncontrollable semiconductor device, which should be forward biased to be turned on and conduct the current and reverse biased to be turned off. BJTs (Bipolar Junctions Transistors), MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors) are the most common controllable semiconductors. However, at high frequencies, IGBTs and MOSFETs are dominant. Diodes, MOSFETs, and IGBTs are explained in more detail in the following subsections.

1.2.1 Diodes

The following figure shows a diode and its current and voltage characteristics. A diode consists of anode and cathode sides when the current, i_d, is positive (Fig. 1.1.a) the diode is forward biased and conducts the current but when the voltage, V_d, is negative, it works as an open circuit and does not conduct the current, and this is called reverse biased. Therefore, the current can be flowed in only one direction from the anode to cathode. Fig. 1.1.b and Fig. 1.1c show actual and ideal characteristics of a diode respectively.

As can be seen from Fig. 1.1.c, an ideal diode does not conduct any negative current. However, as is shown in Fig. 1.2, in reality when the current through the diode decreases to zero, for a moment the current goes to negative and then reaches zero. This negative current, called reverse recovery current, and its duration are defined as t_{rr}, which is equal to the time that the current takes to reach negative and return to zero.

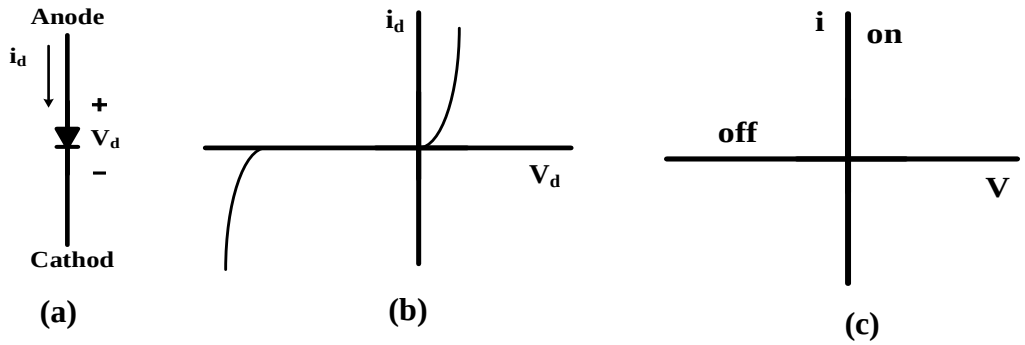


Fig. 1.1. (a) Symbol of a diode; (b) actual i-v characteristic; (c) idealized i-v characteristic

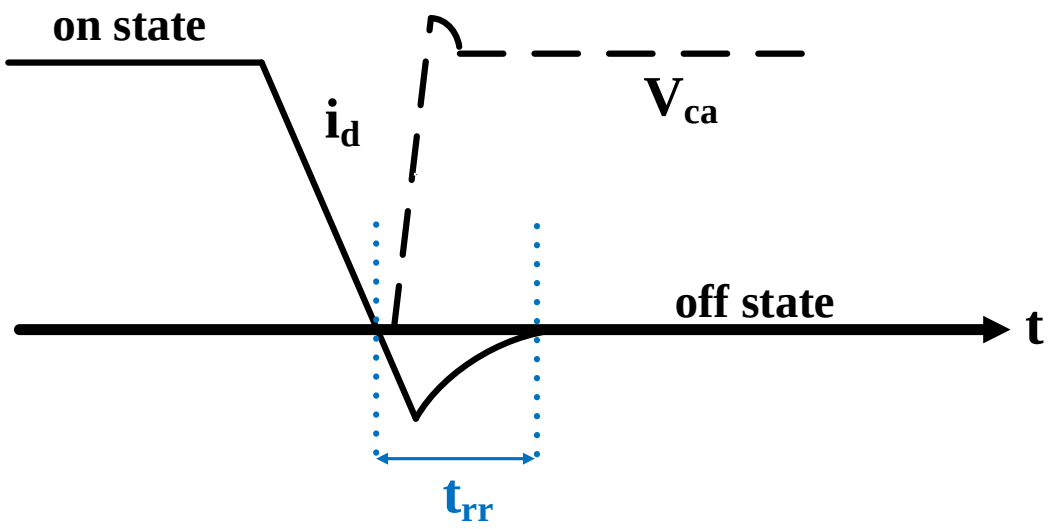


Fig. 1.2. Reverse recovery current of a diode

It can be seen from Fig. 1.2 that, during t_{rr}, voltage and current overlap and therefore reverse recovery current causes power losses in the diode. The other drawback of reverse recovery in a power electronic circuit is EMI (electromagnetic interference), which leads to malfunctions in the system. By increasing the frequency, reverse recovery losses will be increased; thus, power electronic engineers use fast recovery diodes that have a short t_{rr}. It should be noted that there is no overlap between current and voltage in the discontinuous mode because the current reaches and stays zero for a predetermined amount of time and reverse recovery loss is eliminated.

1.2.2 MOSFETs

The MOSFET (metal oxide field effect transistor) is one of the most common types of power semiconductor switches and consists of three terminals: gate (G), source (S) and drain (D). In Fig. 1.3, a circuit symbol of a power MOSFET is shown. MOSFETs are the best choice for lower power, higher switching frequency applications (> 100 kHz) for several reasons. The first reason is that their switching speed is fast, the second is that their on-state losses are low when operating with low drain-source voltage, and a third reason is that a small voltage needs to initiate the on/off transition of the forward current (i_{DS}) in MOSFETs because of the high impedance gate. Although MOSFETs are controllable semiconductor devices and can block positive drain-source voltage V_{DS}, they cannot block negative V_{DS} because they have an intrinsic anti-parallel diode. Voltage between the gate and source (V_{GS}) should be higher than about 4 V to conduct current. This voltage is called the threshold voltage, and MOSFETs can be considered to be open circuits for voltages less than this value. Therefore, by maintaining the gate voltage at a higher value (close to 10 V), MOSFETs can conduct drain current i_D and are considered to be on. During an on-state, a real MOSFET has a small resistor between the drain and source R_{DS}(on) that leads to conduction losses in the device. This conduction loss is one of the main reasons why MOSFETs are not the best choice for high power applications.

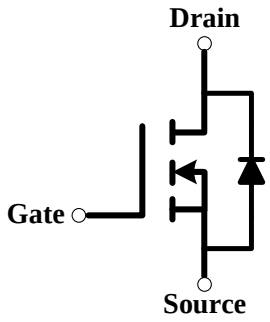


Fig. 1.3. Circuit symbol of an N-Channel power MOSFET

1.2.3 IGBTs

The IGBT (insulated gate bipolar transistor) is a combination of a MOSFET and a BJT (bipolar junction transistor). Its on-state is like that of BJT, while its gate is like that of MOSFET. This device consists of three terminals: a gate (G), an emitter (E) and a collector

(C). In Fig. 1.4, a circuit symbol of an IGBT is shown. Unlike MOSFET, IGBT may or may not have anti-paralleled body diodes.

Conduction losses in MOSFETs increase as the amount of current i_D increases, while those in BJTs are fixed; thus, for higher power applications, BJTs have lower conduction losses than MOSFETs. BJTs, however, are slower devices than MOSFETs because they require continuous base current to operate, and since IGBTs share some of the characteristics of BJTs, IGBTs are slower than MOSFETs. IGBTs turn off more slowly than MOSFETs because they have a current tail due to the fact that they are minority carrier devices. This means that electrons must be removed from these devices before they are turned off so that a significant overlap of voltage and current appears during this switching transition. Switching losses of IGBTs are higher than those of MOSFETs, but IGBTs are preferred over MOSFETs for higher power, lower switching frequency applications (< 100 kHz).

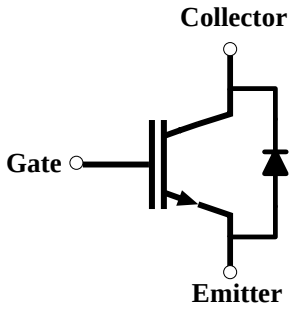


Fig. 1.4. Circuit symbol of an IGBT with an anti- parallel diode

1.3 High Switching Frequency Operation

Main energy storage in converters includes capacitors, inductors, and transformers. Usually, the size and weight of a converter depend on its energy storage components, which are necessary for storing and transferring energy. The size of the energy storage can be decreased by increasing the switching frequency of the converter, for instance, capacitors and inductors can store enough voltage and current respectively for a shorter amount of time, which leads to a lighter and smaller converter. Therefore, one of the advantages of increasing the switching frequency is reducing the overall size and weight of the converter.

In ideal switches, during turning on and turning off, there is no overlap between current and voltage and, as a result, there is no power loss.

On the other hand, in actual switches, current and voltage overlap, as shown in the next figure, which leads to power losses. This is one of the restrictions and disadvantages of increasing the switching frequency. In Fig. 1.5, Is and Vs are defined as current through and voltage across the switch respectively.

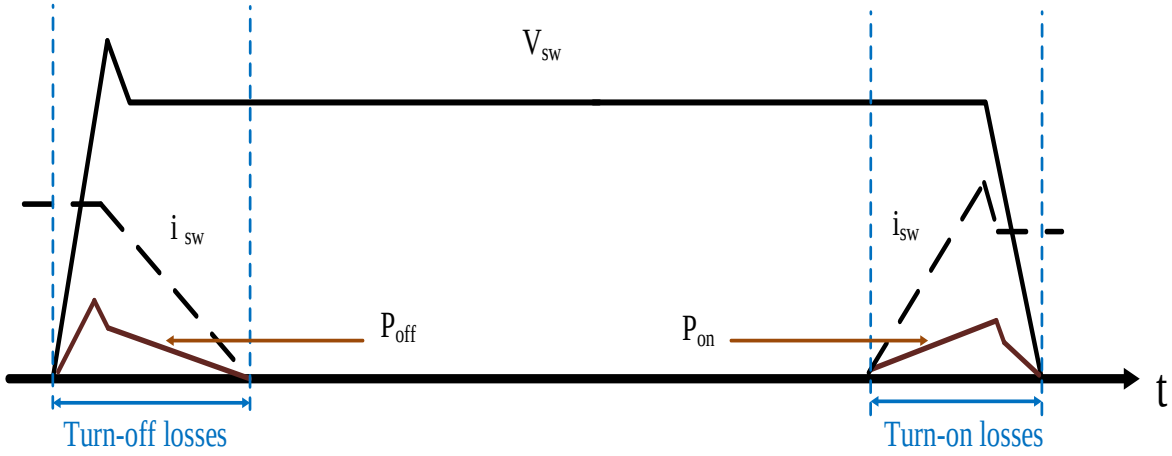


Fig. 1.5. Typical actual switch voltage and current waveforms

It can be seen from Fig. 1.5 that, in an actual switch, current and voltage overlap during the switching transition from on to off and vice versa. As power losses in switching are related to the multiplication of current and voltage, by increasing the switching frequency, the switching losses increase as well.

The dominant switching losses for a MOSFET happen while turning the switch on because the capacitor, which is placed between the drain and source of the MOSFET, stores the energy, and when the MOSFET is turned on, this capacitor discharges the voltage. Therefore, there is an overlap between current and voltage until the capacitor is discharged completely. However, the main switching losses for an IGBT, as shown in Fig. 1.6, occur while turning the switch off because it has the current tail. Thus, when it is turned off, the current tail and voltage overlap until the current tail goes to zero. These kinds of switching methods are called hard switching in the literature.

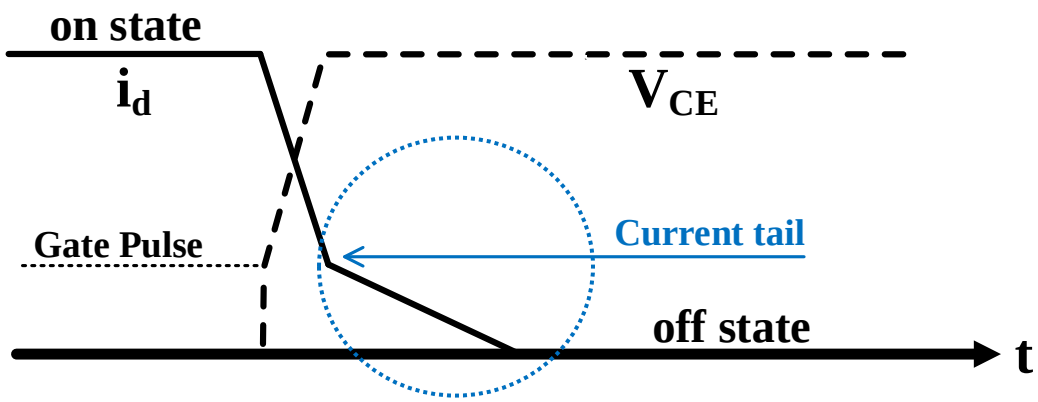


Fig. 1.6. Current tail in an IGBT

1.4 Soft Switching

Based on the abovementioned discussions, so as to operate a converter in high switching frequency, the problem of hard switching, which leads to power losses, should be solved. This problem can be tackled by soft-switching techniques. The techniques that should be implemented in converters in order to make the switching transition to something more gradual, are called soft-switching in the power electronics literature. Based on these techniques, one of the voltages or currents should be zero during the switching transition time. Therefore, because there is not any overlap between voltage across and current through the switch, switching losses can be almost eliminated. Since the transition is not sudden and is gradual, EMI will be reduced significantly as well.

Soft switching techniques can be categorized into two main types: ZVS (zero current switching) and ZCS (zero current switching) methods. Here some general information about these two main approaches is presented. The ZVS principle of operation is based on forcing the voltage to zero just before turning the switch on or off and keeping it zero during the switching transition time. In industry, all the MOSFETs and many kinds of IGBTs have the anti-parallel diode in their body, which allows them to conduct the current in the reverse direction. In other words, by having anti parallel diodes, MOSFETs can conduct current from the source to drain and for IGBTs from the emitter to collector. For IGBTs that have anti-parallel diodes and all MOSFETs, turning on under ZVS can be achieved by conducting the current through the body diode just before the switch is turned

on. As a result, during the switching transition, the voltage of the switch can be assumed to be zero. In addition, when the turning the switch off with ZVS, the rate of voltage rising across the switch should be decreased so as to restrict the overlap between voltage and current during the switching transition time. This can be done by adding a capacitor in parallel with the switch.

On the other hand, the ZCS technique can be achieved by forcing the current through the switch to zero just before the switch is turned on or off and maintain it at zero during the switching transition time. When turning the switch off with ZCS, the current should be diverted from the switch just before the switching. The most common way to do this is to impose a negative voltage across the switch or in a current path of the switch. Also, when turning the switch on with ZCS, the rate of current rising through the switch should be reduced in order to limit the overlap between voltage and the current of the switch during the switching transition time.

As discussed before, MOSFETs have $R_{DS,on}$ and should be used in high switching frequencies and low current applications. Most often, MOSFETs operate with ZVS as they have a fairly high drain-source capacitance. Therefore, as is shown in Fig. 1.7, MOSFETs are usually turned on and off with ZVS by adding a capacitor in parallel with them.

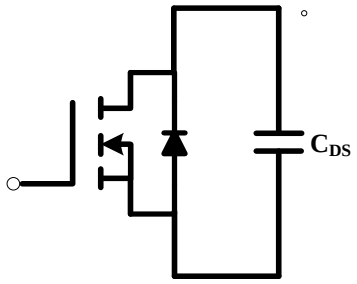


Fig. 1.7. Applying ZVS for MOSFET

On the other hand, because IGBTs have tail current, they are used in high current and lower switching frequency applications in comparison with MOSFETs. Usually, the soft-switching technique that are used for IGBTs are ZCS as they are minority-carrier devices (as shown in Fig. 1.8). It is worth noting that the most important switching losses for

MOSFETs and IGBTs, which should be eliminated, are turning-on and turning-off losses respectively. In this thesis, soft switching of IGBT under ZCS will be presented.

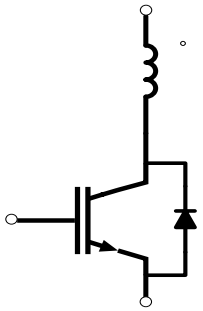


Fig. 1.8. Applying ZCS for IGBT

1.5 Single-Phase AC-DC Converters (Rectifiers)

AC-DC converters are essential in both of low and high-frequency applications. For instance, HVDC (high voltage direct current) is one of the areas in which inverters in the low -frequencies, where the switching frequency is almost the same as the line frequency, should be implemented. However, in this thesis, the focus is on high-frequencies where AC-DC converters can be used at battery chargers, telecommunication power supplies, uninterrupted power sources (UPS), medical devices, personal computers, information technology applications, and so on. One of the most important features that AC-DC converters should possess is that, their power factor should be close to one. In other words, input voltages and currents of these converters should be purely sinusoidal and in phase with each other to meet harmonic standards such as IEC 1000-3- 2 2, IEC-61 000-3-2, IEC 1000-3-4 and IEEE-519-1992. By increasing the power factor, the efficiency of the inverter, in terms of real power, can be increased. Power factor can be written as follows:

$$PF = \frac{P_{ave}}{P_{app}} \tag{1-1}$$

Where, P_{ave} and P_{app} are average power and apparent power respectively. It should be noted that, the input power factor of a current-fed converters is higher than a voltage-fed converter. Thus, power factor can be increased by using a current-fed converter.

1.5.1 The Boost Converter Topology

Boost AC-DC converters are used, when an AC input voltage should be stepped-up to meet a DC load voltage, which is higher than the AC source voltage. The topology of a boost AC-DC inverter is shown in Fig. 1.9, where a diode bridge rectifier is used to convert the input AC to DC. Then, four main components are used to boost the DC voltage, including: a semiconductor switch (S) such as MOSFETs and IGBTs in high –frequencies which should be turned on and off periodically, a diode (D), an inductor (L), and an output filter capacitor (C). The output voltage is dependent on the time in which the switch conducts, over the time of the switching cycle, which is the inverse of the switching frequency $T_S = \frac{1}{f_s}$. This ratio called duty cycle (D) and can be obtained as follows:

$$D = \frac{T_{on}}{T_S} \tag{1-2}$$

When switch is turned on, the current flows through the inductor and can be stored there. At this mode of operation, the output capacitor supplied the load. The voltage across the inductor at this time is equal to the input voltage. When the switch is turned off, the diode is forward-biased, thus the input current flows to the output. Now, voltage across the inductor is equal to V_{in}-V_o. Since, the output voltage is higher than the input voltage, this value is negative.

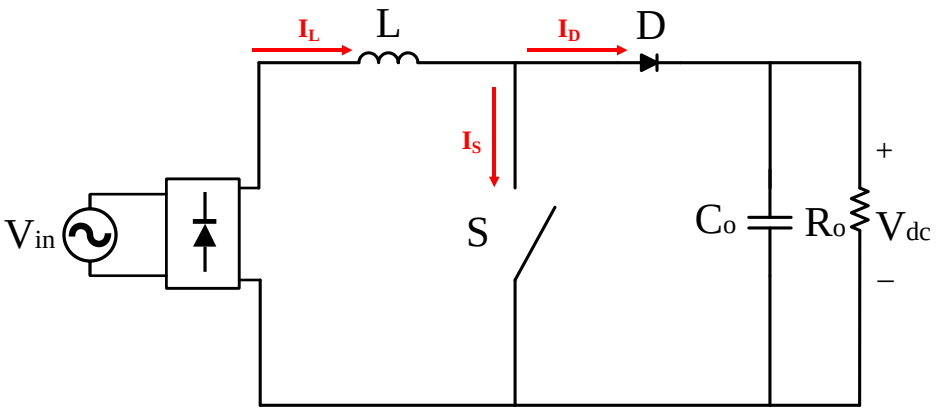


Fig. 1.9. Topology of a basic AC-DC boost converter

It should be noted that, ZVS and ZCS for a boost converter can be achieved by using resonant converters or resonant-transition converters frequently. In resonant converters, which use a resonant inductor (L_r) and a resonant capacitor (C_r), like Fig. 1.10 (ZVS) and Fig. 1.11 (ZCS), there are high peak switch voltage or current stress which leads to high conduction losses.

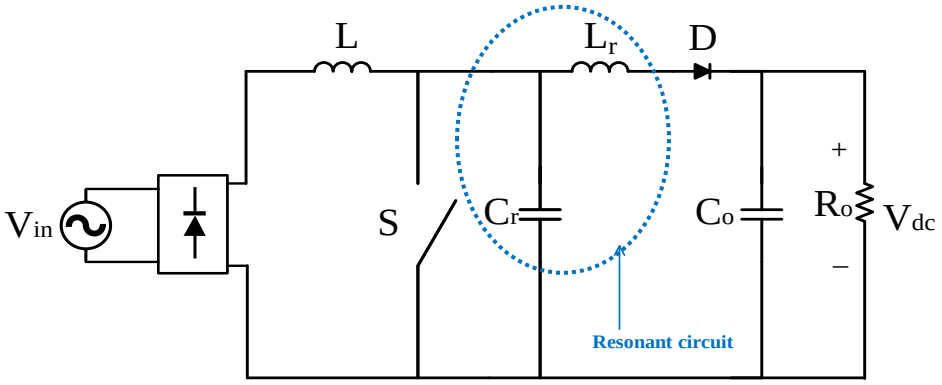


Fig. 1.10. Topology of a resonant boost converter operating with ZVS

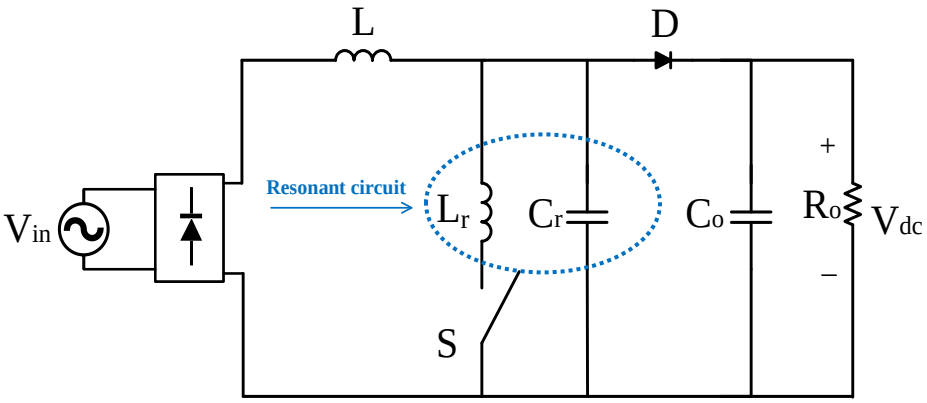


Fig. 1.11. Topology of a resonant boost converter operating with ZCS

On the other hand, since in resonant-transition converter an additional circuitry that is not a part of the main power circuit is used to perform ZCS or ZVS, it does not suffer from high peak switch voltage or current stress, so conduction loss is less than a resonant converter. In this thesis, the main idea is turning the auxiliary switch on only before turning the main switches off and then turning the auxiliary switch off right after it. Therefore, the

auxiliary switch operates for only a small portion of the switching cycle. In other words, the resonant-transition converter operates almost like a conventional converter.

1.5.2 The Interleaved Boost Converter Topology

A two-phase boost interleaved technique, applies two boost converters in parallel so as to conduct the current evenly through the two inductors and reduce the size of filter components. As is shown in Fig. 1.12, a boost interleaved converter is consisted of two switches S_1 and S_2, which are IGBTs in this thesis and need a periodic pulse that should be applied between gate and emitter terminals to turn them on and off periodically, two inductors (L_1, L_2), and two diodes (D_1, D_2) which are connected to a common filter capacitor (C_O) and load. Therefore, each inductor encounters with half current in comparison with conventional boost converters. Since, switches operate 180° out of phase, the inductors ripple currents are decreased by each other. The effective switching frequency is doubled while the input current is reduced. Thus, peak-to-peak variation in capacitor current is reduced as well which leads to use a smaller filter capacitor in comparison with a single boost converter with the same output voltage ripple. Smaller inductors and capacitor are needed; therefore, price and size of the inductors and capacitor are decreased significantly.

It can be seen from Fig. 1.12 that, voltage across each inductor when its switch is turned on and off is equal to V_{in} and V_{in}-V_{out} respectively. These values are exactly the same as the boost converter which was discussed previously. The duty cycle of the switch, D, which relates the width of this periodic pulse to the length of the switching period, determines the ratio of the output to the input voltage. Converters that have this property are called pulse-width modulated (PWM) converters. If the current through the inductor never drops to zero it would be operated in CCM (continuous current mode). The voltage gain of the boost converter in this condition is calculated as follows:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{1-3}$$

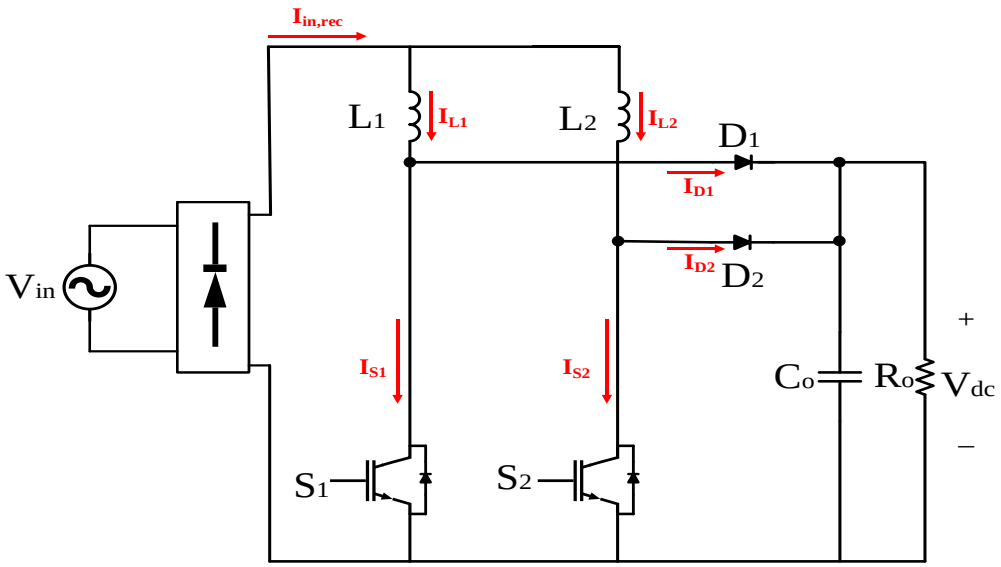
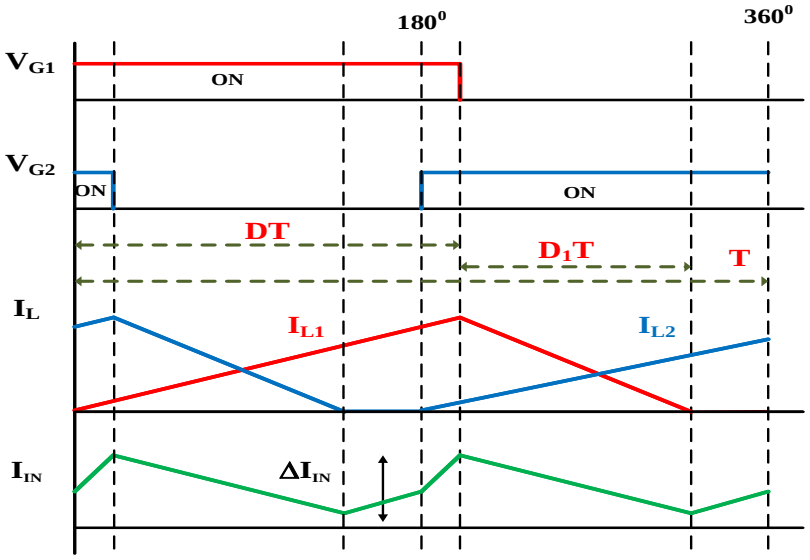


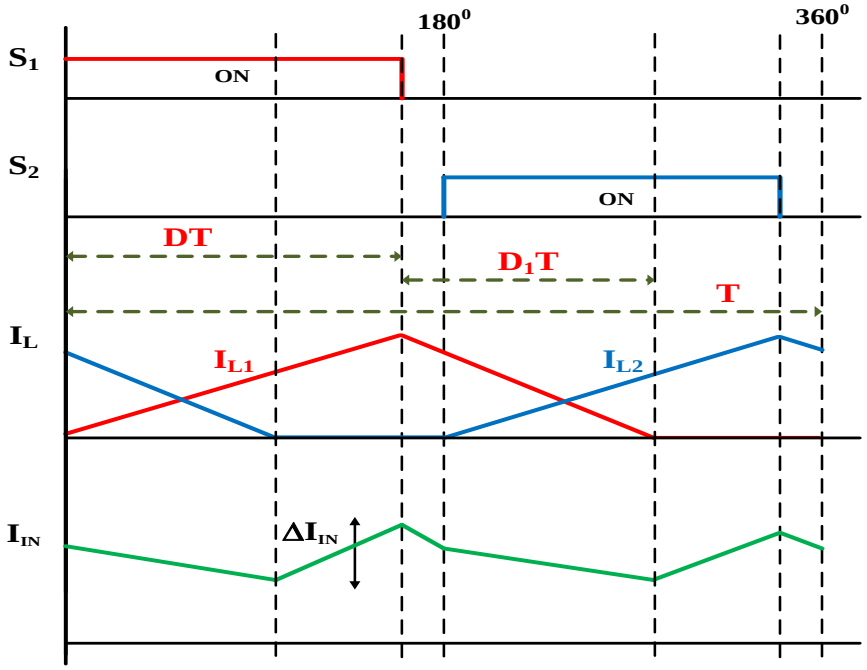
Fig. 1.12. Topology of a basic AC-DC interleaved boost converter

By using interleaving method, the input current of each module can be designed to be discontinuous (drops to zero) which leads to reduction of the size of the input inductors. This can be done, as interleaving can reduce the high ripple in each module and produce a net input current with a ripple that is comparable to that achieved with a single boost converter module with a large input inductor. In addition, there is less current stress on the converter components since they handle a fraction of the overall current, and the control is easier as more sophisticated control methods, which are needed for continuous current mode (CCM), are avoided.

Besides, by operating interleaved boost converter in DCM, switches can be turned on with ZCS, reverse recovery losses of diodes are eliminated, and the small size inductances can also be used. However, the turn- off losses of the switches still exist and should be tackled by soft switching method, which is ZCS in this thesis and will be explained in the next chapter in more details. The inductor current waveforms are shown in Fig. 1.13, according to the switching pattern in the DCM for $D \geq 0.5$ and $D < 0.5$.



(a)



(b)

Fig. 1.13. Inductor current waveforms according to the switching pattern in the DCM.

As can be seen from Fig. 1.13, inductor current ripple is reduced by using interleaved technique. Since an AC input source can be considered to be a DC input source during a very short switching cycle, different equations such as voltage gain can be derived by assuming input source as DC. In the following equations, DT and D_1T are defined as the switching on-time and the time period in which the phase current becomes zero after DT respectively:

$$\frac{di_{L1,2}}{d_t} = \frac{V_{in}}{L_{1,2}} \quad \text{(rising slope)} \tag{1-4}$$

$$\frac{di_{L1,2}}{d_t} = \frac{V_{in} - V_{out}}{L_{1,2}} = \frac{-D\,V_{in}}{L_{1,2}\,D_1} \quad \text{(falling slope)} \tag{1-5}$$

Voltage gain of the interleaved boost converter is obtained as follows:

$$\frac{V_{out}}{V_{in}} = \frac{D + D_1}{D_1} \tag{1-6}$$

As discussed before, half of the input current flows from each boost converter. Thus, the average diode current is obtained:

$$I_{D1,2} = \frac{1}{2}\left(\frac{V_{in}DT}{L_{1,2}}\right)D_1 = \frac{1}{2}\,\frac{V_{out}}{R} \tag{1-7}$$

By rearranging:

$$D_1 = \left(\frac{V_{out}}{V_{in}}\right)\frac{L}{RDT} \tag{1-8}$$

Substituting equ. (1-8) into equ. (1-6) results in:

$$\left(\frac{V_{out}}{V_{in}}\right)^2 - \left(\frac{V_{out}}{V_{in}}\right) - \frac{D^2RT}{L_{1,2}} = 0 \tag{1-9}$$

In this thesis, by using an additional circuitry that is not a part of the main power circuit, ZCT is performed in an interleaved converter. As discussed previously, in the resonant-transition converter, the auxiliary switch operates only for a small portion of the switching cycle. Before turning each main switch off, the auxiliary switch is turned-on which makes a capacitor in the auxiliary circuit undergoes resonance with the auxiliary inductors. By resonating this capacitor, a negative voltage is imposed across the auxiliary inductor-switch, so the currents of the main switches force to be reduced to zero before the pulses at the gate of main switches are removed. Therefore, main switches can be turned -off with ZCS method. In the next section, some of the soft switching methods which have been proposed in the referred papers for interleaved converter will be presented.

1.6 Literature Review

AC-DC converters with input power factor correction (PFC) that consist of two or more interleaved boost converter (IBC) modules are used widely in industry [1-18]. As it was discussed previously, soft-switching approaches for these converters can either be zero-voltage switching (ZVS) if they are implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. The main idea of this thesis is performing ZCS condition for turning IGBTs on and off. Most of these use an auxiliary circuit that is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS.

ZCS methods in boost converters have at least one of the following drawbacks [13-27]:

• The auxiliary circuit causes the main converter switch to operate with a higher peak current stress that creates a need for a higher rated device for the main switch.

• The auxiliary switch should be turned on for a long time which reduces the efficiency.

• The main switches or auxiliary switch need a floating driver which makes driving more complicated and increase the noise.

• Auxiliary circuit components must be placed in the main part of the converter so that the auxiliary circuit is not completely separated from the main converter. This means conduction losses can be increased and higher current rated components need to be used.

• Each module of an interleaved AC-DC boost converter must have its own ZCS auxiliary circuit to help its main switch to be turned-off with ZCS. This adds cost to the overall interleaved converter.

Now the above-mentioned drawbacks of the previous papers are explained by some sample papers.

ZCS-PWM converters that use an auxiliary circuit to help the main converter switch turn-on with ZCS are generally less efficient than hard-switching converters at light loads. The main reason for this is that the auxiliary circuit losses dominate when the converter is operating under these conditions. Auxiliary circuit losses include the turning on and off of the auxiliary switch and additional conduction losses as there can be an increased amount of circulating current flowing in the converter. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads when the main switch switching losses that are eliminated - especially the IGBT current tail losses - are greater than the auxiliary circuit losses.

Ideally, the auxiliary circuit used to achieve ZCS operation in a ZCS-PWM converter should be activated only when the converter is operating with heavier loads and not used when the converter is operating with light load. Operating the converter in such a manner would ensure the optimal efficiency profile over the entire load range. This, however, generally cannot be done with ZCS-PWM converters because of the presence of an inductor placed in series with the main switch. As can be seen in the example converters shown in Figs. 1.14 and 1.15, an inductor is typically placed in series with the main switch so that it can turn on with ZCS. The series inductor slows down the rate of rise in current after the switch has been turned on so that the overlap between voltage and current in this switch can be reduced.

Although the presence of this series inductor in a ZCS-PWM converter is beneficial, it prevents the auxiliary circuit from being disengaged from the main converter when the converter is operating under light load conditions. As long as this series inductor is in the converter, the auxiliary circuit must be used at all times, across the full load range – even when it is not necessary under light load conditions – because failure to do so would result in the damage of the main switch. Given the size of the series inductance, which may be relatively small compared to that of the input boost inductor but is not insignificant, the energy in this inductance would result in the appearance of high voltage spikes across the switch when it is turned off as there would be no path for current to flow through.

There are several possible solutions to the problem of having an inductor placed in series with the main switch, but none of them are truly satisfactory. It may be possible to place a bypass switch of some sort across the series inductor so that when the auxiliary circuit is not needed, the bypass switch would be turned on and current would bypass the inductor, but this would add cost and make the converter more complex.

Another possible solution is to implement the converter with an active auxiliary circuit and a passive snubber. With such a scheme, the active auxiliary circuit would be activated only when the converter is operating with heavier loads and the passive snubber would be used to deal with the series inductor energy when the main converter switch is turned off with the auxiliary circuit is disengaged from the main circuit. This approach would again increase the cost and the complexity of the converter.

If the main switch could somehow be made to turn on with ZCS without having an inductor in series with the main switch, then it would be possible to avoid using the auxiliary circuit when the converter is operating under light load conditions. This is, in fact, possible when the converter is operating with a discontinuous input inductor current. In such a case, the main converter switch would turn on with ZCS as initially there would be no current flowing through the switch. Current through the switch would rise gradually, given the size of the input boost inductor.

Discontinuous current mode operation is advantageous when a boost converter is implemented with two converter modules in parallel and the modules are interleaved with

respect to each other with a phase difference of 180°. Interleaving is commonly used as a means of reducing current ripple in power converters. In the scheme being described, if the individual converter modules are ZCS-PWM converters, then it would be possible to disengage the auxiliary circuit from the main circuit as there would be no need of a series inductance to help the main switch turn on with ZCS.

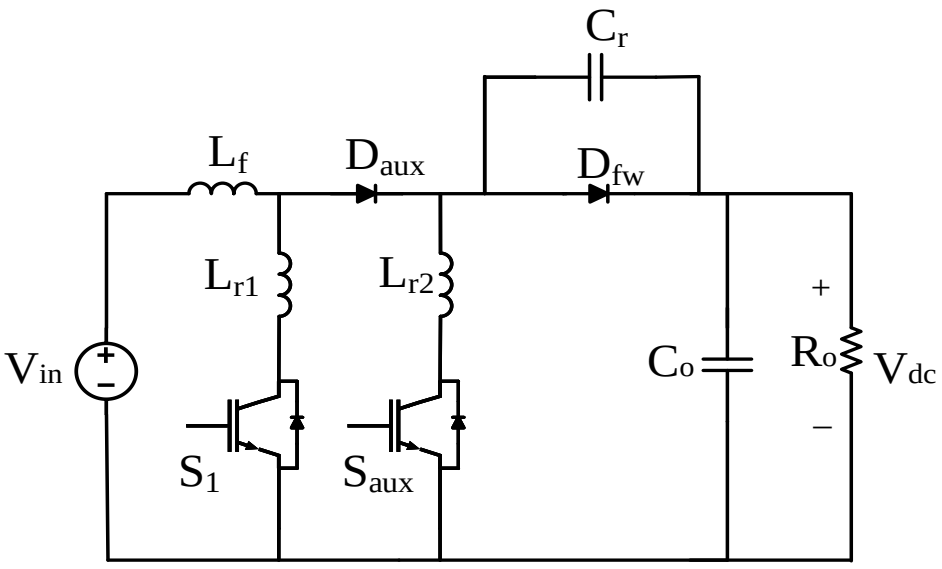


Fig. 1.14. ZCS boost converter proposed in [19]

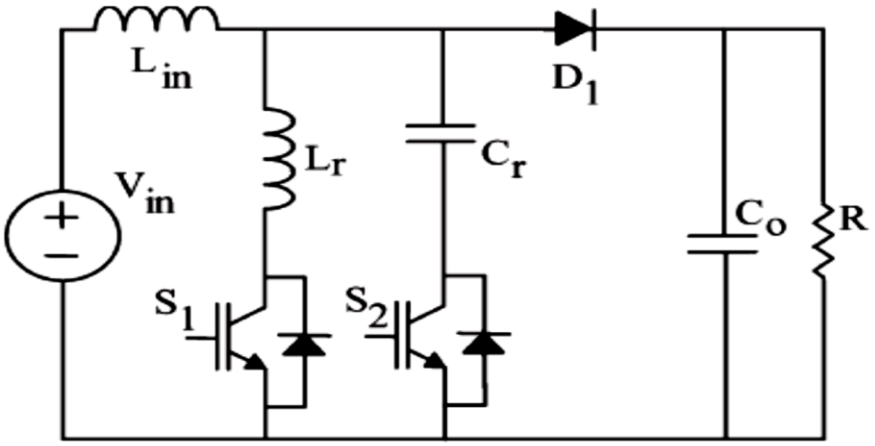


Fig. 1.15. ZCS boost converter proposed in [20]

One of the basic topologies, which is shown in Fig. 1.16, has been presented in [14]. The main drawback is that, each module of the proposed interleaved AC-DC boost converter must have its own ZCS auxiliary circuit to help its main switch turn off with ZCS. Since two switches should be used, the price and complexity of the converter are increased. Another disadvantage of this topology is that, the converter in the absence of high-voltage conversion ratio does not have an appropriate ZCS. The next problem is that, each auxiliary switch should not be turned -off exactly after turning its main switch off. It means that, both of auxiliary switches need some time after turning their main switches off to be turned off with ZCS, which increases the conduction losses.

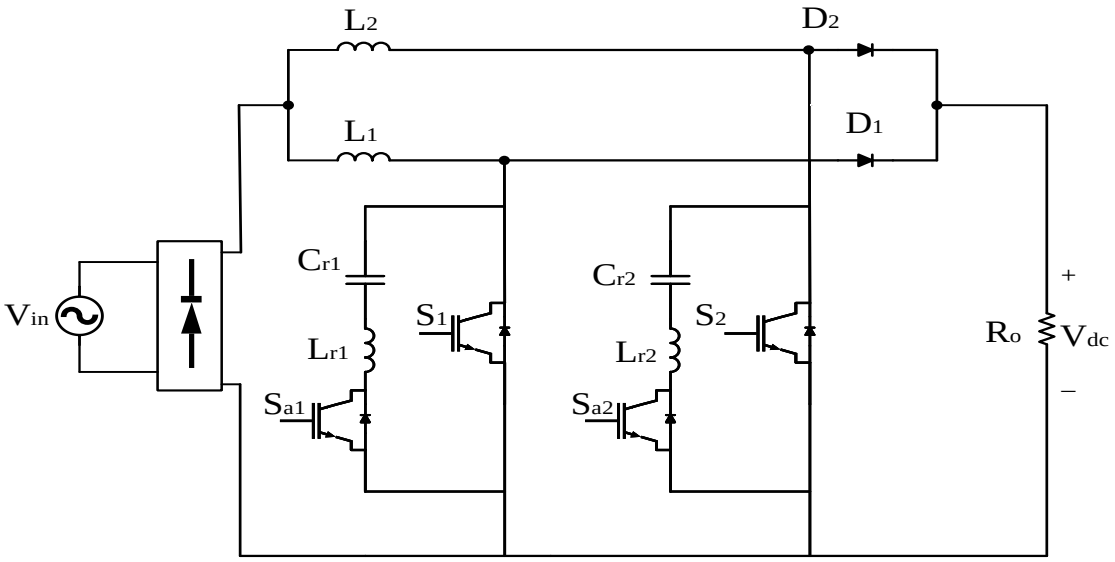


Fig. 1.16. Interleaved ZCT boost converter proposed in [14]

In the auxiliary circuit proposed in [16], main switches are turned on and off with ZVS and ZCS respectively. But one of the drawbacks of this topology is that, the resonant switch operates with hard switching. Besides, as it needs soft switching for turning the main switches on as well, the auxiliary switch should be operated four times in each switching cycle for turning on and off main switches which leads to higher switching losses.

Although the problem of hard switching of the auxiliary switch is solved in [11], yet it works like that of [16], which means that the auxiliary switch should be operated four times in each switching cycle to turn main switches on and off with ZVS and ZCS respectively.

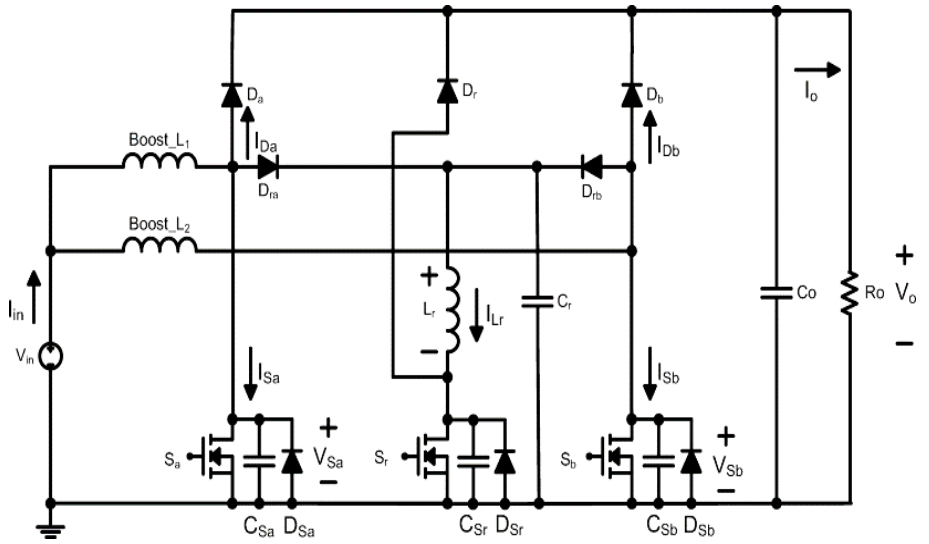


Fig. 1.17. Interleaved ZVS/ZCS boost converter proposed in [16]

Another disadvantage of this topology is that, it needs a bulky clamping capacitor C_1 which is placed in the path of the main power circuit, so the auxiliary circuit is not completely separated from the main converter. Therefore, the auxiliary circuit cannot be disengaged from the main power circuit in the light loads.

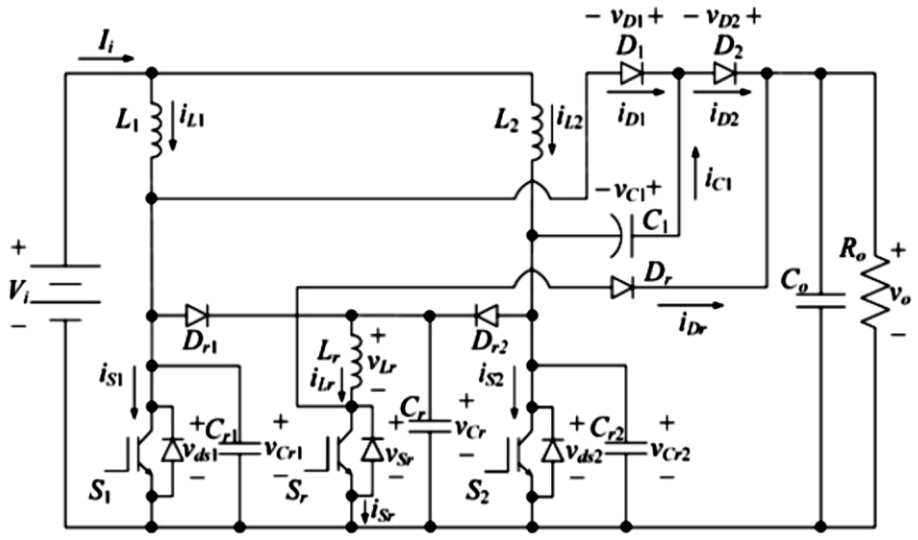


Fig. 1.18. Interleaved ZVS/ZCS boost converter proposed in [11]

In some papers such as [17], the auxiliary diodes are in series with the main power circuit. Since, these diodes should tolerate higher average current rating, their price and conduction losses are increased. In addition, maximum voltage across D_o in [17] is twice the output voltage. Also, as auxiliary inductor is in series with the main circuit path, maximum voltage across the main switches, auxiliary switch and the main diodes are higher than the output voltage.

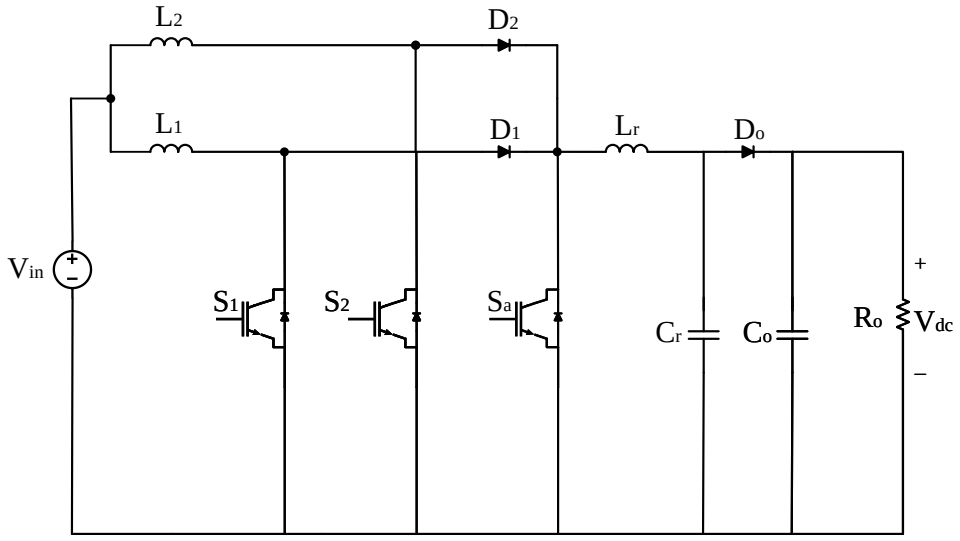


Fig. 1.19. Interleaved ZCS boost converter proposed in [17]

The auxiliary circuit proposed in Paper [21] can be seen in Fig. 1.20, where voltages across D_{a1} and D_{a2} are twice the output voltage. The auxiliary inductor is in the path of the main power circuit therefor voltage across the main switches, auxiliary switch and main diodes are higher than the output voltage.

Since in the auxiliary circuit in [22], two switches do not share the common ground, auxiliary switch needs a floating gate driver, which increases the noise and complexity of the proposed circuit

The authors in [18] have used two inductors in series with the input inductors. Because auxiliary inductors are in the path of the main power circuit, voltage across the main switches and diodes are higher than the output voltage. Voltage across the auxiliary switch is almost two times of the output voltage

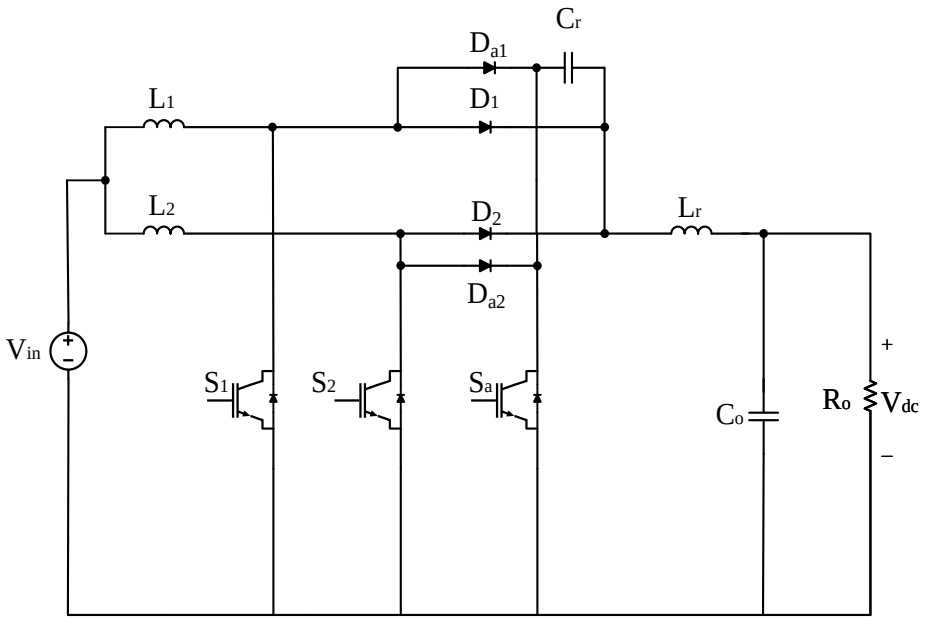


Fig. 1.20. Interleaved ZCS boost converter proposed in [21]

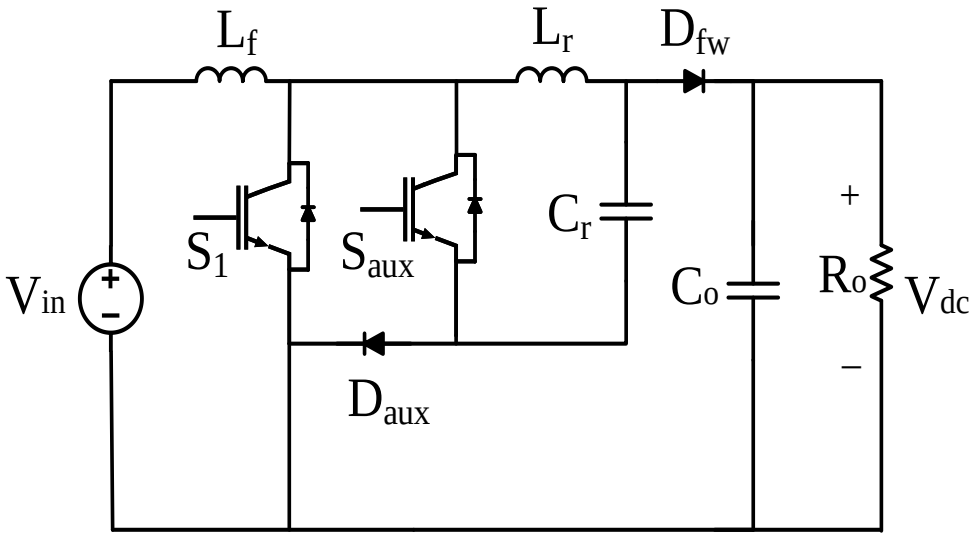


Fig. 1.21. ZCS boost converter proposed in [22]

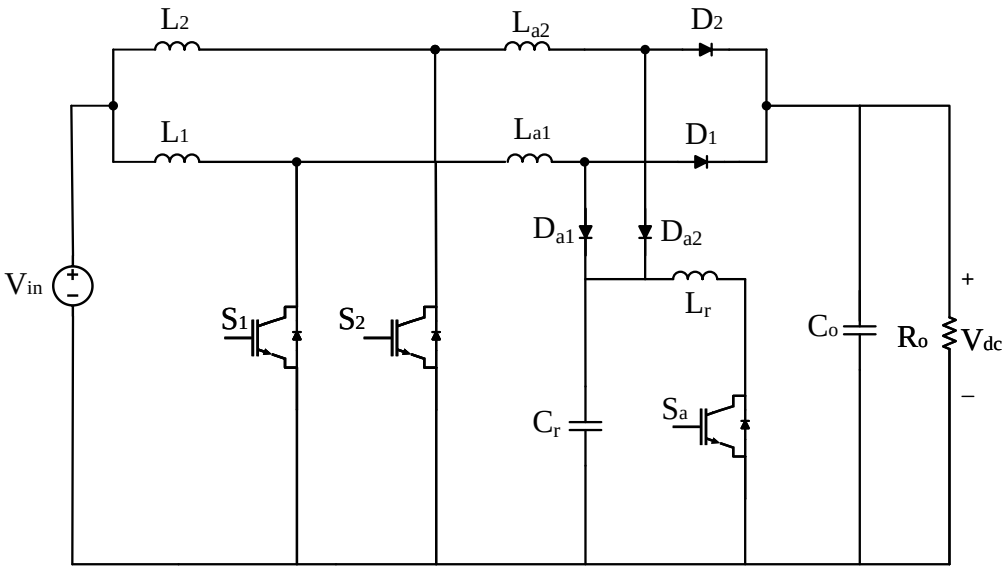


Fig. 1.22. Interleaved ZCS boost converter proposed in [18]

1.7 Thesis Objectives

The main objectives of this thesis are as follows:

- To propose a novel AC-DC interleaved ZCS-PWM boost converter that does not have any drawbacks that mentioned for the converters reviewed in this chapter, without adding any new component in the main power path.
- To analyze the steady-state characteristic of the proposed converter by mathematical analysis so that it can be properly designed.
- To derive design procedure for the new interleaved converter which can be used for selecting the proper components
- To confirm the feasibility of the proposed converter proposed in this thesis by computer simulation and experimental results obtained from a proof-of-concept prototype.

1.8 Thesis Outline

The thesis is organized as follows:

- In Chapter 2, the new interleaved boost converter which has a single auxiliary switch to perform ZCS for all switches will be introduced, its modes of operation will be explained and its features will be described.
- In Chapter 3, circuit analysis of the proposed converter will be analysed mathematically based on the different modes of operation discussed in Chapter 2. Then equations which describe the voltage and current of the different components of the converter in steady-state will be derived.
- In Chapter 4, the results of the mathematical equations derived from the proposed interleaved converter in the steady-state condition in Chapter 3, will be used to determine the condition of operating main switches and auxiliary switch with ZCS. The characteristic curves for the key parameters of the proposed converter will be presented by applying the MATLAB simulations according to the steady-state equations. Effects of each key component on the operation of the converter will be discussed. Then, the design procedure will be explained by an example. By using characteristic curves generated by MATLAB program and the circuit simulator PSIM, the value of each component will be determined in order to satisfy the key design objectives. Selected values will be used in the next chapter to build a laboratory prototype.
- In Chapter 5, the design procedure discussed in Chapter 4 will be validated by the laboratory proof-of-concept prototype. The results of the voltages and currents obtained from Oscilloscope will be plotted. The efficiency of the proposed AC-DC interleaved ZCS-PWM boost converter will be compared with the conventional one.
- In Chapter 6, the content of this thesis will be summarized, and the conclusion will be presented. Then the main contributions of this thesis will be stated and suggestions for future works will be presented.

Chapter 2

2 Modes of Operation of the Novel AC-DC Interleaved Boost Converter

2.1 Introduction

As was explained in Chapter 1, interleaving multiple AC-DC converter modules is advantageous as input current ripple can be reduced and smaller input inductors can be used. If soft-switching is desired, then either ZVS or ZCS can be used, depending on what is used for the switching devices. If IGBTs are used, then ZCS is preferred as it eliminates the turn-off current tail that these devices have, which contributes to turn-off switching losses.

Previously proposed interleaved ZCS-PWM AC-DC converters have several drawbacks, including higher cost due to the need for multiple auxiliary circuits to help the main witches turn off with ZCS. A new interleaved ZCS-PWM AC-DC converter that does not have many of the drawbacks of previously proposed converters of the same type is proposed in this chapter. In this chapter, the general operation of the proposed converter is explained, its modes of operation are discussed in detail, and its features are stated.

2.2 Modes of Operation

The proposed converter, shown in Fig. 2.1, consists of two boost converter modules, one with L_1, S_1, and D_1, the other with L_2, S_2 and D_2. The gating signals of the two main switches, S_1 and S_2 are identical but shifted 180^o with respect to each other. The currents in L_1 and L_2 are designed to be discontinuous and identical, with 180^o phase shift with respect to each other. The two boost modules are connected to the same auxiliary circuit, which consists of interfacing diodes D_{a1} and D_{a2}, reverse blocking diode D_{a3}, switch voltage clamping diode D_{a4}, resonant inductors L_{r1} and L_{r2} and resonant capacitor C_{r1}. The auxiliary switch needs to be activated whenever one of the two main switches is about to be turned off and is active for only a fraction of the switching cycle.

The various modes of operation that the proposed converter goes through during a switching cycle are explained in this section. The modes of operation are studied for the case when the converter is operating in steady-state, which can be defined as the converter components having the same voltage and current at the end of a switching cycle (and the start of a new one) as thy have at the start of the cycle. In other words, the voltage and

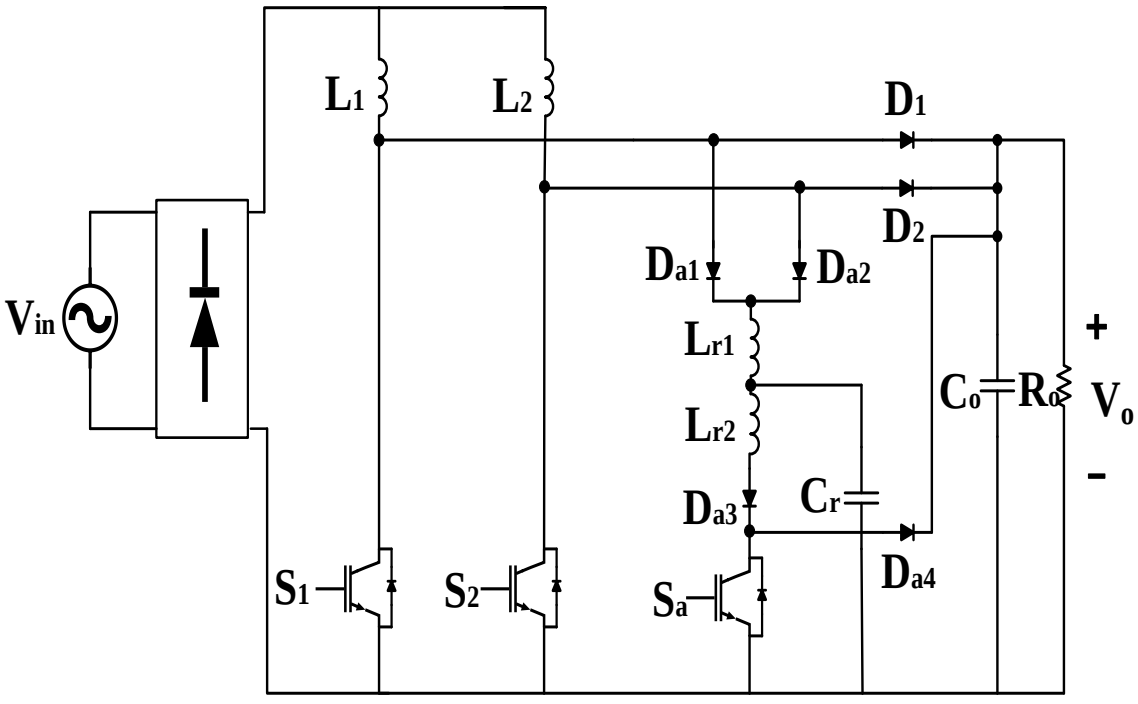


Fig. 2.1. Proposed interleaved AC-DC ZCS-PWM boost converter

current waveforms of all components of the proposed interleaved converter should be identical for every switching cycle when the converter is operating in steady-state.

Typical voltage and current waveforms of the proposed converter are shown in Fig. 2.2 and equivalent circuit diagrams of each mode are shown in Figs. 2.3 to 2.9 for a half switching cycle, for the case when duty cycle $D \geq 0.5$ and S_2 is turned on and S_1 is turned off. The modes of operation for the other half-cycle when S_1 is turned on and S_2 is turned off are identical. The following assumptions have been made in Figs. 2.3-2.9:

- The proposed circuit has two boost modules that are designed to be operated in DCM so that the input inductor current of each module is discontinuous, but the input current, which is the sum of the inductor currents, is continuous.
- Since the AC input source voltage is equivalent to a DC voltage during a very short amount of time such as a switching cycle, it is considered as a DC input voltage.
- The output filter capacitor, C_o, is large enough to be considered as a voltage source, V_o.
- All semiconductor switches are ideal with no parallel output switch capacitor across them.
- All inductors and capacitors are ideal and have negligible resistances.
- All diodes are ideal and have no reverse recovery current.
- The duty cycle D is greater or equal to 0.5.

Mode 1 ($T_0 < t < T_1$): This mode begins when switch S_2 is turned on. The rectified voltage is applied to L_2 and the current through the L_2 linearly increases as does the input current in the input inductor I_{in}. The slope of the current is $\frac{V_{in}}{L_2}$. Since I_{in} is the summation of the I_{L1} and I_{L2}, it will increase with greater slope.

Mode 2 ($T_1 < t < T_2$): This mode begins when the auxiliary switch (S_a) is turned on in preparation to turn off main switch S_1 with ZCS. S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases.

Mode 3 ($T_2 < t < T_3$): This mode begins when the voltage across C_r, V_{Cr}, is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. The voltage

across D_1 and D_2 is limited to the output voltage. The current through L_{r1} increases, thus I_{L1} and I_{L2} flow through the L_{r1}. The current in L_2 is less than L_1, thus the current through S_1 becomes zero and S_1 can be turned off with ZCS. The current through S_2 becomes negative and flows through its body diode.

Mode 4 ($T_3 < t < T_4$): This mode begins when the current in L_{r2} reaches zero because of its resonance with C_r; S_a can then be turned off with ZCS condition. During this mode, energy in L_{r1} is transferred to C_r, thus increasing its voltage so that V_{Cr} becomes less negative and is in the process of eventually becoming positive.

Mode 5 ($T_4 < t < T_5$): This mode begins when the net voltage across the C_r and L_{r1} becomes positive, thus auxiliary diode D_{a2} stops conducting and I_{L2} flows through S_2. D_{a1} continues to conduct during this mode.

Mode 6 ($T_5 < t < T_6$): This mode begins when V_{Cr} reaches the output voltage V_o. D_4 clamps the voltage across the auxiliary switch to V_o as well and the stored energy in L_{r1} is transferred to the output so that the current in the L_{r1} decreases. When the current through L_{r1} becomes less than I_{L1}, diode D_1 starts to carry the current difference. The voltage across L_1 becomes (V_o-V_{rec}) and the current through L_1 starts to decrease linearly.

Mode 7 ($T_6 < t < T_7$): This mode begins when the current in L_1 reaches zero. This is the last mode of the half-cycle. The next half-cycle begins when S_1 is turned on under ZCS.

When D is less than 0.5, the modes of operation of the converter are identical to those shown in Figs. 2.3-2.9 except for Mode 1 when only switch S_1 is on.

The proposed converter has the following features:

(i) All the converter switches turn on and off with ZCS.

(ii) There is only one active auxiliary circuit for both main switches instead of each main switch needing its own active auxiliary circuit to help it turn off with ZCS.

(iii) The main switch does not have increased peak and RMS current stresses as it the case with resonant type ZCS auxiliary circuits because no current from the auxiliary circuit flows into the main circuit.

(iv) None of the auxiliary circuit components are in the main power path so that they only handle a fraction of the current that the main circuit components handle.

(v) The voltage stress of the auxiliary switch is clamped to the output voltage and does not exceed this voltage.

(vi) The main boost diodes do not have reverse recovery current as the input inductor currents are discontinuous.

(vii) The auxiliary circuit does not interfere with the interleaving operation of the converter thus all the advantages of interleaving are maintained.

(viii) The auxiliary circuit can be deactivated when the converter is operating under light-load conditions, unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load; thus light-load efficiency is improved because there is no auxiliary circuit component in the main power circuit.

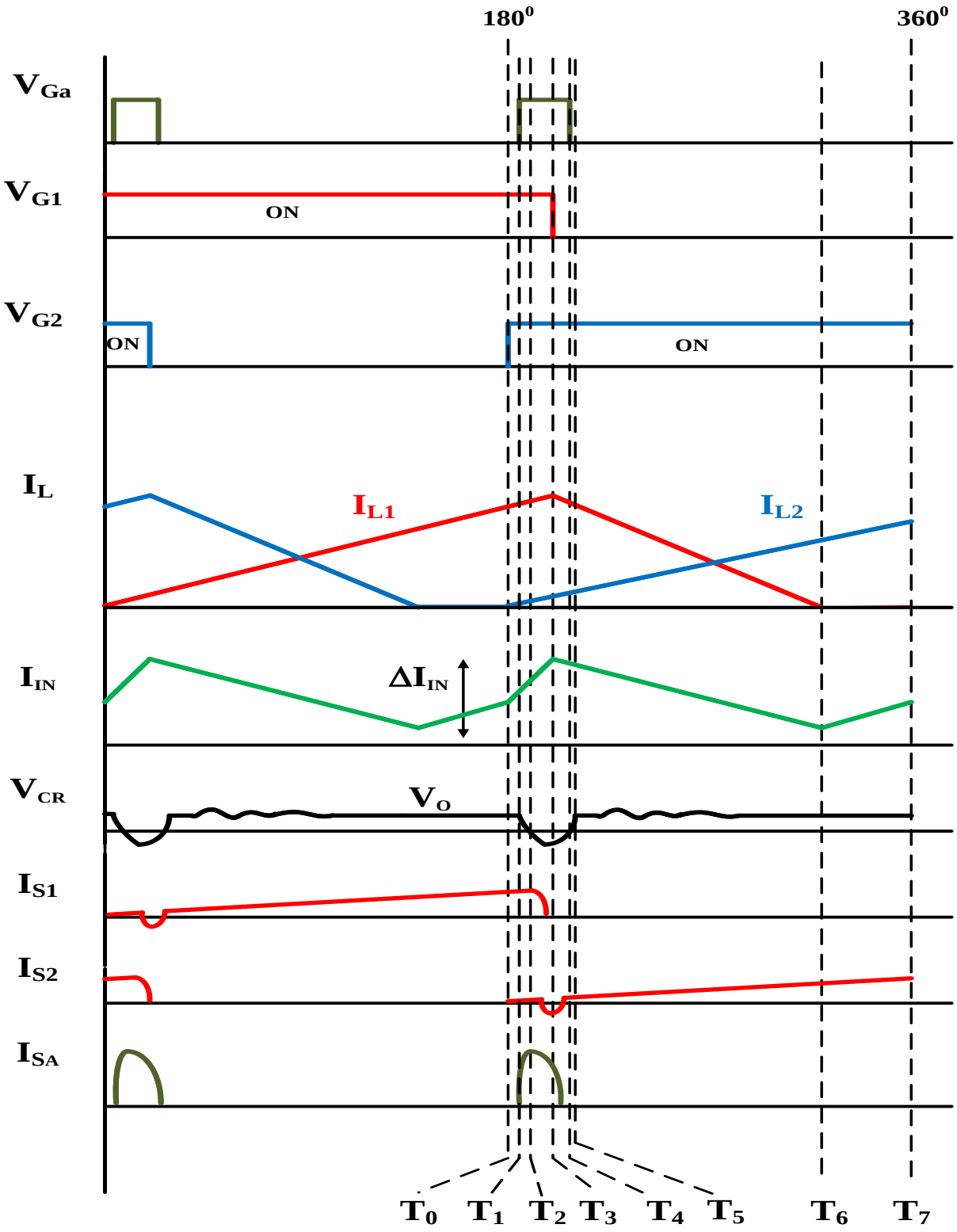


Fig. 2.2. Voltage and current waveforms of different circuit components of the proposed interleaved boost converter in steady state.

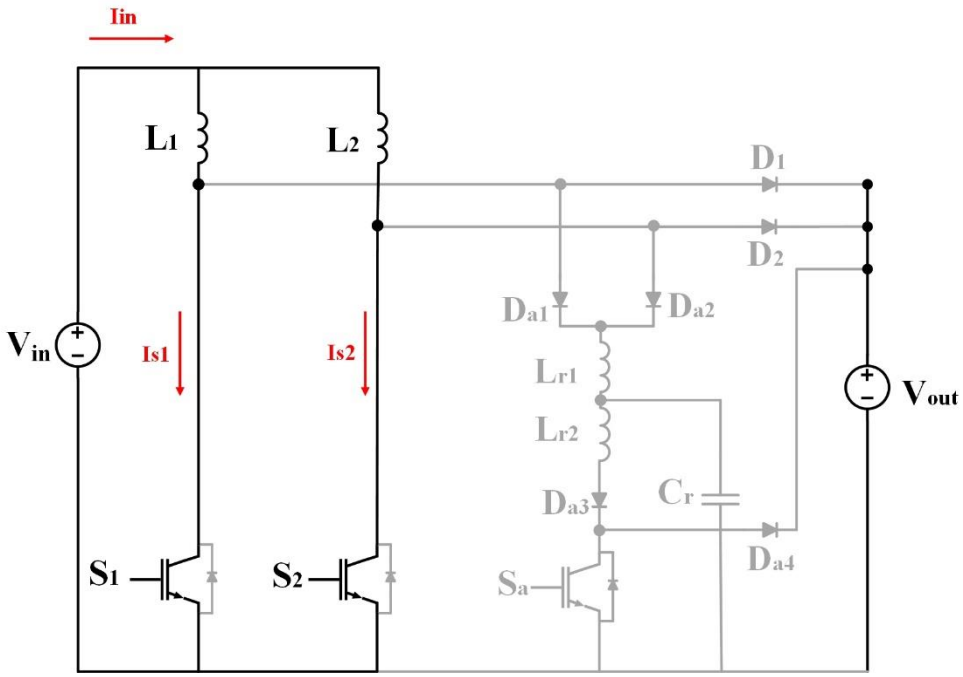


Fig. 2.3. Current flow in Mode 1

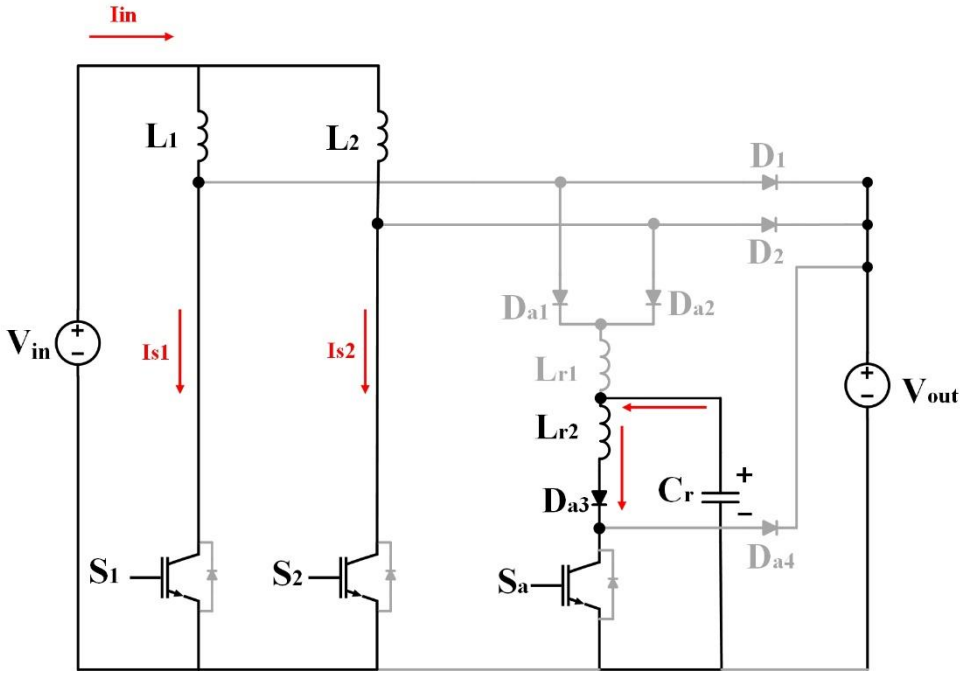


Fig. 2.4. Current flow in Mode 2

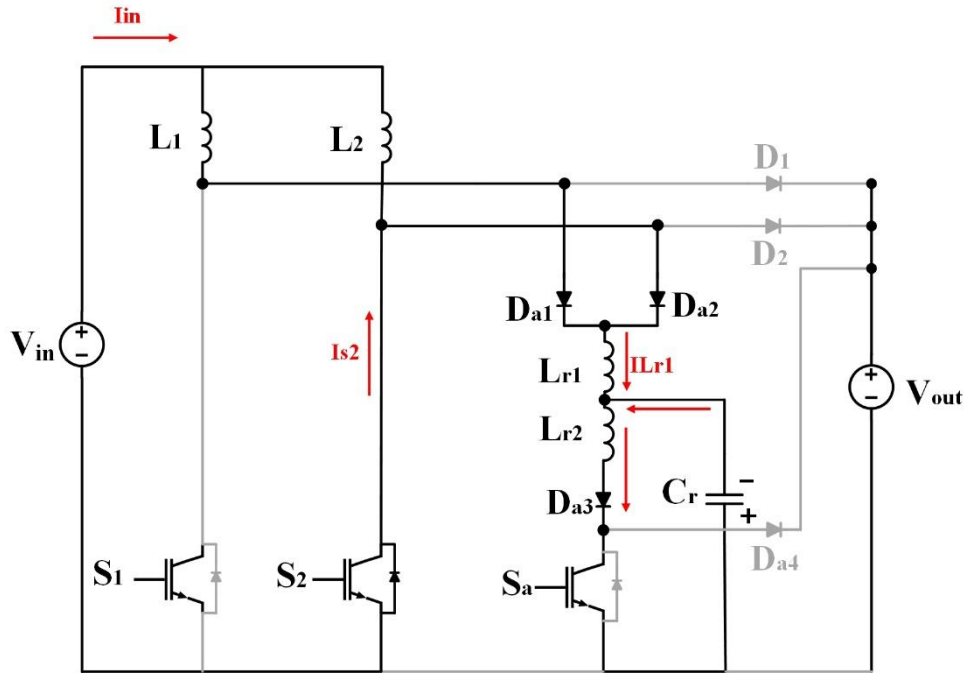


Fig. 2.5. Current flow in Mode 3

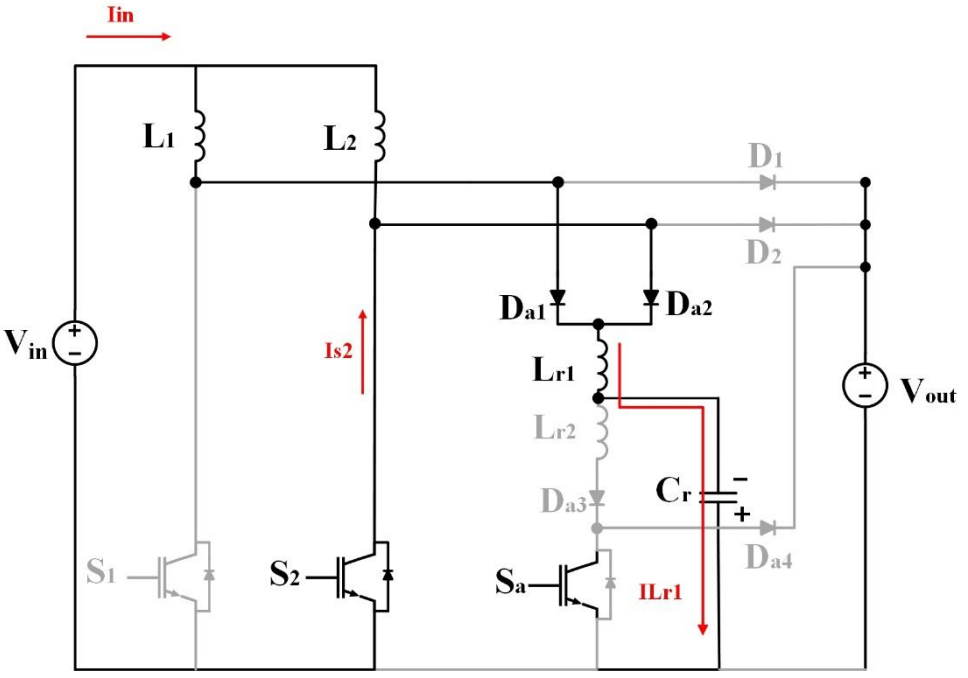


Fig. 2.6. Current flow in Mode 4

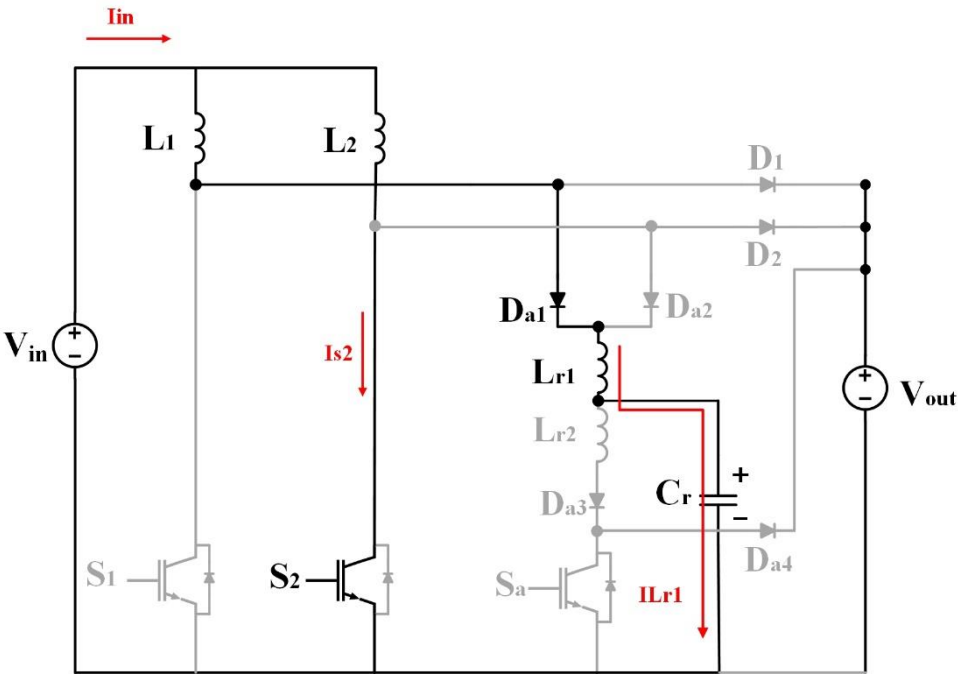


Fig. 2.7. Current flow in Mode 5

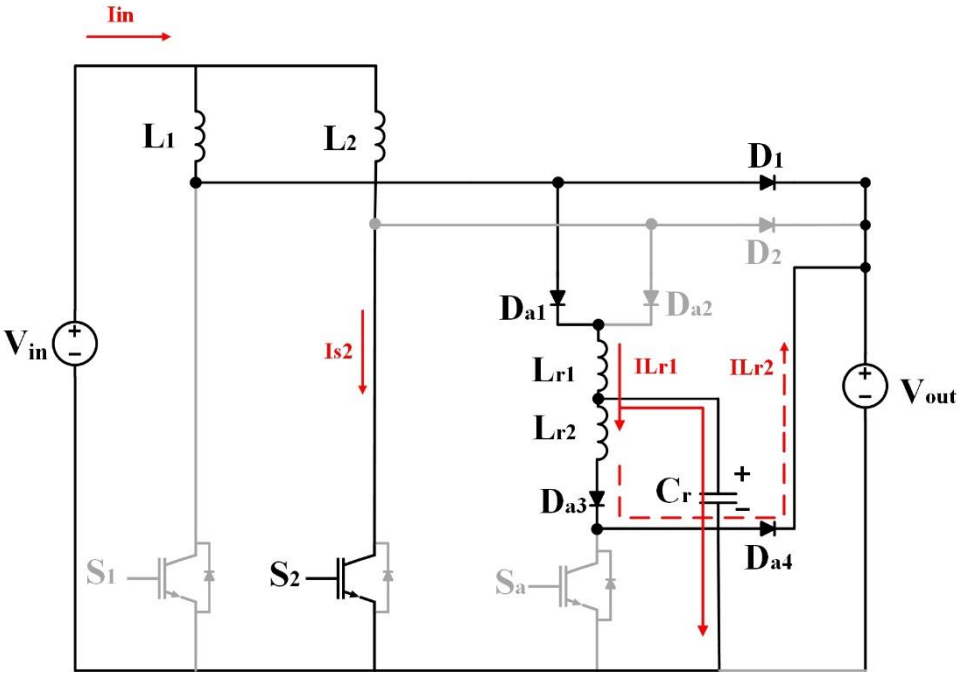


Fig. 2.8. Current flow in Mode 6

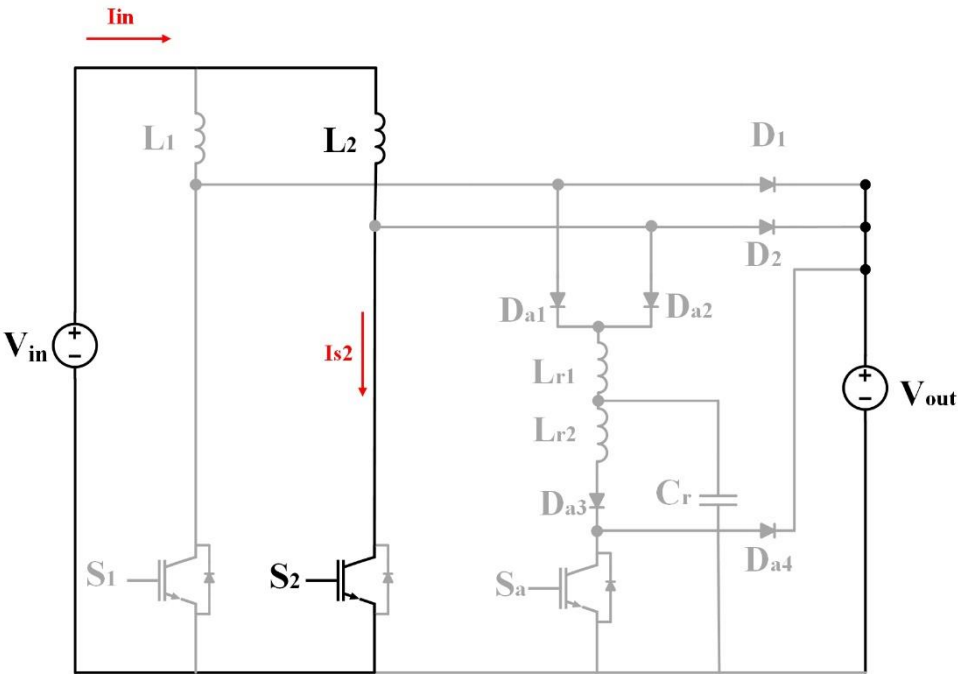


Fig. 2.9. Current flow in Mode 7

2.3 Conclusion

In this chapter, the modes of operation of the proposed PWM interleaved AC-DC boost converter which uses only a single active auxiliary circuit to assist all the main converter switches operate with ZCS and operates with ZCS itself was proposed. It was shown that the proposed circuit has fourteen intervals in each switching cycle which can be divided into two identical half cycles. Then seven different modes of operation which are distinct from each other in terms of the voltage across and current through the different components were illustrated. As it was shown, the auxiliary switch works in a very small instant of time in comparison with the switching cycle. Thus, except during a small fraction of the switching cycle, the proposed converter operates as a conventional PWM interleaved boost converter. The modes of operation, which were stated in this chapter, will be used for deriving mathematical equations in the next chapter.

Chapter 3

3 Circuit Analysis of the Novel AC-DC Interleaved Boost Converter

3.1 Introduction

The modes of operations that the proposed AC-DC interleaved ZCS boost converter goes through during a switching cycle were discussed in the previous chapter. In this chapter, mathematical equations of each mode in steady- state are derived to demonstrate the effects of the proposed auxiliary circuit on each component. These equations can be used to determine the parameters that should be met to satisfy the ZCS conditions. Thus, characteristic behaviors of different components are specified so as to use in design analysis. It should be noted that, since during the most intervals, the proposed interleaved converter operates like that of a conventional one, only the equations for the time in which the auxiliary circuit operates will be derived.

3.2 Circuit Analysis

The equations are derived based on the following assumptions:

- The input inductor current of each module is discontinuous, while the input current of the converter is continuous.
- The input voltage of the proposed converter can be assumed to be DC. This assumption is valid as the AC source can be considered to be DC during a switching cycle as the duration is of this cycle is much shorter than that of the line cycle.
- The output filter capacitor, C_o, is large enough to be considered as a voltage source V_o.
- All semiconductor switches are ideal, which means that they have no conduction losses and no parallel capacitor across them.
- All inductors and capacitors are ideal and have negligible resistance.
- All diodes are ideal with negligible reverse recovery time and forward voltage drop.

The analysis in this chapter is done with D ≥ 0.5, S_2 turned on, and S_1 turned off; the analysis and formulas for the other half-cycle when S_1 is turned on and S_2 is turned off is identical.

The following figure shows the equivalent circuit for Mode 1:

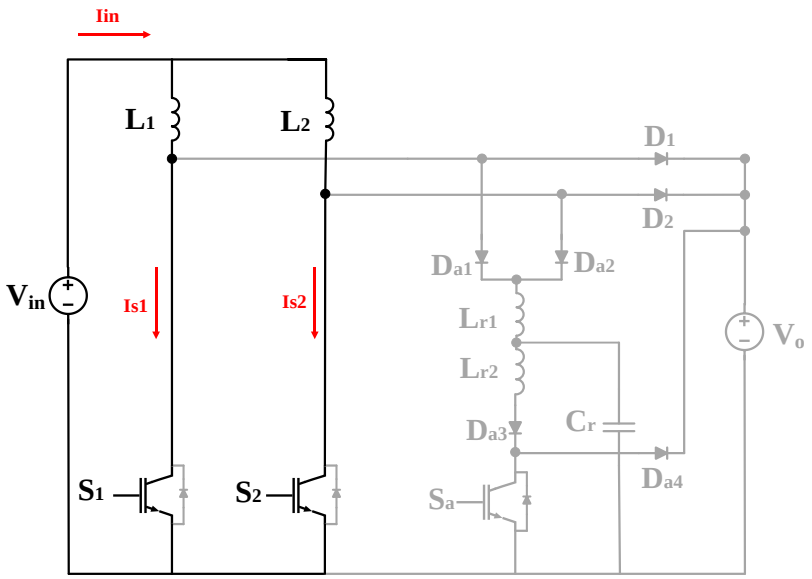


Fig. 3.1. Currents flow in Mode 1

When switch S_2 is turned on, the rectified voltage is applied to L_2 and this leads to a gradual increase of the current through L_2 and the input current in the input inductor, I_{in}. The slope of L_2, which is equal to the slope of S_2, rises according to:

$$V_{in} = L_2 \frac{dIL_2(t)}{dt} \tag{3-1}$$

By integrating from time T_0 to T_1, the main switch current can be expressed as

$$I_{S2}(t) = \frac{V_{in}}{L_2} (T_1 - T_0) \tag{3-2}$$

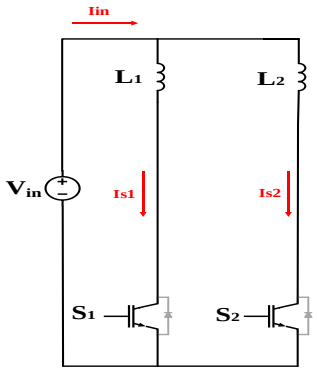


Fig. 3.2. Reduced equivalent circuit of Mode 1

All the input current goes through S_1 and S_2 so that

$$I_{in} = I_{S1} + I_{S2} \tag{3-3}$$

The next mode begins when the auxiliary switch (S_a) is turned on in preparation for the ZCS turn-off of main switch S_1. The equivalent circuit diagram at time T_2 is shown in Fig. 3.3. This diagram can be further simplified in order to demonstrate the auxiliary circuit current during this mode of operation as shown in Fig. 3.4.

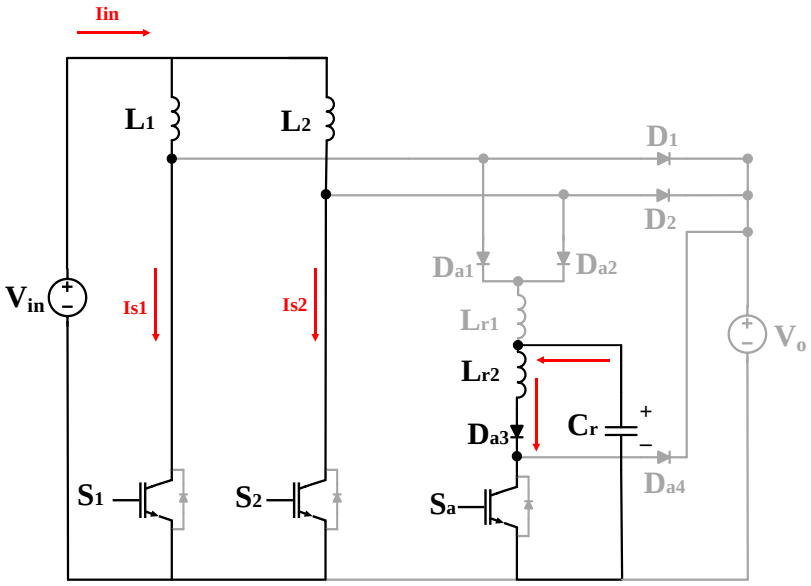


Fig. 3.3. Current flow in Mode 2

By applying KVL in Fig. 3.4, the following equation can be obtained:

$$V_{Cr}(t) = \quad L_{r2}\ \frac{d}{dt}\ i_2(t) \tag{3-4}$$

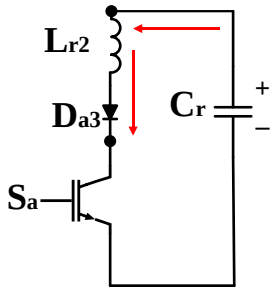


Fig. 3.4. Reduced equivalent circuit of the auxiliary circuit of Mode 2

By applying KCL in Fig. 3.4, the following equation can be obtained:

$$i_{Lr2}(t) = i_{Cr}(t) = \ -\ \frac{d}{dt}\ q_{Cr}(t) = \ -C_r\ \frac{d}{dt}\ V_{Cr}(t) \tag{3-5}$$

By substituting equ. (3-5) into equ. (3-4), the following result can be obtained:

$$V_{Cr}(t) = \ -L_{r2}\ C_r\ \frac{d^2}{dt^2}\ V_{Cr}(t) \tag{3-6}$$

In order to solve the above- mentioned equations, the initial capacitor voltage $V_{cr}(0)$ and the initial auxiliary inductor $i_{Lr2}(0)$ should be defined. $V_{cr}(0)$ is assumed to be equal to V_o and $i_{Lr2}(0)$ is equal to zero in this mode. As a result, the derivative of the capacitor voltage $dV_{cr}(0)/dt$ can be determined to be:

$$[\frac{d}{dt}V_{Cr}(t)]_{t=0} \ = \ -\left(\frac{1}{C_r}\right)[\frac{d}{dt}q_{Cr}(t)]_{t=0} = \ \left(\frac{1}{C_r}\right)[i_{Lr2}(t)]_{t=0} \tag{3-7}$$
$$= \ 0$$

By using equ. (3-7) into equ. (3-6), the following can be obtained:

$$V_{Cr}(t) = V_o \cos \omega_2 t \quad \text{for} \quad T_1 < t < \ T_2 \tag{3-8}$$

Based on the initial conditions of this mode, the following equation can be written:

$$i_{Lr2}(t) = i_{Cr}(t) = -C_r \frac{d}{dt} V_{Cr}(t) = C_r V_o \omega_2 \sin \omega_2 t \qquad (3\text{-}9)$$

$$= \frac{V_o}{Z_2} \sin \omega_2 t \qquad \text{for } T_1 < t < T_2$$

In the above equation, $\omega_2 = \frac{1}{\sqrt{L_{r2} C_r}}$ and the characteristic impedance of the auxiliary circuit is defined as $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$. Mode 2 is finished when the voltage of the auxiliary capacitor V_{cr} reaches zero; therefore, the duration of this mode can be calculated by making equ. (3-8), equal to zero as follows:

$$V_{Cr}(t) = V_o \cos \omega_2 t = 0 \quad \text{for } t = T_2 \qquad (3\text{-}10a)$$

where

$$\omega_2 t = \frac{\pi}{2}$$

$$T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2} C_r} \qquad (3\text{-}10b)$$

Thus the current at $t=T_2$, which is the time in which the maximum current flows through the auxiliary circuit, can be determined to be

$$i_{Lr2}(t) = i_{Lr2}(T_2) = \frac{V_o}{Z_2} \sin \omega_2 t \qquad (3\text{-}11)$$

$$i_{Lr2}(T_2) = \frac{V_o}{Z_2} \qquad \text{for } t = T_2$$

The next mode begins when the voltage across the resonant capacitor is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} begin to conduct. In Mode 3, current through the main switch S_1 and auxiliary S_a switch should go to zero or negative before turning them off so that this is done with ZCS.

The equivalent circuit diagram at time T_2 is shown in Fig. 3.5; it can be be further simplified as shown in Fig. 3.6:

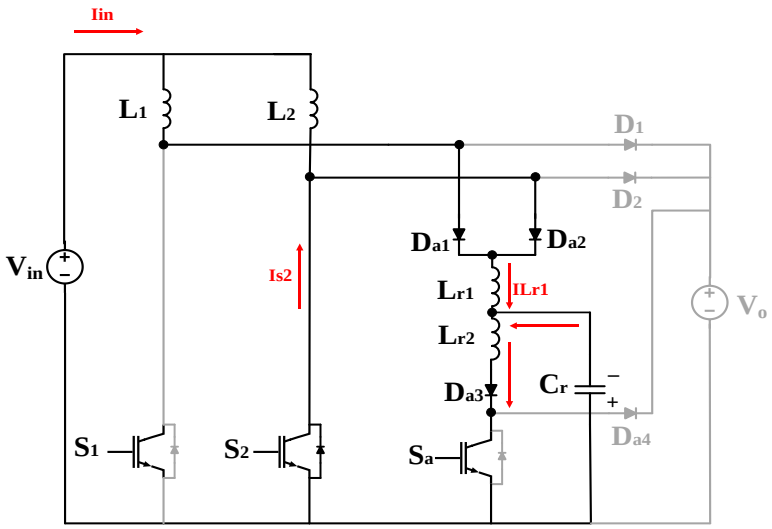


Fig. 3.5. Current flow in Mode 3

It can be seen from the Fig. 3.6 that

$$i_{Lr1}(t) = \ i_{Lr2}(t) + i_{Cr}(t) \tag{3-12}$$

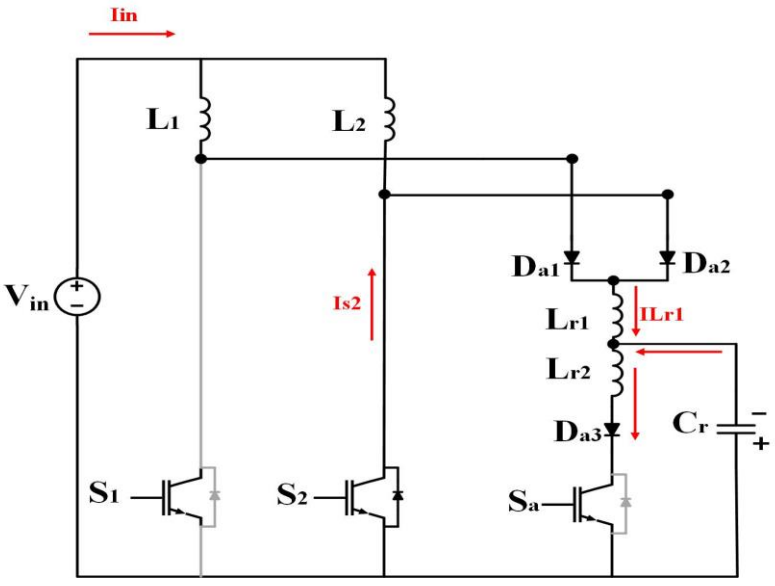


Fig. 3.6. Reduced equivalent circuit of Mode 3

Initial conditions for Mode 3, which should be derived from the previous mode, show that the initial value of voltage across the auxiliary capacitor V_{Cr} (t_2) and current through the auxiliary inductor i_{Lr1} (t_2) are zero, while the initial current through the second auxiliary inductor i_{Lr2} (t_2) in this mode is equal to

$$i_{Lr2}(T_2) = \frac{V_o}{Z_2} \tag{3-13}$$

Since D_{a3} is conducting, the voltage across auxiliary circuit inductor L_{r2} is

$$V_{Lr2} = V_{Cr} \tag{3-14}$$

Since D_{a2} is conducting the voltage across auxiliary circuit inductor L_{r1} is

$$V_{Lr1} = -V_{Lr2} = -V_{Cr} \tag{3-15}$$

By differentiating equ. (3-12) with respect to time, the following equation is obtained:

$$\frac{d}{dt} i_{Lr1}(t) = \frac{d}{dt} i_{Lr2}(t) + \frac{d}{dt} i_{Cr}(t) \tag{3-16a}$$

which can be rewritten as

$$\frac{V_{Lr1}}{L_{r1}}(t) = \frac{V_{Lr2}}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) \tag{3-16b}$$

By substituting equ. (3-15) into equ. (3-16b), the following result is obtained:

$$\frac{V_{Cr}}{L_{r1}}(t) + \frac{V_{Cr}}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0 \tag{3-16c}$$

which can be rewritten as

$$\frac{V_{Cr}}{L_{r1}}(t)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r2}}(t)\frac{L_{r1}}{L_{r1}} + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0 \tag{3-16d}$$

$$\frac{V_{Cr}(L_{r1}+L_{r2})}{L_{r1}L_{r2}}(t)+C_r\frac{d^2}{dt^2}V_{Cr}(t)=0 \tag{3-16e}$$

By defining $L_{eq}=\frac{L_{r1}L_{r2}}{L_{r1}+L_{r2}}$, equ. (3-16e) can be simplified to

$$\frac{V_{Cr}}{L_{eq}}(t)+C_r\frac{d^2}{dt^2}V_{Cr}(t)=0 \tag{3-16f}$$

which is equal to

$$\frac{V_{Cr}}{L_{eq}}(t)=-C_r\frac{d^2}{dt^2}V_{Cr}(t) \tag{3-16g}$$

and be rearranged to be

$$\frac{V_{Cr}}{L_{eq}C_r}(t)=-\frac{d^2}{dt^2}V_{Cr}(t) \tag{3-16h}$$

By defining $\omega_e=\frac{1}{\sqrt{L_{eq}C_r}}$ and substituting it into equ. (3-16h), the following equation can be obtained:

$$V_{Cr}(t){\omega_e}^2=-\frac{d^2}{dt^2}V_{Cr}(t) \tag{3-16i}$$

As mentioned previously, the initial voltage of the auxiliary capacitor is zero. The derivative of the initial magnitude of the auxiliary capacitor can be determined to be:

$$[\frac{d}{dt}V_{Cr}(t)]_{t=0}=-\left(\frac{1}{C_r}\right)[\frac{d}{dt}q_{Cr}(t)]_{t=0}=-\left(\frac{1}{C_r}\right)[i_{Lr2}(t)]_{t=0} \tag{3-17}$$

Substituting equ. (3-13) into equ. (3-17) results in

$$[\frac{d}{dt}V_{Cr}(t)]_{t=0}=-\left(\frac{V_o}{Z_2C_r}\right) \tag{3-18}$$

and by using equ. (3-16i), the voltage across capacitor Cr can be determined to be:

$$V_{cr}(\mathrm{t}) = -\left(\frac{V_o}{\sqrt{\left(1+\frac{L_{r2}}{L_{r1}}\right)}}\right)\sin\omega_e\, t \tag{3-19}$$

Applying KVL to Fig. 3.6 results in:

$$V_{Lr1}(t) = -\ V_{Cr}(t) = -V_{Lr2}(t) \tag{3-20a}$$

Since the voltage across an inductor is generally related to the derivative of the current through it, this can be rewritten as

$$L_{r1}\frac{d}{dt}i_{Lr1}(t) = -L_{r2}\ \frac{d}{dt}\ i_{Lr2}(t) \tag{3-20b}$$

Substituting equ. (3-20a) into equ. (3-20b) results in

$$\frac{d}{dt}i_{Lr1}(t) = -\frac{V_{Cr}}{L_{r1}}(t) \tag{3-20c}$$

which can be rewritten as:

$$di_{Lr1}(t) = -\left(\frac{V_{Cr}}{L_{r1}}(t)\right)dt \tag{3-20d}$$

The above equation can be solved by integrating it during the interval of this mode of operation. The initial magnitude of the auxiliary inductor I_{Lr1}, which is equal to zero, can be derived from the previous mode as shown in Fig. 3.3 and is

$$i_{Lr1}(t) = \left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right)(1-\cos\omega_e t) \tag{3-20e}$$

During this mode of operation, I_{S1} should go to zero or negative in order to meet the ZCS condition; thus the direction of current through S_1 is changed and flows through its body

diode. Based on Fig. 3.6, the following condition should be satisfied to ensure the soft switching of S_1:

$$\text{prerequisite of ZCS of } I_{S1}: \qquad i_{in}(t) - i_{Lr1}(t) \leq 0 \tag{3-21a}$$

This means that current through i_{Lr1} should be more than $i_{in}(t)$. Substituting equ. (3-20e) into equ. (3-21a) results in

$$i_{in}(t) - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right)(1 - \cos\omega_e t)\right] \leq 0 \tag{3-21b}$$

By applying KVL to Fig. 3.6, the following expression can be written:

$$V_{Cr}(t) = L_{r2}\frac{d}{dt} i_{Lr2}(t) \tag{3-22a}$$

which can be rewritten as

$$di_{Lr2}(t) = \left(\frac{V_{Cr}}{L_{r2}}(t)\right) dt \tag{3-22b}$$

Based on equ. (3-13), the initial current through the second auxiliary inductor i_{Lr2} (t_2) in this mode is equal to $i_{Lr2}(T_2) = \frac{V_o}{Z_2}$. By substituting equ. (3-19) into equ. (3-22b), the current through the L_{r2} can be determined to be:

$$i_{Lr2}(t) = \frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}}\right)(1 - \cos\omega_e t)\right] \tag{3-22c}$$

As explained in Chapter 2, auxiliary switch S_a is turned on to help the main switches turn off with ZCS and it should be turned off soon afterwards. At the end of this mode of operation, I_{Sa} should go to zero or become negative so that it turns off with ZCS as well. It can be seen from Fig. 3.6 that

$$I_{Sa}(t) = i_{Lr2}(t) \tag{3-23}$$

In order to turn off the auxiliary switch, S_a, with ZCS, $i_{Lr2}(t)$ should be zero or negative; this can be expressed as:

$$\text{prerequisit of ZCS of } I_{Sa}: \quad I_{Sa}(t) = i_{Lr2}(t) \leq 0 \tag{3-24a}$$

Substituting equ. (3-22c) into equ. (3-24a) results in

$$\frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}}\right)(1 - \cos \omega_e t)\right] \leq 0 \tag{3-24b}$$

The voltage across the main diodes, V_{D1} and V_{D2}, can be derived based on the KVL in Fig. 3.5 to be

$$V_{D2} + V_o = 0 \tag{3-25}$$

$$V_{D1} - V_{Cr} - V_{Lr1} + V_o = 0 \tag{3-26a}$$

Based on equ. (3-15) during this mode, $V_{Lr1} = -V_{Cr}$, so that equ (3-26a) can be rewritten as

$$V_{D1} + V_o = 0 \tag{3-26b}$$

The above-mentioned equations show that, in this mode of operation, the voltage across each main boost diodes are equal to the output voltage. This is one of the advantages of this topology that the maximum voltage across the main diodes is equal to the output voltage.

Based on equ. (3-24a), at the end of this mode, i_{Lr2} should be zero or negative in order to turn off the auxiliary switch with ZCS; however, by using blocking diode, D_{a3}, the negative current cannot flow through L_{r2}. The equations for the rest of the modes are not required to characterize the converter and are thus not presented.

It is worth noting that the maximum voltage across the auxiliary capacitor, which is achieved in Mode 6, due to the resonance among C_r, L_{r1} and L_{r2} when the capacitor voltage reaches to the output voltage should be determined.

The equivalent circuit diagram in the sixth interval is shown in Fig. 3.7, which can be further simplified as shown in Fig. 3.8:

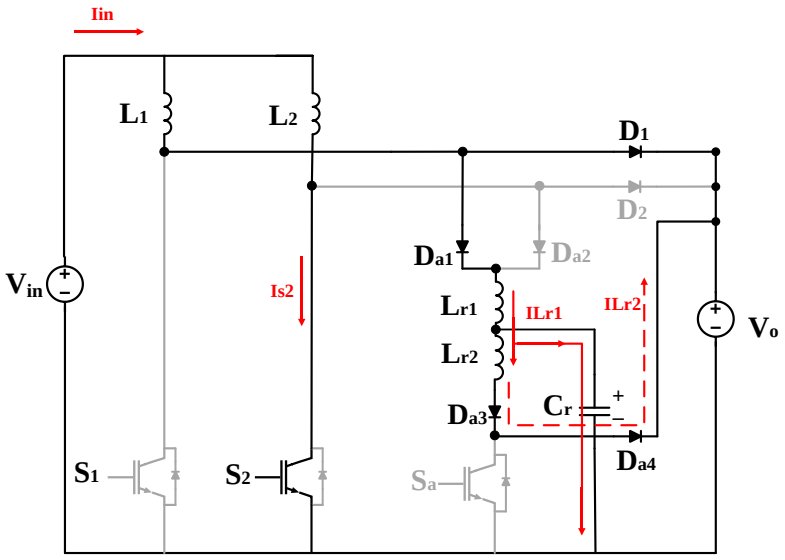


Fig. 3.7. Current flow in Mode 6

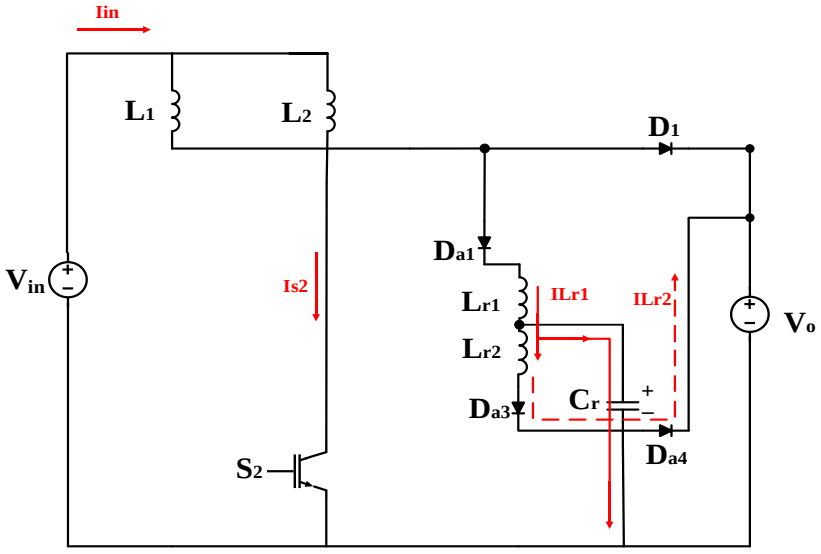


Fig. 3.8. Reduced equivalent circuit of Mode 6

From the above figure, the following equations can be written:

$$i_{Lr1}(t) = i_{Lr2}(t) + i_C(t) \tag{3-27}$$

$$V_{Cr}(t) = V_o + L_{r2}\frac{d}{dt}i_{Lr2}(t) \tag{3-28}$$

$$V_{Cr}(t) = V_o - L_{r1}\frac{d}{dt}i_{Lr1}(t) \tag{3-29}$$

Differentiating equ. (3-27) with respect to time results in:

$$\frac{d}{dt}i_{Lr1}(t) = \frac{d}{dt}i_{Lr2}(t) + \frac{d}{dt}i_{Cr}(t) \tag{3-30a}$$

Which can be rewritten as:

$$\frac{V_{Lr1}}{L_{r1}}(t) = \frac{V_{Lr2}}{L_{r2}}(t) + C_r\frac{d^2}{dt^2}V_{Cr}(t) \tag{3-30b}$$

By substituting equ. (3-28) and equ. (3-29) into equ. (3-30b) results in:

$$\frac{V_{Cr}-V_o}{L_{r1}}(t) + \frac{V_{Cr}-V_o}{L_{r2}}(t) + C_r\frac{d^2}{dt^2}V_{Cr}(t) = 0 \tag{3-30c}$$

Which can be rewritten as:

$$\frac{V_{Cr}-V_o}{L_{r1}}(t)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}-V_o}{L_{r2}}(t)\frac{L_{r1}}{L_{r1}} + C_r\frac{d^2}{dt^2}V_{Cr}(t) = 0 \tag{3-30d}$$

$$\frac{(V_{Cr}-V_o)(L_{r1}+L_{r2})}{L_{r1}L_{r2}}(t) + C_r\frac{d^2}{dt^2}V_{Cr}(t) = 0 \tag{3-30e}$$

By defining $L_{eq} = \frac{L_{r1}L_{r2}}{L_{r1}+L_{r2}}$, it is simplified to:

$$\frac{V_{Cr} - V_o}{L_{eq}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0 \quad (3\text{-}30f)$$

Which is equal to:

$$\frac{V_{Cr} - V_o}{L_{eq}}(t) = -C_r \frac{d^2}{dt^2} V_{Cr}(t) \quad (3\text{-}30g)$$

It can be rearranged as:

$$\frac{V_{Cr} - V_o}{L_{eq}C_r}(t) = -\frac{d^2}{dt^2} V_{Cr}(t) \quad (3\text{-}30h)$$

By defining $\omega_e = \frac{1}{\sqrt{L_{eq}C_r}}$ and substituting it into equ. (3-30h), the following equation can be derived:

$$(V_{Cr} - V_o)(t){\omega_e}^2 = -\frac{d^2}{dt^2} V_{Cr}(t) \quad (3\text{-}30i)$$

Mode 6 begins when the voltage across the auxiliary reaches to the output voltage, therefore the initial voltage of the auxiliary capacitor is equal V_o. The derivative of initial magnitude of the auxiliary capacitor is calculated as:

$$\left[\frac{d}{dt} V_{Cr}(t)\right]_{t=0} = \left(\frac{1}{C_r}\right)[i_{Lr1}(t)]_{t=0} = \left(\frac{1}{C_r}\right)[i_{L1}(t)]_{t=0} \quad (3\text{-}31)$$

Therefore, the equ. (3-33g) is solved as:

$$V_{cr}(\mathrm{t}) = i_{L1} Z_e \sin \omega_e t + V_o \quad (3\text{-}32)$$

Where characteristic impedance is defined as: $Z_e = \sqrt{\frac{L_{eq}}{C_r}}$. The following equation shows the time in which the voltage of the resonant capacitor reaches its maximum value at the start of this mode of operation:

$$\omega_e\, t = \frac{\pi}{2} \tag{3-33}$$

$$t = \frac{\pi}{2}\sqrt{L_{eq}C_r}$$

Thus, at the above time in Mode 6, V_{Cr} reaches its maximum value which is equal to:

$$V_{cr}\left(\frac{\pi}{2}\sqrt{L_{eq}C_r}\right) = i_{L1}Z_e + V_o \tag{3-34}$$

During this mode of operation, current through the input inductor L_{r1} decreases based on the following equation:

$$\frac{d}{dt}i_{L1} = \frac{V_{in} - V_o}{L_1} \tag{3-37}$$

Because the input inductor current of each converter is discontinuous, this mode ends when i_{L1} at T_5 reaches zero:

$$V_{cr}(\mathrm{T_5}) = V_o \tag{3-38}$$

The last mode of the half cycle likes that of the conventional boost converter so equations for this mode are not required to characterize the converter and are thus not presented. It should be noted that the equations for the other half-cycle, when S1 is turned on and S2 is turned off, are identical.

3.3 Conclusion

The circuit analysis of the proposed converter was stated in this chapter. Since, the modes of operations can be divided into two identical half cycles, one half cycle with all intervals were analyzed and relevant mathematical equations for each mode of operation were derived. These formulas and analysis can be used in designing procedure of the proposed converter, which will be presented in the next chapter.

Chapter 4

4 Design Procedure and Example of the Proposed AC-DC Interleaved ZCS-PWM Boost Converter

4.1 Introduction

In this chapter, the results of the mathematical equations derived from the proposed interleaved converter in the steady-state condition in the previous chapter, will be presented. All the analysis and equations that have been presented in previous chapters, have been derived from a DC input voltage, because AC input voltage of the proposed AC-DC interleaved ZCS boost converter can be considered to be a DC source during a very short switching cycle. Therefore, the characteristic curves for the key components of the proposed converter will be presented by using MATLAB simulations, based on the equations derived in Chapter 3. Then, the value of each component can be determined so as to satisfy the key design objectives. Finally, an example will be given to illustrate the design procedure that will be used in the next chapter.

4.2 Conditions for ZCS Turn off of all Switches of the Proposed AC-DC Interleaved ZCS-PWM Converter

There are some parameters that should be satisfied so that all the switches of the proposed PWM AC-DC interleaved converter, shown in Fig. 4.1, can be turned off with ZCS.

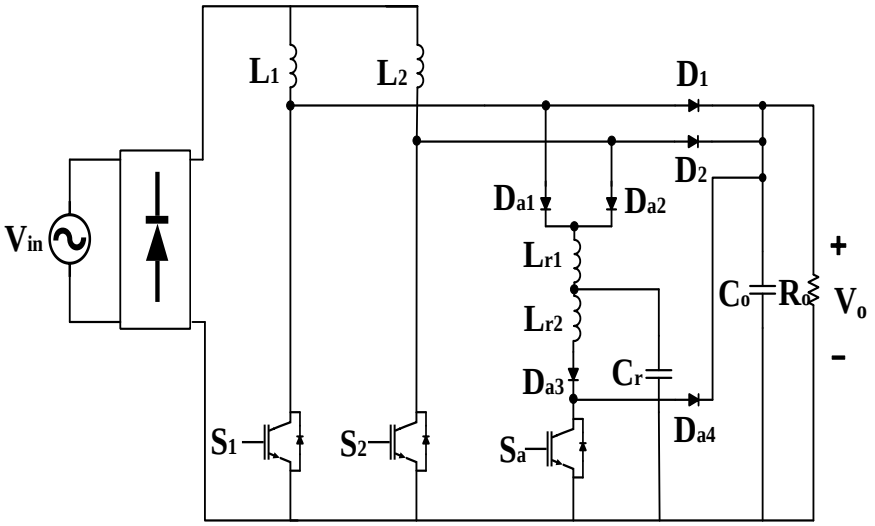


Fig. 4.1. Proposed interleaved AC-DC ZCS-PWM boost converter

Based on the modes of operation presented in Chapter 2, the ZCS condition for the main switches should be met when the proposed converter operates in Mode 3. Moreover, as was shown in the previous chapter, since the auxiliary switch should be turned off right after turning off a main switch, the auxiliary switch should also turn off with ZCS as well. The equation that determines the ZCS condition for the main switches was derived as follows:

$$i_{Lr1}(t) = \left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right)(1 - \cos \omega_e t) \tag{4-1a}$$

It was shown that I_{S1} should go to zero or negative in order to meet ZCS condition; thus the current through S_1 should change direction and flow through the switch's body diode. According to the Fig. 3.6 and equ. (3-21a), current through i_{Lr1} should be more than $i_{in}(t)$ in order for S_1 to turn off with ZCS according to

$$i_{in}(t) - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right)(1 - \cos \omega_e t)\right] \leq 0 \tag{4-1b}$$

As explained in Chapter 3, I_{Sa} should be zero or negative at the end of Mode 3 of operation in order for S_a to turn off with ZCS condition. This can be confirmed if the following condition is met:

$$I_{Sa}(t) = \frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}}\right)(1 - \cos \omega_e t)\right] \leq 0 \quad (4\text{-}2)$$

It should be noted that negative values of I_{S1} and I_{Sa} in equ.(4-1b) and equ. (4-2) represent a flow of current through the body diodes of the main and auxiliary switches respectively.

As can be seen from the above-mentioned equations, the prerequisite for meeting the ZCS condition for auxiliary switch depends mainly on the output voltage, and current through the main switch depends on both output voltage and input current (i_n), which can be determined as follows:

$$i_{in} = \frac{\sqrt{2}P_o}{\eta\, V_{in}} \quad (4\text{-}3)$$

where the parameters of the above equation are defined as:

I_{in}= Rectified input current,

V_o= Output power,

V_{in}= Rectified input voltage,

η = Efficiency of the proposed interleaved converter.

When designing the converter components, it should be noted that, the maximum magnitude of I_{in} should be considered as the worst-case scenario. It can be seen from the equ. (4-1b) that, if the ZCS condition can be met when the input current is at its maximum value I_{in}= $I_{in,max}$, then soft-switching can be ensured for lower rectified input current as well. Based on the equ. (4-3), the maximum input current is obtained by considering the minimum input voltage.

Another design objective that should be considered for the turn-off of the main switch with ZCS is that the current through L_{r2} should be more than the current through L_{r1} in order to divert current from the main switch to the auxiliary switch; thus L_{r1} should be greater than L_{r2} to ensure ZCS under all operating loads. During this time I_{Sa} = I_{Lr2} based on the circuit

analysis in Chapter 3; therefore, the maximum value of the auxiliary switch current can be determined to be

$$I_{Sa,max} = \frac{V_o}{Z_2} \tag{4-4}$$

as it was derived in equ. (3-11).

As explained in Chapter 3, $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$ is defined as the characteristic impedance of the auxiliary circuit and V_o is defined as the output voltage. Minimizing the peak current through the auxiliary switch at the end of the Mode 2 can be considered as another design objective.

Because the peak voltage across all the diodes from the main boost diodes D_1 and D_2 to the auxiliary clamp diode D_4 is equal to the output voltage, there is no need to consider them as design objectives. On the other hand, based on the following equation, which was derived in Chapter 3, the maximum voltage across the auxiliary capacitor can be determined to be

$$V_{cr,max} = i_{L1}Z_e + V_o \tag{4-5}$$

where L_{eq} and Z_e are defined as $\frac{L_{r1}L_{r2}}{L_{r1}+L_{r2}}$ and $\sqrt{\frac{L_{eq}}{C_r}}$ respectively. Minimizing the maximum voltage across the auxiliary capacitor during Mode 6 can thus be considered as another design objective.

By and large, the main objectives that should be considered when designing the converter are as follows:

- The prerequisites in equ. (4-1b) and equ. (4-2b) should be satisfied for the ZCS turn-off of all main and auxiliary switches respectively. Since the proposed interleaved converter operates with its input inductors in discontinuous current mode, all switches inherently turned on with ZCS.
- The peak current through the auxiliary switch, presented in equ. (4-4), should be minimized.

- The peak voltage across the auxiliary capacitor, presented in equ. (4-5), should be minimized.

4.3 Characteristic of the Proposed AC-DC Interleaved ZCS-PWM Converter

As explained in Chapter 3, although the equations have been derived by considering a DC input voltage, they can also be used for analyzing the characteristics of the proposed AC-DC interleaved ZCS-PWM boost converter when it operates with an AC input source as AC input source can be considered to be a DC input source during a very short switching cycle. For example, the DC source voltage can be set as the peak AC voltage so that analysis for certain peak parameter values or worst-case operating conditions can be considered. The equations can be used to draw various different graphs of steady-state characteristic curves that illustrate the behavior of the proposed converter.

In this thesis, the graphs are generated by a MATLAB computer program. The related codes of MATLAB are presented in Appendixes A-F. Since curves of steady-state characteristics should be drawn, the most important feature of the graphs generated by MATLAB is that the current through and voltage across any component of the proposed converter at the start of a switching cycle must be the same as that at the end of the switching cycle. After applying the above derived equations in MATLAB to simulate the converter's modes of operations, the current and voltages of key components should be checked to determine whether they are at the same state with respect to their voltage and current at the end of the previous switching cycle. When this prerequisite is satisfied, the voltage across and current through each component can be determined. If this procedure is done for an interval of values for each component, then their characteristic curves and graphs can be obtained by MATLAB. These graphs indicate how changing a particular component value such as an inductor or a capacitor affects the current and voltage of converter components.

The next step after generating characteristic curves and graphs is to select an appropriate value for each component according to certain desired performance criteria. Typically, some sort of trade-off or compromise must be made when selecting the values.

Based on the above-mentioned explanations, graphs of steady-state characteristic curves shown in Figs. 4.2-4.5 are drawn to demonstrate the relation between the value of each component and the design objectives that were defined at the end of the previous section.

The curves are generated for the following operating condition:

Output Voltage V_0= 400 Volts DC

Output Power P_0= 1 Kw

Input Voltage V_{in}= 85- 265 Volts RMS

Expected Efficiency $\eta = 95\ \%$

Switching Frequency $= f_S = \frac{1}{T_S} =$ 50 KHz.

It should be noted that the maximum value of i_{in} in Fig. 4.1, should be considered in designing the converter as the worst-case scenario. As discussed in the previous section, according to the equ. (4-1b), if the ZCS condition can be met by the maximum value of the i_{in}, then soft switching can be ensured by lower values of rectified input current as well. Although the input voltage varies from 85 to 265 volts RMS, based on equ. (4-3), the design should be done when the input voltage is at its minimum value which is 85 Volts RMS.

By substituting V_{in}= 85 V in equ. (4-3), the following can be written:

$$i_{in,max} = \frac{\sqrt{2}\,P_o}{\eta\,V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 *\ 85} = 17.5\ A$$

Based on the equ. (4-1b) and equ.(4-2b) the auxiliary capacitor C_r has an vital role in achieving the ZCS turn-off of all main switches and auxiliary switch. As discussed in Chapter 2, in the second mode of operation, by turning-on the auxiliary switch, C_r starts to

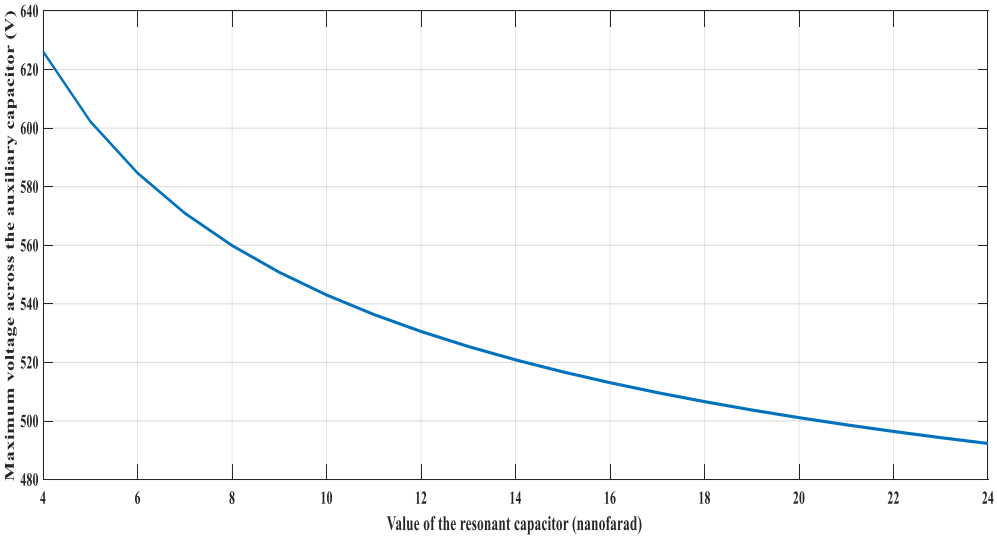


Fig. 4.2. Characteristic graph of variation of maximum voltage across auxiliary capacitor with the variation of C_r when other parameters are constant

resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases. During the third mode of operation V_{cr}

The graph in Fig. 4.2 is generated by MATLAB program (Appendix A) and illustrates the variation of the maximum voltage across the auxiliary capacitor $V_{Cr,max}$ with different values of C_r, when other parameters are constant. The maximum voltage across the auxiliary capacitor can be calculated by equ. (4-5).

During Mode 3, C_r is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. The current through L_{r1} is increased by the flow of I_{L1} and I_{L2} through L_{r1}. In the first half cycle, the current in L_2 is less than that in L_1, thus the current through S_1 becomes zero. In other words, current through both the main and auxiliary switches is diverted as the voltage across the resonant capacitor is negative. As a result, all auxiliary and main switches can be turned off with ZCS.

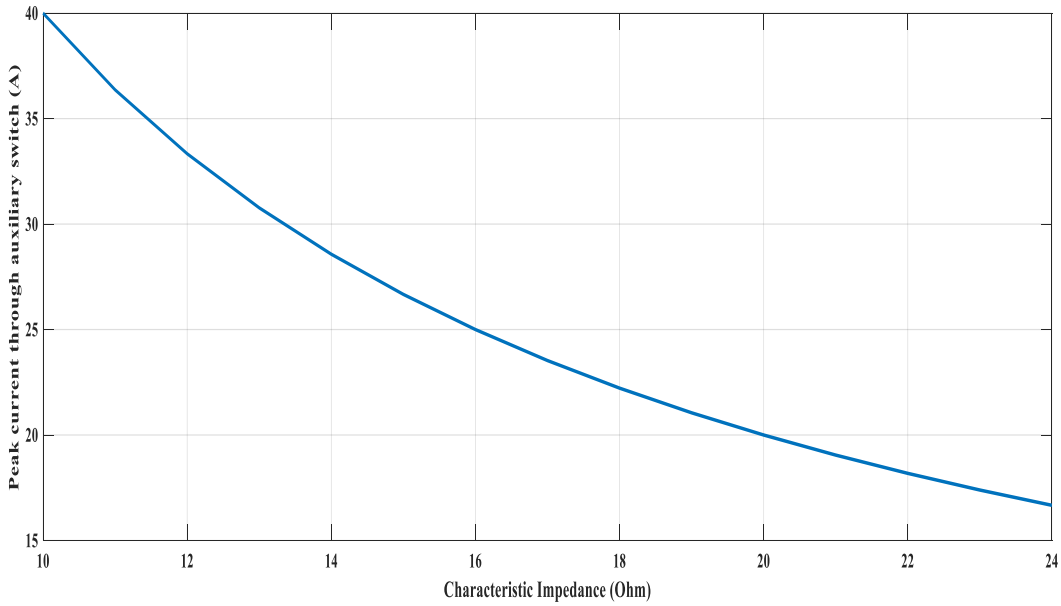


Fig. 4.3. Characteristic graph of variation of peak current through auxiliary switch with the variation of characteristic impedance of the auxiliary circuit

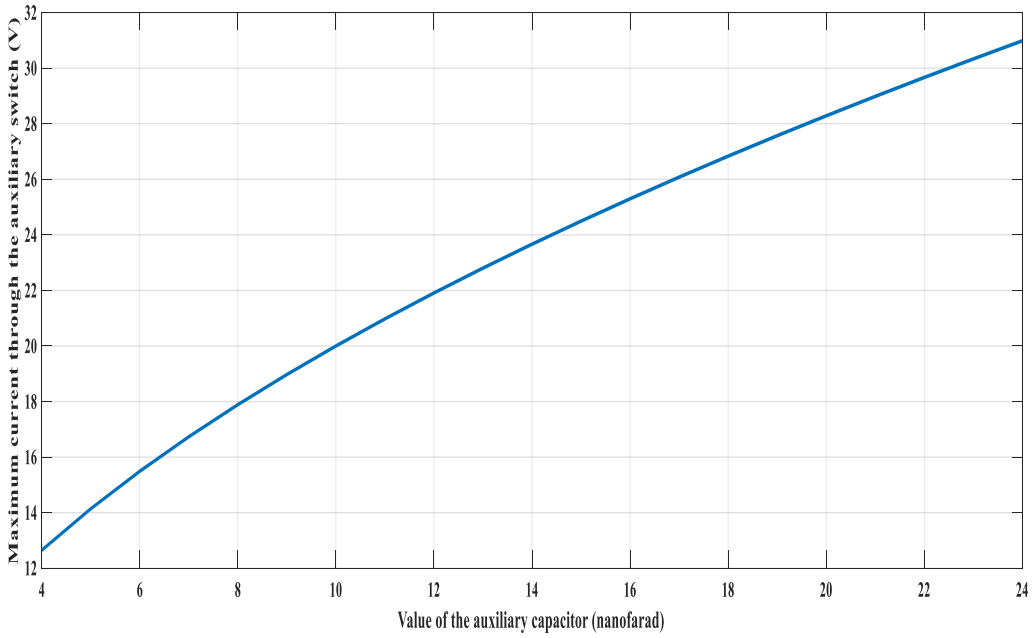


Fig. 4.4. Characteristic graph of variation of peak current through auxiliary switch with the variation of resonant capacitor when other

The resonant capacitor is decreased, but increasing the increasing the value of the auxiliary capacitor means that the peak current through the auxiliary switch is increased as well. Fig. 4.3 is generated by MATLAB program (Appendix B) and illustrates the characteristic graph of variation of peak current through auxiliary switch with respect to the variation of characteristic impedance of the auxiliary circuit Z_2, which is defined as $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$; it is inversely proportional to the resonant capacitor. The peak current through the auxiliary circuit is one of the key design objectives. As can be seen from the graph shown in Fig. 4.3, the peak current through the auxiliary circuit decreases as the value of the characteristic impedance of the auxiliary circuit increases; the value of C_r cannot be chosen to be very high.

It was shown in Fig. 4.2 that the peak voltage across the resonant capacitor can be reduced by increasing C_r. On the other hand, based on Fig.4.3, increasing the value of resonant capacitor increases the peak current through the auxiliary circuit. As a compromise, L_{r2} is assumed to be 4 μH in Fig. 4.4. It can be concluded that, the value of the resonant capacitor should not be very low because $V_{cr,max}$ would increase considerably, while a high value of resonant capacitor creates additional stress in S_a by increasing $I_{Sa,max}$.

The most significant design objective of the proposed interleaved converter is achieving a ZCS turn-off for all the main and auxiliary switches. The equations that determine the ZCS condition for the main and auxiliary switches can be derived from equ. (4-1b) and equ. (4-2b) respectively. The result of these equations should be negative in order to divert the current from the main and auxiliary switches. A negative result in equ. (4-2b) proves that the auxiliary switch is turned off with ZCS. In order to ensure that ZCS is achieved, the current through the main and auxiliary switches should be zero or negative for an appropriate amount of time. The characteristic graphs illustrated in Figs. 4.5-4.8, are used to indicate the amount of time during which the current through the main and auxiliary switches are negative.

It should be noted that the value of the characteristic impedance Z_2 of the auxiliary circuit should be such that $I_{S2,max} = \frac{V_o}{Z_2} > I_{in,max}$.

$$i_{in,max} = \frac{\sqrt{2}\,P_o}{\eta\,V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5\ A$$

so that

$$\frac{V_o}{Z_2} = \frac{400}{Z_2} > i_{in,max} = 17.5\ A \quad \xrightarrow{\text{yields}} \quad Z_2 < 22.8\ \Omega$$

Z_2 should thus be less than 22.8 **Ω**. In order to be have some margin, Z_2=18 **Ω** will be assumed for all of the following figures.

An initial time t=0 in Figs. 4.5-4.8 indicates the beginning of Mode 3, where V_{cr} is charged to a negative voltage and diverts the current from S_1, S_2, and S_a; therefore, current through all the switches is reduced to zero and reaches negative value during this mode of operation. It should be taken into account that the time in which current through main and auxiliary switch falls to zero should be minimized to shrink the time that auxiliary switch operates so that conduction losses can be reduced by shrinking the duty cycle of auxiliary circuit.

The characteristic graphs in Fig. 4.5 and Fig. 4.6, which are generated by the MATLAB program given in Appendix C and Appendix D, show the current through the main and auxiliary switches vs time respectively for various values of L_{r2} when other parameters in equ. (4-1b) and equ. (4-2b) such as C_r and L_{r1} are constant. According to equ. (4-4), by increasing L_{r2} when C_r is constant, the peak current through the auxiliary circuit decreases. It should be noted that $i_{Sa,max}$ should be greater than $i_{in,max}$.

It can be seen from Fig. 4.5 and fig. 4.6 that by increasing L_{r2} when other parameters are constant, the time in which current through the main and auxiliary switches reduce to zero increase as well. As a result, the conduction losses are increased. On the other hand, from Fig. 4.5 can be concluded that by increasing the L_{r2}, the time window for ZCS increases as the current through the main switch can be in negative side for a longer time; therefore, a trade off should be made between the length of time that current through the main switch

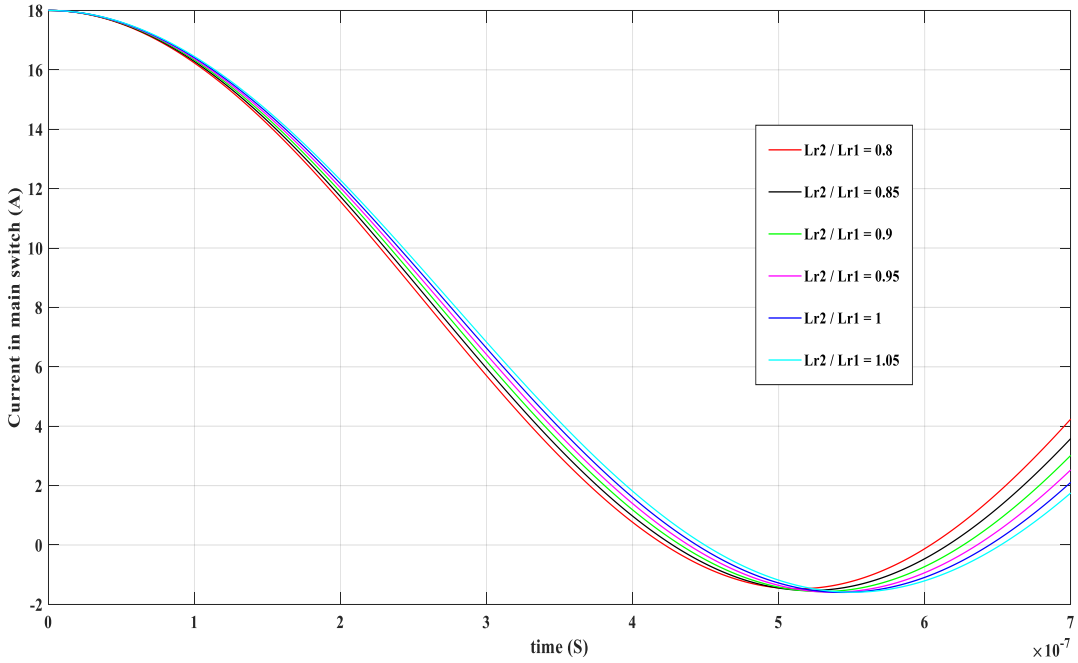


Fig. 4.5. Characteristic graph of time in which main switch current get reduced to zero with the variation of L_{r2} while other parameters are constant

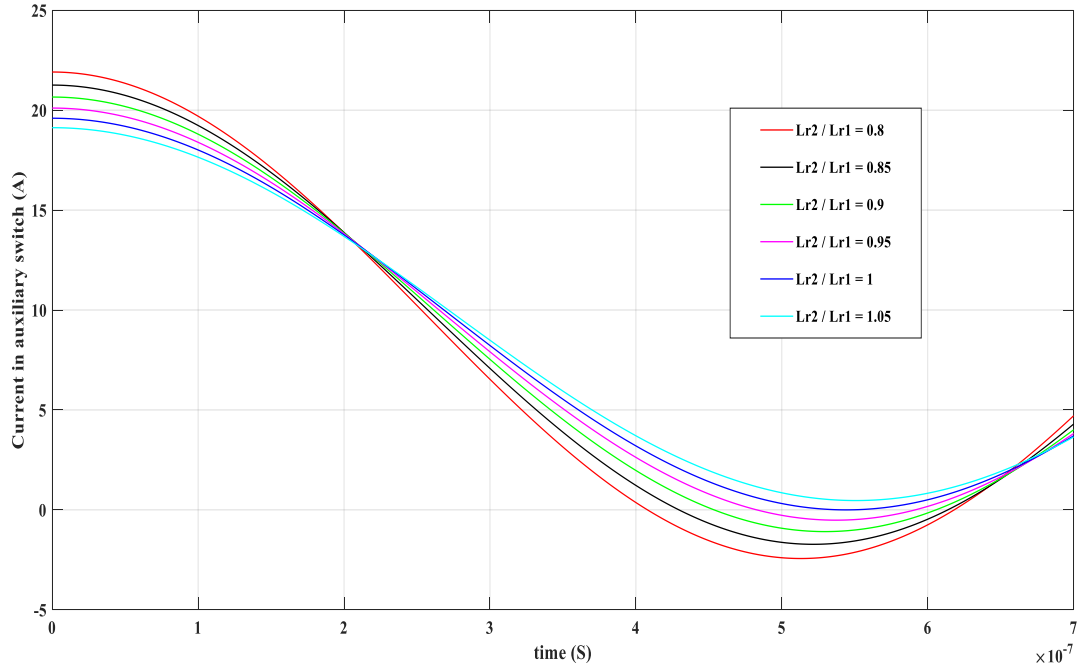


Fig. 4.6. Characteristic graph of time in which auxiliary switch current get reduced to zero with the variation of L_{r2} while other parameters are constant

goes to zero and the length of time during which the current stays negative.

As discussed previously, one of the prerequisites for diverting current from the auxiliary circuit to provide ZCS is that the current through L_{r1} should be less than current through L_{r2} in Mode 3 of operation; thus, the value of L_{r1} should be more than the value of L_{r2}. As can be seen from Fig. 4.6 when the value of L_{r1} is equal or less than L_{r2}, the current through the auxiliary switch does not go to zero so S_a cannot be turned off with ZCS.

The graphs in Fig. 4.7 and Fig. 4.8, which are generated by the MATLAB program in Appendix E and Appendix F, show the current through the main and auxiliary switches vs time respectively for various values of L_{r1} when other parameters in equ. (4-1b) and equ. (4-2b) such as C_r and L_{r2} are constant. The characteristic impedance of the auxiliary circuit Z_2 is constant for these graphs.

It can be seen from Fig. 4.7 that by increasing L_{r1} when other parameters are constant, the time in which current through the main switch falls to zero increases as well and thus conduction losses are also increased. Whereas as it is shown in Fig. 4.8, by increasing L_{r1} when other parameters are constant, the time in which the current through the auxiliary switch is reduced to zero decreases. In addition, it can be concluded from Fig. 4.7 that, by increasing the L_{r1} the window for ZCS decreases as the current through the main switch is negative for a shorter amount of time.

The same results can be observed from Fig. 4.6 as that of Fig. 4.8. It means that, the value of L_{r1} should be higher than the value of L_{r2} in order to turn the auxiliary switch off with ZCS. As can be seen from Fig. 4.8, when the value of L_{r1} is equal or less than L_{r2}, the current through the auxiliary switch does not reduce to zero so S_a cannot be turned off with ZCS. Thus, as the value of Lr_1 becomes more than L_{r2}, the possibility of reducing the current through the auxiliary switch to zero increases considerably. However, this action reduces the chance of ZCS for the main switches. Therefore, $\frac{L_{r2}}{L_{r1}}$ should be designed in a way that all the switches can be turned off with ZCS.

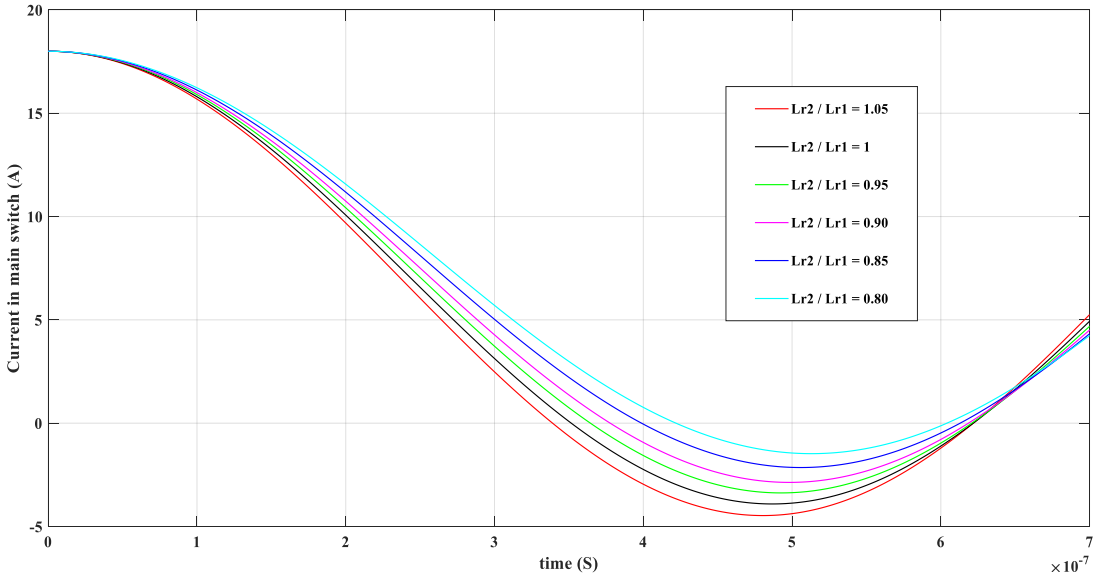


Fig. 4.7. Characteristic graph of time in which main switch current get reduced to zero with the variation of L_{r1} while other parameters are constant

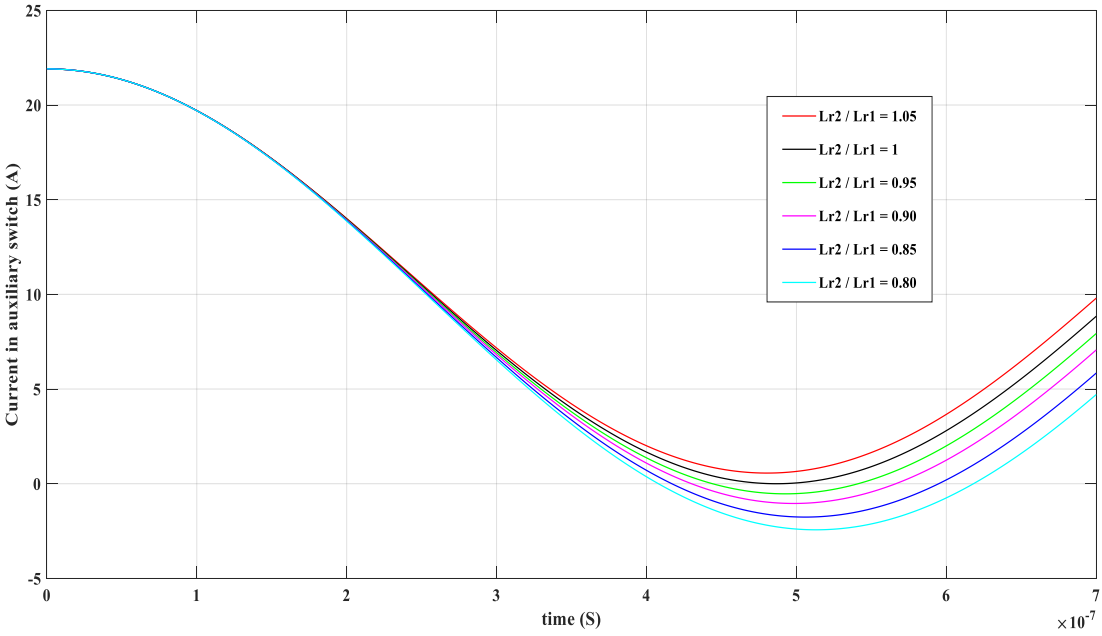


Fig. 4.8. Characteristic graph of time in which auxiliary switch current get reduced to zero with the variation of L_{r1} while other parameters are constant

4.4 Design Example of the Proposed Converter

In this section, a design example of the proposed AC-DC interleaved ZCS-PWM boost converter will be presented in detail. The converter will be designed according to the following specifications:

Output Voltage V_o = 400 Volts DC

Output Power P_o = 1 kW

Input Voltage V_{in}= 85- 265 Volts RMS

Switching Frequency $= f_S = \frac{1}{T_S} =$ 50 KHz.

It is worth noting that, the design procedure is an iterative one. Several iterations should be done to find the most appropriate values. In this thesis, only the last iteration will be illustrated for designing the example.

4.4.1 Design Procedure for the Main Power Circuit

In this thesis, the design procedure is divided into two parts including a main power circuit design which is the same as that for the conventional boost interleaved converter in discontinuous mode and an auxiliary circuit design. The main power circuit components, which should be designed, are comprised of two input inductors L_1 and L_2, two main boost diodes D_1 and D_2, two main switches S_1 and S_2, and an output capacitor C_o.

4.4.1.1 Design Procedure for Input Inductors L_1 and L_2

While designing the input inductors in this thesis, it should be taken into account that with interleaving, the input current of each module can made to be discontinuous and the size of their input inductors since interleaving can reduce the high ripple in each module and produce a net input current with a ripple that is comparable to that achieved with a single boost converter module with a large input inductor. Moreover, there is less current stress on the converter components as they handle a fraction of the overall current and the control

is easier as more sophisticated control methods needed for continuous current mode (CCM) operation are avoided.

The maximum value for the input inductors to work in discontinuous mode is calculated as follows:

$$L_{in,max} < \frac{D(1-D)^2 R}{2f} \tag{4-6}$$

Where the parameters of the above equation are defined as:

$L_{in,max}$= Maximum value for input inductors in order to work in DCM,

D= Duty cycle of the main switches,

R= Load,

f = main switch frequency.

Therefore, to solve equ. (4-6), the above-mentioned parameters should be obtained. f is the main switches frequency which is 50 KHz in this example. R is obtained as:

$$P_o = \frac{{V_o}^2}{R} \tag{4-7}$$

By substituting design specifications for this example into equ. (4-7):

$$R = \frac{{V_o}^2}{P_o} \xrightarrow{\text{yields}} \frac{400^2}{1000} = 160\ \Omega$$

$$\frac{V_o}{V_{in,peak}} > \frac{1}{1-D_{max}}$$

By rewriting, the maximum value of duty cycle in discontinuous mode can be calculated as follows:

$$D_{max} < 1 - \frac{V_{in,peak}}{V_o} \tag{4-8}$$

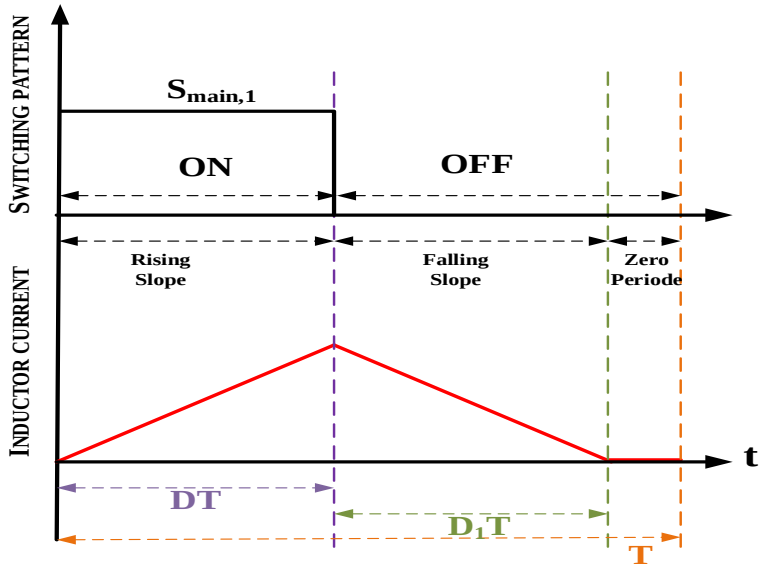


Fig. 4.9. Profile of the input inductor phase current according to the switching pattern in DCM

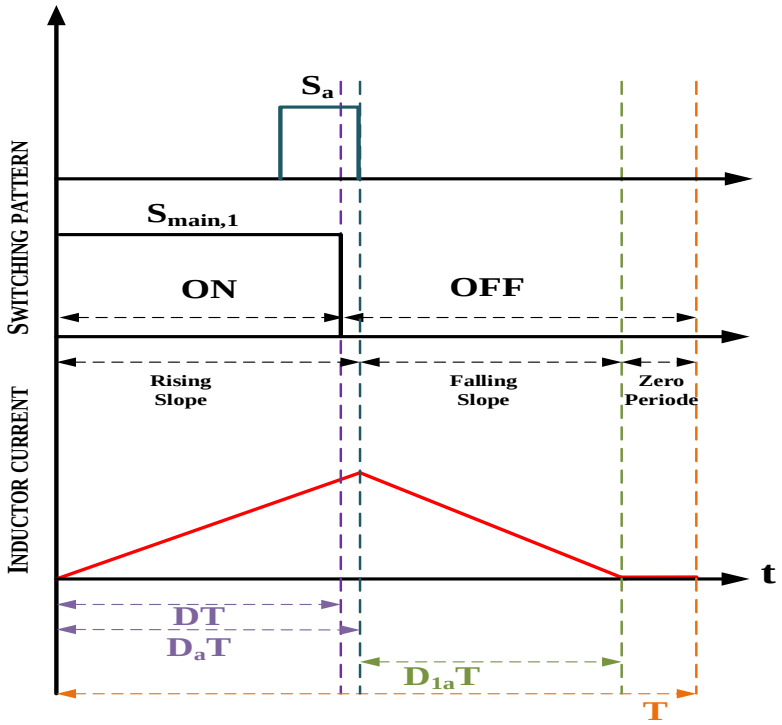


Fig. 4.10. Profile of the input inductor phase current of the proposed interleaved

Substituting design specifications into equ. (4-8) results in:

$$D_{max} < 1 - \frac{\sqrt{2} * 85}{400} \xrightarrow{\text{yields}} D_{max} < 0.7$$

In order to choose the maximum value for duty cycle of the main switch to work in discontinuous mode, the lowest input voltage should be selected, which is 85 Volts in this example.

The Fig. 4.9 shows discontinuous mode of the input current. Where DT is defined as time in which main switch is conducted. D_1T indicates the time after DT when phase current of the input inductor becomes zero. It should be noted that, because of working in DCM, summation of D and D_1 should be less than one. In using equ. (4-8) it should be considered that, it works for conventional AC-DC interleaved converters while in this thesis an auxiliary circuit is used, thus the profile of the input phase current is changed as shown in Fig 4.10. It means that, DT is changed to D_aT which is equal to DT plus the time that after turning the main switch off, auxiliary switch conducts. $D_{1a}T$ shows the time after D_aT when phase current of the input inductor becomes zero. Therefore, D_{max} in equ. (4-8) is equal to D_a. Thus, in order to be in the safe zone, D should be less than 0.65 to work in DCM.

The equ. (4-6) can be solved:

$$L_{in,max} < \frac{D(1-D)^2 R}{2f} \xrightarrow{\text{yields}} \frac{0.65 * (1-0.65)^2 * 160}{2 * 50000} < 127\ \mu H$$

For a more conservative design L_{in} is designed as 125 μH:

L_1=L_2= 125 μH

4.4.1.2 Design Procedure for Output Capacitor C_o

There are different factors that should be considered in selecting the output capacitor including: the second harmonic ripple current, the switching frequency ripple current, the ripple of output voltage, and holdup time. In design phase, the holdup time is usually used as the dominant factor. The capacitor should be selected appropriately to store enough energy to maintain the output voltage above a specified minimum voltage, V_{min}, in the

worst case scenario when the input voltage is not available for a specified amount of time,T_h. In this thesis, V_{min} which is defined as the minimum output voltage that the load equipment can work appropriately is selected 350 volts and holdup time is chosen to be 20 ms for the worst-case scenario. During this time, the following amount of energy is transferred to the output:

$$\mathrm{E} = P_o T_h$$

This energy which is the same as the discharged energy by the capacitor is calculated by:

$$E = \frac{C_o({V_o}^2 - {V_{o,min}}^2)}{2} \tag{4-9}$$

Therefore, the output capacitor is obtained by:

$$C_o \geq \frac{2P_o T_h}{({V_o}^2 - {V_{o,min}}^2)} \xrightarrow{\text{yields}} \frac{2 * 1000 * 0.02}{(400^2 - 350^2)} = 1.06\, mF$$

4.4.1.3 Design Procedure for Main Boost Diodes D_1 and D_2

While designing the main boost diodes, there are two main factors which should be taken into account. These factors are the maximum currents through them and the maximum voltages across them. According to the Mode 4, the maximum currents through the main boost diodes are just less than the maximum currents through the input inductors. The maximum currents through the input inductors of the proposed interleaved converter are the same as the maximum input current where $D < 0.5$ while for duty cycle more than half, as shown in the first mode of operation, $I_{in,max} > I_{L1,2,max}$. As discussed previously, the maximum input current can be derived from equ. (4-3) where V_{in} should be selected from 85-265. For the worse case design, 85 volts is selected:

$$i_{D1,max} = i_{D2,max} < i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2}\,P_o}{\eta\, V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5\ \mathrm{A}$$

Therefore, 17.5 amperes through the main boost diodes can be assumed for the worst-case scenario. The second parameter that should be designed, is the maximum voltages across

the diodes. As can be concluded from Mode 3, the maximum voltage across main boost diodes are clamped to the output voltage:

$$V_{D1,max} = V_{D2,max} = V_o = \ 400 \text{ V}$$

Two fast recovery diodes with voltage stress and current stress which are respectively more than 400 V and equal to 17.5 A should be chosen. Two BYC10DX with 400 voltage stress and 20 A current stress are chosen.

4.4.1.4 Design Procedure for Main Switches S_1 and S_2

As it has been shown in Chapter 1, in AC-DC interleaved boost converters, so as to achieve low harmonic, fast dynamic response and high-power density the frequency should be increased that will lead to higher losses. This is the reason that the soft switching techniques must be implemented. The soft-switching methods for these converters can either be zero-voltage switching (ZVS) if they are implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. The proposed interleaved converter operates with ZCS turn-off of all the switches so two IGBTs should be used as the main switches. ZCS is beneficial for IGBTs as it eliminates the current tail that would otherwise exist when turning off. This current tail overlaps with the switch voltage and causes significant turn-off losses. In designing the main boost switches, the maximum currents through them and the maximum voltages across them as two main factors should be considered. The maximum currents through them are less than maximum currents through the input inductors as follows:

$$i_{S1,max} = i_{S2,max} < i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2}\,P_o}{\eta\, V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * \ 85} = 17.5 \ \text{A}$$

Thus, 17.5 A through the main switches can be assumed for the worse case design. The second parameter that should be considered is the maximum voltages across the switches. As can be seen from Mode 6, maximum voltage across the main switches are clamped to the output voltage:

$$V_{S1,max} = V_{S2,max} = V_o = \ 400 \text{ V}$$

Two STGP 10NC60KD with 400 voltage stress and 20 A current stress are chosen.

4.4.2 Design Procedure for the Auxiliary Circuit

Auxiliary circuit components that should be designed include: one auxiliary switch S_a, two auxiliary inductors Lr_1 and Lr_2, four auxiliary diodes Da_1, Da_2, Da_3, and Da_4, and a resonant capacitor Cr. The auxiliary diodes Da_1 and Da_2 connect L_1 and L_2 to the auxiliary circuit. The maximum currents through Da_1 and Da_2 are equal to the maximum currents through input inductors:

$$i_{Da1,max} = i_{Da2,max} = i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2}\,P_o}{\eta\,V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2}*1000}{0.95*\ 85} = 17.5\ \text{A}$$

maximum voltage across Da_1 and Da_2 are clamped to the output voltage:

$$V_{Da1,max} = V_{Da2,max} = V_o = \ 400\ \text{V}$$

These auxiliary diodes are attached in series with Lr_1 in order to make a path between the input inductors and Lr_1 that diverts the current from the main switches to provide ZCS for turning them off by resonating with L_{r2} and C_r. Since, the proposed converter is operating in DCM, it does not have the reverse recovery problem of the main power boost diodes. Therefore, to design L_{r1}, L_{r2} and C_r characteristic graphs presented in Fig 4.2-4.8 should be used.

As discussed previously, the value of characteristic impedance of the auxiliary circuit Z_2 should be designed in a way that $I_{S2,max} = \frac{V_o}{Z_2} >$ $I_{in,max}$. According to the design specifications:

$$\frac{V_o}{Z_2} = \frac{400}{Z_2} > i_{in,max} = 17.5\ A \quad \xrightarrow{\text{yields}} \quad Z_2 < 22.8\ \Omega$$

Thus, Z_2 should be less than 22.8 ohm. In order to be more conservative, based on Fig. 4.3, Z_2=18 is selected:

$$I_{S2,max} = \frac{V_o}{Z_2} = \frac{400}{18} = 22.22\ A$$

It should be taken into account that the time in which the current through the main and auxiliary switches is reduced to zero should be minimized to shrink the operation time of the auxiliary switch. Then, the conduction losses can be reduced by shrinking the duty cycle of the auxiliary circuit. At the end of Mode 2 was shown that when the voltage of the auxiliary capacitor V_{cr} reaches zero, the currents through the main and auxiliary switches start to be reduced to zero. Therefore, by shrinking the duration time of Mode 2, the auxiliary switch needs to be operated for a less amount of time that results in decrease in the conduction losses. This time can be calculated by equ. (3-10), and based on the trade off it can be assumed to be less than 0.5 μs time to minimize the conduction losses. Thus, the two following equations should be satisfied:

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} = 18\ \Omega$$

$$T_2 - T_1 = \frac{\pi}{2}\sqrt{L_{r2}C_r} < 0.5\ \mu s$$

As it was shown in Fig. 4.2, the value of the resonant capacitor should not be selected very low, because in this situation $V_{cr,max}$ increases significantly while high value of the resonant capacitor creates additional stress in S_a by increasing $I_{Sa,max}$ and the operating time of the auxiliary switch. On the other hand, by increasing L_{r2} when C_r is constant, peak current through the auxiliary circuit decreases while the time in which current through the main and auxiliary switches is reduces to zero, increases. Based on the above-mentioned reasons and formulas, an appropriate trade off should be made in designing them. L_{r2}= 4 μH and C_r=12 nf are selected as the best trade off.

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} = \sqrt{\frac{4 * 10^{-6}}{12 * 10^{-9}}} = 18.25\ \Omega$$

$$T_2 - T_1 = \frac{\pi}{2}\sqrt{L_{r2}C_r} = \frac{\pi}{2}\sqrt{4 * 10^{-6} * 12 * 10^{-9}} = 0.34\ \mu s$$

It was shown in Fig. 4.6 and Fig. 4.8 that the value of L_{r1} should be more than the value of L_{r2} in order to divert the current from auxiliary circuit to turn off the auxiliary switch with ZCS. However, based on Fig 4.7, by designing the $\frac{L_{r2}}{L_{r1}}$ close to one, the chance of ZCS for main switches increases. Based on the above-mentioned reasons and characteristic graphs show in Figs 4.5-4.8, $\frac{L_{r2}}{L_{r1}} = 0.8$ is selected as an appropriate trade off. It means that L_{r1} = 5 μH should be selected. The maximum voltage across the resonant capacitor shown in Fig. 4.2 plotted according to the selected values of L_{r1} and L_{r2}. As can be seen from the Fig. 4.2, by choosing C_r=12 nf, $V_{cr,max}$ is equal to 535 V.

The maximum current through the blocking diode Da_3 which is attached in series with the auxiliary switch is equal to the $i_{sa,max}$:

$$I_{Da3,max} = I_{S2,max} = \frac{V_o}{Z_2} = \frac{400}{18} = 22.22\ A$$

The maximum voltage across the blocking diode is obtained in Mode 4, when the current should be diverted from auxiliary switch to be turned it off with ZCS. $V_{Da3,\,max} = Vc_r = -V_{Lr1}$ at Mode 4 when V_{cr} is reduced to zero, therefore the maximum voltage across the clamping diode is low and well under 100 V.

The maximum current through the clamping diode D_{a4}, which clamps the voltage of auxiliary switch to the output voltage, is almost equal to the input current $I_{in,max}$ in Mode 6.

$$I_{Da4,max} < I_{in,max} = 17.5\ A$$

Since, the voltage across it is clamped to the output voltage, $V_{Da4,max} = V_o$ = 400 V.

The proposed interleaved converter can be simulated by applying selected values of all inductors, capacitors, and switches in the circuit simulator PSIM. The following simulations can verify the selections of all component in worse case design. It can be seen

form Figs. 4.11-4.13. that, ZCS condition for all switches are met and maximum voltage across the capacitor is the same as shown in Fig. 4.2.

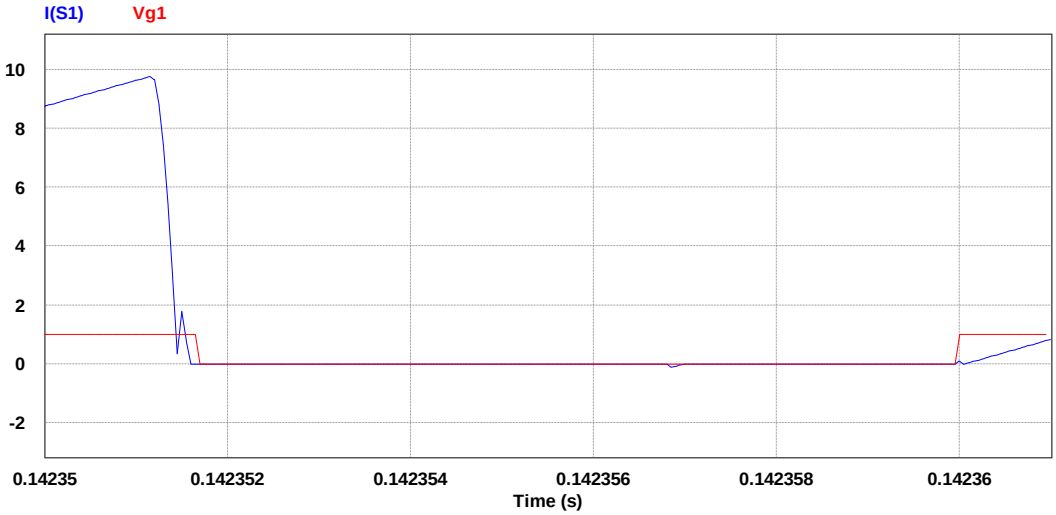


Fig. 4.11. PSIM simulation of current and gate signal of main switch

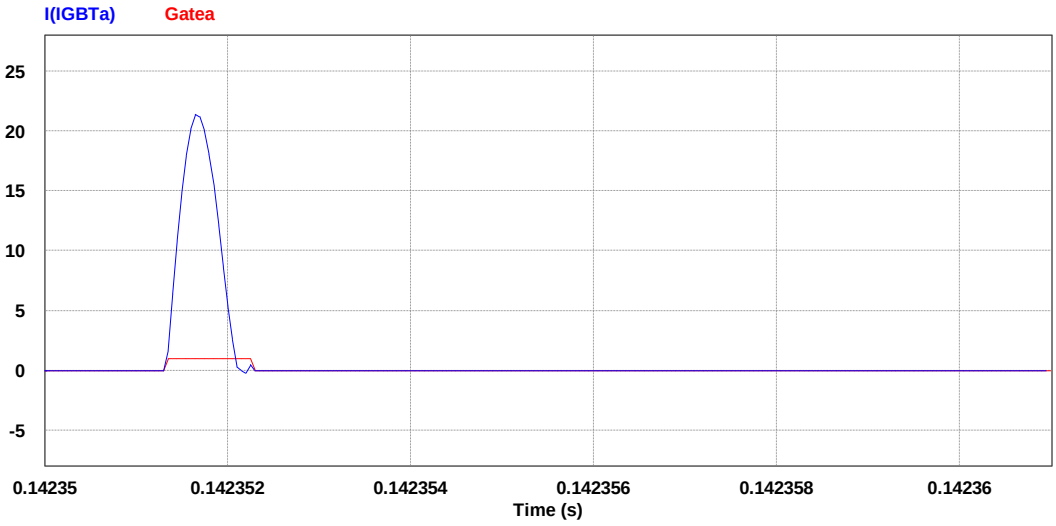


Fig. 4.12. PSIM simulation of current and gate signal of auxiliary switch

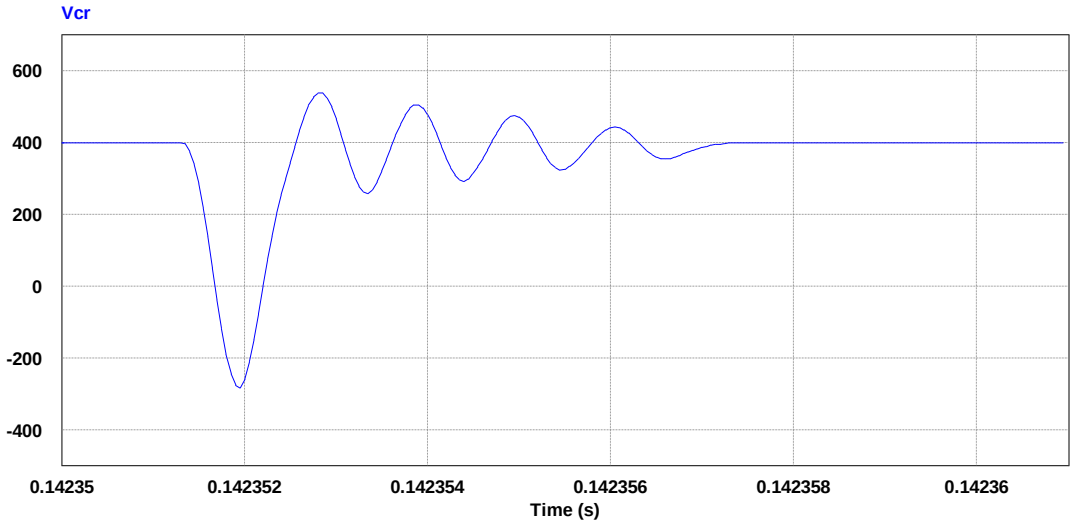


Fig. 4.13. PSIM simulation of resonant capacitor

Data used for choosing devices by PSIM

The following data is extracted from simulations from PSIM in a switching cycle.

Average Current through S_1 3.1 Amps	Maximum Voltage across S_1 400 Volts	Average Current through S_a 0.98 Amps	Maximum Current through S_a 21.68 Amps
Maximum Voltage across S_a 400 Volts	Maximum Voltage across C_r 535 Volts	Minimum Voltage across C_r -280 Volts	Average Current through D_1 0.45 Amps
Maximum Current through D_1 8.12 Amps	Maximum Voltage across D_1 400 Volts	Average Current through Da_1 1.29 Amps	Maximum Current through Da_1 11.2 Amps
Minimum Voltage across Da_1 400 Volts	Average Current through Da_3 2.59 Amps	Maximum Current through Da_3 21.68 Amps	Maximum Voltage across Da_3 75 Volts
Average Current through Da_4 1.61 Amps	Maximum Current through Da_4 11.7 Amps	Maximum Voltage across Da_4 400 Volts	

Above data proves that all the method used for designing the circuit in this chapter are correct. For example, the maximum voltage across the resonant capacitor is 535 volts, and maximum current through auxiliary switch is 21.68 amps. Therefore, the following circuit components are chosen for the proposed interleaved converter:

1) Auxiliary Switch S_a: FGP3440G2
2) Auxiliary Diodes $D_{a\,1,2,4}$: STTH20RD4
3) Auxiliary Diode $D_{a\,3}$: SF3003PT
4) Resonant Capacitor C_r: 0.012 μF / CDV30FF123JO3

4.5 Conclusion

In this chapter, the results of the mathematical equations derived from the proposed interleaved converter in the steady-state condition in the previous chapter were used. The characteristic curves for the key components of the proposed converter were presented by using MATLAB simulations according to the steady-state equations. Effects of each key component on the operation of the converter were shown. At the end of this chapter, an example was given to illustrate the design procedure. By applying characteristic curves generated by MATLAB program and circuit simulator PSIM, value of each component was determined in order to satisfy the key design objectives. The selected values can be used in the next chapter as an experimental result.

Chapter 5

5 Experimental Results

5.1 Introduction

In this chapter, the design procedure of the proposed AC-DC interleaved ZCS-PWM boost converter explained in Chapter 4 will be validated by the laboratory prototype. Voltages and currents waveforms of the key component will be plotted to approve that design objectives are satisfied. The efficiency of the proposed converter will be compared to that of a same converter with hard-switching to show the improvement of the efficiency with soft-switching. It will be shown that because the auxiliary circuit is not in the path of main power circuit, in order to increase the efficiency, the proposed converter can be operated with hard-switching in output power less than 600W and operating with soft-switching in output power more than 600 W.

5.2 Experimental Results

In this section, the feasibility of the proposed AC-DC interleaved ZCS-PWM boost converter verified with PSIM in previous chapter will be validated with the experimental prototype designed in Chapter 4 with the following specifications:

Output Voltage V_0= 400 Volts DC

Output Power P_0= 1 Kw

Input Voltage V_{in}= 85- 265 Volts RMS

Switching Frequency $= f_S = \frac{1}{T_S} =$ 50 KHz.

The experimental prototype was implemented by using the appropriate values for each component of the proposed converter selected in Chapter 4. As discussed in the previous chapter, the following components should be used for the laboratory prototype:

- Input Inductances $L_{1,2}$: 125 μH /25 Turns on 77194A7 core
- Main Boost Diodes $D_{1,2}$: BYC10DX
- Main Switches $S_{1,2}$: STGP 10NC60KD
- Output Capacitor: 2X560µF 3316(M)
- Auxiliary Switch S_a: FGP3440G2
- Auxiliary Diodes $D_{a\ 1,2,4}$: STTH20RD4
- Auxiliary Diode $D_{a\ 3}$: SF3003PT
- Resonant Inductor L_{r1}: 5 μH /8 Turns on CO55894A2 core
- Resonant Inductor L_{r2}: 4 μH /7 Turns on CO55894A2 core
- Resonant Capacitor C_r: 0.012 μF/ CDV30FF123JO3

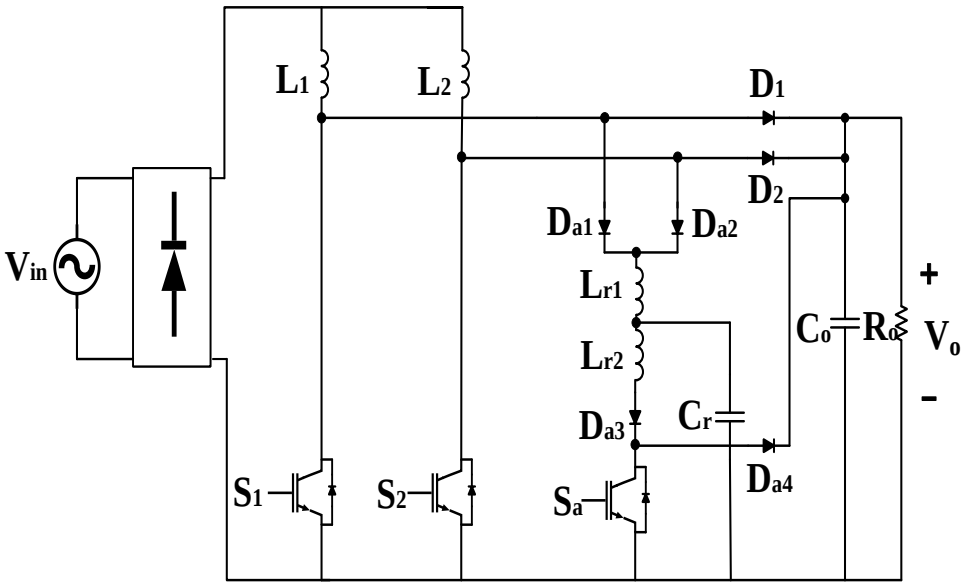


Fig. 5.1. Proposed AC-DC interleaved ZCS-PWM boost converter

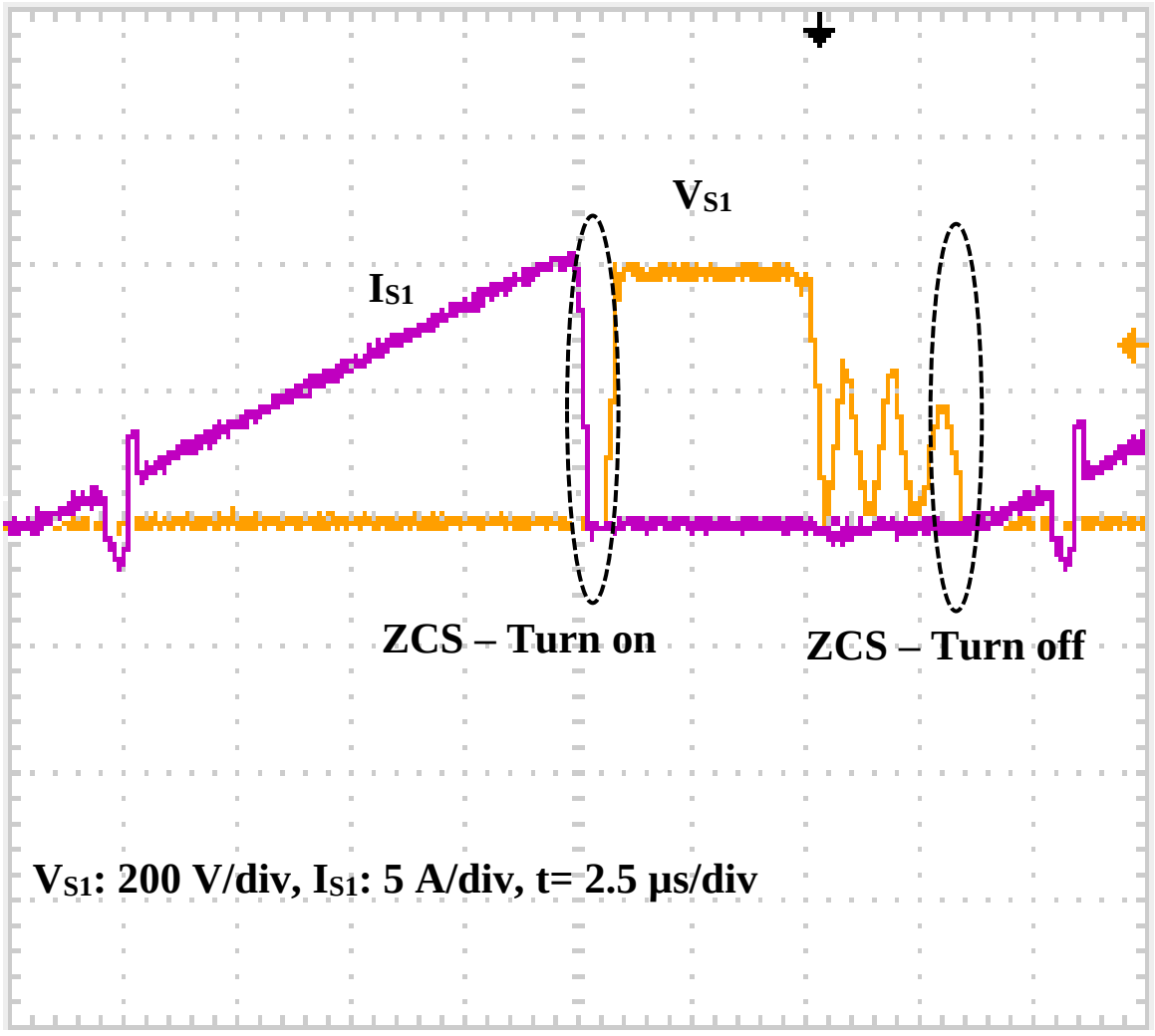


Fig. 5.2. Main switch S_1 voltage and current waveforms V_{S1}, I_{S1}

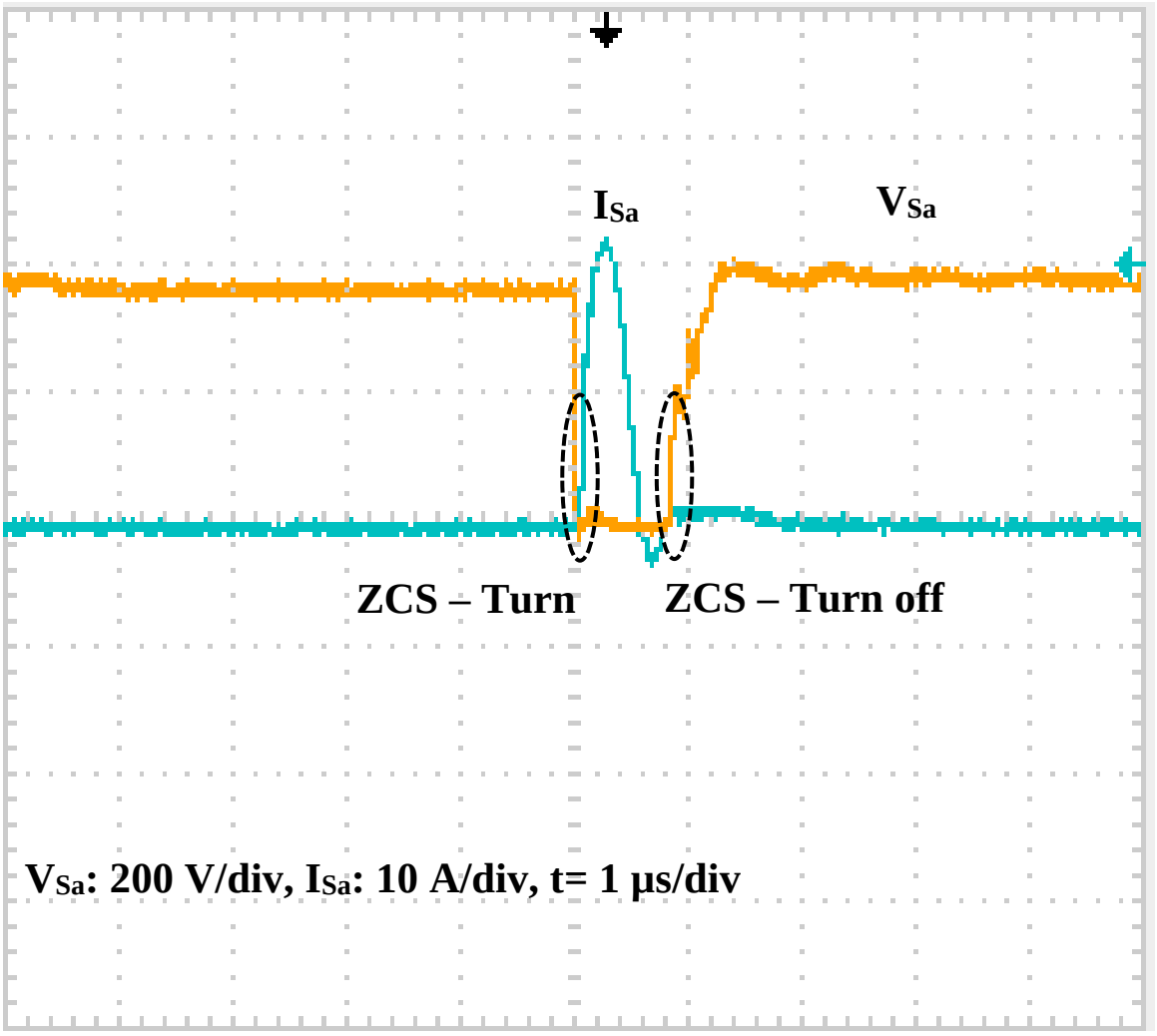


Fig. 5.3. Auxiliary switch S_a voltage and current waveforms V_{Sa}, I_{Sa}

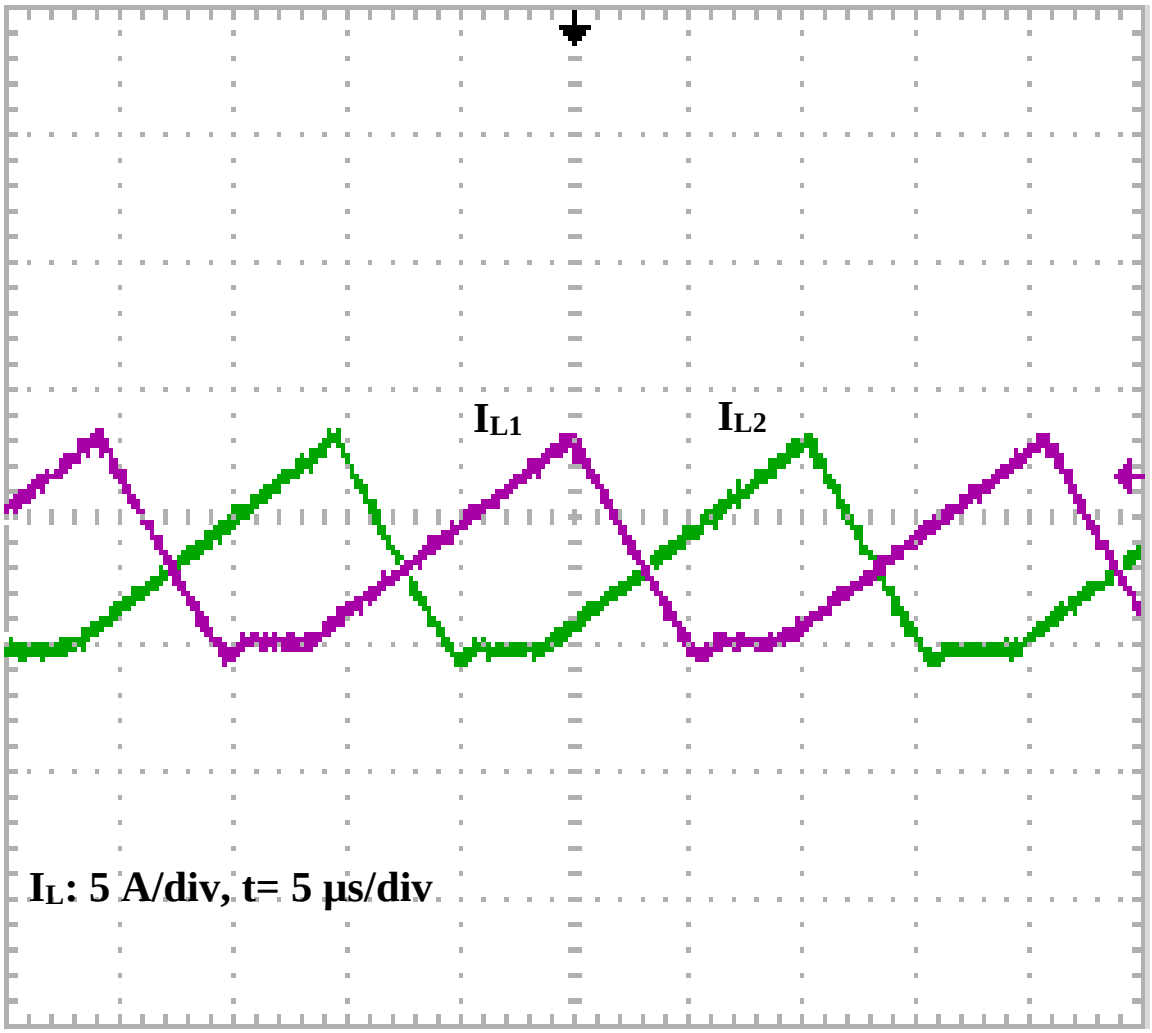


Fig. 5.4. Main input inductors L_1 and L_2 current waveforms I_{L1}, I_{L2}

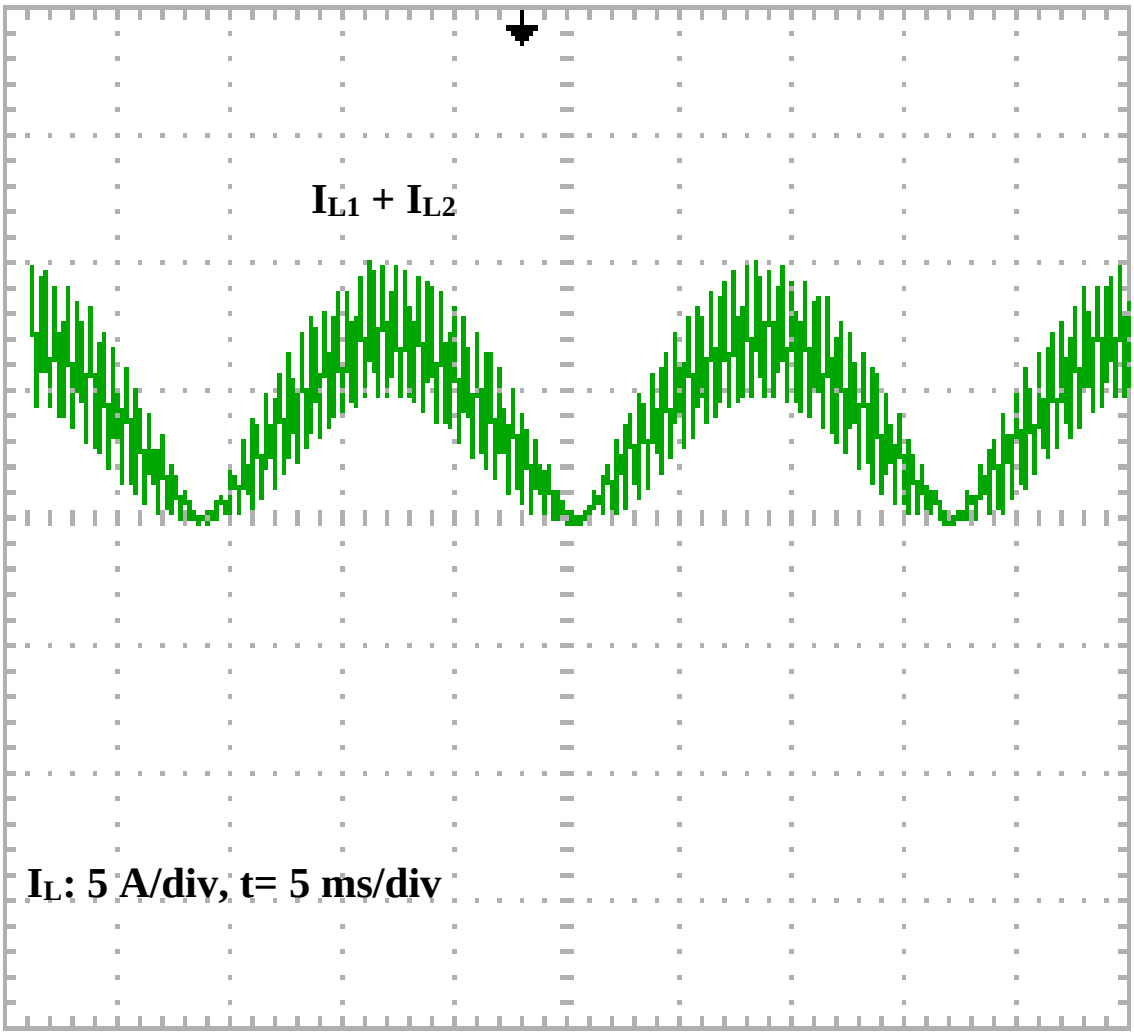


Fig. 5.5. Rectified input current waveform I_{L1}+ I_{L2}

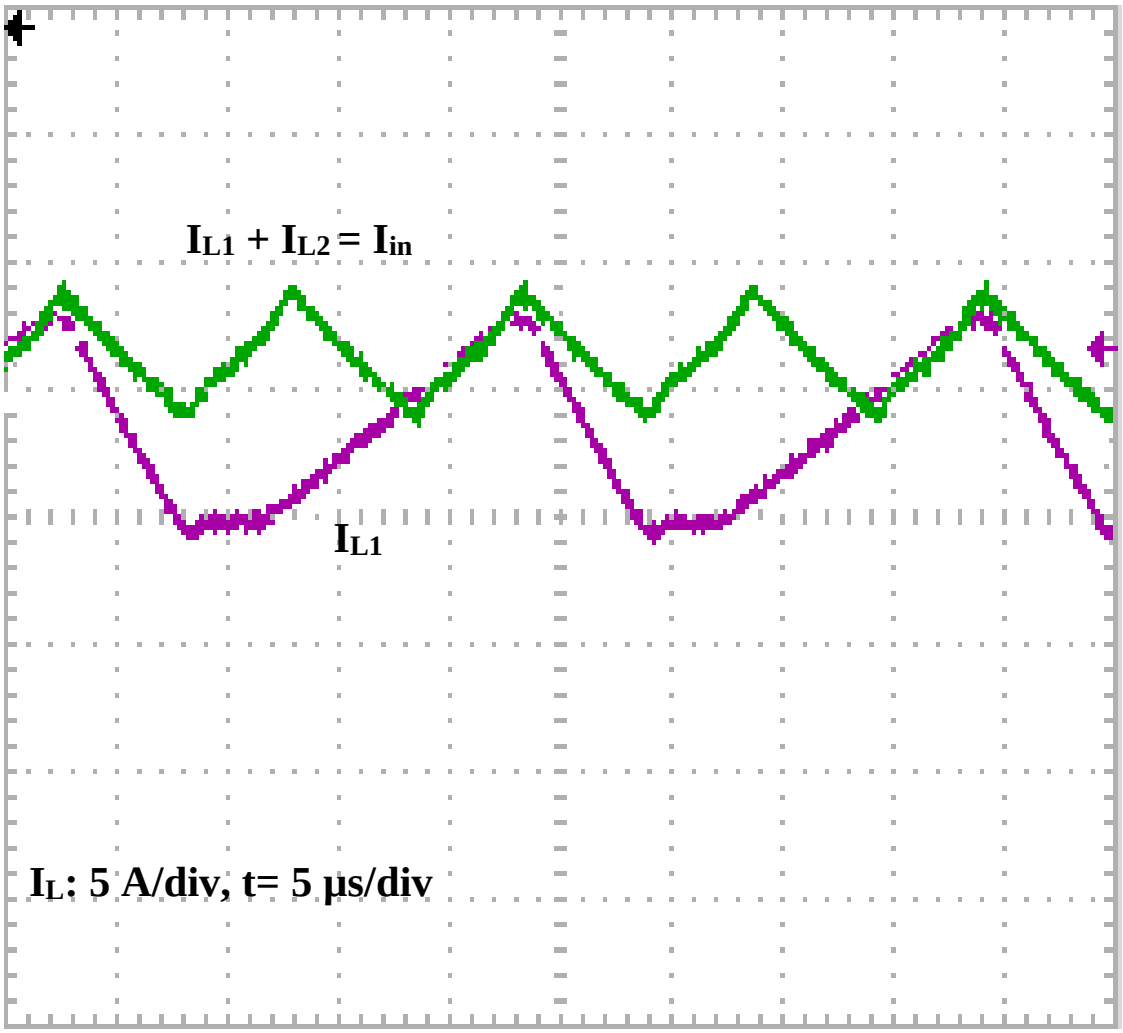


Fig. 5.6. Rectified input current ripple and I_{L1} waveforms

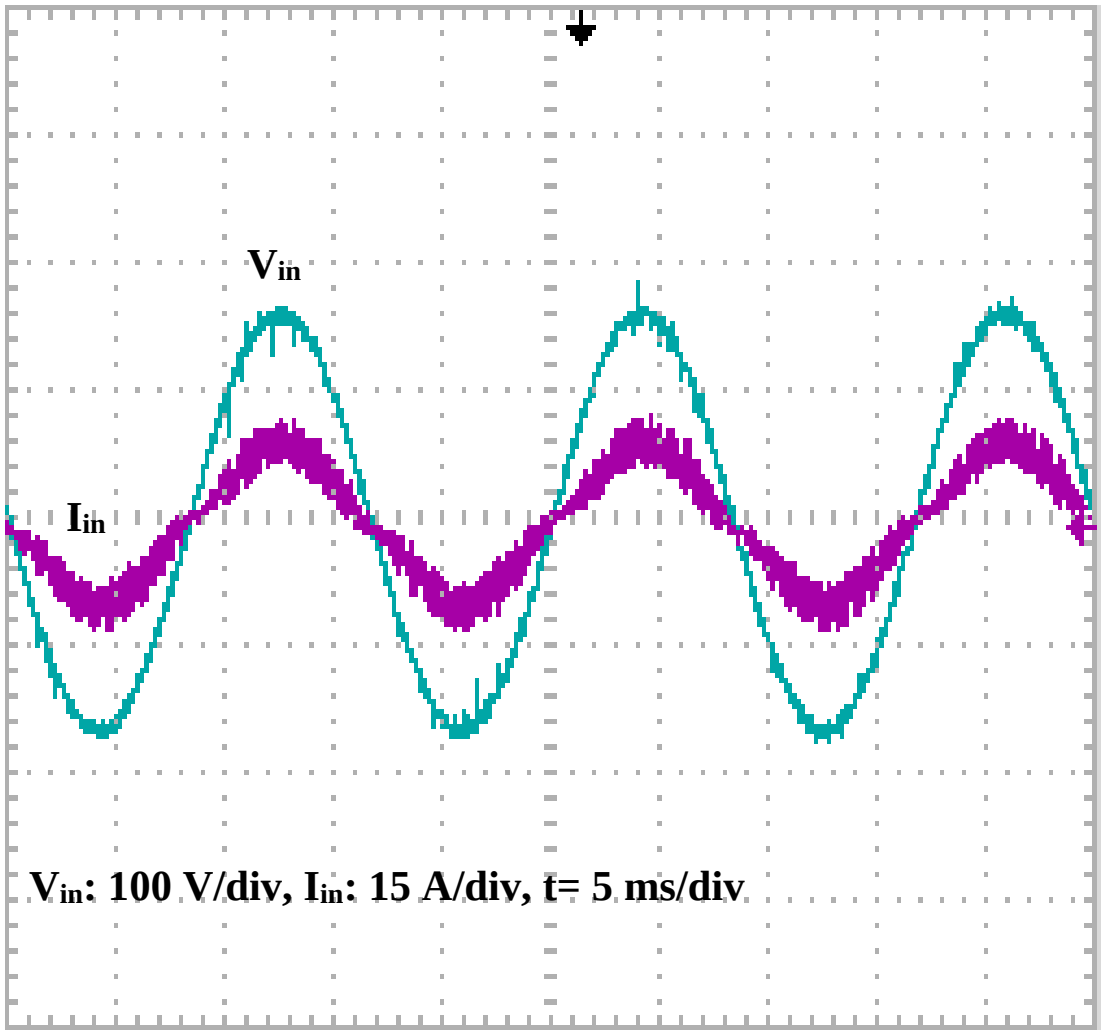


Fig. 5.7. Input voltage and current waveforms V_{in}, I_{in}

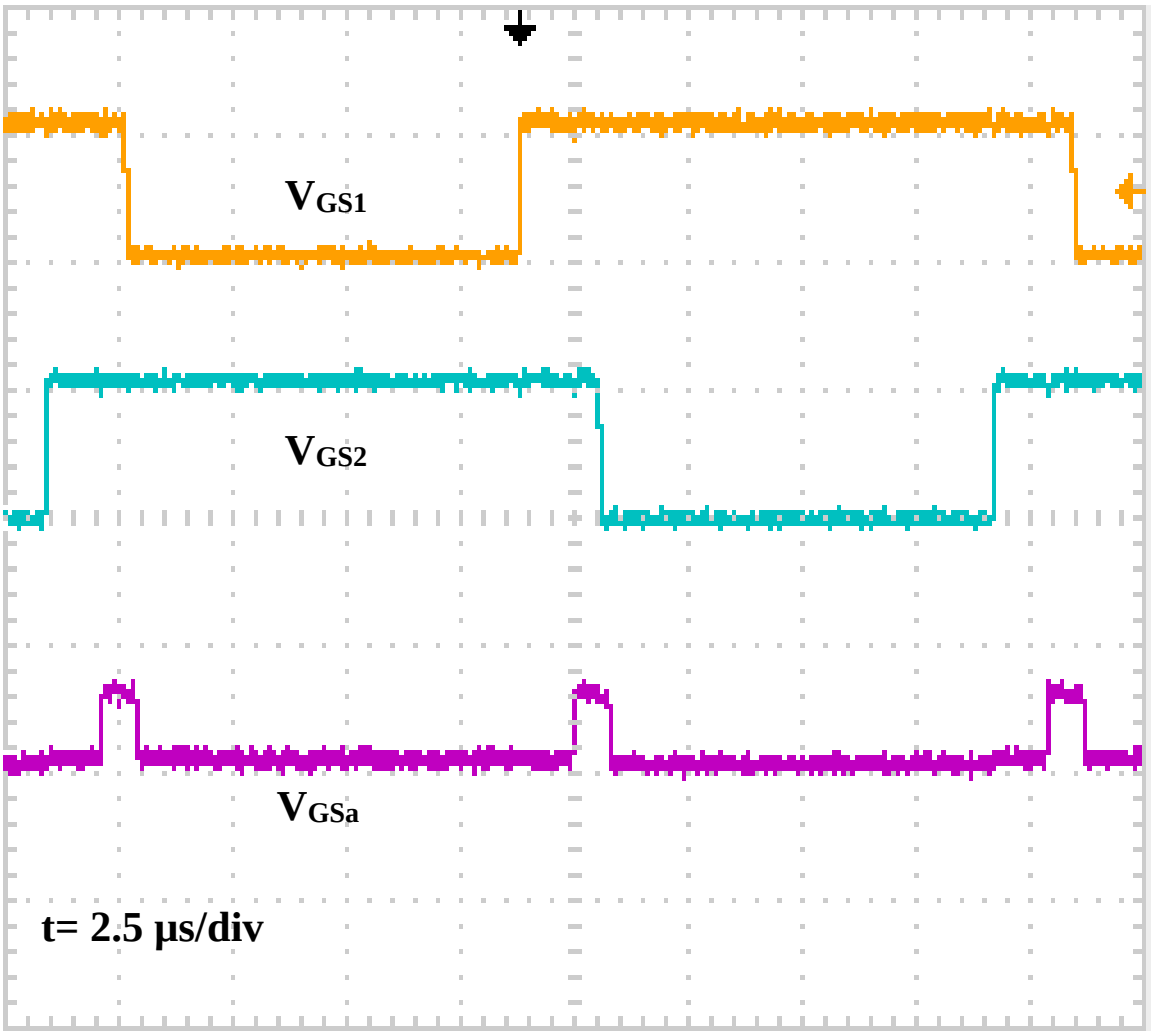


Fig. 5.8. Gating signals of main switches and auxiliary switch V_{Gs1}, V_{Gs2}, V_{Gsa}

5.3 Conclusion from Experimental Results

The gating signals of main switches and the auxiliary switch are shown in Fig. 5.8. The ZCS operation of one of the main switches and the auxiliary switch during turn-on and turn-off are shown in Fig. 5.2 and Fig. 5.3 respectively by illustrating their current and voltage waveforms. The input currents of the proposed converter and the input inductors are shown in Figs. 5.4 -5.6. The input voltage and current of the converter is shown in Fig. 5. 7. The following conclusions can be made by observing the waveforms presented in Fig. 5.2 – 5.8:

- It can be seen from Fig. 5.8 that the auxiliary switch operates only in a fraction of the time which main switches conduct. The reason is that it should be turned on just for performing ZCS condition for main switches during turn-off. Thus, the frequency of the auxiliary switch gating signal is twice that of the main switches gating signals.
- It can be seen from Fig. 5.4 and Fig. 5.5 that the input current of each module is designed to be discontinuous while the input current which is the summation of them is continuous. As a result, the size and price of the input inductors are reduced considerably in comparison CCM method.
- It can be seen from Fig. 5.6 that the input current ripple is reduced significantly by interleaving method. Because switches operate 180° out of phase so the inductors ripple currents are decreased by each other. Smaller inductors are needed which leads to use cheaper and lighter inductors.
- It can be seen from Fig. 5.7 that the input current is sinusoidal and in phase with input voltage. As a result, power factor correction is almost 1.
- It can be seen from Fig. 5.2 that the current through one of the main switches (S_1) goes to zero before turning it off. It happens because after Sa is turned on, C_r begins to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases. When the Vcr is charged to a negative voltage, D_{a1} and D_{a2} start to conduct. The current through L_{r1} increases, thus I_{L1} and I_{L2} flow through the L_{r1}. The current in L_2 is less than L_1, thus the current through S_1 becomes zero and S_1 can be turned off with ZCS. The current through S_2 becomes negative and flows

through its body diode. Besides, as the input current of each module is discontinuous, main switches are turned on with ZCS too.

- It can be seen from Fig. 5.3 that the current through the auxiliary switches (S_a) goes to zero before turning it off. During turning main switches off, the current in L_{r2} reaches to zero because of its resonance with C_r hence S_a can then be turned off with ZCS condition. Another point that can be observed from this figure is that because of using L_{r2} in series with S_a, the current through the auxiliary switch is risen gradually hence there is no overlap between voltage and current which leads to turn the auxiliary switch on with ZCS too.

5.4 Efficiency Results

In this section, the efficiency of the novel AC-DC interleaved ZCS-PWM boost converter is compared with the conventional one, which operates with hard- switching. As can be seen from Fig. 5. 10, the efficiency of the conventional converter is decreased by increasing the load while the efficiency of the proposed converter is increased. As can be seen from Fig. 5.10., when the power is less than 600W (light load), hard-switching method is more efficient while for higher power (more than 600 W) the proposed soft-switching method is more efficient.

The main reason for this, is that the auxiliary circuit losses dominate when the converter is operating under light loads. Auxiliary circuit losses include the turning on and off of the auxiliary switch and additional conduction losses as there can be an increased amount of circulating current flowing in the converter. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads when switching losses of the main switches that are eliminated - especially the IGBT current tail losses - are greater than the auxiliary circuit losses.

Therefore, the optimum efficiency can be obtained when the auxiliary circuit is used to achieve ZCS operation in a ZCS-PWM converter only when the converter is operating with heavier loads and not used when the converter is operating with light load. Operating the converter in such a manner would ensure the optimal efficiency profile over the entire load

range. It can be achieved in this thesis as the auxiliary circuit of the proposed converter can be disengaged during light loads.

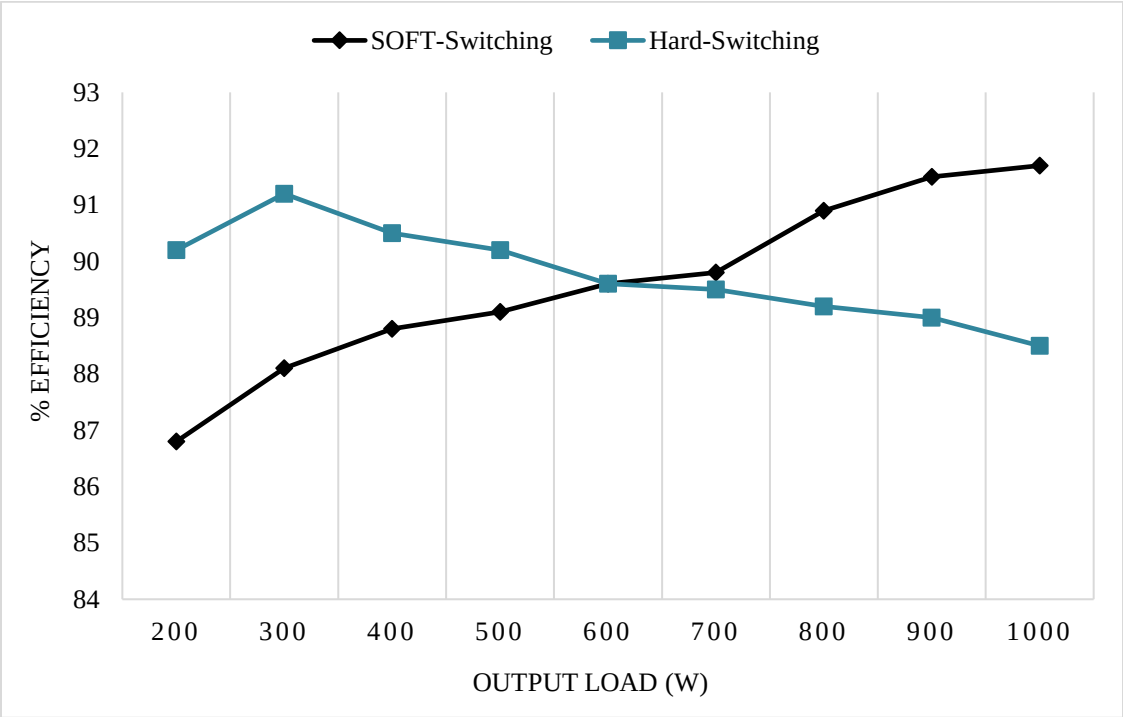


Fig. 5.9. Comparative of efficiency graphs between soft-switching and hard-switching for different output loads at input voltage of 110 V and output voltage 400V.

5.5 Conclusion

In this chapter, the modes of operation of the proposed PWM interleaved AC-DC boost converter which uses just a single active auxiliary circuit to assist all the main converter switches operate with ZCS and operates with ZCS itself was proposed. It was shown that the proposed circuit has fourteen intervals in each cycle which is divided into two identical half cycles. Then seven different modes of operation which are distinct from each other in terms of voltage across and current through the different components were illustrated. As it was shown, auxiliary circuit works in a very small instant of time in comparison with the whole switching cycle. Thus, at most of time, the proposed converter works as a conventional PWM interleaved boost converter. These modes of operation will be used for deriving mathematical equation in the next chapter.

Chapter 6

6 Summary and Conclusion

6.1 Introduction

In this chapter, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work done in the thesis are presented and the main contributions of the thesis to the field of power electronics are stated. Finally, the potential future researches that can be done based on this thesis will be suggested.

6.2 Summary

AC–DC converters have a significant role in new technologies such as adjustable-speed drives, plugged- in hybrid electric vehicles, power supplies for telecommunication systems, and battery chargers. In AC-DC interleaved boost converters, so as to achieve low harmonic, fast dynamic response, high power density, and low size the frequency should be increased. However, this will result in higher switching losses. To address this issue, soft-switching methods should be implemented. When the frequency range is 50 kHz, insulate gate bipolar transistor (IGBT) is the common switch. Since IGBT has current tail because of the minority carrier characteristic, it is turned off slowly. Thus, there is an overlap between the voltage and current in this condition that leads to losses in the IGBTs. Zero voltage switching (ZVS) and zero current switching (ZCS), are two dominant methods for tackling this problem. Due to tailing current of IGBT, applying ZVS needs a large parallel capacitor. On the other hand, turn off losses of the IGBT can be eliminated by the ZCS method appropriately. Based on above-mentioned reasons, the proposed circuit uses IGBT switches that can be properly turned off by ZCS.

The main objective of this thesis was to propose, analyze, design, implement, and confirm the feasibility of the novel AC-DC interleaved ZCS-PWM boost converter by an experimental proof-of-concept prototype. The new converter uses just a single active

auxiliary circuit to assist all the main converter switches to operate with ZCS and operates with ZCS itself. This circuit does not increase the peak voltage or current stresses of the main switches and does not have any components in the main power path of the current so the auxiliary switch only handles a fraction of power that main switches should handle. Besides, by operating interleaved boost converter in DCM, switches can be turned on with ZCS inherently, reverse recovery losses of diodes are eliminated, and small input inductors can be used that leads to decrease in the size, weight and price of the converter.

In Chapter 1, main reasons for applying soft-switching methods such as ZVS and ZCS were discussed. Then each soft-switching method, particularly ZCS in IGBT, was explained in detail. Conventional AC-DC interleaved boost converter was introduced, some of the papers which have been used soft switching for interleaved boost converters were reviewed, and the thesis objectives were stated.

In Chapter 2, the modes of operation of the new PWM interleaved AC-DC boost converter that uses only a single active auxiliary circuit to assist all the main converter switches operate with ZCS and operates with ZCS itself was proposed. Then its features were stated.

In Chapter 3, the different modes of operation of the proposed converter which were discussed in Chapter 2 were analyzed mathematically. Then the voltage and current equations that described the operation of the auxiliary circuit and other related components of the novel converter in steady-state were derived.

In Chapter 4, the results of the mathematical equations derived from the proposed interleaved converter in the steady-state condition in Chapter 3, were used to determine the condition of operating all switches with ZCS. The characteristic curves for the key parameters of the proposed converter were generated by MATLAB program based on the steady-state equations. The effects of each key component on the operation of the converter were discussed. The design procedure was explained by an example. Afterward, the value of each component was determined by using characteristic curves generated by MATLAB program and circuit simulator PSIM so as to satisfy the key design objectives and confirm the feasibility.

In Chapter 5, the design procedure discussed in Chapter 4 were tested and validated by a 1000 W laboratory proof-of-concept prototype. The efficiency of the proposed AC-DC interleaved ZCS-PWM boost converter was compared with the conventional one that operates with hard-switching to confirm the increase of efficiency by the proposed converter.

6.3 Conclusion

The following significant conclusions can be made based on the work done in this thesis:

- A novel auxiliary circuit with only one auxiliary switch for both main switches can be used in an AC-DC interleaved boost converter to perform ZCS in the main switches of the converter and also to increase the overall efficiency.
- The auxiliary switch operates with ZCS as well.
- The main switches do not have increased peak and RMS current stresses because no current from the auxiliary circuit flows into the main circuit.
- The auxiliary circuit does not interfere with the interleaving operation of the converter thus all the advantages of interleaving are maintained.
- Since, the input current of each module is designed to be discontinuous the size and price of the input inductors are reduced considerably in comparison with CCM method. In addition, reverse recovery losses of the main diodes are eliminated.
- The input current is sinusoidal and in phase with the input voltage. As a result, power factor correction is almost 1.

6.4 Contributions

The most significant contributions of this thesis are as follows:

- A new AC-DC interleaved ZCS-PWM boost converter was proposed and its feasibility was confirmed by an experimental prototype.
- The steady-state analysis of the proposed converter was done, its mathematical equations were derived, and its characteristics were determined.

- The operation of the auxiliary circuit was described and shown how it can perform ZCS for all the main switches and increase the overall efficiency. Besides, it was shown how this new converter has the priority to other contemporary interleaved converters.
- Guidelines for satisfying objectives of the design were given and design procedures were explained by an example.

6.5 Future Work

In this section, future works based on the work done in this thesis are suggested as follows:

- The proposed converter is non-isolated interleaved converter. Thus, research can be done to implement this new converter with transformer to increase the efficiency.
- This topology can be used for DC_DC applications, which have high current and low voltage characteristics, such as fuel cells and solar cells.

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Appendix A

MATLAB program which used to generate Fig. 4.2

```
IL1=9.6;

vo=400;

cr=4:24;

le= 2220;

ze=sqrt(le./cr);

vcrmax=(IL1*ze)+vo;

plot(cr,vcrmax)

grid on

xlabel( 'Value of the auxiliary capacitor (nanofarad)')

ylabel('Maximum voltage across the auxiliary capacitor (V)')
```

Appendix B

MATLAB program which used to generate Fig. 4.3

```
z=10:24;
ip=400./z;
plot(z,ip)
grid on
xlabel( 'Characteristic Impedance (Ohm)')
ylabel('Peak current through auxiliary switch (A)')
```

Appendix C

MATLAB program which used to generate Fig. 4.5

```
lr11=0.000005;  lr21=0.000004;  lr22=0.00000425;  lr23=0.0000045;  lr24=0.00000475;
lr25=0.000005;   lr26=0.00000525;

cr=0.000000012;

 z1=sqrt(lr21/cr);

le1=lr11*lr21/(lr11+lr21);

we1=sqrt(1/(le1*cr));

z2=sqrt(lr22/cr);

le2=lr11*lr22/(lr11+lr22);

we2=sqrt(1/(le2*cr));

 z3=sqrt(lr23/cr);

le3=lr11*lr23/(lr11+lr23);

we3=sqrt(1/(le3*cr));

 z4=sqrt(lr24/cr);

le4=lr11*lr24/(lr11+lr24);

we4=sqrt(1/(le4*cr));

 z5=sqrt(lr25/cr);

le5=lr11*lr25/(lr11+lr25);

we5=sqrt(1/(le5*cr));

z6=sqrt(lr26/cr);

le6=lr11*lr26/(lr11+lr26);

we6=sqrt(1/(le6*cr));

 t=0:0.000000001:0.0000007;

 I11=18-(400/z1)*(le1/lr11)*(1-cos(we1*t));
```

```
I12=18-(400/z2)*(le2/lr11)*(1-cos(we2*t));

I13=18-(400/z3)*(le3/lr11)*(1-cos(we3*t));

I14=18-(400/z4)*(le4/lr11)*(1-cos(we4*t));

I15=18-(400/z5)*(le5/lr11)*(1-cos(we5*t));

I16=18-(400/z6)*(le6/lr11)*(1-cos(we6*t));

plot(t,I11,'r')  hold on;

plot(t,I12,'k')  hold on;

plot(t,I13,'g')  hold on;

plot(t,I14,'m')  hold on;

plot(t,I15,'b')  hold on;

plot(t,I16,'c')

grid on;

xlabel('time (S)')

ylabel('Current in main switch (A)')
```

Appendix D

MATLAB program which used to generate Fig. 4.6

```
lr11=0.000005;  lr21=0.000004;  lr22=0.00000425;  lr23=0.0000045;  lr24=0.00000475;
lr25=0.000005;   lr26=0.00000525;

cr=0.000000012;

z1=sqrt(lr21/cr);

le1=lr11*lr21/(lr11+lr21);

we1=sqrt(1/(le1*cr));

z2=sqrt(lr22/cr);

le2=lr11*lr22/(lr11+lr22);

we2=sqrt(1/(le2*cr));

z3=sqrt(lr23/cr);

le3=lr11*lr23/(lr11+lr23);

we3=sqrt(1/(le3*cr));

z4=sqrt(lr24/cr);

le4=lr11*lr24/(lr11+lr24);

we4=sqrt(1/(le4*cr));

z5=sqrt(lr25/cr);

le5=lr11*lr25/(lr11+lr25);

we5=sqrt(1/(le5*cr));

z6=sqrt(lr26/cr);

le6=lr11*lr26/(lr11+lr26);

we6=sqrt(1/(le6*cr));

t=0:0.000000001:0.0000007;

I21=(400/z1)-(400/z1)*(le1/lr21)*(1-cos(we1*t));
```

```
I22=(400/z2)-(400/z2)*(le2/lr22)*(1-cos(we2*t));

I23=(400/z3)-(400/z3)*(le3/lr23)*(1-cos(we3*t));

I24=(400/z4)-(400/z4)*(le4/lr24)*(1-cos(we4*t));

I25=(400/z5)-(400/z5)*(le5/lr25)*(1-cos(we5*t));

I26=(400/z6)-(400/z6)*(le6/lr26)*(1-cos(we6*t));

plot(t,I21,'r')  hold on;

plot(t,I22,'k')  hold on;

plot(t,I23,'g')  hold on;

plot(t,I24,'m')  hold on;

plot(t,I25,'b')  hold on;

plot(t,I26,'c')

grid on;

xlabel('time (S)')

ylabel('Current in auxiliary switch (A)')
```

Appendix E

MATLAB program which used to generate Fig. 4.7

```
lr11=0.0000038;  lr12=0.0000040;  lr13=0.0000042;  lr14=0.0000044;  lr15=0.0000047;
lr16=0.000005;  lr21=0.000004;
cr=0.000000012;
z1=sqrt(lr21/cr);
le1=lr11*lr21/(lr11+lr21);
we1=sqrt(1/(le1*cr));
z2=sqrt(lr21/cr);
le2=lr12*lr21/(lr12+lr21);
we2=sqrt(1/(le2*cr));
z3=sqrt(lr21/cr);
le3=lr13*lr21/(lr13+lr21);
we3=sqrt(1/(le3*cr));
z4=sqrt(lr21/cr);
le4=lr14*lr21/(lr14+lr21);
we4=sqrt(1/(le4*cr));
z5=sqrt(lr21/cr);
le5=lr15*lr21/(lr15+lr21);
we5=sqrt(1/(le5*cr));
z6=sqrt(lr21/cr);
le6=lr16*lr21/(lr16+lr21);
we6=sqrt(1/(le6*cr));
```

```
t=0:0.000000001:0.0000007;
I11=18-(400/z1)*(le1/lr11)*(1-cos(we1*t));
I12=18-(400/z2)*(le2/lr12)*(1-cos(we2*t));
I13=18-(400/z3)*(le3/lr13)*(1-cos(we3*t));
I14=18-(400/z4)*(le4/lr14)*(1-cos(we4*t));
I15=18-(400/z5)*(le5/lr15)*(1-cos(we5*t));
I16=18-(400/z6)*(le6/lr16)*(1-cos(we6*t));
plot(t,I11,'r')  hold on;
plot(t,I12,'k')  hold on;
plot(t,I13,'g')  hold on;
plot(t,I14,'m')  hold on;
plot(t,I15,'b')  hold on;
plot(t,I16,'c')
grid on;
xlabel('time (S)')
ylabel('Current in main switch (A)')
```

Appendix F

MATLAB program which used to generate Fig. 4.7

```
lr11=0.0000038;  lr12=0.0000040;  lr13=0.0000042;  lr14=0.0000044;  lr15=0.0000047;
lr16=0.000005;  lr21=0.000004;
cr=0.000000012;
z1=sqrt(lr21/cr);
le1=lr11*lr21/(lr11+lr21);
we1=sqrt(1/(le1*cr));
z2=sqrt(lr21/cr);
le2=lr12*lr21/(lr12+lr21);
we2=sqrt(1/(le2*cr));
z3=sqrt(lr21/cr);
le3=lr13*lr21/(lr13+lr21);
we3=sqrt(1/(le3*cr));
z4=sqrt(lr21/cr);
le4=lr14*lr21/(lr14+lr21);
we4=sqrt(1/(le4*cr));
z5=sqrt(lr21/cr);
le5=lr15*lr21/(lr15+lr21);
we5=sqrt(1/(le5*cr));
z6=sqrt(lr21/cr);
le6=lr16*lr21/(lr16+lr21);
we6=sqrt(1/(le6*cr));
t=0:0.000000001:0.0000007;
```

```
I21=(400/z1)-(400/z1)*(le1/lr21)*(1-cos(we1*t));

I22=(400/z2)-(400/z2)*(le2/lr21)*(1-cos(we2*t));

I23=(400/z3)-(400/z3)*(le3/lr21)*(1-cos(we3*t));

I24=(400/z4)-(400/z4)*(le4/lr21)*(1-cos(we4*t));

I25=(400/z5)-(400/z5)*(le5/lr21)*(1-cos(we5*t));

I26=(400/z6)-(400/z6)*(le6/lr21)*(1-cos(we6*t));

plot(t,I21,'r')  hold on;

plot(t,I22,'k')  hold on;

plot(t,I23,'g')  hold on;

plot(t,I24,'m')  hold on;

plot(t,I25,'b')  hold on;

plot(t,I26,'c')

grid on;

xlabel('time (S)')

ylabel('Current in auxiliary switch (A)')
```

Curriculum Vitae

Name: Ramtin Rasoulinezhad

Post-secondary Education and Degrees:
Western University
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2017-2017 M.Sc.

Related Work Experience
Teaching Assistant, Research Assistant
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Publications:

1: Ramtin Rasoulinezhad, Adel Absonina, Gerry Moschopoulos.; "A novel AC-DC interleaved ZCS-PWM boost converter" to be published in. *IEEE Aplied Power Electronic Conference (APEC) 2018.*

2: Hamdi Abdi, Ramtin Rasoulinezhad, Mohammad Salehi Maleh. Chapter 5 (fuel cells) of the book in ELSEVIER.; "Distributed generation systems: design, operation and grid integration",*ELSEVIER*, ISBN: 9780128042083, Imprint: *Butterworth-Heinemann, 2017.*

3: Abbas Zabihi, Ramtin Rasoulinezhad, Seyedreza Baharisaravi.; "Effect of Decrease in Energy Consumption by Heaters at Sari-Akand City Gate Station on Greenhouse Gas Emissions", 5th Annual International Conference on Sustainable Energy and Environmental Sciences (SEES 2016), Singapore, 2016.

4: Seyedreza Baharisaravi, Ramtin Rasoulinezhad.; "How Could Green Supply Chain Management Facilitate the Operations of Business?", 2nd International Conference on Social Sciences Economics and Finance, Montreal, Canada, 2016.

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