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Design of Analog CMOS Circuits for Batteryless Implantable Telemetry Systems

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A thesis submitted in partial fulfillment of the requirements for the Master of Engineering Science degree in Electrical and Computer Engineering

DESIGN OF ANALOG CMOS CIRCUITS FOR BATTERYLESS IMPLANTABLE TELEMETRY SYSTEMS

(Thesis format: Monograph)

by

Kyle De Gannes

Graduate Program in Electrical and Computer Engineering

A thesis submitted in partial fulfillment
of the requirements for the degree of
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The School of Graduate and Postdoctoral Studies
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Abstract

A wireless biomedical telemetry system is a device that collects biomedical signal measurements and transmits data through wireless RF communication. Testing medical treatments often involves experimentation on small laboratory animals, such as genetically modified mice and rats. Using batteries as a power source results in many practical issues, such as increased size of the implant and limited operating lifetime. Wireless power harvesting for implantable biomedical devices removes the need for batteries integrated into the implant. This will reduce device size and remove the need for surgical replacement due to battery depletion. Resonant inductive coupling achieves wireless power transfer in a manner modelled by a step down transformer. With this methodology, power harvesting for an implantable device is realized with the use of a large primary coil external to the subject, and a smaller secondary coil integrated into the implant. The signal received from the secondary coil must be regulated to provide a stable direct current (DC) power supply, which will be used to power the electronics in the implantable device. The focus of this work is on development of an electronic front–end for wireless powering of an implantable biomedical device. The energy harvesting front–end circuit is comprised of a rectifier, LDO regulator, and a temperature insensitive voltage reference. Physical design of the front–end circuit is developed in 0.13 μm CMOS technology with careful attention to analog layout issues. Post–layout simulation results are presented for each sub–block as well as the full front–end structure. The LDO regulator operates with supply voltages in the range of $1V$ to $1.5V$ with quiescent current of 10.5 μA The complete power receiver front–end has a power conversion efficiency of up to 29%.

Keywords: CMOS, rectifier, LDO regulator, bandgap reference, wireless power transfer

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I would like to thank the many people who have helped me throughout my graduate studies. First and foremost I would like to thank my adviser and mentor Dr. R. Sobot. My thanks goes out to my current and former colleagues: Kyle Fricke, Sneha Lele, Shawon Sejuti, Mengye Cai, Ziyu Wang, along with many others who I am grateful to have worked and studied with in my time at Western University.

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K.G.A.D.

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List of Abbreviations, Symbols, and Nomenclature

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
FET	Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-channel Metal-Oxide Semiconductor
PMOS	P-channel Metal-Oxide Semiconductor
RF	Radio Frequency
AC	Alternate Current
DC	Direct Current
SCMR	Strongly Coupled Magnetic Resonance
MRC	Magnetic Resonance Coupling
PCE	Power Conversion Efficiency
MIM capacitor	Metal-Insulator-Metal Capacitor
LDO	Low–dropout
PTAT	Proportional To Absolute Temperature
CTAT	Complementary To Absolute Temperature
ADC	Analog-To-Digital Converter
rms, RMS	Root-Mean-Square
μ_p	Mobility of PMOS transistors
μ_n	Mobility of NMOS transistors
C_{ox}	MOS gate capacitance
V_{th}	Threshold voltage
V_T	Thermal voltage

Chapter 1

Introduction

1.1 Motivation

Implantable biomedical telemetry systems are devices that measure and wirelessly transmit biosignal data. Implantable telemetry systems have many applications in scientific and healthcare research. In medical research, implantable telemetry systems are used to monitor left ventricular cardiac pressure and volume of small rodents under the influence of new medical treatments [1]. Current biomedical research of cardiac monitoring in rodents is based on insertion of a wired catheter probe while the subject is anaesthetized [2]. Relatively large implantable devices are acceptable for implantation into larger subjects, such as large mammals. Implantable devices for smaller subjects such as mice require a sufficiently miniaturized device. Further miniaturization of implantable devices for implantation into small rodents is an active area of research [1]. A considerable portion of the volume of an implant is due to the battery. Decreasing the size of the battery will reduce the overall size of the implant. However, battery depletion of an implantable device requires surgical replacement. The proposed solution is to develop wireless power transfer to implantable devices. Wireless power transfer will enable batteryless devices, which will reduce the overall size of the implant.

The proposed telemetry system is to be implanted into a small rodent, as shown in Fig.

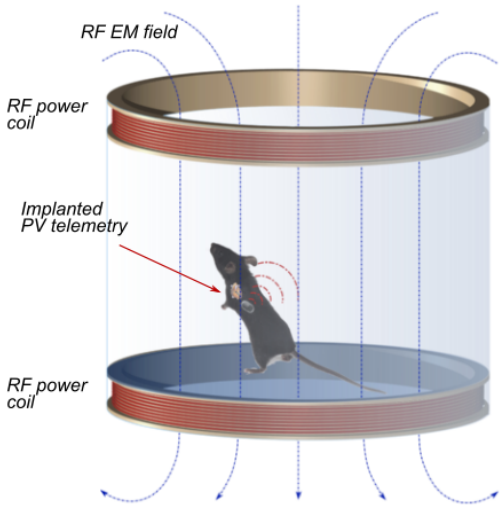


Figure 1.1: Implanted Wireless Telemetry System [2]

1.1. A miniature telemetry device is implanted in the subject and biosignal data is transmitted through a wireless link to a computer for logging and processing. Fully implanted telemetry systems in small subjects can allow researchers to monitor cardiac data of test subjects while the subject is conscious and not under the affect of anaesthesia. The proposed environment for the test subject is a cage containing communication antennas and wireless power transfer infrastructure, as shown in Fig. 1.1.

A method of wireless power transfer that has gained popularity in research is magnetic resonance coupling (MRC) [3]. This method achieves power transfer between two inductor coils in a manner modelled by a step–down transformer. A large coil external to the subject is excited with an AC signal. Through inductive coupling, a signal is induced in a small coil integrated into the implantable device.

Strongly coupled magnetic resonance (SCMR) is a phenomena based on LC resonance to transfer power through mutual inductance. SCMR based power transfer transmits power between coils without radiating electromagnetic waves [4]. Research into the use of SMRC based power transfer indicates that this methodology is also promising for wireless power transfer to biomedical devices [5]. A prototype of magnetic resonance based energy transmission for implantable devices is presented by Bhuyan et al [6]. Experimentation of MRC power

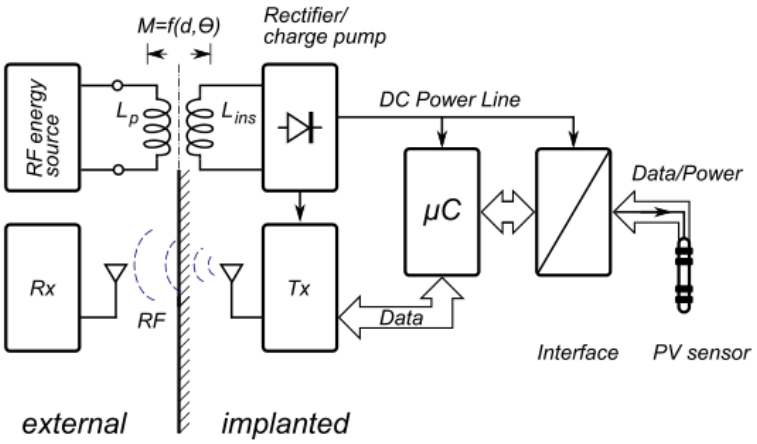


Figure 1.2: Energy harvesting front–end block diagram

transmission efficiency through agar phantom tissue is presented by Zhang et al [7]. Since the maximum power transfer can only be achieved when the external and implanted coils are perfectly aligned, the powering system must have low sensitivity to the coil orientation and distance. Research results presented in [8] examine effects of axial and angular misalignment of the primary and secondary inductors, which occurs due to random movement of the subject [8]. It is concluded from these studies that MRC should be suitable for providing power to various implanted medical devices.

A block diagram of an implantable biomedical telemetry system is shown in Fig. 1.2. The electronics of the implant include a microcontroller, interface circuitry, and a wireless transceiver. DC output of the energy harvesting front–end is intended to power these sub–blocks in lieu of a battery.

The focus of this work is on the design of an electronic front–end that will convert the power received through a wireless power transfer link to a stable DC power supply. A block diagram of the proposed energy harvesting front–end is shown in Fig. 1.3. The architecture consists of a rectifier, linear regulator, and voltage reference. The rectifier converts the AC signal across the coil into an unregulated DC signal. A linear regulator converts the rectifier output to a constant DC power supply rail for on–chip electronics. An on–chip temperature insensitive voltage reference is used to bias the linear regulator. The circuit blocks of the power harvesting

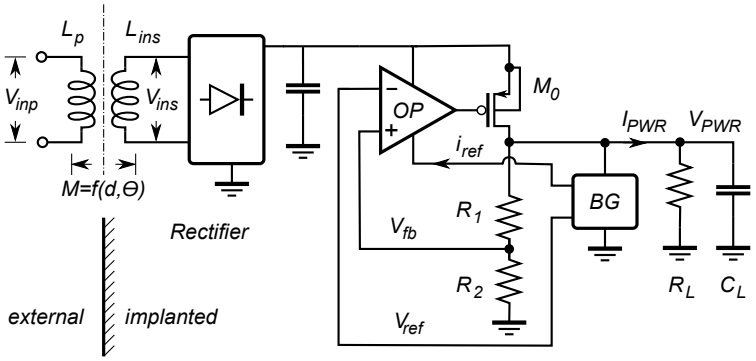


Figure 1.3: Energy harvesting front–end block diagram

front–end are implemented in 0.13μm CMOS technology.

A CMOS rectifier structure capable of power conversion efficiency (PCE) of up to 65% is presented by [9] and [10]. These rectifier structures are presented for use in passive RFID systems, but are well suited to wireless power transfer for wireless biomedical telemetry systems.

A linear regulator for wireless power harvesting that consumes a total of 13.5 μA is presented by [11], however this structure operates at a supply voltage of 2.2 V. Low voltage regulator structures presented in [12, 13, 14] report reference voltage circuits that consume 10—30 μA of current. A low–voltage and low–power structure operating at sub-1 V power supply with microwatt current consumption will provide higher efficiency than the aforementioned designs.

A supply voltage of between 0.9 V to 1 V provides reasonable overhead voltage in 0.13 μm CMOS technology. Accordingly, output voltage of the regulator structure is selected to be approximately 1 V. The minimum output voltage of the rectifier must be the minimum voltage required by the regulator to produce the nominal 1 V output voltage.

1.2 Research Objectives

The main objective of this work is to develop a low–power energy harvesting front–end for batteryless implantable biomedical telemetry systems.

- Design analog sub–blocks to implement a power harvesting front-end for implantable biomedical devices: Rectifier, LDO regulator, bandgap reference

- Develop the physical layout for the power harvesting front–end that can be included in a mixed–signal ASIC for future biomedical implants
- Develop practical research prototype for future testing

1.3 Organization of the Thesis

In this thesis, the design of a wireless energy harvesting front–end is presented. In Chapter 2, design of a CMOS rectifier for AC to DC conversion is presented. In Chapter 3, regulator architectures are introduced and the low–dropout regulator is discussed in detail. The design of the low dropout regulator from schematic sub-block design to layout is presented along with post–layout simulation results of the LDO regulator design. In Chapter 4, design of a bandgap voltage reference circuit is presented. Physical design principles and methodology for analog and mixed–signal integrated circuit design are presented in Chapter 5. In Chapter 6, post–layout simulation results are presented for the top–level regulator architecture containing each block. The research work is summarized in Chapter 7 and proposed future research work is presented.

Chapter 2

Rectifier

Transferring power between magnetically coupled coils results in an AC signal induced across the implanted coil. The AC signal must be converted to DC in order to be regulated to provide a stable power supply rail. The goal in designing the rectifier is to convert the RF signal to DC with high efficiency. The rectifier structure will be implemented entirely on–chip in CMOS 0.13 μm technology.

It has been shown that RF power transfer through dispersive tissue is more efficient at frequencies above 1 GHz [15]. Thus, the rectifier operates at approximately 1 GHz and power conversion efficiency (PCE) of the rectifier at various frequencies will be examined through simulation.

2.1 Background

The conventional rectifier circuit is comprised of two diodes and two capacitors. The forward voltage drop across the diode when turned on is denoted as V_D. When the input voltage falls below the reference node voltage (i.e. ground), diode D_1 turns on and capacitor C_1 charges to $V_{in} - V_D$. As the input rises above the reference node voltage, diode D_2 turns on and D_1 turns

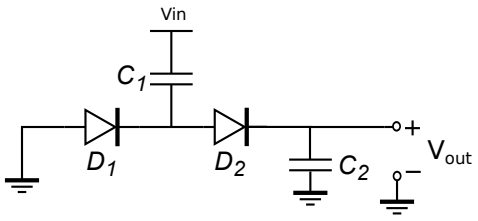


Figure 2.1: Diode–Capacitor rectifier

off. The output voltage V_{out} of the rectifier is

$$V_{out} = 2(V_{in} - V_D)$$

Power conversion efficiency (PCE) is the ratio of power at the output of the rectifier to the power received.

$$PCE = \frac{P_{in}}{P_{out}} \tag{2.1}$$

where P_{in} is power at the input port and P_{out} is power at the output port. Efficiency of the diode–capacitor rectifier is limited by the forward voltage drop of the diode. Larger forward voltage drop across a diode results in decreased power conversion efficiency. Discrete regulator structures are typically implemented with Shottky diode devices, which have a low forward turn on voltage of 200–300mV.

2.2 CMOS Rectifier

Shottky diode devices are not supported in 0.13μm CMOS technology. The diode–capacitor regulator structure can be implemented in CMOS technologies using MOS devices. A diode is a two–terminal device in which the device conducts when the voltage across the terminals is larger than the threshold, and does not conduct when below threshold. The cutoff and saturation regions of MOS device operation are similar to the “on” and “off” states of a diode. A MOS device with the gate and drain terminals connected as shown in Fig. 2.2 is functionally equivalent to a

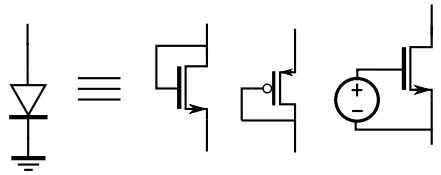


Figure 2.2: Diode connected CMOS devices

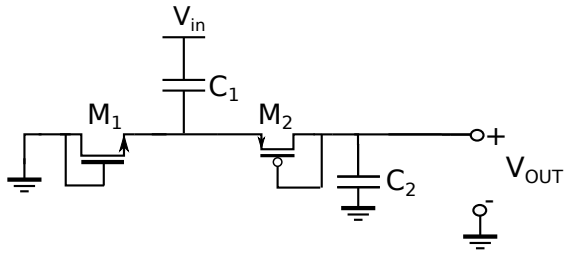


Figure 2.3: CMOS diode rectifier

diode.

A NMOS device operates in saturation under the following conditions

$$V_{gs} > V_{th} \tag{2.2}$$

$$V_{ds} >= V_{gs} - V_{th} \tag{2.3}$$

where V_{gs} is the gate–source voltage , V_{ds} is drain–source voltage, and V_{th} is threshold voltage of the MOS device. The device will operate in saturation when the gate–source voltage is equal to the threshold voltage, similar to the diode "on" state. It can be assumed that drain current is zero when the gate voltage is less then V_{th}, which puts the diode in the "off" state.

A MOS rectifier structure can be formed using only NMOS or PMOS devices or both. Fig. 2.3 shows a conventional rectifier structure using diode connected CMOS devices.

Threshold voltage of MOS transistors will reduce efficiency of the rectifier. Threshold voltage of a diode connected MOS device is equivalent to the forward voltage drop of a diode. The threshold voltage of a MOS transistor in CMOS 0.13 μm technology is approximately 0.45 V. Reducing the effect of the threshold voltage will increase the PCE of the rectifier.

If the gate of the MOS device is biased at a non–zero voltage, then the required drain–

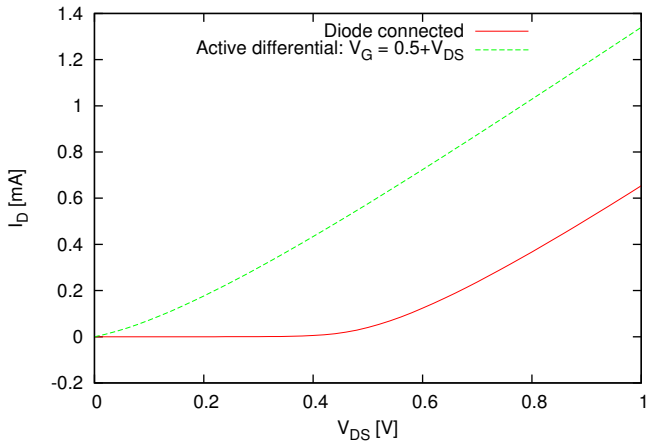


Figure 2.4: Diode connected CMOS devices

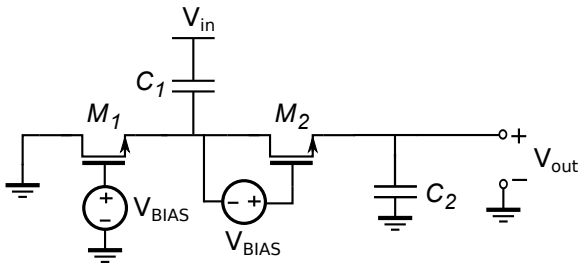


Figure 2.5: NMOS diode rectifier with external V_{th} cancellation

source voltage is reduced. For instance, if the gate is biased at the threshold voltage then the drain–source voltage must only be larger than zero.

Simulated characteristics of a $0.13\mu m$ MOS diode and overdriven MOS device are shown in Fig. 2.4. These characteristics are for an NMOS device of $0.13\mu m$ length and $1\mu m$ width. It is evident that the threshold of the diode device is reduced when there is a gate overdrive voltage. In order to increase the power conversion efficiency, gate overdrive can be used to reduce the threshold of the of the MOS device switch.

A straightforward method of biasing the MOS device gate is to provide a bias voltage generated through another DC supply rail, as in Fig. 2.5. This method is referred to as external V_{th} cancellation (EVC) [16]. This method is not feasible for completely passive rectifiers since another DC supply is required.

An alternate method of providing a bias voltage is DC feedback from a voltage divider at

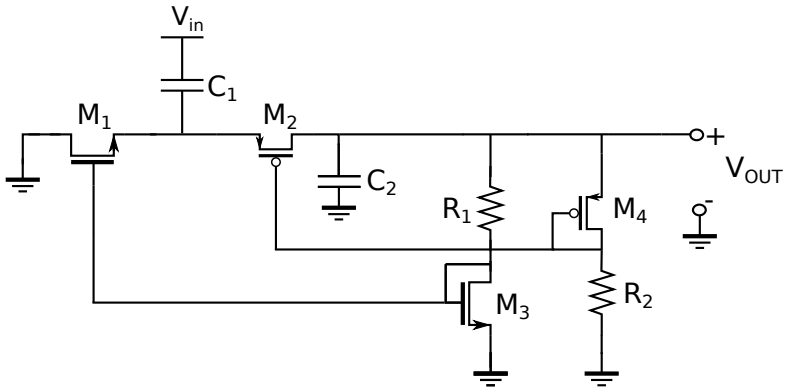


Figure 2.6: NMOS diode rectifier with internal V_{th} cancellation

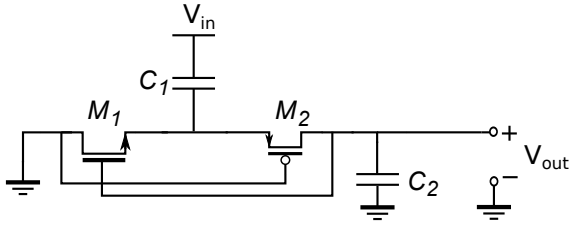


Figure 2.7: CMOS diode rectifier with self V_{th} cancellation

the output of the rectifier, as shown in Fig. 2.6. This method is known as internal V_{th} cancellation (IVC) [17]. The implementation of IVC shown in Fig. 2.6 contains two voltage dividers with diode connected MOS devices and resistors. The MOS device in this voltage divider are identical to the devices in the rectifier, such that the correct bias voltage is generated. Since there is no need for another DC supply rail, this method can be used for passive rectifier devices. However, drawing current for the voltage divider reduces the efficiency of the rectifier.

A third method of threshold reduction is connecting the MOS transistor gates to internal nodes of the rectifier. The PMOS gate is connected to the lowest potential and the NMOS to the highest potential within each stage, as shown in Fig. 2.7. This method is known as self V_{th} cancellation (SVC) [10]. Using the SVC structure, the effective threshold of the MOS devices are reduced without requiring another DC power supply or drawing additional power from the output of the rectifier.

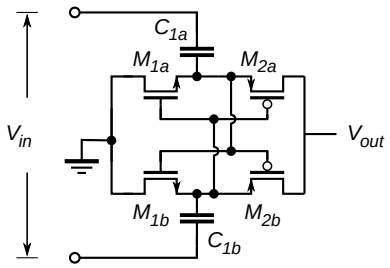


Figure 2.8: Differential SVC rectifier

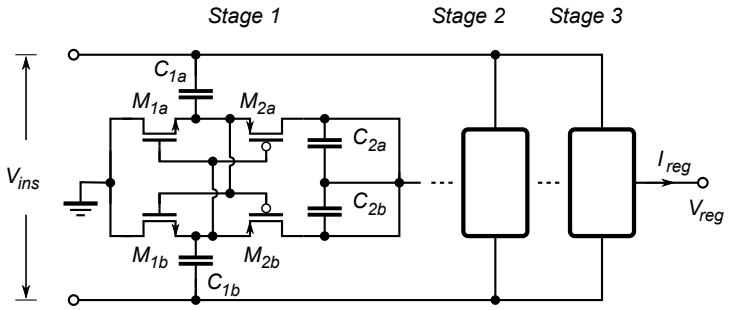


Figure 2.9: Three stage differential SVC rectifier

2.3 Diffferential SVC CMOS rectifier

In order to implement wireless power transfer, improved power conversion efficiency is desirable. Higher PCE can be achieved using differential rectifier structures compared to single ended structures [10]. The differential SVC CMOS rectifier structure presented in [10] has been demonstrated to provide PCE of up to 65%. A single stage of the rectifier structure is shown in Fig. 2.8.

The differential SVC unit structure consists of two pairs of MOS devices with the gates connected to the source and drain of the opposite MOS devices. The gates of the MOS devices are connected through the capacitor to one end of the input terminal. When the voltage at the gate terminals of the MOS devices becomes positive, the NMOS device is turned on with a large gate–source overdrive voltage. Conversely, when the gate voltage becomes negative, the PMOS device is turned on.

A three stage CMOS SVC rectifier is shown in Fig. 2.9. The output of each stage is the DC reference node for subsequent stages, which builds the DC voltage higher with each stage.

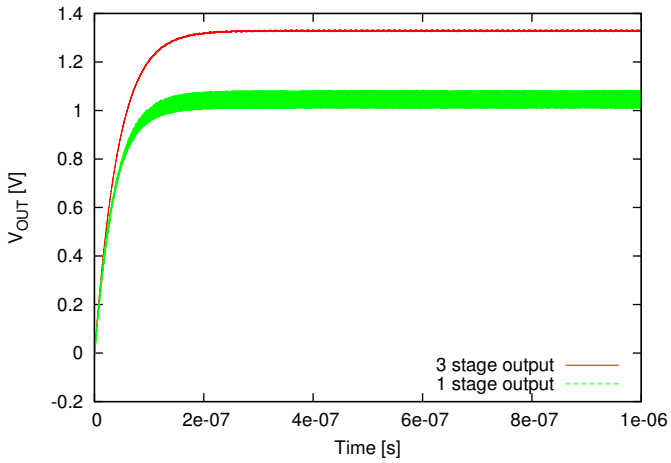


Figure 2.10: Pre–layout Differential SVC rectifier transient simulation - $2V_{pk-pk}$ input

Simulation of the three stage circuit showing the output voltage after the first and third stage is shown in Fig. 2.10. It is observed from the simulation results that the output voltage of the three stage rectifier has a larger DC component and smaller ripple amplitude than single or two–stage structures. For the simulation shown in Fig. 2.10, the load at the output of the rectifier is a $10k\Omega$ resistor and $10pF$ capacitor in parallel. The 10pF capacitor is added on–chip to filter ripple at the output.

The differential SVC rectifier structure has a higher power conversion efficiency than the prior discussed structures [10]. Thus, the SVC rectifier is implemented for the proposed power harvesting structure.

For maximum power transfer between the receiving coil and rectifier input, a matching network is necessary. Input impedance of the rectifier must be measured at each frequency. If the output of the rectifier will be connected to an IC pin, the parasitic capacitance should be used to offset the matching network capacitance [10].

2.4 Physical Design

The singe stage layout is developed and three identical instances are cascaded to form the three stage rectifier. Capacitor devices available in CMOS $0.13\mu m$ technology are metal–insulator–

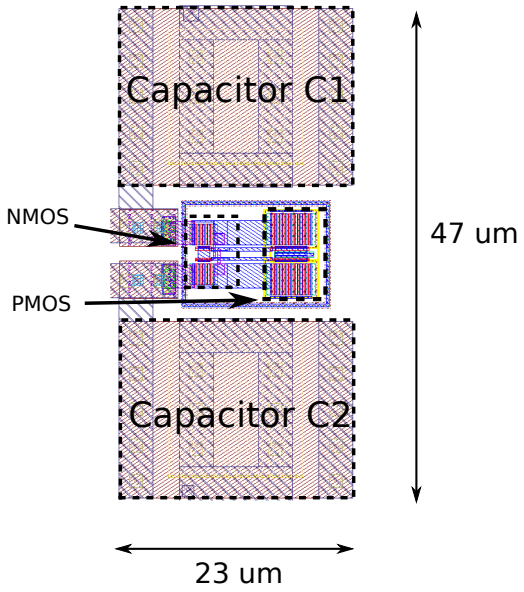


Figure 2.11: Single stage CMOS rectifier

metal (MIM) and MOS varactor structures. MOS varactors provide higher capacitance density than MIM capacitors, but are intended for uses with one terminal grounded. The MIM capacitor block is used in the rectifier design because the varying capacitance of a MOS varactor devices is not suitable for a rectifier. Layout of a single rectifier block is shown in Fig. 2.11. Three of the rectifier blocks are connected to form a three stage rectifier, as shown in Fig. 2.12. Added resistance of interconnects will reduce PCE of the rectifier structure. To reduce added resistance, interconnects between stages are made wider than the minimum width specified for manufacturing. Approximately 70% of the rectifier layout area is occupied by the capacitors.

Post–layout extracted simulation includes estimated parasitic components based on geometry of the physical layout. Pre–layout schematic simulations assume ideal interconnects, unless the parasitic components are explicitly modelled. Post–layout simulation provides a more accurate estimation of circuit performance.

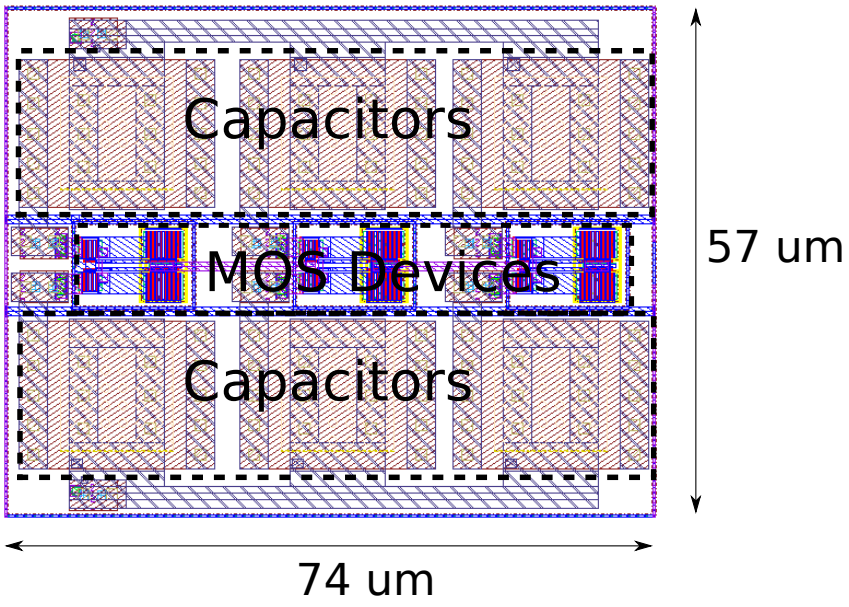


Figure 2.12: Three stage CMOS rectifier

2.5 Post–layout Simulation

A transient simulation of the rectifier at varying input voltages is shown in Fig. 2.13. The AC input voltage for the simulation testbench is at a frequency 915 Mhz, with load impedance of a 10 pF capacitor and 10 kΩ resistor in parallel. Sufficient DC output voltage level for a power supply rail is approximately 1 V, which will require approximately 2 V peak–to–peak at the input of the rectifier.

Post–layout simulations indicate slightly lower output voltage than the pre–layout schematic simulation. DC output voltages of the post–layout simulation are approximately 4% smaller than the pre–layout simulation results. DC output voltage of the rectifier reaches 1 V at in AC input of approximately 2 V peak–to–peak. This means that induced voltage on the implanted coil must be correspondingly 2 V peak–to–peak.

Comparison of PCE of pre- and post-layout are shown in Fig. 2.14. PCE is approximately 8% lower for post layout simulation results than the pre–layout simulation.

PCE for various input frequencies is shown in Fig. 2.15. Lower frequencies result in improved PCE for the SVC rectifier structure [10]. Input frequency selection at the system level

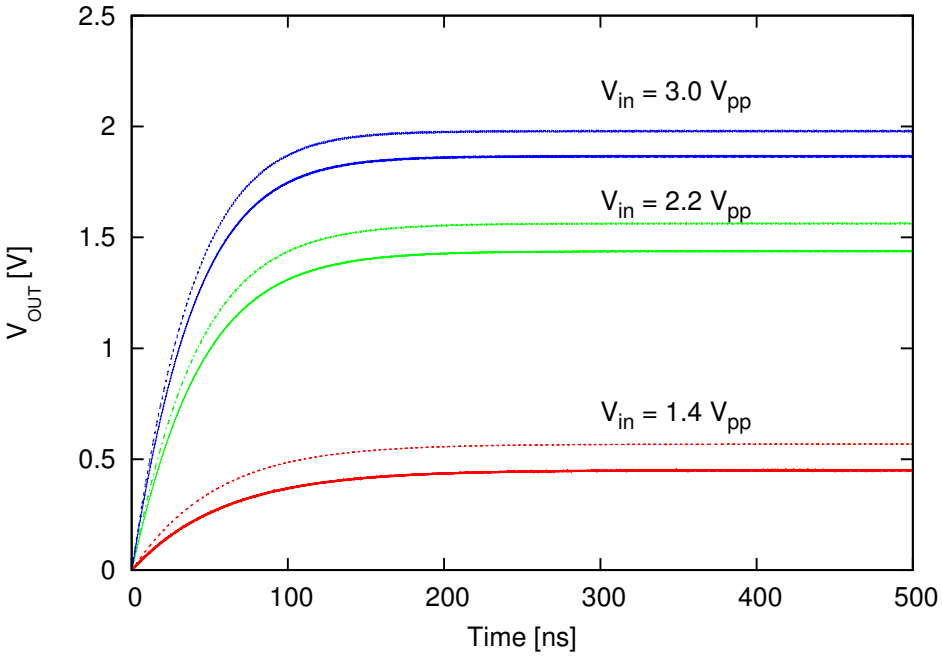


Figure 2.13: Transient Simulation at 915MHz input with 10KΩ load, solid line pre–layout and dashed line is post–layout

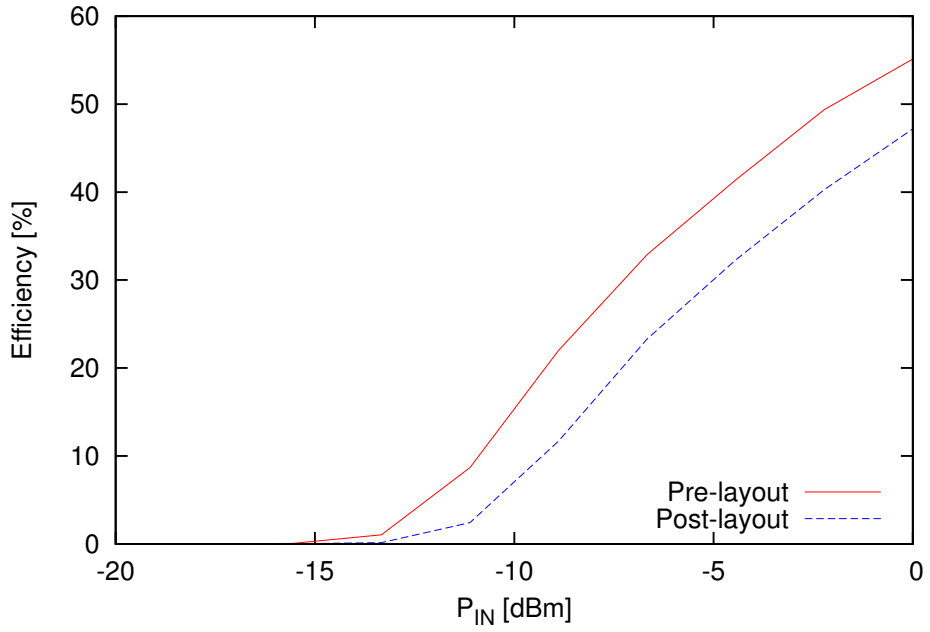


Figure 2.14: PCE vs input power at 915MHz input, 10kΩ load

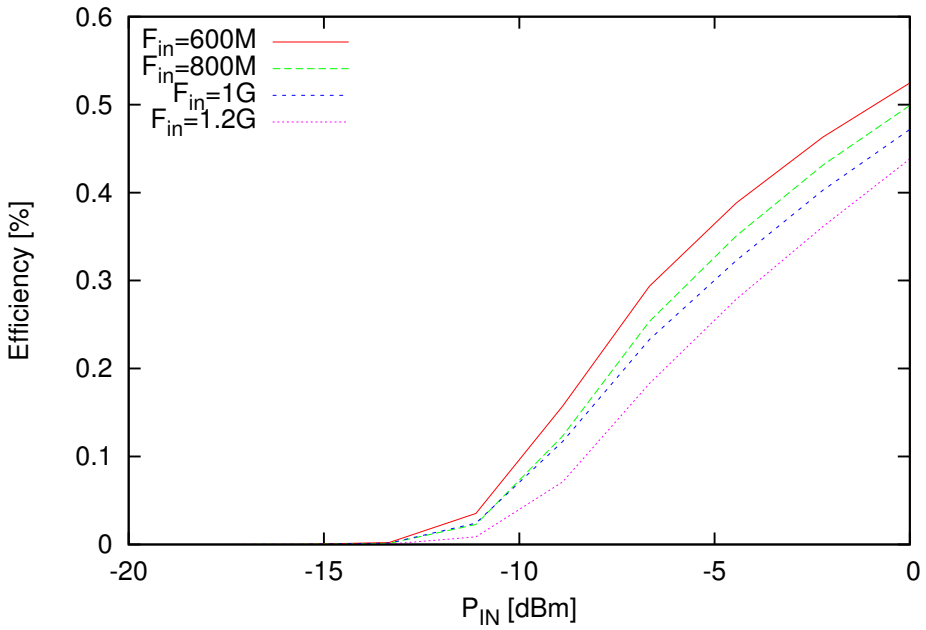


Figure 2.15: Post–layout simulation of PCE with differing input frequency

must selected based on PCE of the rectifier in addition to coil power transfer efficiency.

Although the post–layout results are degraded by resistance or interconnects, the results indicate that this circuit is adequate for powering low–power implantable telemetry systems. In order to reduce losses in interconnects, the interconnects connecting the rectifier to additional circuitry must be designed to be as wide and short and possible.

2.6 Summary

In this chapter the design of a CMOS rectifier is presented. Conventional MOS rectifier structures are presented with different methods for improvement of power conversion efficiency. A differential input self V_{th} cancellation CMOS rectifier is presented. Physical design of the rectifier in 0.13 μm CMOS is presented along with post–layout simulation results, indicating power conversion efficiency of up to 50%.

Chapter 3

Low–Dropout Regulator

3.1 Overview

The rectified output signal of the wireless power transfer system must be regulated in order to provide a stable power supply rail. The low–dropout (LDO) regulator is a linear DC-DC regulator that is commonly used in low power applications. In many cases, switching regulators are more power efficient than linear regulators. The main drawback of a switching regulator is that a pulse signal is required to drive the switching regulator architecture, in contrast to a linear regulator which does not require such a signal [18].

For many applications it is not feasible to provide the pulse signal required by a switching regulator. For this reason, linear regulators such as the LDO regulator are commonly used in low power applications. LDO regulators typically used as the main power supply in many biomedical implant device implementations, such as [1].

A LDO regulator is composed of an error amplifier, feedback network, pass device, and voltage reference [19]. LDO regulators can be classified as series or shunt. The block diagram of the series and shunt LDO regulators are displayed in Fig. 3.1. A voltage reference is applied to the negative input of the op–amp, with the output of the op–amp applied to the pass element. The series LDO structure uses an amplifier to modulate the pass element such that the output

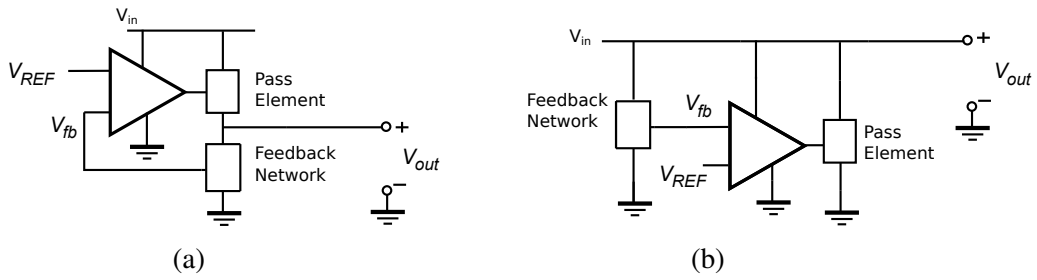


Figure 3.1: Low Dropout Regulator structures: a) series, b) shunt

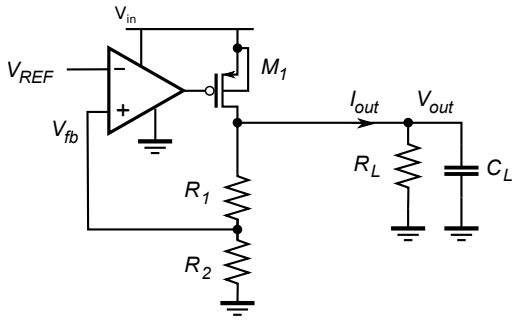


Figure 3.2: Low Dropout Regulator with PMOS pass element

voltage is a scaled by the reference voltage. The shunt LDO structure is comprised of the same components as the series structure, however the pass device shorts the input voltage such that it becomes the specified output regulator voltage. For power harvesting applications, the series LDO structure is more power efficient and thus is the more suitable structure [18].

The pass device can be implemented with either a bipolar or MOS transistor. Since BJT devices are current controlled, a BJT pass device requires a considerable quiescent current. In addition, the base current is proportional to the load current, which wastes more power at higher loading and may cause large current draw at start–up. Since MOS transistors are voltage controlled, the quiescent current is independent of regulator loading and is much lower compared to the BJT device. Thus MOS transistors are preferred as a pass device for better power efficiency in low–power LDO regulators [20]. A LDO regulator with PMOS pass device is shown in Fig. 3.1. Regulator output voltage is controlled by the error amplifier through negative feedback. Assuming large DC op–amp gain, the voltage at the input terminals of the op–amp become virtually equal. The resistive voltage divider feedback network scales the output such that the feedback voltage is equal to the reference voltage when the output is at the

specified regulator output value. The output voltage of the regulator is

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \tag{3.1}$$

where V_{out} is the regulator output voltage, R_1 and R_2 the resistance of resistors R_1 and R_2, and V_{REF} is a reference voltage. Regulator output voltage is controllable through the reference voltage and the ratio of the feedback resistors. The regulator output voltage can not be more precise or stable over temperature than the reference voltage. A temperature independent reference circuit is used to provide the LDO reference voltage. Design of the voltage reference is presented in Chapter 4.

Since the resistors have identical temperature dependence and the reference is temperature independent, the regulator output will be independent of temperature. The feedback resistors should have a relatively high value in order to minimize power consumption.

System level feedback in the loop must be negative to prevent instability. Connecting the feedback such that the system level feedback is positive will result in instability, causing the output to hang at one of the supply rails. A LDO regulator with a PMOS pass device must have feedback connected to the positive op–amp input.

Consider the feedback loop of a LDO regulator with a PMOS pass device. As the feedback voltage to the positive op–amp input increases, the op–amp output voltage also increases. An increase in gate voltage of the pass device results in a decrease of the PMOS overdrive voltage, and a decrease in the drain current. Decreasing drain current results in a decrease in the feedback voltage, thus the loop has negative feedback regulation.

An alternate LDO regulator configuration is a NMOS pass device with feedback to the negative op–amp input, as shown in Fig. 3.3. In the case of a NMOS pass device, the op–amp output voltage must be larger to provide the necessary overdrive voltage. Using a PMOS pass device allows the output of the op–amp to remain close to the lower power supply rail, which is typically ground. Thus, the LDO regulator structure for this design has a PMOS pass device, as

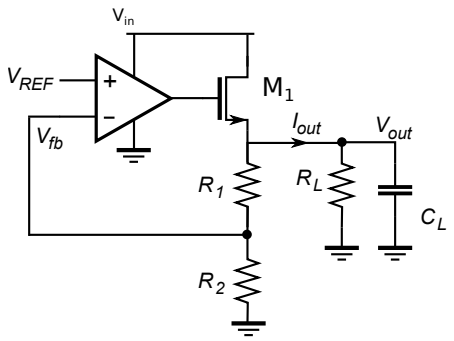


Figure 3.3: Low Dropout Regulator with NMOS pass device

shown in Fig. 3.2.

3.2 Operational Amplifier Design

The LDO error op–amp processes regulator feedback and drives the pass device. The op–amp amplifies the difference between reference and feedback voltage to produce the desired regulator output voltage. To improve the efficiency of the LDO regulator, the op–amp should be low power, while providing adequately high DC gain and high power supply rejection. Increasing DC gain of the op–amp will result in closer matching between the reference voltage and the feedback voltage, meaning the output will be more precisely controlled. However, designing the op–amp for higher DC gain will also increase power consumption.

Since the regulator is in a negative feedback loop, stability of the op–amp is important in ensuring stability of the complete loop. The error op–amp is loaded by the gate of a FET, which is purely capacitive. Thus, the op–amp requires a single ended output and should be optimized for driving capacitive loads. In this section, op–amp structures are discussed and compared analytically and through simulation.

3.2.1 Single Stage Op–Amp

The simplest op–amp structure is a single stage op–amp. The single stage op–amp is a differential pair with current mirror load, as shown in Fig. 3.4. Low frequency gain of this op–amp

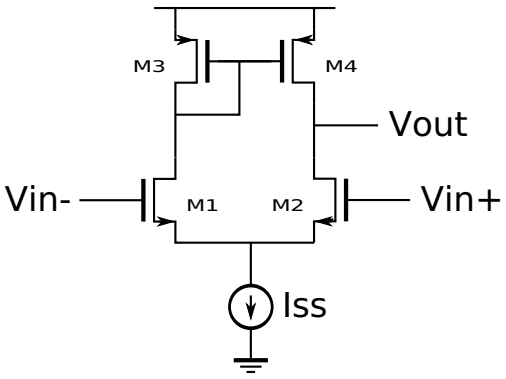


Figure 3.4: Single Stage Op–Amp

is

$$\frac{v_{out}}{v_{id}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{3.2}$$

where v_{id} is the differential input defined as

$$v_{id} = v_{in+} - v_{in-}$$

v_{out} is the single ended output voltage of the op–amp, g_{m1} is transconductance of the differential pair devices, g_{ds2} and g_{ds4} are drain–source transconductance of devices M2 and M4 respectively. Transconductance g_m of a MOS device is proportional to the ratio of width to length of the device. Drain–source transconductance g_{ds} is inversely proportional to the length of the device.

Typically, higher gain is required than the simple single stage op–amp can provide. Gain of the op–amp stage, as in equation (3.2), is the product of input device transconductance and output impedance. Aside from increasing the transconductance of the input devices, an increase in gain can be achieved by increasing the output impedance. Fig. 3.5 shows a modified single stage op–amp known as the telescopic op–amp [21]. In comparison to the simple single stage op–amp, output impedance of both paths to ac ground is increased through the use of cascoding structures. The PMOS mirror is modified to a wide swing cascoded current mirror, and NMOS common gate devices are added above the differential pair.

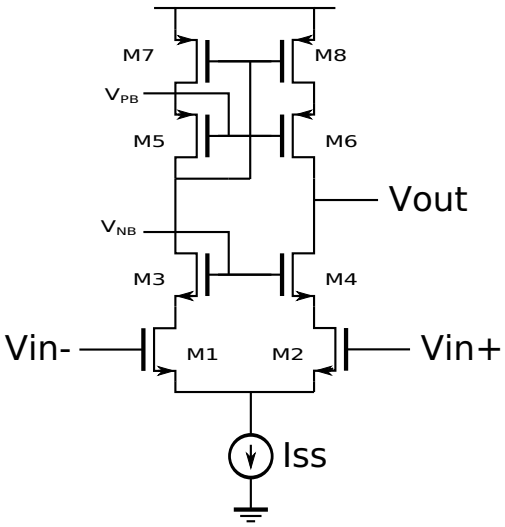


Figure 3.5: Telescopic Op–Amp

Low frequency gain of the telescopic op–amp is

$$\frac{v_{out}}{v_{id}} = g_{m1}\frac{g_{m4}r_{ds4}r_{ds2}}{g_{m6}r_{ds6}r_{ds8}} \tag{3.3}$$

Drain–source resistance r_{ds} is the inverse of drain–source transconductance g_{ds}. Drain–source resistance is proportional to the length of the device.

3.2.2 Two–Stage Op–Amp

The classic two-stage op–amp, Fig. 3.6, is a versatile structure used in many applications [22]. This op–amp structure is comprised of a differential pair with current mirror load and a current sink inverter. An alternate two–stage op–amp structure is to use a PMOS differential pair and current source load inverter output stage. Regardless of which type of device is used for the input pair, typically the overall DC gain is unaffected since there is always one stage with a NMOS transconductance device. Although two–stage op–amps presented in the literature commonly have NMOS input devices, there are many advantages to using PMOS devices for the input stage [23]. Flicker noise, or 1/f noise, is typically lower for PMOS devices since holes have a lower probability of being absorbed at surface states [23]. Using a NMOS transconductance

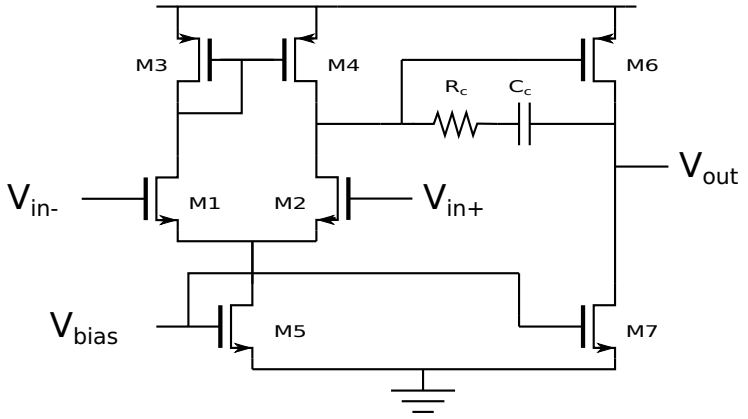


Figure 3.6: Two-Stage Op–Amp with Miller Compensation

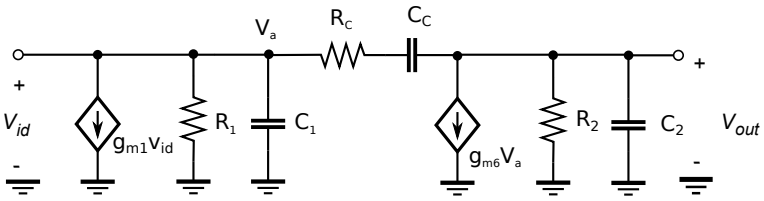


Figure 3.7: Small signal model of two–stage op–amp

device in the output stage reduces the slew–rate. Slew–rate is not a concern in this particular op–amp design, as the load is the gate of a single mos device. The major disadvantage of PMOS input devices is an increase in thermal noise [23].

Frequency Response and Compensation

The two–stage op–amp requires compensation to increase phase margin to an acceptable amount. In a negative feedback configuration a phase shift of 180° around the loop at unity gain will result in oscillation. It should be noted that compensation may be required in the LDO loop in addition to the op–amp compensation.

Fig. 3.7 is the small signal model of the two–stage op–amp, including the compensation capacitor. This compensation technique is referred to as Miller compensation, since the effective capacitance of the compensation capacitor is increased due to the Miller effect.

The transfer function is found from the small signal model as [24],

$$\frac{V_{out}(s)}{V_{id}} = \frac{(g_{m1}g_{m6}R_1R_2)[1 + sC_C(R_C - \frac{1}{g_{m6}})]}{as^3 + bs^2 + cs + 1} \tag{3.4}$$

Where the denominator coefficients are

$$a = R_1R_2R_CC_1C_2C_C$$
$$b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C) + R_CC_C(R_1C_1 + R_2C_2)$$
$$c = R_1(C_1 + C_C) + R_2 + C_C) + g_{m6}R_1R_2C_C + R_CC_C$$

The poles of the transfer function can be approximated as [24]

$$\omega_{p1} \approx \frac{1}{R_1(C_{gd6} + C_1) + R_2(C_{gd6} + C_2) + g_{m6}R_1R_2C_{gd6}} \tag{3.5}$$

$$\omega_{p2} \approx \frac{g_{m6}C_{gd6}}{(C_1 + C_2)C_{gd6} + C_1C_2} \tag{3.6}$$

where C_{gd} is gate to drain capacitance. The feedforward path through the compensation capacitor results in a zero in the transfer function. Without the compensation resistor, the zero is located at

$$\omega_{z_1} = \frac{g_{m6}}{C_c} \tag{3.7}$$

This zero is located in the right half–plane (RHP), which will limit the achievable unity gain bandwidth [22]. A nulling resistor, R_c, is added in series with the compensation capacitor to either eliminate the zero or move the RHP zero to the right half–plane on top of p_2. To eliminate the zero by moving it to infinity a nulling resistance of $R_C = 1/g_{m6}$ is used. Alternatively, setting

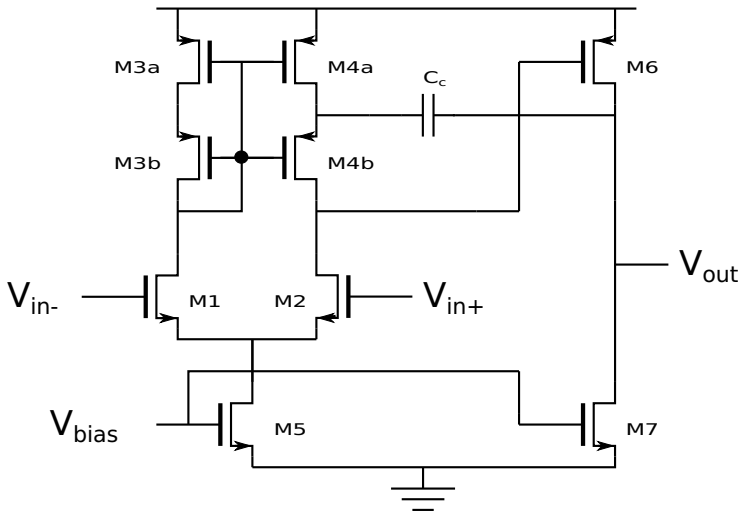


Figure 3.8: Two-Stage Op–Amp with indirect feedback compensation

the zero equal to p_2 results in

$$R_C = \frac{1}{g_{m6}}\left(1 + \frac{C_2}{C_C}\right) \tag{3.8}$$

The pole–zero cancellation resulting from equation (3.8) of the nulling resistor calculation is usually preferred in order to achieve a higher phase margin [24].

Miller compensation of two–stage op–amps is based on direct feedback between outputs of the two stages. Connecting the output of the two stages results in a right–half plane zero, which must be moved to the left–half plane with a nulling resistor. If the compensation capacitor is not connected between the output of the two stages, the RHP zero is avoided. This method of indirect feedback compensation of op–amps is presented by [25]. A two–stage op–amp with indirect feedback compensation is shown in Fig. 3.6. Using the split length current mirror structure, Fig. 3.8, requires minimal changes to the miller compensated structure. A Miller compensated structure can be converted to indirect feedback by splitting the length of the PMOS mirror devices [26]. Using indirect compensation, the RHP zero is removed and the compensation capacitor is 4 to 10 times smaller than a comparable Miller compensated structure [26].

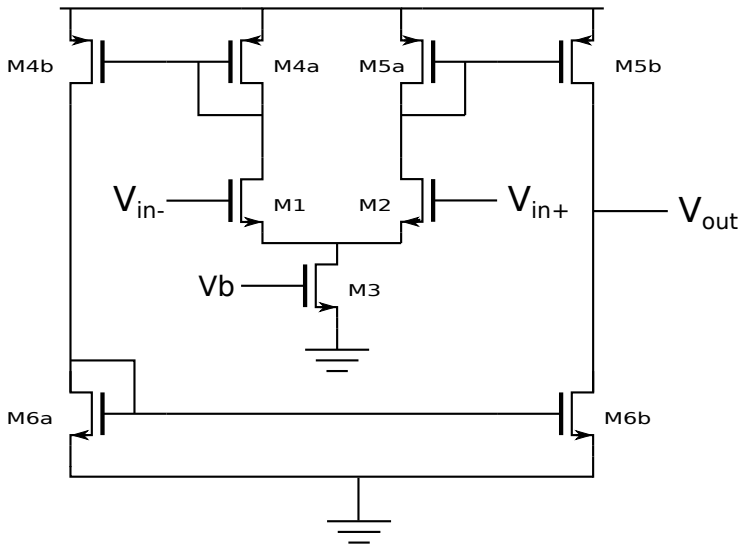


Figure 3.9: Current Mirror Op–Amp

3.2.3 Current Mirror Op–Amp

Another variation of the two–stage op–amp that is commonly used in low power applications is shown in Fig. 3.9 [22]. This structure is referred to in the literature as the current mirror op–amp [24]. In this op–amp structure, both input voltage signals are converted to current signals, and mirrored to the output node. The negative input is mirrored twice, through the M3 and M5 current mirrors.

The circuit of Fig. 3.9 typically does not provide a large DC voltage gain [24]. An additional amplifying stage at the output of the current mirror op–amp structure can increase gain to typically 80 dB [22]. Gain as large as 80 dB is not required in this application, and another amplifying stage will increase power consumption considerably. Gain of this structure can be improved with a cascoded structure as shown in Fig. 3.10 [24]. Increase output impedance of the cascoded current mirrors results in an increase in gain of the cascoded current mirror op–amp shown in Fig. 3.10 compared to the simple current mirror op–amp shown in Fig. 3.9.

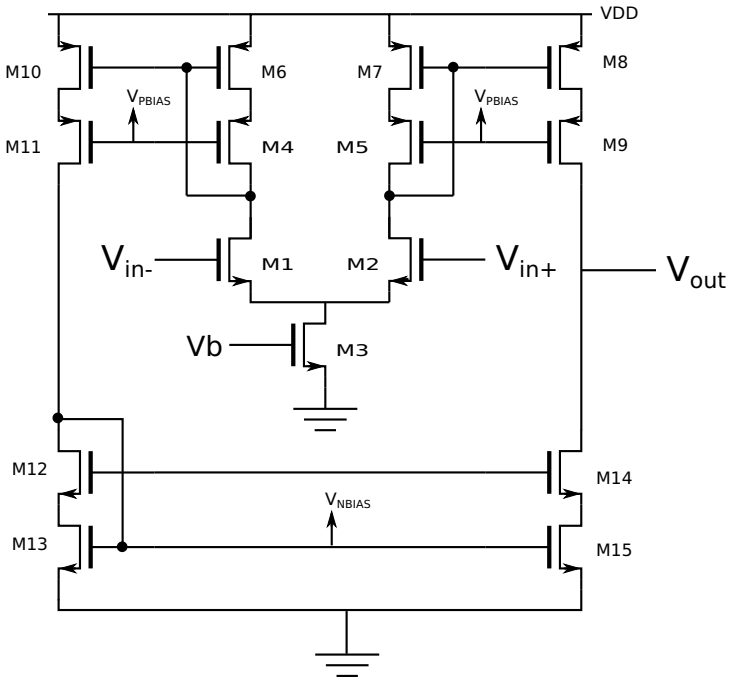


Figure 3.10: Cascoded Current Mirror Op–Amp

3.2.4 Folded Cascode Op–Amp

The folded cascode op–amp, Fig. 3.11, is a structure that is well suited for driving capacitive loads. Cascoded structures from output to both power supply rails provides moderately large gain. High output impedance makes this structure unsuitable for driving resistive loads, but well suited to driving small capacitive loads. Since the load of a LDO regulator is the gate of a mos device, which is equivalent to a small capacitance, the folded–cascode structure is well suited for use in LDO regulators. Since the output pole will be affected by load capacitance, folded–cascode op–amps are typically compensated by the load capacitor. The gain and frequency response of the folded cascode amplifier is analyzed from the small signal model shown in Fig. 3.12. Gain of the folded cascode amplifier is

$$A_v \approx \frac{3}{4} x(gmNr_{dsN})^2$$

where x is a constant between 0 and 1 that depends on the relative values of MOS device transconductances [22].

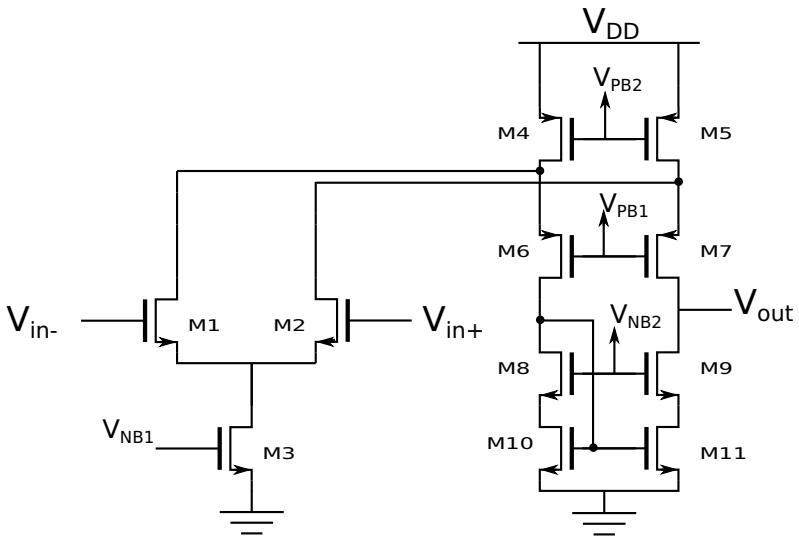


Figure 3.11: Folded Cascode Op–Amp

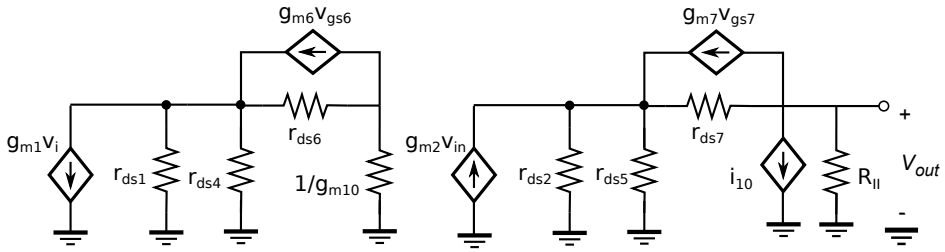


Figure 3.12: Small signal model of folded cascode op–amp

Table 3.1: Simulated op–amp specifications

Specification	Telescopic	Two–stage	Cascoded Current mirror	Folded–cascode
DC Gain [dB]	29	48	30	37
Phase Margin	61°	89°	24°	81°
Gain Bandwidth [Hz]	15.5M	12.8M	45M	8M
PSRR @DC [dB]	31	53	54	81
ICMR [V]	0.1 to 1.1	0.1 to 1.2	0.1 to 1.1	0.1 to 1.1
Supply current [A]	2.5 μ	2.5 μ	2.5μ	2.6 μ

3.2.5 Comparison of Op–Amp Architectures

Specifications of different op–amp structures designed for the LDO error amplifier are listed in Table 3.1. For this application it is important that the power consumption is as low as possibles. There are various methods presented in the literature to boost the gain of an op–amp [22], however this design requires a tradeoff between low power consumption and moderate gain. The nominal supply current of the op–amp is selected to be 2.5 μA, which allows sufficient biasing current in this technology.

3.3 LDO Regulator Loop

The folded cascode op–amp structure is selected for the error amplifier. High power supply rejection ratio and moderate gain make the folded cascode topology well suited for the error amplifier of and LDO regulator. The op–amp biasing current of the differential pair will be provided by the bandgap reference for to reduce the complexity and power consumption.

3.3.1 Frequency Response

In a closed loop configuration with negative feedback, oscillation will occur if the phase shift around the loop is 180° when the gain is unity. To prevent oscillation, it is important to have an acceptable phase margin for the open loop transfer function of the LDO.

An alternative to the compensation capacitor is the addition of a source follower NMOS device cascoded with the pass device [27]. This addition stacked device would also increase power supply rejection, and the voltage drop can be used to reduce the power supply level by a constant amount if the unregulated supply voltage is too large [28]. Addition of this source follower device will reduce the efficiency of regulator architecture because of the loss across the device.

Methods of compensation presented in the literature include active devices such as buffers [29] and Miller compensation capacitance [30]. For maximum power efficiency, compensation

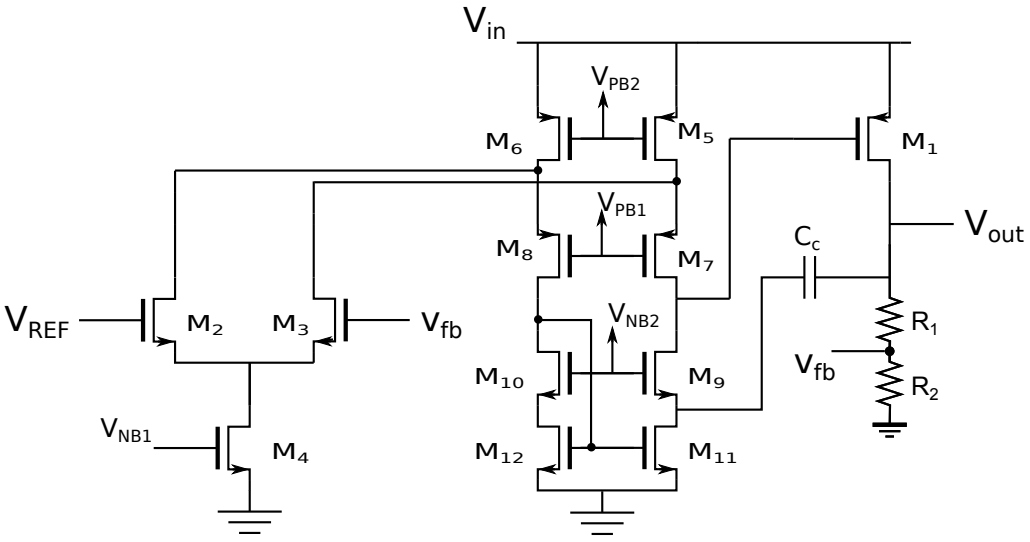


Figure 3.13: LDO regulator with folded–cascode op–amp

using a feedback capacitor is selected for the folded cascode based LDO structure.

A transistor level diagram of the LDO is shown in Fig. 3.13. For stability compensation, the pole at the output of the op–amp is brought to a lower frequency with a compensation capacitor C_C. The compensation capacitor can be connected between the output of the op–amp and the regulator output, however this would introduce a right half–plane zero. Similar to the indirect feedback compensation method presented for the two–stage op–amp, the compensation capacitor is connected at a low impedance node of the cascoded current sink of the folded–cascode op–amp. Indirect feedback compensation allows for a smaller compensation capacitor and does not require a nulling resistor [26].

Open loop stability of the LDO is characterized with the circuit of Fig. 3.14. The feedback path of the loop is broken to find the open loop transfer function v_{fb}/v_i. The DC gain A_{d1} of the op–amp is approximated as

$$\begin{aligned} A_{d1} &= g_{m2} r_{out} \\ &\approx g_{m2}[(g_{m8} r_{ds6}(r_{ds6} \| r_{ds8})) \| (g_{m12} r_{ds10}) r_{ds12}] \end{aligned}$$

where g_{m2}, g_{m8}, and g_{m12} are the transconductance of transistors M_2, M_8, and M_12, r_{ds6}, r_{ds8},

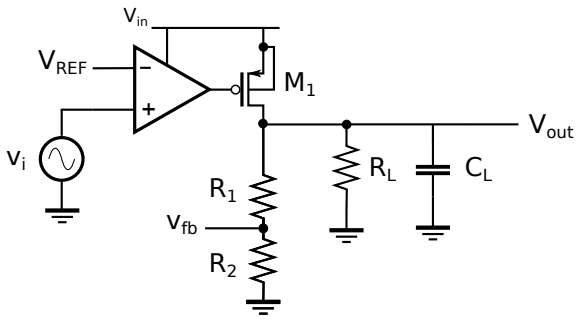


Figure 3.14: LDO regulator open loop test

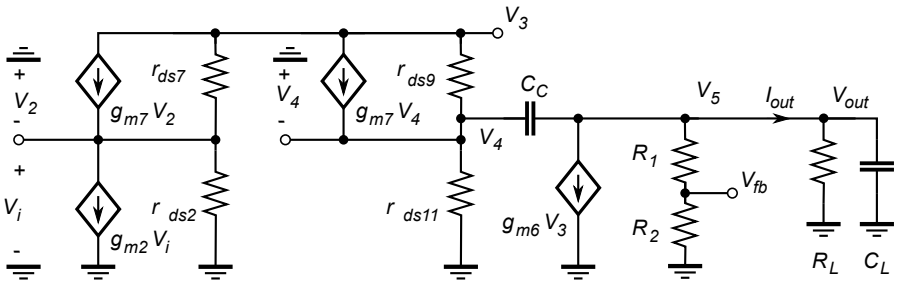


Figure 3.15: Schematic diagram of the regulator open loop small signal equivalent network.

r_{ds10},r_{ds12} are drain–source resistance of transistors M_6, M_8, M_10, and M_12. The open loop gain A_{op} relative to the node V_{fb} is

$$\begin{aligned} A_{op} =& \frac{V_{fb}}{V_i} = A_d\beta \approx A_{d1}g_{m1}R_L\frac{R_2}{R_1+R_2} \\ \approx& g_{m1}R_Lg_{m2}[(g_{m8}r_{ds6}(r_{ds6}||r_{ds8}))||(g_{m12}r_{ds10})r_{ds12}] \end{aligned} \tag{3.9}$$

where $\beta \approx 0.5$ is the loop feedback factor.

A simplified open loop equivalent half–circuit model network of the regulator is shown in 3.15. Transfer function of the regulator open loop is found as as

$$\frac{V_{out}}{V_i} = \frac{A_{d1}A_{d2}\left(1+\frac{s}{G4/C_c}\right)}{(1+sC_cg_{m1}R_LR_{out3})\left(1+\frac{sC_L}{g_{m1}G_2r_{o4}}\right)} \tag{3.10}$$

where,

$$R_{out3} \approx \frac{(g_{m9}r_{ds9}r_{rds11} + r_{ds9} + r_{ds11})(g_{m7}r_{ds7}r_{ds5} + r_{ds7} + r_{ds5})}{(g_{m9}r_{ds9}r_{rds11} + r_{ds9} + r_{ds11}) + (g_{m7}r_{ds7}r_{ds5} + r_{ds7} + r_{ds5})}$$

$$A_{d1} = g_{m2}R_{out3}$$

$$A_{d2} = g_{m1}R_L$$

Hence, the loop transfer function has one zero, ω_z, and two poles, ω_{p1} and ω_{p2},

$$\omega_z = \frac{G_4}{C_c} = \frac{g_{m9} + g_{ds9} + g_{ds11}}{C_c} \tag{3.11}$$

$$\omega_{p1} = \frac{1}{R_{out3}A_{d2}C_c} \tag{3.12}$$

$$\omega_{p2} = \frac{g_{m1}}{C_L} \tag{3.13}$$

As $\omega_{p2}, \omega_z \gg \omega_{p1}$, the unity gain bandwidth, ω_0 is set by $|H(s)| = 1$ as

$$\omega_0 = \frac{g_{m1}}{C_c} \tag{3.14}$$

The phase margin of this loop is approximated as

$$\begin{aligned} PM \approx & 180 + \tan^{-1}\frac{\omega_0}{\omega_z} - \tan^{-1}\frac{\omega_0}{\omega_{p1}} - \tan^{-1}\frac{\omega_0}{\omega_{p2}} \\ = & 180 + \tan^{-1}\frac{g_{m2}}{g_{m10} + g_{ds10} + g_{ds12}} \\ & - \tan^{-1}(g_{m2}R_{out3}A_{d2}) \\ & - \tan^{-1}\frac{g_{m2}C_L}{g_{m1}C_c} \end{aligned} \tag{3.15}$$

The phase margin is affected by input and output stage transconductance and by the values of the loading and compensation capacitance. Simulation of the open loop frequency response is displayed in Fig. 3.16. Simulations results indicate a phase margin of 52° , which is an acceptable value for the complete loop structure.

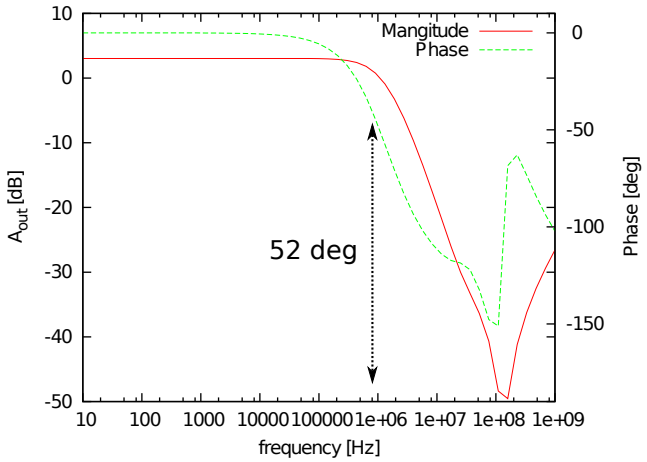


Figure 3.16: LDO regulator open loop simulation

3.4 Physical Design of LDO Loop

Layout of the LDO regulator loop is shown in Fig. 3.17. Critical sub-blocks of the two-stage amplifier are the differential pair and current mirrors, which must be precisely matched. Mismatch of the differential pair will increase the offset voltage of the op–amp. Mismatch of the NMOS current mirror will affect the DC biasing of the op–amp.

There is considerable variance for absolute resistance values in integrated circuit processes. Foundry documentation for 0.13 μm CMOS technology indicates that resistance values can vary by as much as 43% from the nominal value. However, integrated circuit devices can be very precisely matched. Physical design techniques, discussed in Chapter 5, enable the ratio of the two resistors to be within 1% tolerance [31].

The differential pair is interdigited and surrounded with dummy fingers. The complete differential pair block is then surrounded with a guard ring for noise isolation. Similarly, the current mirrors are arranged into interdigited structures and surrounded with dummy devices.

3.4.1 Op–Amp Characterization

Based on the methods presented in [22], important characteristics of the op–amp are extracted through post–layout simulations.

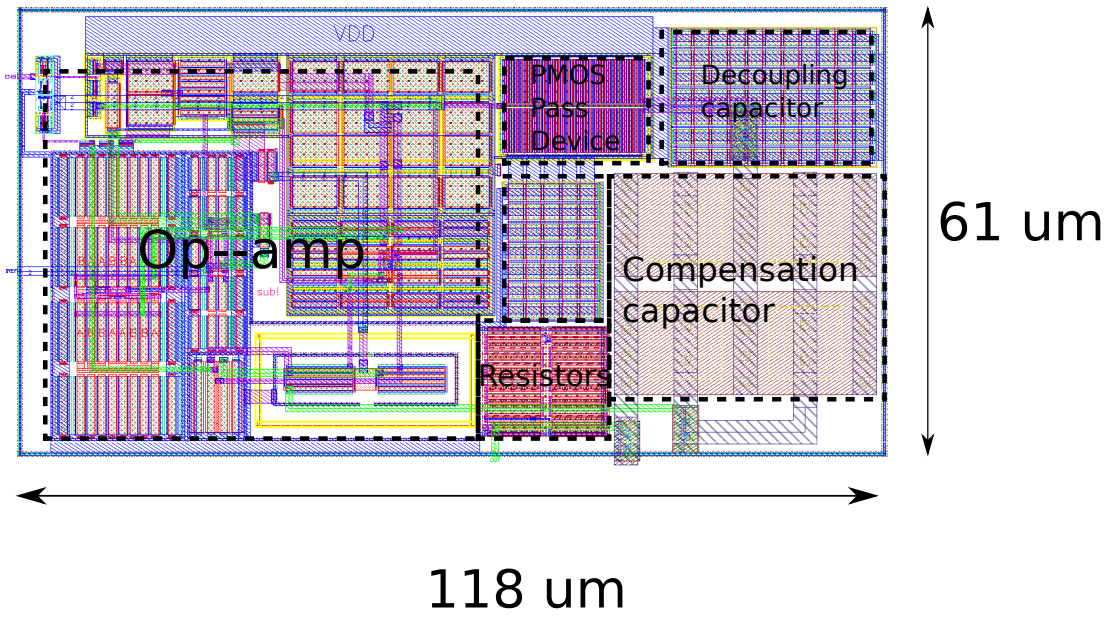


Figure 3.17: LDO regulator layout

Open Loop Frequency Response

The op–amp frequency response is important to the stability of the complete LDO loop. Phase margin of this op–amp will be the upper limit of the phase–margin of the complete loop. A schematic level simulation of the open loop frequency response is presented in section 3. Fig. 3.18 displays a post layout simulation result of the open loop gain and phase. Open loop DC gain is 47 dB and the phase margin is 75° .

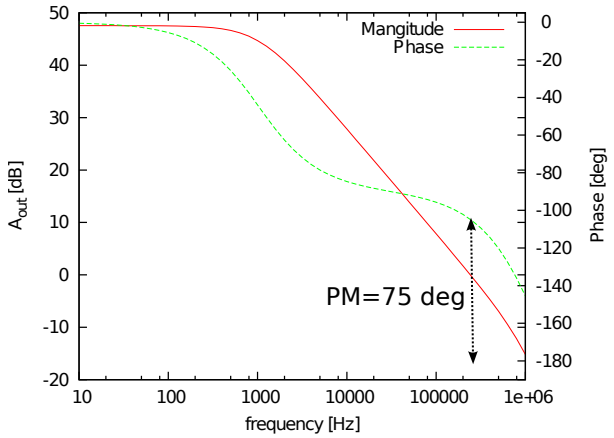


Figure 3.18: Folded cascode op–amp open loop frequency response

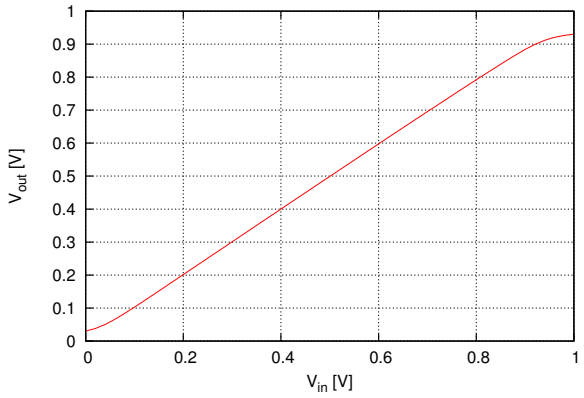


Figure 3.19: Folded cascode op–amp ICMR

Input Common Mode Range

Simulations of the input common mode range (ICMR) of the folded cascode op–amp is shown in Fig. 3.19 for a power supply of 1 V. ICMR characterizes the range of differential input voltages for which the op–amp has constant gain. When the op–amp is used to process an analog signal, ICMR indicates the maximum and minimum signal voltages to avoid distortion. However, ICMR is not of critical concern for this application, as non linearity of the gain does not affect DC operation of the LDO regulator.

The voltage swing of the op–amp for 1 V power supply is shown in Fig. 3.20. Output swing characterizes the range of output voltages that the op–amp can produce. Maximum and minimum limits of the current supply of the LDO regulator will be proportional to the output swing of the op–amp. For a LDO regulator with a PMOS pass device, the maximum current output occurs when the output of the error amplifier is at the lower supply rail, which is 0 V in this case. For a LDO regulator with PMOS pass device, the op–amp must be capable of producing an output voltage as low as the lower supply rail in order to increase the maximum current supply of the regulator. Minimum current supply of the op–amp is set by the maximum output voltage of the op–amp. As shown in Fig. 3.20, the folded cascode op–amp provides a minimum output voltage of 0 V and maximum output slightly lower than V_{DD}. This will enable the maximum LDO regulator output current to be limited only by the pass device width.

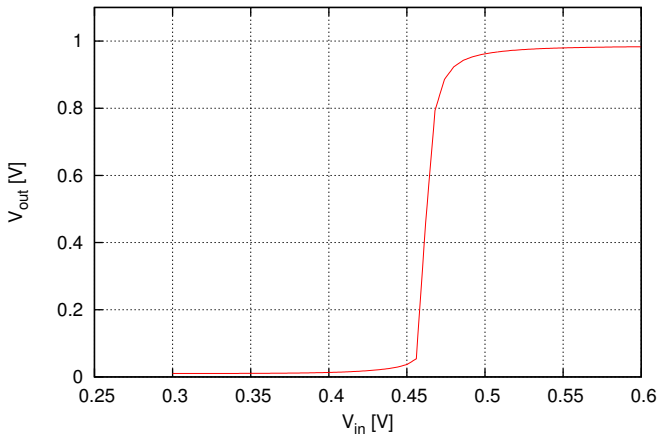


Figure 3.20: Folded cascode op–amp output swing

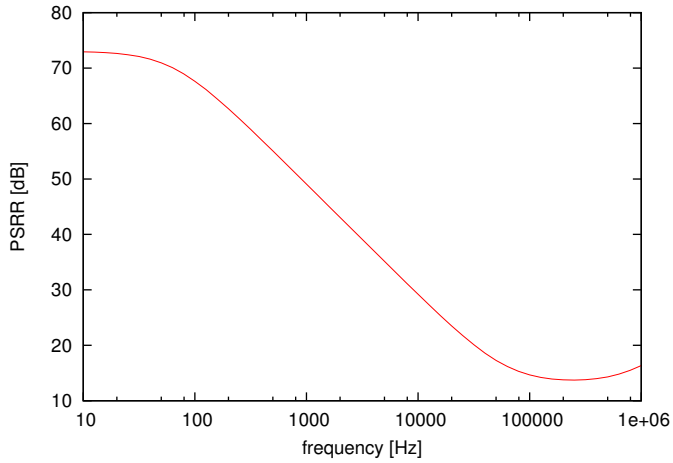


Figure 3.21: Post–layout Folded cascode op–amp power supply rejection ratio

Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is measured by superimposing an AC signal on the power supply rail and measuring the gain at the output with respect to the power supply signal. Frequency characteristics of power supply rejection ratio of the designed folded–cascode op–amp is plotted in Fig. 3.21. A considerably large PSRR of 72 dB is measured fro simulation results, which is desirable for improved power supply rejection of the LDO structure.

Folded Cascode Op–Amp Summary

Table 3.2 summarizes the characteristics of the folded–cascode op–amp design. Post–layout

Table 3.2: Post–layout folded cascode op–amp characterization

Parameter	Value
Open Loop DC Gain	37 dB
Gain Bandwidth	350 kHz
Phase Margin	81°
PSRR @ DC	72 dB
Output Range	0V to 1.2V
ICMR	0.1V to 1.1V

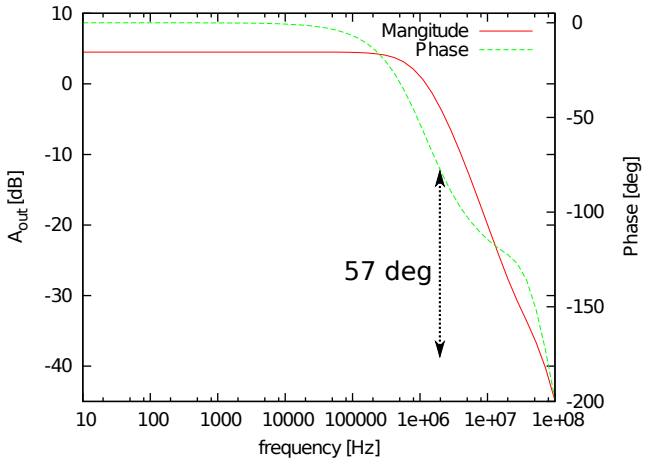


Figure 3.22: Post–layout LDO open loop frequency response

simulation of the LDO structure including the voltage reference is presented in the following subsections. A summary of the simulated LDO characteristics is listed in Table 3.2.

3.4.2 Open–Loop Response

Pre–layout open–loop simulation of the LDO regulator is shown in Fig. 3.16. Stability of the layout must also be verified post–layout, which will provide a more accurate characterization. Fig. 3.22 shows the post–layout open–loop response of the LDO regulator design. Post–layout simulated phase margin is 57°, compared to the schematic simulation of 52° . In this case, parasitic components in the layout unintentionally result in slightly improved phase margin.

3.4.3 Dropout Voltage

Fig. 3.23 shows a post–layout simulated DC characteristic of the LDO regulator structure. Operation of the LDO regulator is divided into three regions, as shown in Fig. 3.23. The LDO regulator should only be used in the regulating region, where the output voltage becomes constant regardless of variation in input voltage. If the LDO regulator operates in the dropout region, ripple from the regulator input will appear the output of the regulator. Input voltage must be sufficiently large in order for the regulator to operate in the regulating region.

Dropout voltage is the minimum difference between input and output voltage for which the regulator produces the specified value of regulated output voltage. When a LDO regulator operates in the dropout region, the pass device behaves as a resistor. Dropout voltage is expressed in terms of the on resistance of the PMOS pass device in dropout (R_{on}) [32].

$$V_{dropout} = I_o R_{on} \tag{3.16}$$

Dropout voltage is equivalently measured as

$$V_{dropout} = V_{out,d} - V_{out,reg} \tag{3.17}$$

where $V_{out,reg}$ is the intended regulator output voltage and $V_{out,d}$ is the minimum voltage at which the LDO operates as a regulator. From the curve of Fig. 3.23 dropout voltage of this regulator is measured as 340 mV.

3.4.4 Efficiency

Efficiency η is defined as the ratio of output and input power

$$\eta = \frac{P_{out}}{P_{in}} \tag{3.18}$$

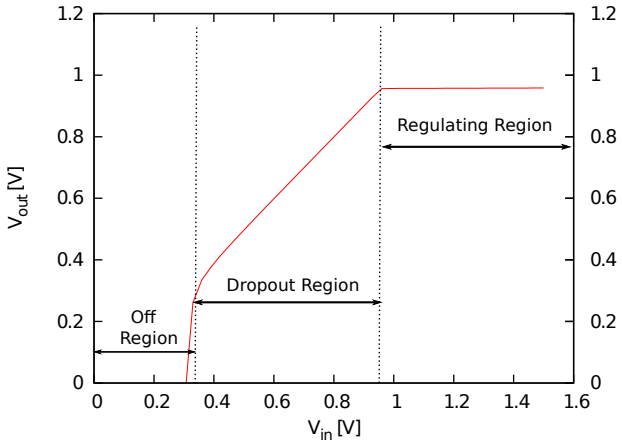


Figure 3.23: LDO regulator DC response

Efficiency of LDO regulators is limited by the quiescent current and dropout voltage. Quiescent current refers to current consumption of the LDO regulator for its own operation. By definition, the quiescent current is the difference between input and output current.

$$I_q = I_i - I_o \tag{3.19}$$

The quiescent current consists of bias currents for the bandgap reference, error amplifier, and feedback resistors. For a LDO regulator, equation (3.18) is expressed as

$$\eta = \frac{I_o V_o}{(I_o + I_q)V_i} \tag{3.20}$$

where V_o and V_i are the output and input voltage respectively. Quiescent current of the LDO regulator design is 10.5 μA.

Efficiency also depends on the input voltage and loading applied to the LDO. Efficiency of the regulator for increasing input power is shown in Fig. 3.24. As the input voltage rises the regulator efficiency decreases as the excess voltage difference between input and output must be dropped across the pass device.

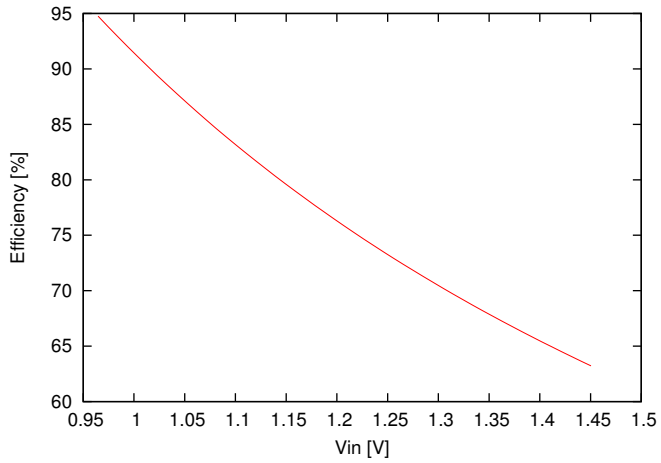


Figure 3.24: LDO regulator efficiency with 1kΩ load

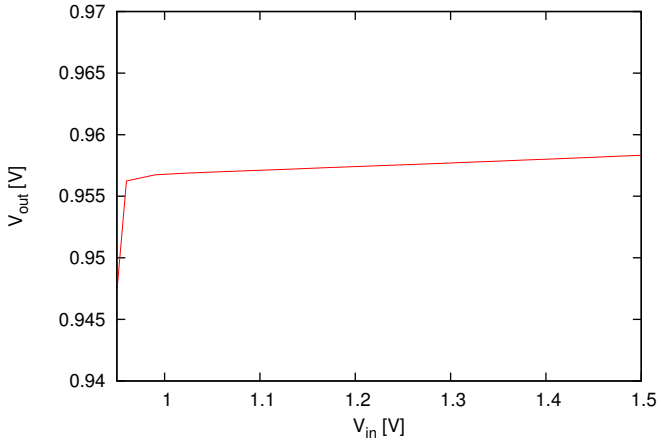


Figure 3.25: LDO Load Regulation

3.4.5 Line Regulation

Line regulation characterizes the sensitivity of the regulated output voltage to variation of the input voltage. Line regulation is typically expressed as

$$\textit{Line Regulation} = \frac{\Delta V_o}{\Delta V_i} \times 100\% \tag{3.21}$$

Line regulation is measured as the slope of output vs input voltage in the regulating region of operation. Post–layout simulation of the LDO operating in the regulating region is shown in Fig. 3.25. Line regulation is measured as 0.14% from the simulation. Increased open loop DC gain

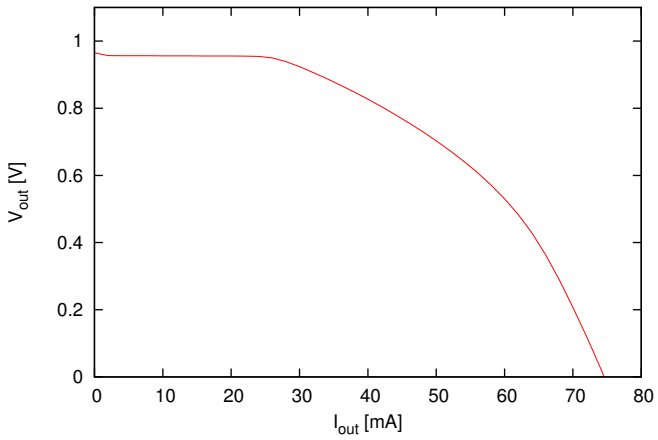


Figure 3.26: LDO Load Regulation

will increase line regulation, however inevitably at the cost of increased power consumption.

3.4.6 Load Regulation

Load regulation characterizes variation of the output voltage under varying load conditions.

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} \tag{3.22}$$

Load regulation is examined by loading the regulator with a current source and varying the load current. Fig. 3.26 shows the output for increasing load current. Regulated voltage drops off at output currents exceeding 20 mA. Considering that the power delivered by the regulator will be transferred across a wireless power transfer link, it is feasible that lass than 1 mW of power will delivered to the regulator. Thus, the load regulation results shown in Fig. 3.26 are sufficient for low power operation with output current lower than 20mA.

The effect of load regulation on the regulated output voltage is shown in Fig. 3.27. As the load current changes, there is momentary variation in the output voltage before returning to stable regulated DC. The increase in load current also results in a slight drop of the regulator output voltage. Higher load regulation reduces the ripple amplitude and decreases settling time of the transient response during variation in load current.

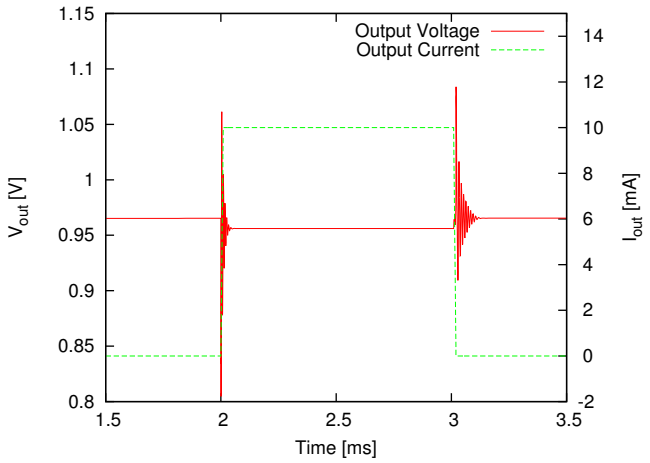


Figure 3.27: LDO Transient Load Regulation

3.4.7 Power Supply Rejection

Power supply rejection ratio (PSRR) of a regulator is the attenuation of ripple at the input. The simulated LDO power supply rejection is shown in Fig. 3.28. Variation of the regulator input voltage will be attenuated and superimposed on the regulated output voltage. Input voltage to the regulator will fluctuate as the received power of the wireless power transfer link fluctuates. DC PSRR of 48 dB, as shown in figure 4.13, indicates that low frequency noise due to variation of the input voltage is divided by a factor of 251 at the output. For example, 100 mV of variation at the input of the regulator would result in approximately 400 μV of variation on the regulated output voltage. This rejection of power supply noise is sufficient to provide a stable power supply rail.

3.5 Summary

In this chapter the design of a low–dropout regulator is presented. A basic overview of low–dropout regulator structures is discussed, and design of various op–amps structures are presented. Stability considerations and simulation results for design of the LDO loop are presented. The LDO structure including voltage reference circuit is characterized with extracted parasitic components. Parameters extracted from post–layout simulations are are listed in Table 3.3.

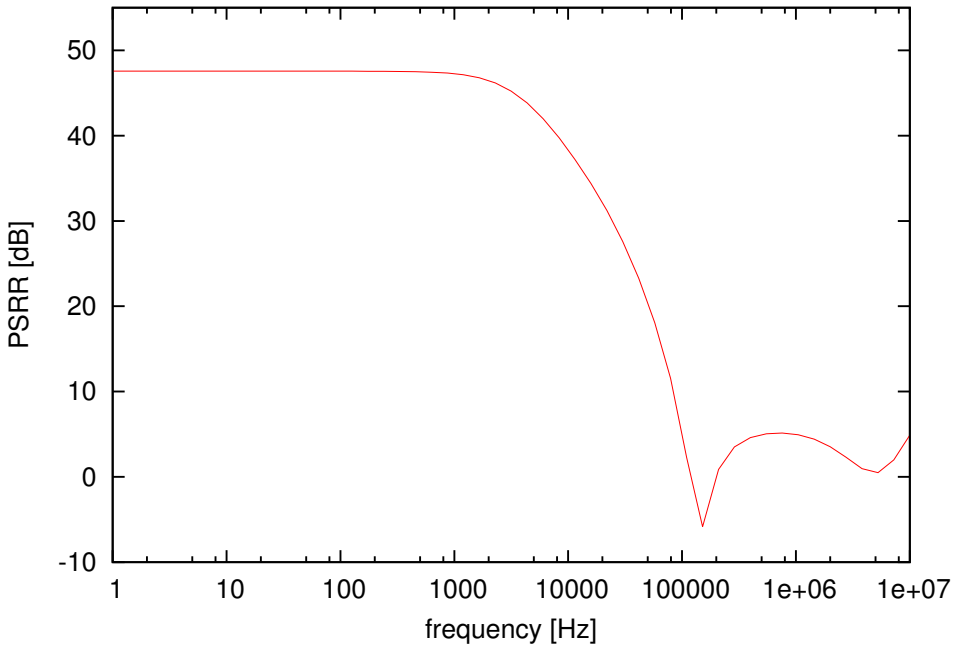


Figure 3.28: LDO power supply rejection ratio

Table 3.3: Performance of LDO regulator with voltage reference

Parameter	This work	[11]	[33]
CMOS technology	0.13 μm	0.18 μm	65nm
Quiescent current [μA]	10.5	28	80
Dropout [mV]	340	300	100
Output [V]	0.97	1	1 to 1.5
Line Regulation [%]	0.14	0.024	1.77
Load Regulation [mV/4mA]	1.16	0.7	3.2
Settling time [μs]	7.9	1.6	7.5
PSRR @1kHz [dB]	48	70	42

Chapter 4

Temperature Independent Reference

The linear regulator architecture presented in Chapter 3 is dependent on a voltage reference source. In this chapter a temperature independent voltage reference is designed to be included as an on–chip reference for the LDO regulator. This voltage reference must be low–power, as it will consume power from the output of the regulator. Output voltage of the reference is specified to be approximately the mid–point of the power supply rail, approximately 0.5V.

4.1 Background

Voltage references are required in many analog and mixed–signal systems. In addition to voltage and current regulators, circuits such as analog–to–digital converters and digital–to–analog converters rely on a stable and temperature independent voltage reference. In many LDO regulator implementations the reference voltage is provided from an off-chip source. In the case of an implantable biomedical device, it is important to minimize the size of system by integrating components on–chip towards the implementation of a single chip or single package system.

Electronic devices have nonlinear characteristics with respect to temperature. A quantity with a positive temperature dependence coefficient is termed proportional to absolute temperature (PTAT). Conversely, a negative temperature dependence is complementary to absolute temperature (CTAT). Summation of a PTAT and CTAT voltage in the correct proportions results

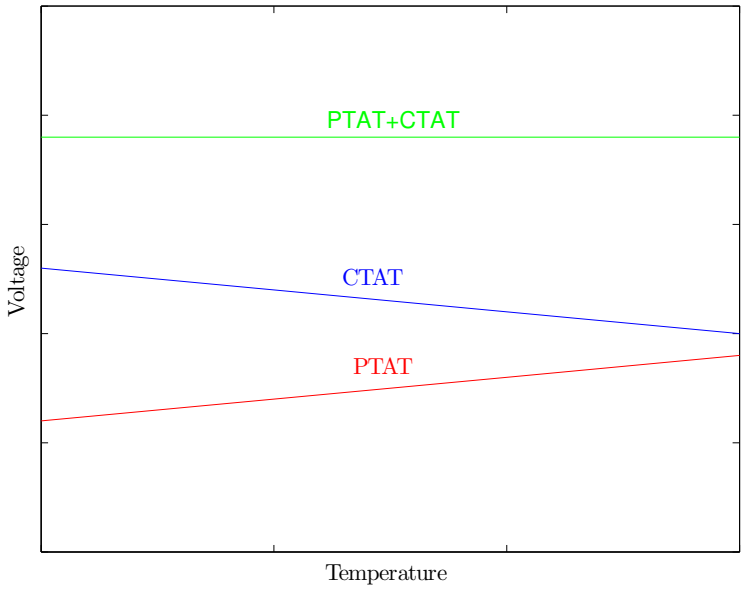


Figure 4.1: Generation of Temperature Independent Reference

in a voltage that is temperature independent, Fig. 4.1. In order to produce a temperature independent quantity, the CTAT and PTAT components must be equal in magnitude with opposite signs. These temperature dependant terms can be either voltage or current. It is important the PTAT and CTAT components are well characterized and designed to meet this specification to implement a high quality temperature independent reference.

In the literature it is convention to refer to any structure that utilizes the temperature characteristics of pn junction devices as a bandgap reference, although the bandgap reference circuit has little to do with the silicon bandgap [22]. The terms “bandgap reference” and “temperature insensitive reference” are used interchangeably. Early bandgap reference circuits produced a reference voltage at nominally the bandgap voltage of silicon [34]. Recent advancement in bandgap reference circuits are capable of generating reference voltages less than the silicon bandgap, often less than 1 V. The bandgap reference must be as low power as possible to achieve higher efficiency for the complete power harvesting front–end circuit.

A PTAT voltage can be generated using pn junction diode devices. The voltage drop V_D

across a diode is

$$V_D = V_t ln\left(\frac{I_D}{I_{SS}}\right) \tag{4.1}$$

Taking the voltage difference across two diodes,

$$\begin{aligned}\Delta V_D &= V_t ln\left(\frac{I_1}{I_{SS1}}\right) - V_t ln\left(\frac{I_2}{I_{SS2}}\right) \\ &= V_t ln\left(\frac{I_1}{I_2}\frac{I_{SS1}}{I_{SS2}}\right)\end{aligned}$$

Assuming the current in both diodes is equal,

$$\begin{aligned}\Delta V_D &= V_t ln\left(\frac{I_{SS1}}{I_{SS2}}\right) \\ &= V_t ln\left(\frac{A_1}{A_2}\right)\end{aligned}$$

$$= \frac{kT}{q} ln\left(\frac{A_1}{A_2}\right) \tag{4.2}$$

where k is Boltzmann's constant, T is temperature, q is the charge of an electron, and A is the size of the diode device. From (4.2) it is evident that if the ratio of the diode sizes, A_1/A_2 is not equal to 1, the voltage difference between the two diodes is proportional to absolute temperature.

A PTAT reference current is generated with the circuit of Fig. 4.2. Feedback to the op–amp forces the voltages at the two op–amp inputs to become equal. Assuming that the PMOS devices

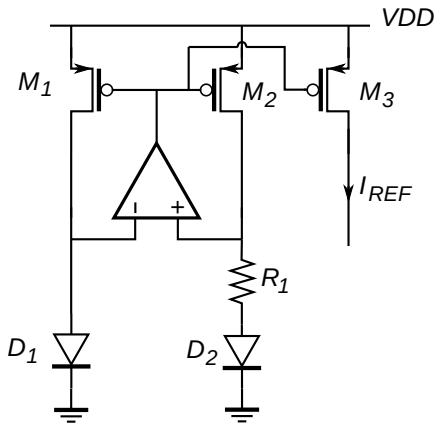


Figure 4.2: Generation of PTAT Current

are operating in saturation, the op–amp input voltages are found as follows.

$$
\begin{aligned}
V_{op} &= A_v(V_- - V_+) \\
I_1 &= \frac{2K'W}{L}(V_{sg} - V_{tp})^2 \\
I_1 &= \frac{2K'W}{L}(V_{DD} - A_v(V_- - V_+) - V_{tp})^2 \\
V_- &= V_+ + \frac{V_{DD} - \frac{L\sqrt{I_1}}{2K'W} - V_{tp}}{A_v}
\end{aligned}
$$

If the op–amp gain A_v is infinitely large then the op–amp input voltages will be equivalent. A practical op–amp gain is a value such as 30 dB, which would results in an offset of approximately 3% between the two op–amp input voltages.

Output voltage of the op–amp is converted to branch currents by the PMOS devices M_1 and M_2. The PTAT voltage difference of the diodes is dropped across the resistor.

$$
\begin{aligned}
V_+ = V_- &= V_{D1} \\
V_- &= V_{D2} + V_{R1} \\
V_{D1} &= V_{D2} + V_{R1} \\
V_{D1} - V_{D2} &= V_{R1} = V_{PTAT}
\end{aligned}
$$

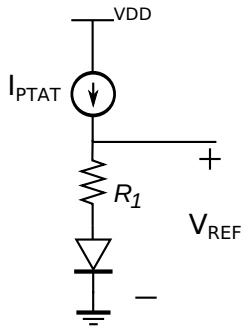


Figure 4.3: Generation of Temperature Independent Reference

Assuming that R_1 is temperature independent, then the voltage across R_1 is PTAT.

$$I_{PTAT'} = \frac{V_{PTAT}}{R_1} \tag{4.3}$$

A real resistor will have temperature dependence, so the current is labelled pseudo-PTAT, denoted by the prime in $I_{PTAT'}$. A true PTAT voltage can be recovered by passing the pseudo-PTAT current through a resistance with an identical temperature sensitivity as the resistor in the PTAT current generating circuit.

A temperature independent reference is implemented by the diagram shown in Fig. 4.3. When a PTAT voltage is passed through a resistor, the resulting voltage across the resistor is also PTAT. It can be found that the voltage of a diode has a CTAT characteristic [22]. Summation of the PTAT and CTAT voltages with the temperature coefficients designed in the correct proportions results in a temperature independent voltage. The reference voltage of the circuit shown in Fig. 4.3 is given by,

$$V_{REF} = V_{PTAT} + V_{CTAT} = I_{PTAT}R + V_D$$

4.1.1 Conventional Bandgap Reference Circuits

A series bandgap reference is implemented by the circuit of Fig. 4.4 [35]. A diode is not available in 0.13 μm CMOS, however a pnp BJT device is supported. The pn junction is implemented

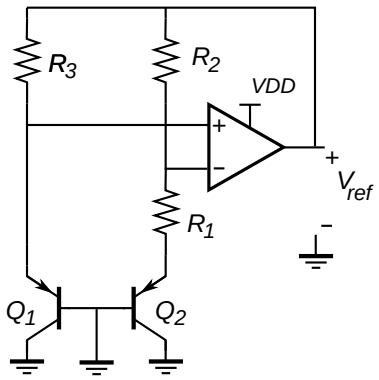


Figure 4.4: Bandgap Reference circuit

with a diode connected BJT device. Neglecting the offset voltage of the op–amp, the reference voltage is found as,

$$V_{REF} = V_{EB2} + I_2 R_2 = V_{EB2} + V_{R1}\left(\frac{R_2}{R_1}\right) \tag{4.4}$$

Substituting the PTAT voltage across R_1

$$V_{REF} = V_{EB2} + \left(\frac{kTR_2}{qR_1}\right) ln\left(\frac{R_2 A_{E1}}{R_2 A_{E2}}\right) \tag{4.5}$$

The temperature coefficients are determined by the ratios of BJT geometry and resistor values. If the input offset V_{os} of the op–amp is nonzero, equation (4.5) becomes [21]

$$V_{REF} = V_{EB2} + \left(\frac{kTR_2}{qR_1}\right) ln\left[\frac{R_2 A_{E1}}{R_2 A_{E2}}\left(1 - \frac{V_{os}}{I_1 R_2}\right)\right] \tag{4.6}$$

Another implementation of a series bandgap reference is shown in Fig. 4.5 [21]. This design is based on the PTAT circuit that was previously presented. A PTAT current is mirrored into the branch through a resistor and diode connected BJT. The output voltage is the sum of the PTAT voltage across the resistor and the CTAT voltage across the diode. As noted previously,

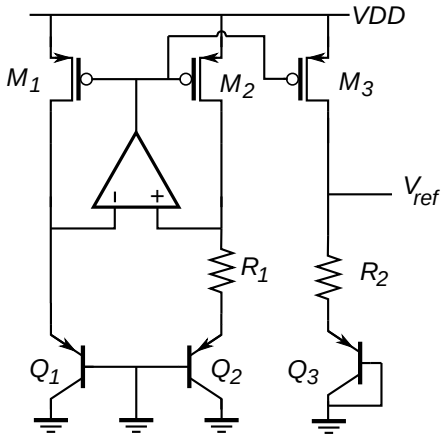


Figure 4.5: Conventional Bandgap Reference Circuit

if the temperature dependence of the two resistors are identical then the nonlinear temperature dependence of the PTAT current is cancelled in the PTAT voltage. The output voltage of this bandgap reference is

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1}\frac{kT}{q}ln(N) \tag{4.7}$$

Where N is the ratio of emitter area of Q_2 to Q_1. Temperature sensitivity of this reference circuit is,

$$\frac{\partial}{\partial T}V_{REF} = \frac{\partial}{\partial T}V_{BE3} + \frac{R_2}{R_1}\frac{k}{q}ln(N) \tag{4.8}$$

It can be seen from equation 4.8 that the design of Q_3 and the PTAT current are arbitrary as long as the temperature coefficients are equal in magnitude.

The diode voltage drop is approximately 0.7 V, with the voltage across the resistor being $I_{PTAT}R_2$. The series voltage drop across the resistor and diode connected BJT results in voltage drop that is larger than the target specification. A bandgap reference circuit structure that will generate a lower output voltage is preferable.

4.1.2 Subthreshold CMOS Voltage References

Simplified models of MOS transistors assume that there is zero drain current when the gate–source voltage is below the threshold voltage. However, MOS devices operating in the subthreshold region have a measurable drain current that is of particular significance to analog and mixed–signal design [36]. Thorough analysis of MOS transistors in weak and moderate inversion are presented in [36] and [37].

In the subthreshold region of operation, MOS transistors have an exponential characteristic reminiscent to that of bipolar transistors [37]. MOS transistors operating in weak inversion can be used to produce a low–voltage temperature independent reference [38].

Using weak inversion devices would enable temperature independent references formed using purely CMOS devices when diode or bipolar devices are not available. A subthreshold CMOS reference would be well suited to using a low power supply voltage, which would reduce the power consumption of the voltage reference. In this application the power supply will be approximately 1V and can not be made lower, thus the weak–inversion design would not be well suited.

4.2 Proposed Bandgap Reference Circuit

The proposed temperature insensitive reference is shown in Fig. 4.6 [28] The PTAT current generating circuit is a modified form of Fig. 4.2 with BJT devices in place of diodes and cascoded PMOS current mirror. The high swing cascode current mirror provides increased precision for matching the currents and increases the power supply rejection ratio.

The proposed CMOS temperature independent reference is based on the complementary to absolute temperature response of PMOS devices. A PTAT current is generated by the aforementioned PTAT circuit, and the CTAT response of the PMOS device results in a nominally temperature independent voltage.

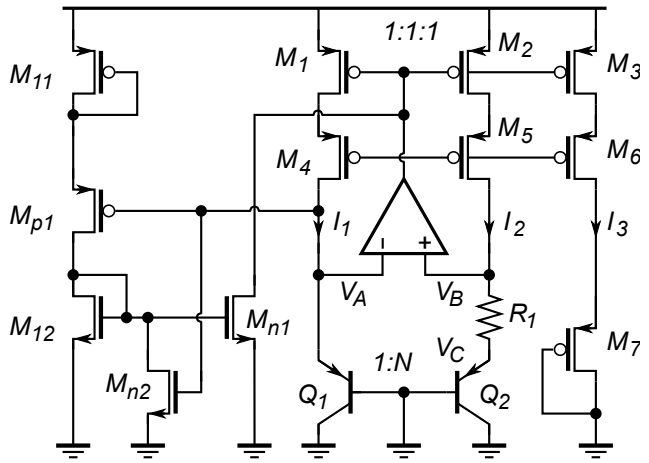


Figure 4.6: Temperature Independent Reference Circuit

The voltage across a diode connected PMOS device is given by

$$|V_{GSp}| = |V_{tp}| + \sqrt{\frac{2I_D}{\mu_p C_{ox}(W/L)}} \tag{4.9}$$

where $|V_{tp}|$ is the PMOS threshold voltage, μ_p is the carrier mobility, C_{ox} is the unit gate oxide capacitance, I_D is the drain current, and (W/L) is the device width to length ratio.

Fig. 4.7 shows the threshold voltage of the device, $|V_{th}|$ across temperature variation. This plot is extracted from the foundry provided BSIM4 model of the device. From these device characteristics it is determined that PMOS threshold voltage temperature dependence is linear with slope of approximately -0.785 $mV/^\circ C$.

The temperature dependence of the second term in (4.9) is nonlinear. In order to cancel the temperature dependence of this term, a curvature correction circuit would be required. A curvature correction circuit would increase power consumption, so a trade–off between accuracy and power consumption must be made. A variation this small is acceptable in this design, particularly since the temperature variation that the implantable device will undergo is very small. Curvature correction circuitry is not implemented in this design in order to minimize the power consumption.

Core body temperature of a mammal is approximately 37° C, thus the temperature coefficient

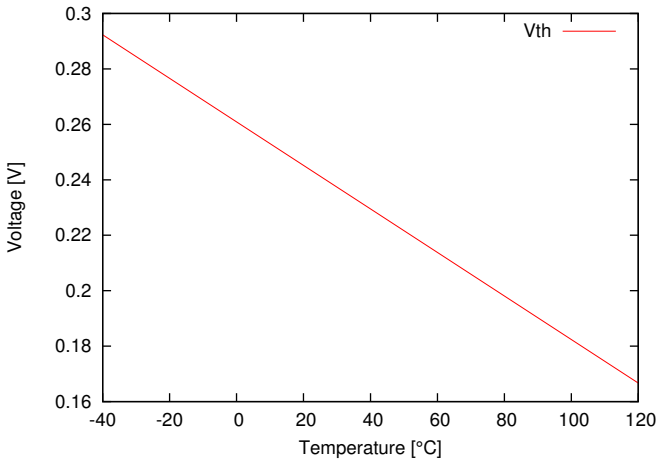


Figure 4.7: PMOS threshold voltage temperature dependence

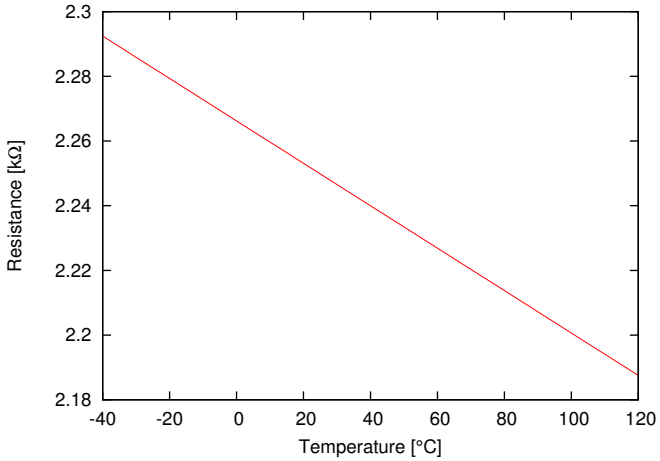


Figure 4.8: Poly resistor temperature dependence

of the curved term is taken at this temperature to minimize curvature in the anticipated range of operating temperatures.

For a given W/L, the negative temperature sensitivity of the PMOS threshold voltage V_{tp} is then cancelled with the positive temperature coefficient of the PTAT current. Temperature coefficient of the PTAT current is determined by the dimensions of the BJT devices and the resistance R_1. The bandgap resistor is implemented with the p-type poly resistor, as it has the smallest temperature dependency of the resistors available in 0.13 μm technology. Temperature dependence of the resistor is measured as 0.625 Ω/° C from the simulation result shown in Fig. 4.8.

The PTAT circuit structure of Fig. 4.6 is based on an op–amp which forces the PTAT voltage drop across the resistor. The op–amp specification is a trade–off between power consumption and DC gain. High DC gain will reduce the offset between the two input nodes in the closed loop configuration. Gain bandwidth of the op–amp can be fairly narrow since it is intended to operate at DC. Most importantly, the power consumption of this op–amp must be as as small as reasonably possible.

It is possible that the bandgap reference is powered from the output of the LDO regulator. The output of the LDO regulator will be between 0.9 V to 1 V, thus the op–amp be capable of operating with a supply voltage as low as 0.9 V. Cascoded op–amp structures require increased overhead to keep devices in saturation. For a low supply overhead, there must be a minimal number of stacked devices. The two–stage op–amp topology is selected for the error amplifier of the PTAT circuit. The classic miller compensated two–stage op–amp is discussed briefly in Section 3.2. The two–stage op–amp is designed with a small biasing current to reduce power consumption.

As discussed in Chapter 3, PMOS input devices offer several advantages but have increased thermal noise in comparison to NMOS devices. NMOS input devices are selected for decreased temperature sensitivity.

4.3 Startup Circuit

The op–amp based PTAT circuit has two stable states of operation, when the voltages V_A and V_B are zero, and when they settle to the desired nonzero value. When the circuit settles to a state where the voltages and current are zero, the startup circuit forces the PTAT circuit to turn on.

A low voltage start–up circuit, Fig. 4.9, is designed to provide current to the PTAT during power–up. The initial condition is that BJT devices have zero collector currents, therefore op–amp input nodes are at ground level. The switch PMOS M_2 is on while the NMOS switch M_4 is off. M_2 turns on another NMOS switch M_5. Consequently, M_5 pulls the node V_p to ground

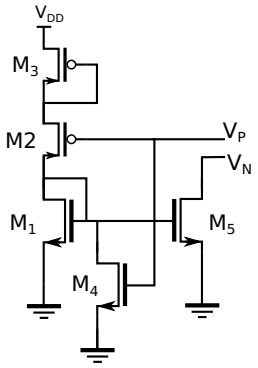


Figure 4.9: Bandgap reference startup circuit

and turns on the PMOS current mirrors. The cascoded devices in the mirrors are biased from the supply rail, so they are on shortly after the power is up. The initial startup current is injected into $Q1$ and $Q2$, which progressively increases voltages at nodes V_A and V_B. The settled voltage at VA is between 0.5 V to 0.8 V over the full temperature range. It turns on M_4 followed by the potential at the M_5 gate being pulled to the ground. Hence, the start–up circuit is disconnected from the PTAT circuit. At the same time, M_2 is sized to be off after V_A settles, therefore it breaks the DC current path in the voltage divider.

Once the PTAT circuit reaches the desired steady state the startup circuit is effectively off, drawing approximately 4nA of current.

4.4 Physical Design

4.4.1 Two–Stage Op–Amp

As discussed in the previous sections, the bandgap reference structure design is based on an error op–amp with feedback to force two nodes to the same voltage. Critical sub–blocks of the op–amp are the differential pair and current mirrors. Layout techniques for matching of devices are presented in Chapter 5. The two–stage op–amp layout contains four major MOS device sub–blocks: differential pair, PMOS current mirror, NMOS current mirror, and biasing circuitry.

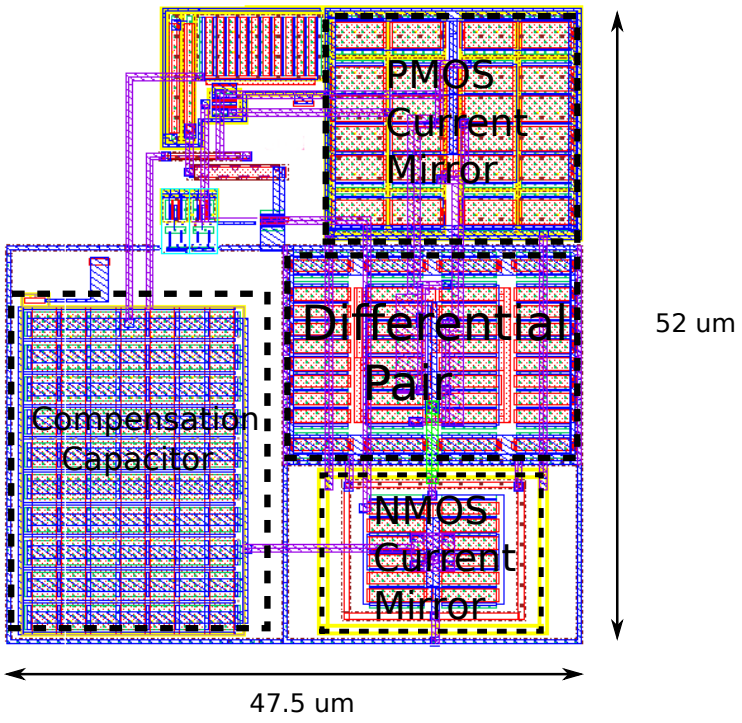


Figure 4.10: Two–stage op–amp layout

4.4.2 Op–amp characterization

The characteristics of this op–amp are extracted using the same techniques presented in section 3.4.1 Chapter 3. Table 4.1 summarizes the characteristics of this op–amp from post–layout simulation. Most importantly, the op–amp has low power consumption, operating at a quiescent supply current of 929nA.

Table 4.1: Two–stage op–amp post–layout characterization

Specification	**Simulation result**
Supply Current	929nA
Open Loop DC Gain	33 dB
Gain Bandwidth	44 kHz
Phase Margin	83 °
PSRR	62 dB
Output Range	629 μ — 1.19V
ICMR	0 to 1.17V

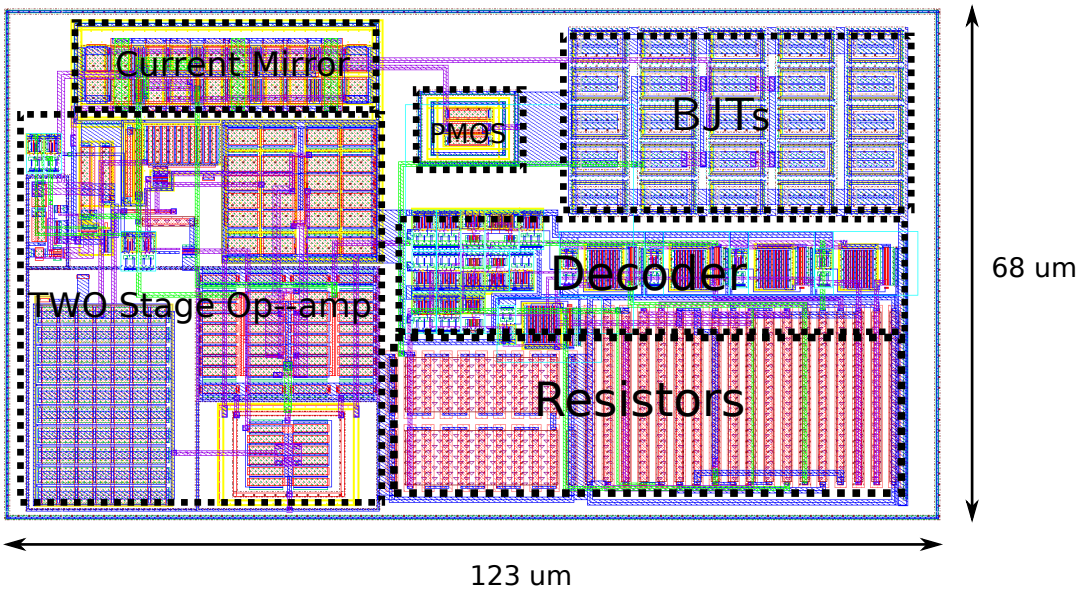


Figure 4.11: Temperature independent voltage reference layout

4.5 Top–Level Temperature Independent Reference Layout

The top the level layout of the temperature independent layout circuit is shown in Fig. 4.11. Layout blocks are arranged so as to make signal interconnects as short as possible. The cascoded current source of the PTAT circuit is intergidited in a common centroid structure with dummy devices at the edges. The PMOS device at the output is surrounded by dummy devices to prevent over–etching, and surrounded by a guardring for noise isolation.

4.5.1 Power Supply Characteristics

The output voltage of the bandgap reference across different power supply voltages is shown in Fig. 4.12. The minimum power supply voltage for proper operation of the bandgap reference is approximately 0.9 V.

Power supply rejection ratio (PSRR) of the reference voltage is displayed in Fig. 4.13. Variation on the power supply rail of the bandgap reference will be attenuated and superimposed on the reference voltage. DC PSRR of 79 dB, as shown in figure 4.13, indicates that low frequency noise on the power supply rail is divided by a factor of 8912 at the output.

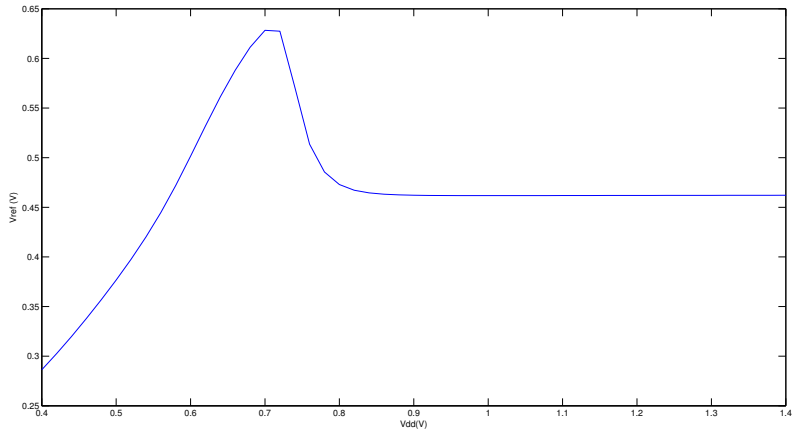


Figure 4.12: Bandgap Reference Power Supply Dependence

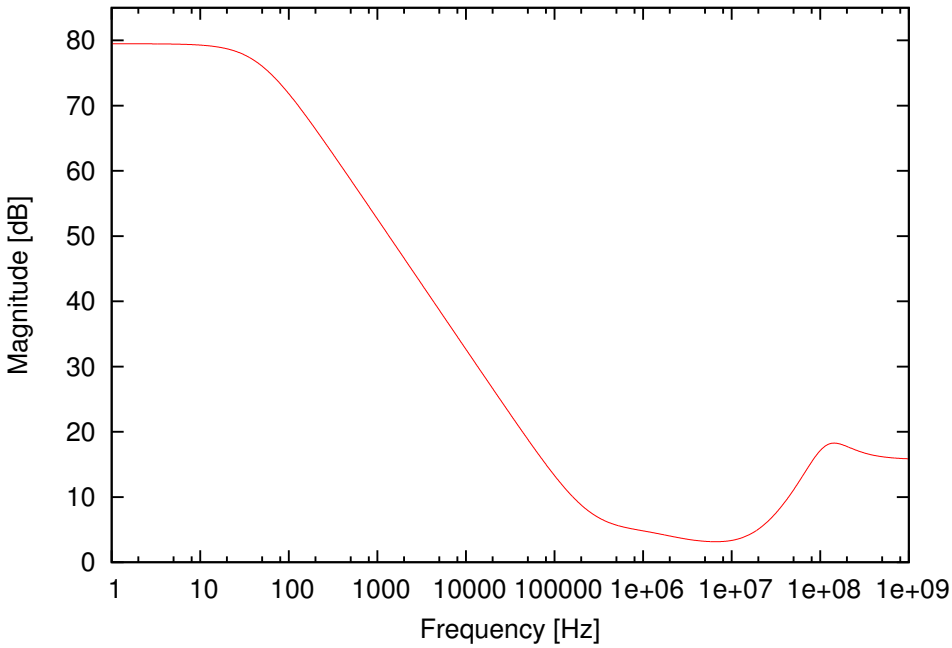


Figure 4.13: Bandgap Reference Power Supply Rejection

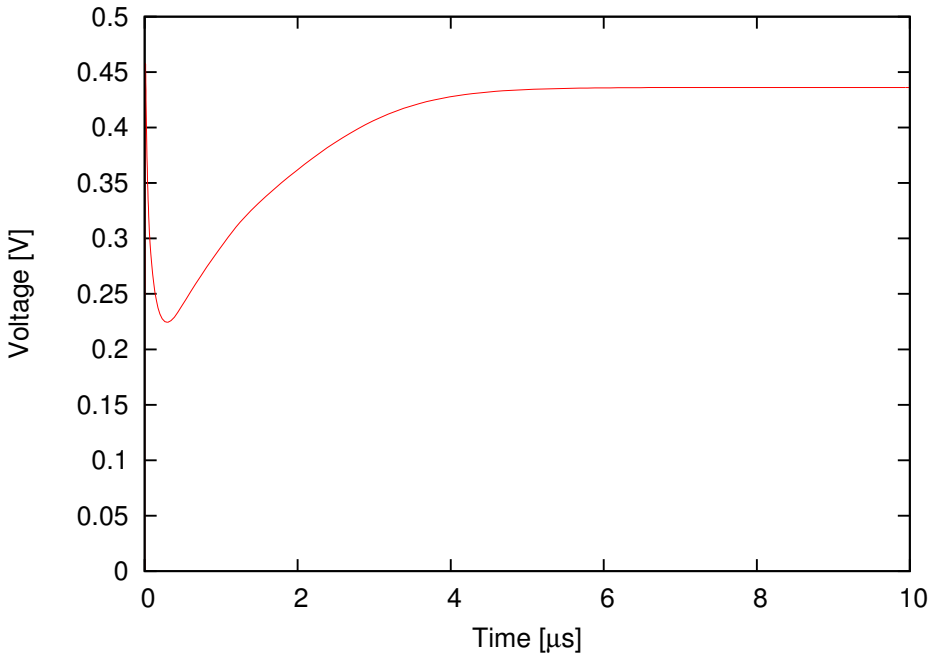


Figure 4.14: Output voltage startup

When a circuit is powered on there is a gradual rise in the voltage until it settles at the intended operating region. Transient response of the bandgap reference for a power supply with a rise time of 100 ps is shown in Fig. 4.14. Settling time of the output is approximately 5 μs. The settling time is related to the settling of the op–amp and impulse applied by the startup circuit.

When the circuit is powered on, the power supply rail raises gradually from zero to the nominal supply voltage. The bandgap reference circuit will require activation of the startup circuit in order to settle properly to the desired state of operation. The transient response of the reference voltage at the output of the regulator during startup is of interest in system level design, as this will dictate the startup behaviour of any blocks dependent on the bandgap reference. Power supply consumption of the circuit during startup transience is also of interest.

Transient simulation of current consumption with various power supply rise time is shown in Fig. 4.15. The current consumption of the startup sub–circuit only is shown in Fig. 4.16. Current consumption of the startup sub–circuit drops to 9nA at 50ns after the power supply begins to ramp–up. The transient current consumption plots of figures 4.15 and 4.16 are plotted on log–lin

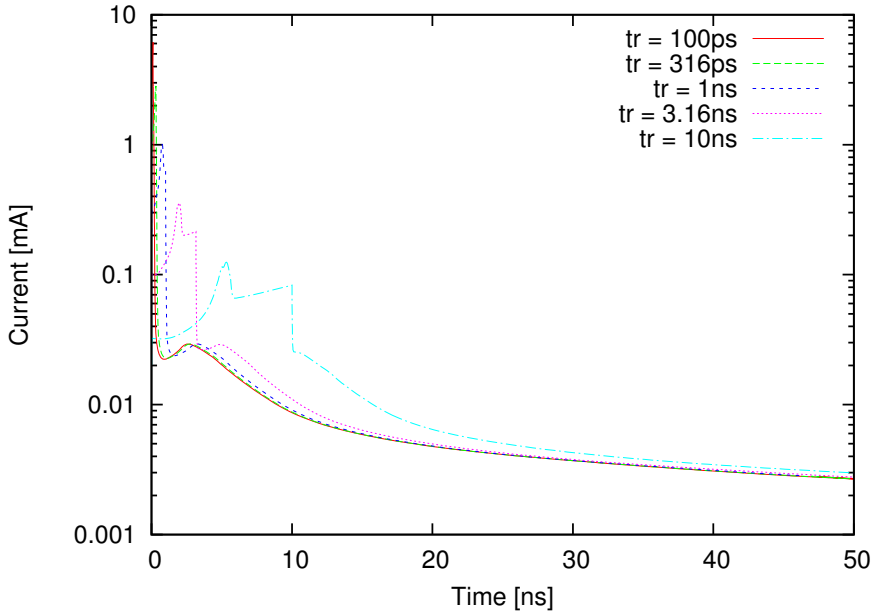


Figure 4.15: Bandgap reference startup current

axes to show the range of current consumption between transience and settled operation.

4.5.2 Temperature Curvature

Non–linearity in component temperature responses results in a slight non–linearity in the output voltage. Post–layout simulation of reference voltage is displayed in Fig. 4.17. Pre– and post–layout simulation results for the temperature curvature of the bandgap reference are identical. The temperature curvature is designed to have a local minimum at around 37° C, which is approximately the internal temperature of the implant subject.

4.5.3 Temperature Independent Reference Characterization

Table 4.2 summarizes the characteristics of the temperature independent reference design in comparison to similar implementations presented in the literature. Tradeoffs made in the design of the bandgap reference result in a decreased performance of certain specifications. However, the primary goal of this design is low–power. The power consumption of the design is approximately 4 μA, which is considerably lower than comparable implementations presented in the

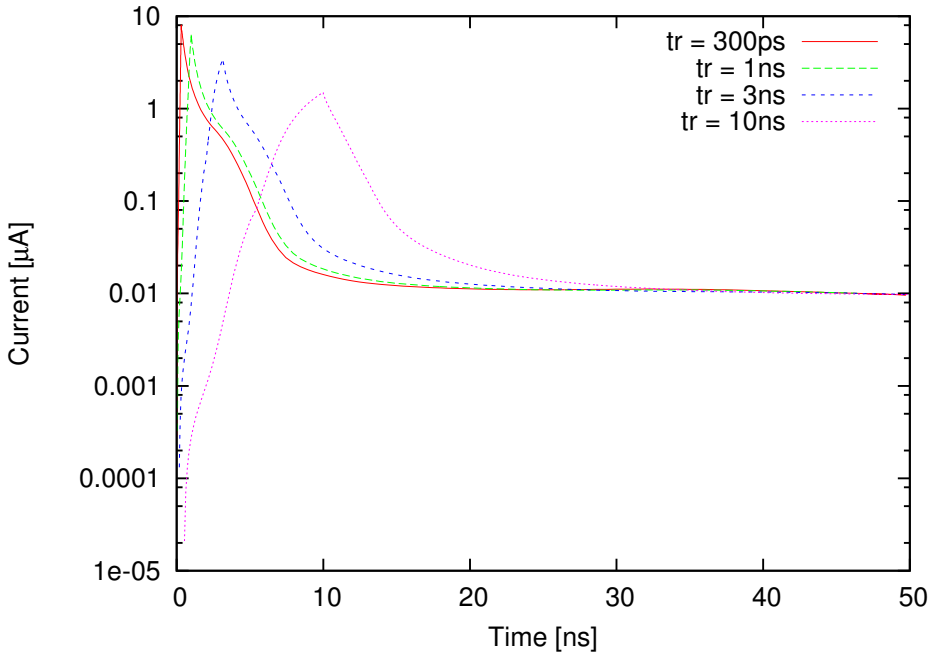


Figure 4.16: Bandgap reference startup circuit current

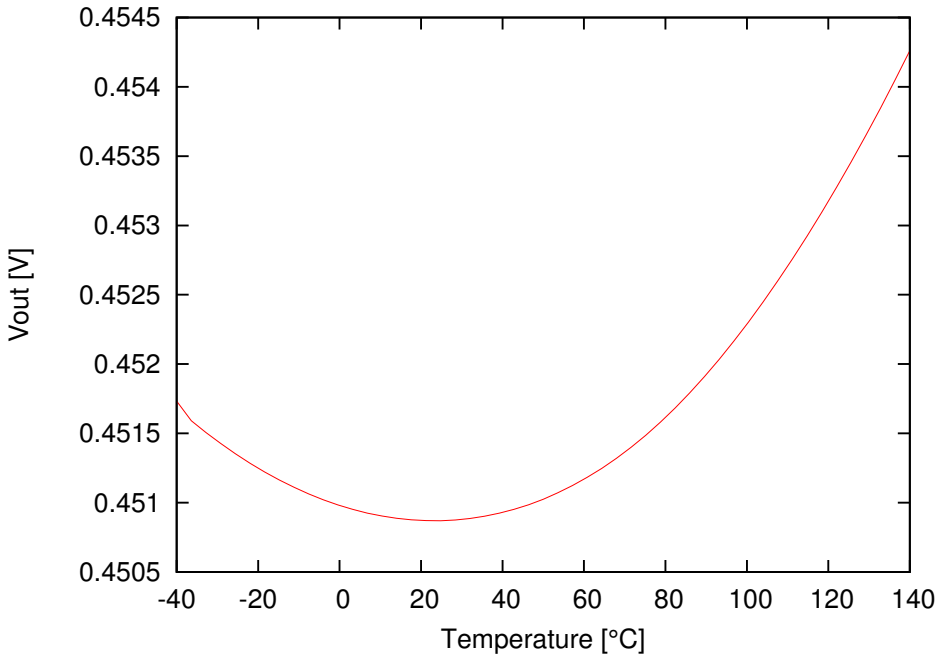


Figure 4.17: Temperature Response of Voltage Reference

Table 4.2: Bandgap Reference post–layout characterization

Parameter	This work	[14]	[33]
CMOS technology	$0.13\mu m$	$0.18\mu m$	65nm
Minimum Power supply [V]	0.9	1	1
Power supply current [μA]	4	29.5	38.2
Output voltage [V]	0.47	0.7395	0.67
Temperature coefficient [ppm/° C]	24.7	6.64	-
PSRR [dB]	79	52	46

literature. Load regulation is sometimes characterized for bandgap reference designs, however it is inconsequential in this application since the bandgap reference will always drive a high impedance load.

4.6 Additional Applications of Bandgap References

The bandgap reference is used to generate the reference voltage of the LDO regulator circuit. In addition to the LDO regulator presented in the previous chapter, bandgap reference circuits are useful for generating reference voltages and currents on–chip. Biasing of analog circuitry such as analog to digital converters require a temperature insensitive reference voltage.

A simple op–amp based regulator, Fig. 4.18, can be used to scale the reference voltage to any value [26]. This block is similar to the LDO regulator, but lacking the pass element. Output voltage of this simple regulator is

$$V_{REF,out} = V_{REF,in}\left(\frac{R_2}{R_1 + R_2}\right) \tag{4.10}$$

This structure is suitable for low impedance loads such as an ADC or op–amp biasing. The typical operation transconductance amplifier would not be suitable for driving a small resistive load. If the load is low impedance then a structure such as the LDO regulator is more capable of providing high current and improved load regulation.

A reference current can be produced from the reference voltage with the circuits shown in

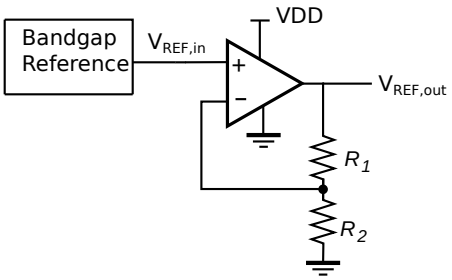


Figure 4.18: Arbitrary Voltage Reference generation

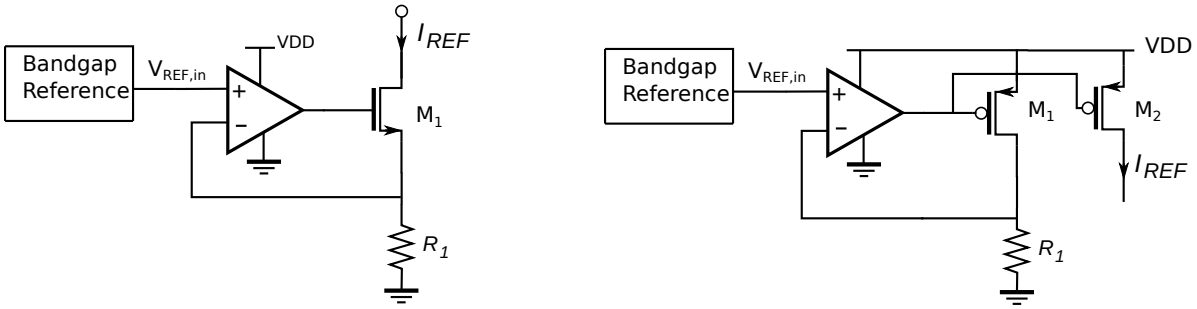


Figure 4.19: Voltage to current reference structures: a) NMOS current sink, b) PMOS current source

Fig. 4.19. For both of the circuits, negative feedback will cause the voltage across R_1 to become equal to the reference voltage, thus the output current will be

$$I_{REF} = \frac{V_{REF}}{R_1} \tag{4.11}$$

The MOS devices used in generating the reference current must be in saturation in order to produce the correct reference current. Overhead voltage required for the NMOS current sink device of Fig. 4.19a is

$$V_{out} > V_{REF} + V_{GS1} - V_{TN} \tag{4.12}$$

For a PMOS current mirror such as Fig. 4.19b the required overhead voltage is $V_{GS} - V_{TP}$

4.7 Summary

In this chapter the design of a CMOS temperature independent reference is presented. Principles of controlled temperature coefficient circuits are presented and a conventional bandgap reference structure is presented. A low–voltage CMOS temperature insensitive reference structure is proposed and design of the components is discussed. Physical design of the bandgap reference is discussed and post–layout simulations results are presented. The bandgap reference is designed for low power consumption, with supply current of 4 μA at a minimum power supply voltage of 0.9 V. The output reference voltage is generated with the use of a MOS device in the output stage, which enables the generation of a low reference voltage of approximately 0.45 V.

Chapter 5

Physical Design

In the previous chapters design of the proposed analog circuits is presented. Electrical characteristics of analog integrated circuits are highly dependent on the physical implementation of the circuit. This is because in the schematic design of analog circuits there are many assumptions that are made about device characteristics. For instance, it is assumed that the electrical properties of certain pairs of devices are very closely matched. The physical design of an analog integrated circuit must be designed meticulously to match the intended device characteristics.

Physical design of integrated circuits is the implementation and placement of devices on the semiconductor die. Physical design is also referred to as IC layout or IC mask design [39]. Design of the IC layout using CAD tools results in a set of photo-lithography masks that will be used to pattern the die and define the feature geometry on the various layers and regions.

The regulator block layout is designed to be integrated into a mixed–signal ASIC for future biomedical implantable devices. Each layout block presented is implemented as a square–shaped unit that will be integrated into future chip designs.

The resistance and current carrying capacity of each metal layer is specified in foundry provided documentation. It is good practice to to use larger than minimum interconnect sizes to reduce interconnect resistance, and to separate interconnects farther apart than the minimum spacing to increase reliability and yield.

Reliability must also be considered in analog layout to prevent failure mechanisms such as latchup. In this chapter, techniques for layout design for preserving circuit characteristics are presented. Layout issues and techniques applied to designing the power harvesting front–end are discussed. Layout designs presented are based on $0.13\mu m$ CMOS, which is a bulk CMOS process.

5.1 Layout issues

5.1.1 Matching Techniques

A common assumption in the design of analog integrated circuits is that components are well matched. This means that the characteristics of two or more devices are assumed to be identical, or have very small deviation. In practice it is possible to have devices matched to within 0.1% variation, however this requires proper application of layout matching techniques. It is suggested that for op–amp and bandgap reference design that moderate matching for approximately ±1% mismatch is required [31].

For devices to be precisely matched, they must be placed in close proximity. There are several reasons why devices that should be matched must be placed close together. There is random mismatch in components due to microscopic irregularities caused by the fabrication process, As devices are farther separated there will be process variance such dopant density and gate oxide thickness. Increasing the size of devices also reduces the effect of random mismatch [22].

The silicon die has stress gradients that are a function of space. This means that the mechanical stress on the die varies at different points and results in slightly varying characteristics. Separating devices that should be matched may introduce mismatch due to the stress gradients. Similar to stress, there will be a temperature gradient across the die. If devices are at different temperatures during operation, mismatch will be introduced due to temperature sensitivity.

In addition to being in close proximity, matched devices should also be in identical orienta-

tion. This is because processing steps such as etching are highly dependant on direction.

It is common in IC technologies that a device is very wide or very long. Excessively wide or long devices are impractical in layout implementation. A mos device that is excessively long or wide will have increased gate resistance and diffusion capacitance. To improve performance, large mos devices are separated into multiple sub–devices, or “fingers”. Fingers are connected in parallel for a wide device and in series for a long device. Arranging the array of fingers into a square shape has the added benefit of making the layout more space efficient.

It is particularly important to break devices into sub–devices, or “fingers”, when devices must be matched. The fingers of matched devices are interdigited, which means that the sub–devices are dispersed in an array of interleaved devices. If there is a gradient in doping concentration, mismatch of devices is minimized if device fingers are dispersed as much as possible and in a pattern that is symmetric. Separating devices into fingers and the technique of interdigiting can be applied to resistor and mos transistor layout.

5.1.2 Common Centroid Layout

In addition to using unit length devices and interdigiting, the pattern of device placement will affect mismatch. Placing devices centred at a common point reduces the effects of linear gradients due to thermal or process effects.

Basic rules for common centroid layout of resistors and MOS devices are presented by Hastings [31]. Some of these rules are summarized as

- Coincidence: Matched devices must have a common central point
- Symmetry: The component matrix must be both vertically and horizontally symmetrical
- Dispersion: devices must be dispersed as much as possible in the matrix, while still preserving symmetry
- Compactness: The matrix should be as compact as possible, ideally in a square shape

- Orientation: Matched devices must have same orientation

Depending on the number of devices and the sizing of each device, an appropriate common centroid matching pattern is chosen. A common centroid layout of two matched resistors with an "ABBA" structure is shown in Fig. 5.1. Devices with the same labelling, i.e. "A" are parts of the same component. The layout shown in Fig. 5.1 is symmetric about a central vertical axis, which results in an even dispersal of doping gradients for improved matching.

5.1.3 Dummy Devices

Etching of polysilicon features is highly dependent on feature density. If there is a device that is adjacent to another identical device on one side, but with nothing on the other side, it will result in over–etching of the exposed device. In order to prevent over–etching, a general rule in IC layout is that the surroundings of each device in an array of device fingers must be identical [39].

A simplified diagram of the layout of a pair of matched resistors with dummy devices is shown in Fig. 5.1. Dummy devices are components that are not part of the circuit, but which are added to prevent overetching [31]. The effect of overetching shown in Fig. 5.1 is exaggerated for illustrative purposes. However, the effect of overetching can cause considerable degradation to circuit performance for sensitive analog circuits.

Dummy devices can be disconnected or shorted to a power supply rail. Disconnected dummy devices may build up electrostatic charge, which can interfere with intended operation of the circuit. Thus, it is usually preferred to make dummy devices electrically neutral by connecting all terminals to a power supply rail. The dummy devices will be susceptible to over–etching, but this is irrelevant as the circuit component devices will be protected from over–etching.

For a device that is much longer than it is wide, dummy fingers should be placed to protect the long sides, but shorter sides can be left exposed since over–etching is less degrading to overall device characteristics. Width of a dummy device is not important, since it only serves to prevent over–etching. To save space, a dummy device can be made thinner than the circuit

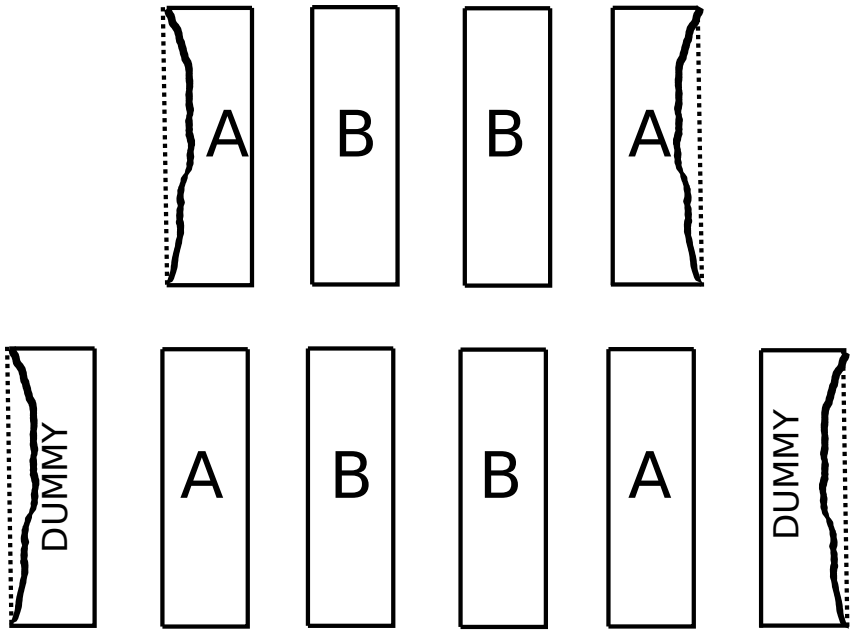


Figure 5.1: Common centroid resistor pair layout with dummy devices

component devices. A common centroid structure is applied such that the devices are symmetric about the vertical axis [31].

5.1.4 Guard Rings

0.13μm CMOS technology is a p-type substrate bulk process. This means that the bodies of NMOS devices are formed in substrate, resulting in electrical coupling of devices through the substrate. Similarly, noise may be coupled to PMOS devices that are in the same n-well.

Triple–well NMOS devices have improved isolation from substrate noise, and these devices are supported by the 0.13 μm process. These devices result in increased layout space however, so standard NMOS devices are preferred.

Individual blocks can be isolated from noise originating from other blocks through the use of guard rings [31]. The type of guard ring commonly supported by CMOS processes is the minority–carrier–collecting guard ring. An electron–collecting guard ring (ECGR) collects electrons from a p-type region, and a hole–collecting guard ring (HCGR) collects holes from an n-type region.

To isolate from substrate noise, an ECGR provides a low impedance path to ground for noise injected into the substrate. For a p-type substrate CMOS process, such as 0.13 μm technology, the guard ring is implemented with a substrate contact. Substrate contacts in 0.13 μm CMOS are p+ diffusion that connect the substrate to ground through the lowest metal layer.

Digital circuits should be placed in a separate n-well than analog PMOS devices to prevent coupling of noise through the n–well. To isolate noise between PMOS devices in the same well, an n–well contact ring is used as a HCGR to separate the sub–blocks.

5.2 MOS Device Layout

Differential pair and current mirror subcircuits are sensitive to mismatch, requiring careful layout and application of the matching techniques presented. Depending on the number of MOS devices to be matched, and the size of the device, an appropriate common centroid structure is chosen. Recommended common centroid array patterns are presented in [31].

As an example, consider a differential pair. If the devices are split in half then the method of cross–quad layout can be applied. A cross–quaded pair of MOS devices is shown in Fig. 5.2. This technique only works for two devices, and each device must be split in half. If there are more than two devices to be matched, or the devices are to be split into more than two fingers, then the cross-quading technique can not be applied. However, if the the devices are split into more than two fingers, a similar common centroid method is applied. Consider a differential pair with each of the NMOS device is to be split into 8 fingers. A layout of this interdigited differential pair is shown in Fig. 5.3. Dispersion of the device fingers using the common centroid pattern results in improved matching between the two devices.

5.3 Resistor Layout

Similar to matched MOS transistor devices, resistors are split into fingers and interdigited in a common-centroid structure. It was alluded in section 3 that the resistors in the LDO feedback

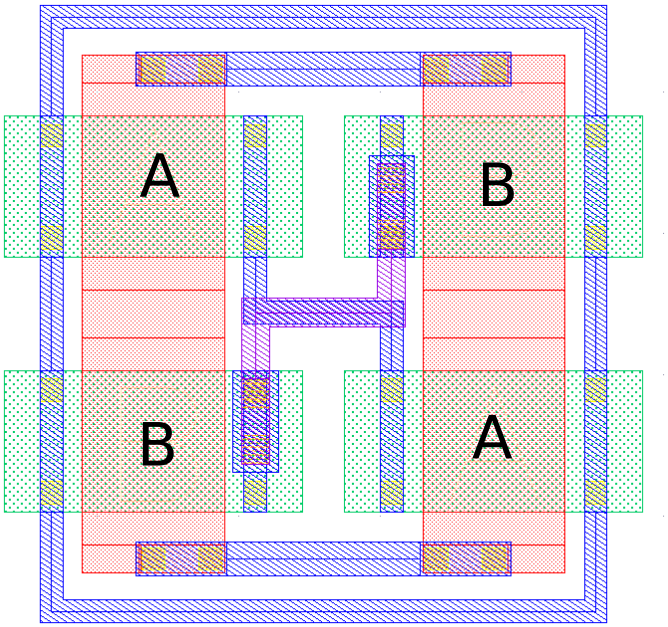


Figure 5.2: Cross–quaded Differential Pair Layout

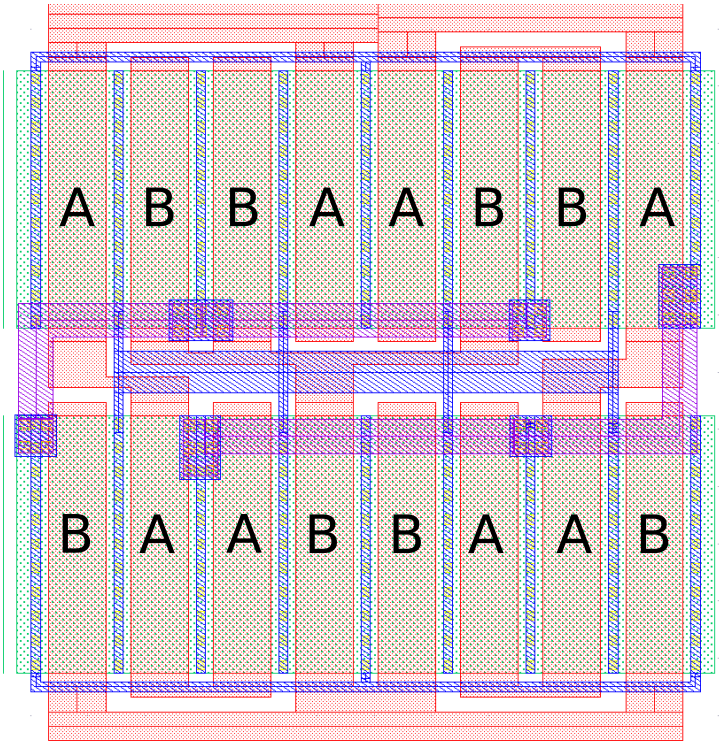


Figure 5.3: Differential Pair layout

voltage divider must track across process variation in order to minimize error in the regulator output voltage. The resistors are split into finger and interdigited, as per the matching discussion of previous sections. Dummy resistor fingers are placed at the ends to protect from over–etching.

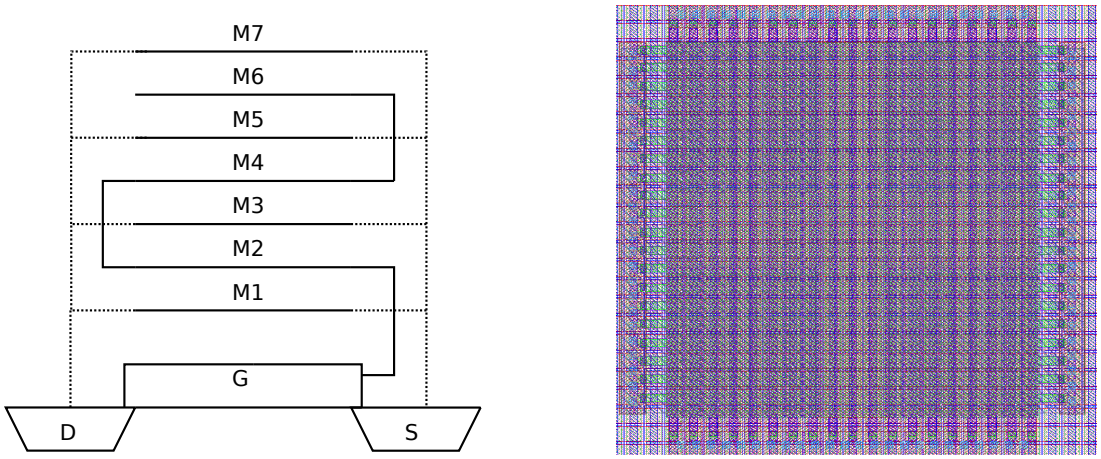
5.4 Capacitor Layout

The two capacitor types used in this design are the MIM and MOS device structures. MIM capacitors can be matched in a similar manner to resistors, however there is no need for precise matching of capacitors in this design. MOS capacitors are used for power supply decoupling at the input of the regulator and bandgap reference. Capacitance values of decoupling capacitors are not important and are arbitrarily chosen. The geometry of the capacitor is chosen to fit the rest of the layout such that the complete layout blocks are approximately square shaped.

Capacitance density of MOS capacitors can be increased using parasitic capacitance of metal interconnect plates. Fig. 5.4a shows a unit sized MOS capacitor with metal layers for added capacitance. This structure utilizes parasitic capacitance between metal layers is utilized to increase the equivalent capacitance of the capacitor device. The bottom plate of this capacitor is comprised of the MOS drain and source diffusions and metal layers 1, 3, 5, and 7. The top plate of the capacitor is comprised of the MOS device gate and metal layers 2, 4, and 6. Capacitors occupy a relatively large area in the IC technology, thus increased capacitance density will reduce the area required to form a particular capacitance value. In addition, there is a minimum required density of each metal layer. Addition of metal layers to the MOS capacitor structure fulfills the required metal density for the higher level metals.

5.5 BJT Layout

BJT devices are used in the bandgap reference circuit to generate a proportional to absolute temperature (PTAT) voltage. Characteristics of the pair of BJT devices must match closely for



(a) (b)

Figure 5.4: MOS capacitor with metal interconnect plates for added capacitance

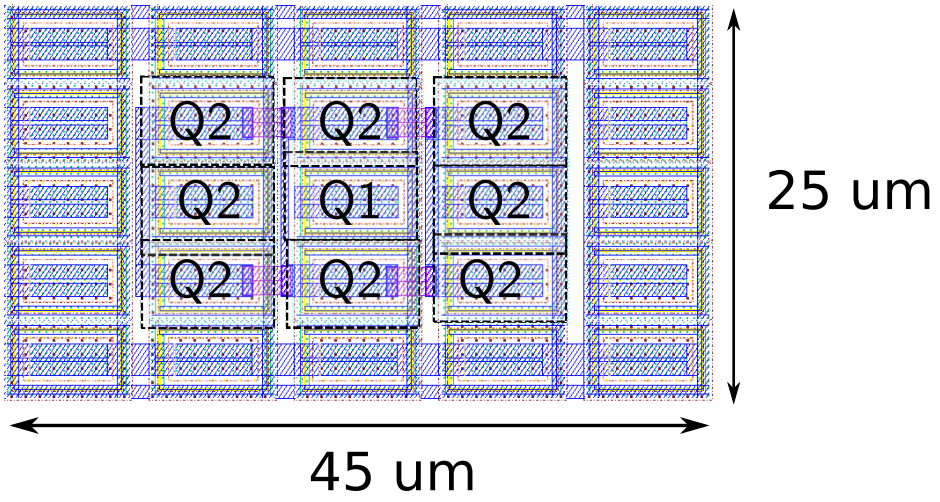


Figure 5.5: Bipolar Transistor Layout

precision of the generated reference voltage.

As discussed in Chapter 4, the emitter area of the two BJT devices must be different in order to generate a PTAT voltage. For layout convenience, the ratio of sizing of the BJT devices are selected to be 8:1, which can be structured as a three by three common centroid array. The smaller BJT device is at the centre, surrounded by the 8 sub–devices connected in parallel to form the larger BJT device. Fig. 5.5 displays the layout of the BJT devices with annotated device labels.

5.6 Digital Layout

For trimming the resistor in the temperature independent reference, a digital decoder is used to control a programmable array or resistors. The digital layout is arranged in the "sea of gates" style, although there are a small number of gates in comparison the millions of gates found in complex ASIC designs [40]. Digital logic layouts are based on a library of logic gates cells that are arranged in a grid to form the digital circuit. Purely digital layouts are typically automatically generated by a CAD tool which places cells into a grid and routes interconnects [41]. Small mixed–signal layouts can be designed manually with reasonable efficiency.

Layout of the decoder, shown in Fig. 5.6, was designed manually. Power rails of the digital layout are arranged to alternate between VDD and VSS, with alternating rows mirrored upside down. Width of the power supply line depends on the number of devices connected. Resistivity information for the 0.13 μm process is used to determine appropriate supply rail widths. The power supply lines should be routed at the lowest metal to reduce the required amount of vias. Unnecessarily using a higher level metal for power rails requires via connections to route to individual devices, causing a bottleneck in the current carrying capacity of the power rail. It is important to avoid notches in a long power rail, as this may result in a fuse that will break under high current flow.

5.7 Top Level Structure

The layout of the complete structure includes the LDO loop, bandgap reference, and rectifier blocks. The differential input to the front–end is connected to a pin for interconnection to off–chip components. Magnetic resonant coupled coils with a matching network will be connected to the input of the rectifier. NMOS device capacitors are connected across the output of the rectifier for decoupling. A space efficient layout is formed by stacking the three sub–blocks and filling the remaining area with the array of decoupling capacitor devices.

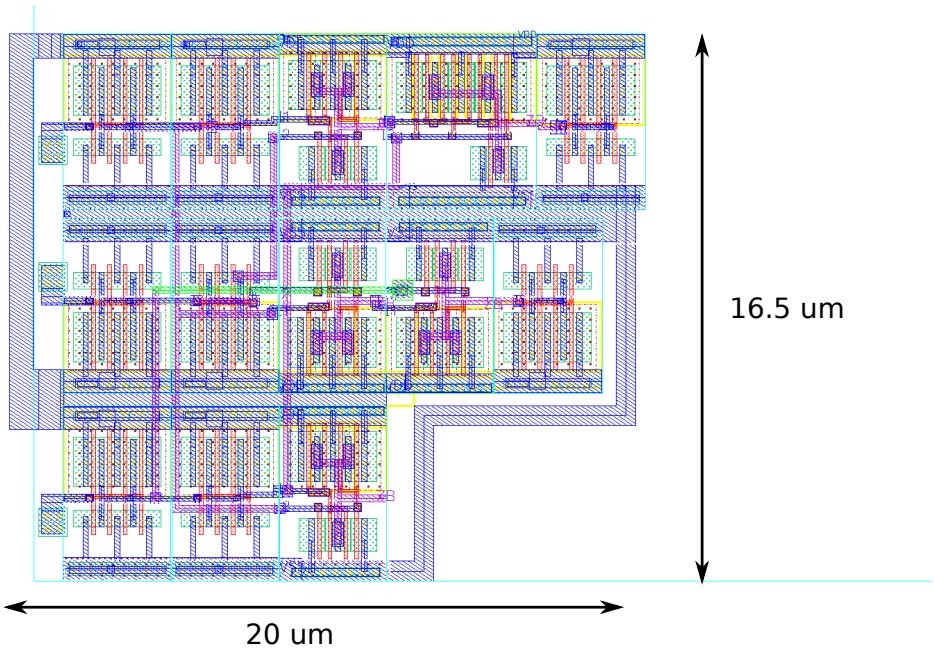


Figure 5.6: Decoder layout

5.8 Chip Level Layout

Manufactured integrated circuit (IC) designs are typically packaged in a plastic or ceramic casing with metallic pins for connection to external circuitry. A top level IC design contains pads which are bonded to pins of the packaging. Pads are metallic regions formed on the highest metal layer. Location of pads depends on the particular IC packaging. For packaging such as DIP, SOIC, or QFP, the pads should be placed at the edges of the die to minimize the length of bonding wires to the package pins. Technologies such as ball grid array packaging and flip–chip allow placement of pads spaced throughout the area of the die. It is also possible to probe pads on an unbonded IC die using specialized equipment.

A typical ASIC design will have a single ring or pads and a power ring at the outer perimeter of the die. A prototype IC does not require a chip–wide power ring however, as each block should have separate power and ground pins. Many ASIC designs are space constrained, meaning that the completed layout has no excess space, but there is possibility of excess pins. Conversely, a pin constrained chip design is one which requires a large number of pins while having excess blank area in the layout. Excess space on the IC can be filled by capacitors for additional

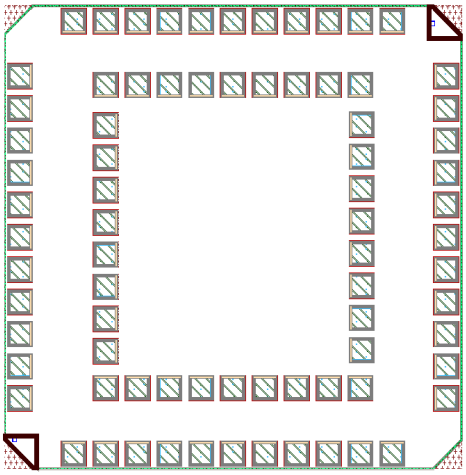


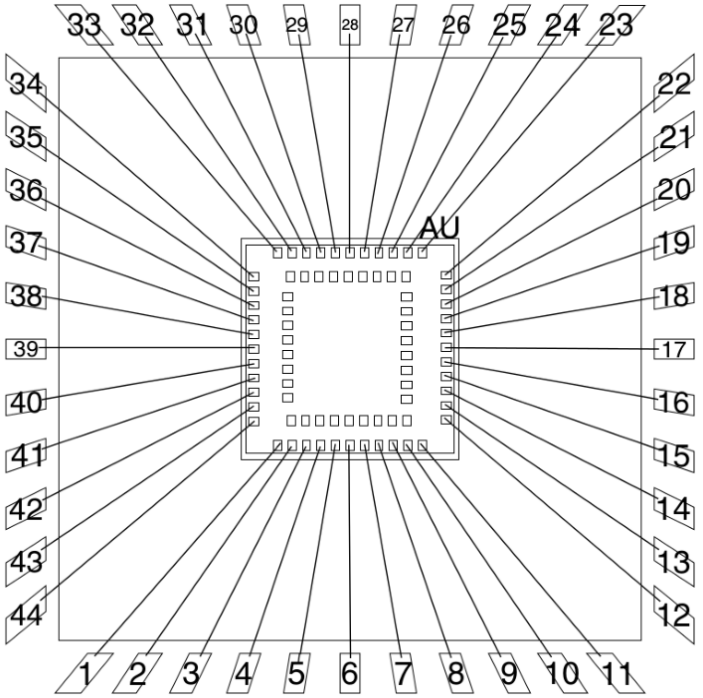
Figure 5.7: Double pad ring structure

decoupling, and will require unconnected metal polygons to meet metal density design rules.

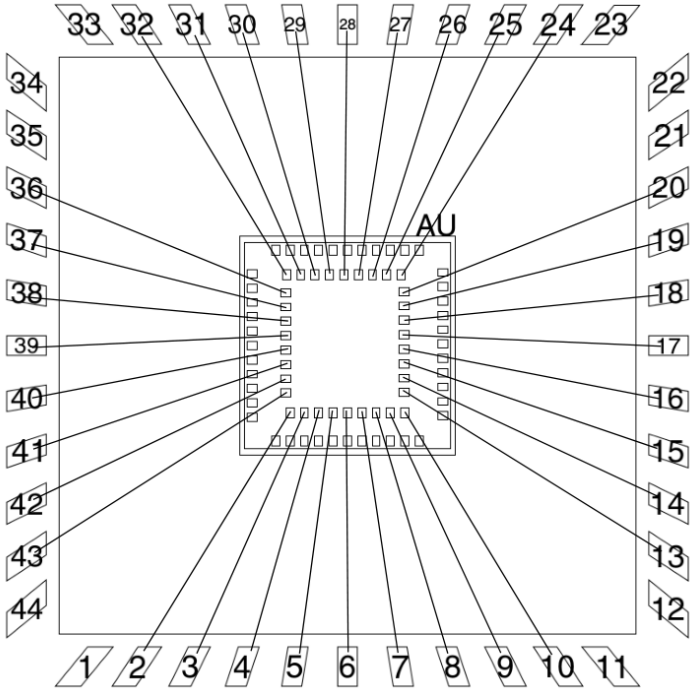
The packaging technology selected for the proposed research prototype is a QFP44 package, which is a 44 pin four sided surface mount IC package. The proposed prototype chip will be pin constrained, so it is desirable to maximize the number of available pins for bonding. In order to increase the pin count, a multiple bonding structure is proposed, as shown in Fig. 5.7. For the two bonding schemes shown in Fig. 5.8 there are two sets of bonded chip packages for the single IC design. The prototype IC is to be fabricated in a single batch, with the identical dies packaged as two separate sets of components.

5.9 Summary

In this chapter, layout design of the regulator structure was presented. Analog layout issues and techniques were discussed. Physical design of analog and mixed–signal blocks is presented and application of appropriate layout techniques was discussed. Top level design of a prototype IC, including design of pad ring structures for packaged IC parts was presented.



(a)



(b)

Figure 5.8: Double pad ring with two bonding schemes

Chapter 6

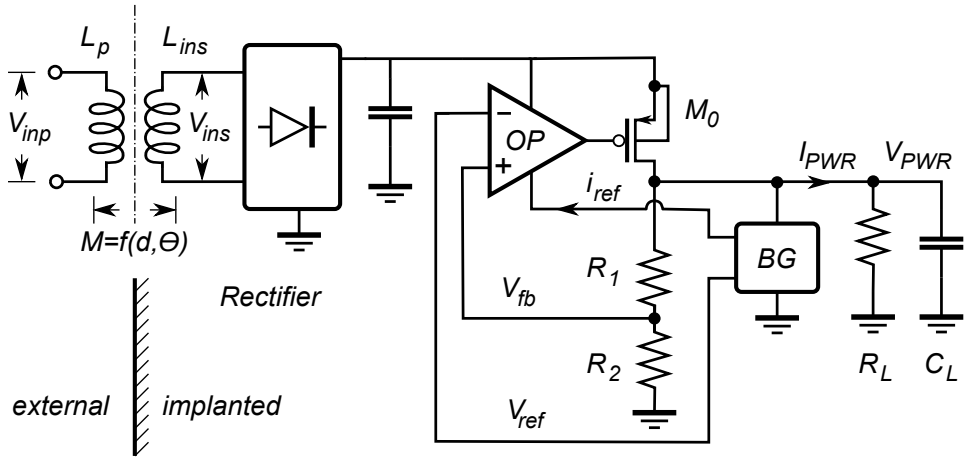
Top–Level Post–Layout Simulations

The top level front–end structure combines the rectifier, LDO regulator, and bandgap reference circuits presented in the previous Chapters. After completion of the layout, parasitic resistances and capacitances are extracted to form a more realistic simulation netlist. Functionality of the complete regulator structure is verified through post–layout simulation.

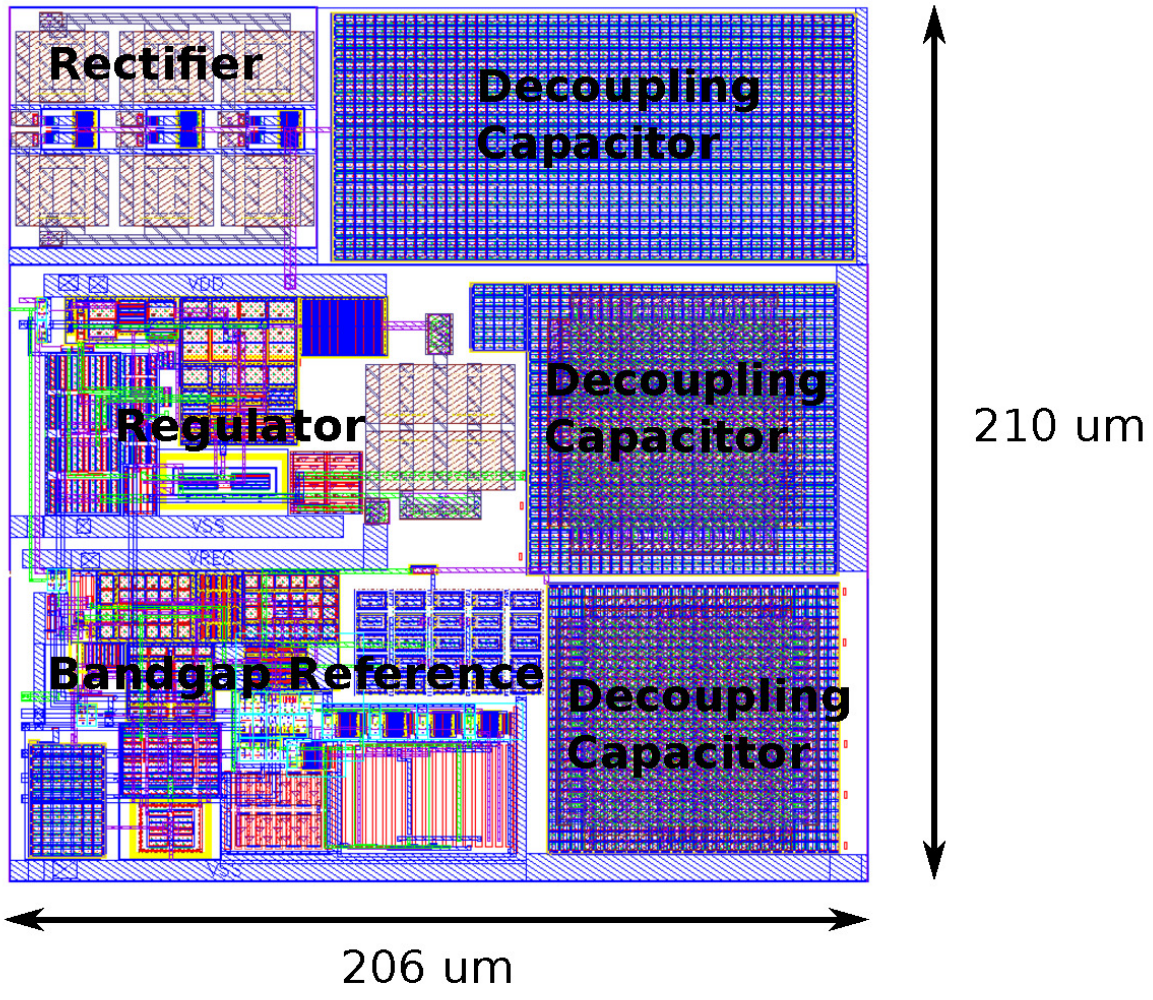
6.1 Top–Level Front–End Architecture

The layout design for the complete front–end was presented in the previous chapter. The top–level front–end architecture combines each of the blocks presented in the previous sections. A block diagram of the system is shown in Fig. 6.1a, and the corresponding top level layout is shown in Fig. 6.1b.

The unregulated output voltage of the rectifier will have a peak–to–peak ripple of approximately 10 mV at 1 GHz. Powering the bandgap reference from the unregulated voltage may result in considerable ripple in the reference voltage and regulated voltage. The power supply connection of the bandgap reference must be considered based on the system specifications and requirements. The bandgap reference circuit must be powered by another available DC power rail or either the input or output of the LDO regulator. For a batteryless device there will be no alternate supply rail, thus received power must be used to power the bandgap reference.



(a)



(b)

Figure 6.1: Energy harvesting front–end (a) block diagram (b) layout

Fully on-chip implementation of the LDO regulator presented by [42] and [19] implement the bandgap reference powered from the same supply rail as the error amplifier. This is typical for a DC to DC converter with minimal ripple in the input voltage. If there is considerable ripple in the input to the regulator it will result in ripple in the reference voltage. Despite the high power supply rejection of the bandgap reference, if the crude power supply contains enough ripple it will result in ripple at the output of the reference voltage. In this case, a stable power supply for the bandgap can be provided by the output of the regulator. Connecting the bandgap reference to the output of the LDO results in a recursive dependency between the regulator output and the reference voltage. In this case a start–up or power on reset circuit is required to ensure that both the bandgap reference and regulator loop reach a stable operating point.

The fully on chip LDO regulator presented by [11] uses this aforementioned architecture, with the bandgap reference powered primarily from the output of the regulator loop, but connected to the input power supply through power on reset (POR) circuitry. Ahmadi et al [43] propose a POR circuit that powers the LDO regulator loop by turning on the pass device at start-up. This circuit forms a closed loop feedback network that connects the output of the regulator to the input of the pass device to raise the output voltage at start-up. The start–up circuit consists of two inverters and two pass devices with the switching threshold of the inverter as proportional to the minimum supply voltage of the bandgap reference, such that the bandgap reference is sufficiently powered. The POR circuit inverter is designed so that the switching threshold corresponds to the minimum supply voltage of the bandgap reference. When the input to the inverter corresponds to the desired regulated voltage, the inverter is designed to be at a low output voltage.

An adapted version of the POR circuit for an LDO with PMOS pass device consists of a single CMOS inverter and an NMOS switch. For a regulator with a PMOS device the POR circuit pulls down the gate of the PMOS pass vice to V_{SS} until the loop beings to function. The inverter senses whether the regulator loop has begun to function, and drives the gate of the NMOS switch accordingly. If the output of the regulator is low, the output of the inverter will

be high, resulting in the gate of the PMOS pass device being pulled to ground and the output of the regulator bring raised to $V_{DD} - V_{DS(SAT)}$, where $V_{DS(SAT)}$ is the minimum drain to source voltage of the PMOS device in saturation.

Using a decoupling capacitor at the output of the rectifier filters the ripple enough that the bandgap reference can be connected directly to this crude power supply. An on–chip array of MOS device capacitor devices are used for decoupling.

For testing purposes it is proposed that the bandgap reference power supply be supplied externally. With an independent power supply the bandgap reference will settle independently without the need for POR or power up supervision. For a prototype IC, it is proposed that all terminals of the bandgap be isolated from the regulator structure. Isolation of blocks in the prototype means that each input and output of the bandgap and rectifier circuits will be connected to pins on the prototype IC. An entirely batteryless configuration can be tested with the prototype by externally connecting the power supply of the bandgap reference to the regulator output. In simulation, the bondpads and bonding wire of the IC are modelled as parasitic resistance and capacitance components. At high frequencies the parasitics of packaging and interconnects degrade circuit performance. Since the output of the circuit operates at DC the parasitic capacitance of bondpad and bonding wire have a negligible effect on circuit performance. AC input voltage is at a frequency of approximately 1 GHz. For adequate power transfer from signal source to input of the rectifier, a matching network will need to be developed based on measurements of the fabricated rectifier prototype.

Fig. 6.2 shows the transient response of the reference voltage and regulated output voltage with the bandgap reference powered from the rectifier output voltage. Wit the bandgap reference power supply connected to the output of the regulator, the initial condition at the output of the regulator is set to 1 V in simulation so that the loop is powered-up correctly. In experimental testing the initial condition can be forced using external circuitry. Once the operation of the LDO and bandgap is verified, further research into POR algorithms and circuit structures can be developed.

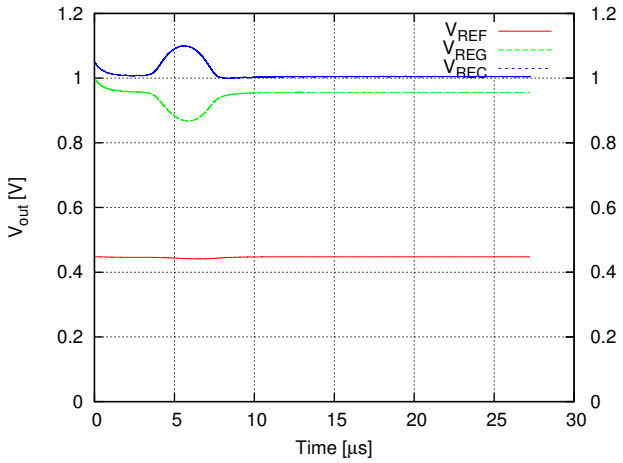


Figure 6.2: Transient simulation of front–end structure

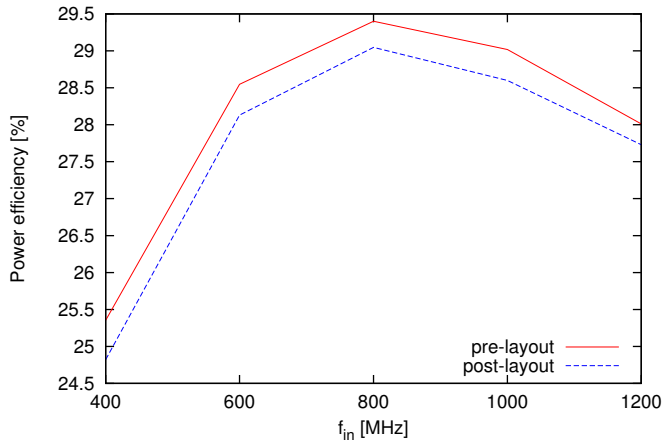


Figure 6.3: Post–layout simulations of power conversion efficiency with 1.6 V peak–to–peak input and 10 kΩ load

The top–level front end simulations include a model of the IC bondpad and packaging between the output of the regulator and the load. Since the output is DC, parasitic capacitance of the bondpad and bonding wires do not have a significant effect on performance. A small DC voltage drop results from the resistance of interconnects.

Total PCE is a combination of PCE of the rectifier structure and efficiency of the LDO regulator. Post–layout simulation of power conversion efficiency (PCE) of the front–end structure is shown in Fig. 6.3 as a function of input frequency.

Post–layout PCE of the complete front–end is slightly lower than the pre–layout simulation

result. Additional resistance due to interconnects cause a small DC drop at the output of the rectifier.

Low–power circuitry in an implantable telemetry system can operate on power in the order of microwatts. An implantable telemetry system with power consumption of 350 μW is presented by [44]. Assuming total power conversion efficiency of 28%, 1250 μW received power at the implanted coil is sufficient to power the fully implantable device presented by [44]. Thus, it is feasible based on the post–layout simulations that the proposed energy harvesting front–end can power a fully implantable telemetry system in lieu of a battery.

6.2 Summary

In this section the complete front–end architecture is presented. Operation of the complete front–end is discussed with various configurations for connecting the bandgap reference circuit. Simulation and proposed testing configuration of the front–end structure is discussed. Post–layout simulation results indicate power conversion efficiency of up to 29% for the complete front end structure.

Chapter 7

Conclusions

The main aim of this thesis is to design and implement a front–end for wireless power transfer to implantable biomedical telemetry systems. It is proposed that power is transferred to the implanted system through magnetic resonance coupled coils. The proposed front–end structure is comprised of a rectifier and LDO regulator with an on–chip bandgap reference circuit. The energy harvesting front–end is implemented in CMOS $0.13\mu m$ CMOS and post–layout simulation results are presented.

7.1 Contributions of Thesis

In this thesis the following achievements are presented

- CMOS sub–circuits for a wireless power harvesting front–end are developed in 0.13 μm CMOS. The self V_{th} cancellation rectifier is presented. A low–power bandgap reference and LDO regulator are presented. The bandgap reference consumes approximately 4 μA of current, considerably less than comparable designs presented in the literature.

- Top level interconnection of front–end blocks is designed and post–layout simulation verification is presented. Post–layout simulation shows power conversion efficiency of up to 29% for the complete front–end structure.

- Each subsystem is developed in the 0.13 μm CMOS technology. Layout design of each block and the full front–end are designed using standard analog layout techniques for enhanced matching and circuit reliability. Layout of the complete front–end circuit occupies a square area of 120 μm by 206 μm

7.2 Future Work

Based on the achievements of this thesis, future work includes,

- Prototyping and experimental verification of the sub–circuits and regulator architecture
- Combination of the front–end circuit with coils for wireless power transfer. Interfacing between the coils and rectifier circuit will require design of a matching network.
- Wireless power transfer implemented into a full biomedical implantable telemetry system

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