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Modeling and Protection of Phase Shifting Transformers

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A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy

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MODELING AND PROTECTION OF PHASE SHIFTING TRANSFORMERS

(Thesis format: Monograph)

by

Umar Naseem Khan

Graduate Program in Electrical and Computer Engineering

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

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Abstract

This thesis is mainly focused on the development of (i) phase shifting transformers (PSTs) mathematical and simulation models that can be used for the short-circuit and protection studies, and (ii) new phase shifting transformers protection methods that provide more secure and sensitive solutions than the standard current differential protection.

The first part of this thesis describes and presents the modeling of the single-core standard-delta, and two-core symmetrical and asymmetrical PST for protection and short-circuit studies. The models already available for such types of PSTs have limitations and require detailed test report data from the manufacturers. However, winding test data at each tap position is seldom available from the manufacturers. Moreover, they are confined to the balanced system conditions. The proposed modeling approach is based on the development of positive, negative and zero-sequence networks. Derived mathematical relations are further used to develop the relations of winding terminal voltages, currents and impedances as a function of tap position. Accuracy of the presented models is verified mathematically with the manufacturer’s test report data. Furthermore, electromagnetic transients program (EMTP) modeling, in commercially available simulation tools such as PSCAD/EMTDC and RTDS, is done in order to further verify the proposed models. The proposed modeling approach does not rely on the availability of the manufacturer test report data and only requires the nameplate information. It can also be used for both balanced and unbalanced system conditions.

The second part of the thesis presents two protection principles: (a) electromagnetic differential protection, and (b) directional comparison-based protection. The main motive behind the development of new protection principles is to develop a solution that is more secure, sensitive and offers high-speed protection. Correct implementation of these techniques for the protection of various kinds of PSTs comes across various problems and hence leads us to the proposed solution of those issues. Both techniques solve the problems of conventional challenges such as magnetizing inrush current, core saturation, non-standard phase shift, external fault with current transformer (CT) saturation, etc. The
electromagnetic differential protection principle can only be applied to the PST it represents and it requires tap position tracking. A directional comparison-based approach can be applied to any kind of PST without tracking the tap position.

Keywords

I dedicate this thesis to my grandfather Abdullah Khan
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Table of Contents

Abstract ............................................................................................................................... ii

Acknowledgments............................................................................................................... v

Table of Contents ............................................................................................................... vi

List of Tables ...................................................................................................................... x

List of Figures ................................................................................................................... xii

List of Appendices ....................................................................................................... xxviii

List of Abbreviations (Acronyms) ................................................................................. xxix

Chapter 1 ............................................................................................................................. 1

Power System Protection ................................................................................................. 1

1.1. Zones of Protection ................................................................................................. 1

1.2. Aspects of the Protection System ......................................................................... 2

1.3. Basic Protection Principles .................................................................................... 3

1.4. Transformer Protection .......................................................................................... 4

1.5. Phase Shifting Transformers ................................................................................ 6

1.6. Research Objective ................................................................................................. 7

1.7. Thesis Outline ......................................................................................................... 9

1.8. List of Publications ............................................................................................... 10

1.9. Summary ............................................................................................................... 10

Chapter 2 ........................................................................................................................... 12

Phase Shifting Transformers - Modeling and Protection ............................................. 12

2.1. Phase Shifting Transformers ................................................................................. 12

2.1.1. Basic Working Principle .................................................................................... 13

2.1.2. Types of Phase Shifting Transformers .............................................................. 13
2.2. Modeling of the Phase Shifting Transformers ...................................................... 16
2.3. Protection of the Phase Shifting Transformers ..................................................... 22
  2.3.1. Current Differential Protection ..................................................................... 22
  2.3.2. Differential Current Measuring Principles (DCMP) ...................................... 23
  2.3.3. Phase Shifting Transformer Differential Protection ....................................... 24
2.4. Limitations of PST Differential Protection ........................................................... 28
  2.4.1. Traditional Problems Associated with PST Differential Protection .......... 29
  2.4.2. Non-Traditional Problems Associated with PST Differential Protection . 33
2.5. Summary ............................................................................................................... 37

Chapter 3........................................................................................................................... 38

Modeling of Phase Shifting Transformers ....................................................................... 38
3.1. Introduction ........................................................................................................... 38
3.2. Modeling of Standard-Delta Phase Shifting Transformer .................................... 39
  3.2.1. Calculation of Positive-Sequence Winding Impedances .......................... 39
  3.2.2. Calculation of Negative-Sequence Winding Impedances ......................... 44
  3.2.3. Calculation of Zero-Sequence Winding Impedances ............................... 44
3.3. Validation of the Derived Positive- And Zero-Sequence Impedances Relations . 46
3.4. Modeling of the Two-core Symmetrical Phase Shifting Transformer ................. 47
  3.4.1. Calculation of Positive-Sequence Winding Impedances ....................... 47
  3.4.2. Calculation of Negative-Sequence Winding Impedances ......................... 54
  3.4.3. Calculation of Zero-Sequence Winding Impedances ............................... 54
  3.4.4. Validation of the Derived Positive- and Zero-Sequence Impedance
         Relations ................................................................................................... 55
3.5. Emtp Modeling of Phase Shifting Transformers .................................................. 56
  3.5.1. Modeling of Standard-Delta PST in EMTP ............................................ 56
3.5.2. Turn-to-Turn, Turn-to-Ground, and Winding-to-Winding Faults Modeling of a Standard-Delta PST ........................................................... 58

3.5.3. Modeling of a Two-Core Symmetrical PST in EMTP ....................... 59

3.5.4. Turn-to-Turn, Turn-to-Ground and Winding-to-Winding Faults Modeling of a Two-core Symmetrical PST .............................................. 61

3.6. Simulation of Terminals Current and Voltage during Normal and Fault System Conditions ................................................................. 63

3.7. Summary............................................................................................................... 67

Chapter 4 ........................................................................................................................... 68

Electromagnetic Differential Protection ................................................................. 68

4.1. Introduction ........................................................................................................... 68

4.2. Electromagnetic Differential Protection Method- Standard Transformer .......... 69

4.3. Electromagnetic Differential Protection Method- Delta-Hexagonal PST (EDP-DHP) ......................................................................................... 70

4.3.1. Proposed Electromagnetic Differential Protection Method I (EDP-DHP I) ........................................................................................................... 70

4.3.2. Problems and Limitations of the Proposed Electromagnetic Differential Protection Method I (EDP-DHP I) ........................................ 73

4.3.3. Proposed Electromagnetic Differential Protection Method II (EDP-DHP II) ........................................................................................................ 74

4.3.4. Fault Detection Algorithm ........................................................................ 79

4.4. Electromagnetic Differential Protection Method–Standard-Delta PST (EDP-SDP) ......................................................................................... 80

4.4.1. Practical Issues and Their Solutions ............................................................. 84

4.4.2. Fault Detection Algorithm ........................................................................ 88

4.5. CVT Transients ..................................................................................................... 89

4.6. Performance Evaluation........................................................................................ 92

4.6.1. Signal Processing .......................................................................................... 92

4.6.2. Selection of the Threshold Setting ............................................................... 92
4.6.3. Simulation Cases........................................................................................................... 93
4.6.4. Test Results................................................................................................................. 95
4.7. Summary......................................................................................................................... 117

Chapter 5................................................................................................................................. 118

A Phase Shifting Transformer Protection Technique Based on a Directional Comparison Approach ................................................................................................................................. 118

5.1. Superimposed or Delta Components ........................................................................... 118
5.2. Fault Detection Based on Superimposed Components.................................................. 121
  5.2.1. Directional Criteria ............................................................................................... 121
  5.2.2. Computations ...................................................................................................... 123
5.3. Practical Issues and the Proposed Solutions .................................................................. 126
  5.3.1. Energization of an Unloaded PST ....................................................................... 126
  5.3.2. Operation of the On-Load Tap-Changer .............................................................. 130
5.4. Performance Evaluation ................................................................................................. 134
  5.4.1. Simulation Cases .................................................................................................... 135
  5.4.2. Energization of the Unloaded PST ....................................................................... 136
  5.4.3. Internal Faults in a Loaded PST ............................................................................ 141
  5.4.4. Turn-to-Turn Faults .............................................................................................. 148
  5.4.5. External Faults in a Loaded PST ............................................................................ 150
5.5. Summary......................................................................................................................... 153

Chapter 6................................................................................................................................. 154

Summary and Conclusions .................................................................................................... 154

6.1. Summary......................................................................................................................... 154
6.2. Conclusions..................................................................................................................... 155

References............................................................................................................................... 160

Curriculum Vitae ..................................................................................................................... 208
List of Tables

Table 4-1: Relay operating times for internal phase-to-ground faults ......................... 98
Table 4-2: Relay operating times for ph-to-ph and double ph-to-ground faults .......... 100
Table 5-1: Relay operating times for switch-on-to internal faults in an unloaded PST . 140
Table 5-2: Relay operating times for internal faults in an unloaded PST for SIR 1 ...... 141
Table 5-3: Relay operating times for internal faults in an unloaded PST for SIR 5 ...... 141
Table 5-4: Relay operating times for internal phase-to-ground faults for SIR=1 ......... 142
Table 5-5: Relay operating times for internal phase-to-ground fault for SIR=0.2 ....... 145
Table 5-6: Relay operating times for internal phase-to-ground fault for SIR=5 ........... 145
Table 5-7: Relay operating times for internal phase-to-phase and 3 ph. faults, SIR=1 .. 146
Table 5-8: Relay operating times for turn-to-turn faults ................................................. 149
Table 5-9: Relay performance in the event of external faults ....................................... 150
Table B-1: Cosine and sine filter coefficients for a 24 point DFT ................................. 175
Table B-2: Cosine and sine filter coefficients for a 48 point DFT ................................. 176
Table C-1: Equivalent sources’ data for Model 1 ........................................................... 179
Table C-2: Equivalent sources’ data for Model 2 ........................................................... 179
Table C-3: Equivalent sources’ data for Model 3 ........................................................... 179
Table C-4: Delta Hexagonal PST ................................................................................... 180
Table C-5: Standard-Delta PST ...................................................................................... 180
Table C-6: Two-core symmetrical PST ......................................................................... 180
Table C-7: Transmission Line Data for Model 1 ............................................................ 181
Table C-8: Transmission Line Data for Model 2 ............................................................ 181
Table C-9: Transmission Line Data for Model 3 ............................................................ 181
Table C-10: Current Transformers Data ......................................................................... 181
Table C-11: Capacitive voltage transformer Data .......................................................... 182
Table D-1: Relay operating times for three-phase and three phase-to-ground faults ..... 189
Table D-2: Relay performance in the event of external faults ....................................... 190
Table E-1: Relay operating times in the event of internal ph-ph and 3-ph faults .......... 195
Table E-2: Relay operating times in the event of internal ph-ph and 3 phase faults, S .. 195
List of Figures

Figure 1.1: Typical zones of protection in power system.................................................. 2

Figure 2.1: Application and working of a phase shifting transformer a) parallel transmission system with PST; b) demonstration of phase shift angle and quadrature voltage.............................................................................................................................................. 14

Figure 2.2: Schematic diagrams of single-core PSTs (a) standard-delta symmetrical, (b) delta-hexagonal symmetrical, and (c) squashed-delta asymmetrical........................................ 15

Figure 2.3: Schematic diagram of a two-core symmetrical PST. ......................................... 17

Figure 2.4: Schematic diagram of a two-core asymmetrical PST. ..................................... 17

Figure 2.5: Core structure of a two-winding transformer................................................. 18

Figure 2.6: Two-winding transformer: (a) equivalent circuit, (b) short-circuit test, and (c) open-circuit test.................................................................................................................. 20

Figure 2.7: Standard transformer differential protection: (a) schematic diagram of a two-winding transformer with differential relay, (b) percentage differential rely characteristic. ........................................................................................................................................... 23

Figure 2.8: Differential current measuring principles of: (a) magnetically-coupled circuit, (b) electrically-connected circuit, and (c) compensated two end currents....................... 24

Figure 2.9: Schematic diagram of primary (87P) and secondary (87S) differential relays for two-core PST.......................................................................................................................... 26

Figure 2.10: Schematic diagram of a delta-hexagonal PST series winding (87M) and exciting winding (87N) differential relays......................................................................................... 28

Figure 2.11: Energization of an unloaded phase shifting transformer (a) magnetizing inrash currents, and (b) differential (I_{diff}) vs. restraining(I_{bias}) current characteristics. .... 30
Figure 2.12: Internal fault during magnetizing inrush currents (a) differential ($I_{diff}$) vs. restraining ($I_{bias}$) currents characteristic, and (b) demonstration of delay operation of the differential relay.

Figure 2.13: External fault with CT saturation: (a) profiles of load-side three phase currents (b) $I_{diff}$ vs. $I_{bias}$ current characteristic.

Figure 2.14: Differential current as a function of tap position (D).

Figure 2.15: Saturation of the series winding: (a) source-side phase voltages, (b) distorted currents of exciting winding terminals, and (c) differential relay characteristic.

Figure 3.1: Winding connections of a standard-delta PST.

Figure 3.2: Single-phase diagram of a standard-delta PST with winding impedances.

Figure 3.3: Positive- and zero-sequence impedance vs. tap position: calculated values using our proposed model (solid line) and values from the manufacturer’s test report data (dots).

Figure 3.4: Winding connections of a two-core symmetrical PST.

Figure 3.5: Single-phase diagram of a two-core symmetrical PST.

Figure 3.6: Positive-sequence impedance and phase-shift vs. tap position: Calculated values using our proposed model (solid line) and values from the manufacturer’s test report data (dots).

Figure 3.7: Positive- and zero-sequence impedance vs. tap position: Measured values from our EMTP model (solid line) and values from the manufacturer’s test report data (dots).

Figure 3.8: Fault modeling of standard-delta PST.
Figure 3.9: Positive-sequence impedance vs. tap position: Measured values from our
emtp model (solid line), measured values from the emtp model proposed in [17] (triangle
dots) and values from the manufacturer’s test report data (square dots) .................... 61

Figure 3.10: Fault modeling of the two-core symmetrical PST ................................. 63

Figure 3.11: Phase shift as a function of the tap position ....................................... 64

Figure 3.12: Profiles of source- and exciting-unit primary winding terminal currents
during energization of PST. ......................................................................................... 64

Figure 3.13: Profiles of phase A voltages at source (S-side), load (L-side) and exciting-
unit primary winding terminal (E-side) for various tap positions .............................. 65

Figure 3.14: Profiles of phase A currents at source(S-side), load (L-side) and primary
winding terminal of exciting-unit (E-side) for various tap positions .......................... 65

Figure 3.15: Profiles of terminals voltages in the event of an internal phase A to ground
fault at location F4. ..................................................................................................... 66

Figure 3.16: Profile of terminal currents in the event of an internal phase A to ground
fault at location F4. ..................................................................................................... 66

Figure 4.1: Two-winding transformer ...................................................................... 69

Figure 4.2: A schematic diagram of a delta-hexagonal PST. .................................... 71

Figure 4.3: Phase A diagram of a delta-hexagonal PST operating at the maximum tap
position D=1. ................................................................................................................. 73

Figure 4.4: Phase A diagram of a hexagonal PST operating at tap position D≠1. ....... 74

Figure 4.5: Schematic diagrams of standard-delta PST a) three phase windings
connections, and b) phase A. .......................................................................................... 82

Figure 4.6: Internal faults in a standard-delta PST. ...................................................... 86
Figure 4.7: Performance comparison of the proposed technique with conventional VT, CVT without filter and CVT with filter for the case of an internal fault. ........................................... 90

Figure 4.8: Performance comparison of the proposed technique with conventional VT, CVT without filter and CVT with filter for the case of an external fault. ......................... 91

Figure 4.9: Fault modeling of a delta-hexagonal PST. ............................................................................................................................... 94

Figure 4.10: Internal phase A-g fault at location F5: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-1). ......................................................... 95

Figure 4.11: Internal phase A-g fault at location F5: profiles of source-side currents, load-side currents, exciting winding terminal currents, and source- and load sides terminal voltages (Case 4-1). ........................................................................................................ 96

Figure 4.12: Internal phase B-g fault at location F5: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-2). ................................................................. 97

Figure 4.13: Internal BC fault at location F5: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-19). ................................................................. 99

Figure 4.14: Internal BC-g fault at location F4: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-20). ................................................................. 100

Figure 4.15: Internal ABC fault at location F8: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-29). ................................................................. 101

Figure 4.16: Internal ABC fault at location F5: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-30). ................................................................. 102

Figure 4.17: Turn-to-ground fault at location F3: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-31). ................................................................. 103

Figure 4.18: Turn-to-turn fault of fault span of 5% of exciting winding: |DIFF| signals computed by RELAY S and RELAY L, and fault inception/trip signals (Case 4-32)........ 104
Figure 4.19: Turn-to-turn fault of fault span of 1.5% of exciting winding: |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-33)........ 105

Figure 4.20: Turn-to-turn fault of fault span of 5% of exciting winding: |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-34)........ 106

Figure 4.21: External phase C-g fault at location F2: Profiles of source-side phase C terminal current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-35)............................................. 108

Figure 4.22: External C-g fault with phase C CT saturation at location F2: Profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-36)................. 108

Figure 4.23: External phase C-g fault at location F1: Profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-37).................................................................. 109

Figure 4.24: External BC fault at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-38). ................................................................. 109

Figure 4.25: External BC fault with phase B CT saturation at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-39)...................... 110

Figure 4.26: External ABC fault at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-40). ................................................................. 110

Figure 4.27: External ABC fault with phase A CT saturation at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-41)...................... 111
Figure 4.28: Energization of an unloaded PST: profiles of source-side, load-side and exciting winding terminal currents (Case 4-42).......................................................................................... 112

Figure 4.29: Energization of an unloaded PST: |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals plots of |DIFF| (Case 4-42).............................. 113

Figure 4.30: Internal phase-to-ground fault at location F3: |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-43). ......................... 114

Figure 4.31: Internal phase-to-ground fault at location F3: |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-44). ......................... 115

Figure 4.32: Saturation of the series windings: profiles of source-side phase A voltage, exciting-winding terminal phase A current, |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-45). ............................................................... 116

Figure 5.1: Illustration of superimposed network: (a) normal power system network, (b) pre-fault positive sequence network, (c) post-fault positive sequence network, and (d) positive-sequence superimposed network................................................................. 120

Figure 5.2: Directional criteria of forward and reverse faults. ............................................ 122

Figure 5.3: (a) Logic diagram of the delta-filter, and (b) logic diagram of the latch memory gate signal. .............................................................................................................. 126

Figure 5.4: Location of the potential transformers at: (a) outside the protection zone, and (b) inside protection zone...................................................................................... 128

Figure 5.5: Measurement of the negative-sequence current during closing operation of the source- and load-side circuit breaker and phase-ground fault.......................... 129

Figure 5.6: Computation of delta impedance in relay L using source-side voltages...... 132

Figure 5.7: Modification in the basic directional criteria. .................................................... 134

Figure 5.8: Fault modeling of two core symmetrical PST.................................................. 136
Figure 5.9: Energization of unloaded PST: profiles of inrush currents, arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS2) and digital output signals (Case 5-1) .................................................................................................................. 137

Figure 5.10: Switch-on-to internal phase A-g fault in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS2) and digital output signals (Case 5-2). .............................................................................................................. 138

Figure 5.11: Switch-on-to internal A-g fault in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS2) and digital output signals (Case 5-3). .............................................................................................................. 139

Figure 5.12: Switch-on-to B-g in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS2) and digital output signals (Case 5-4). .............................................................................................................. 139

Figure 5.13: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 \( \Omega \)) at location F4 (Case 5-24) .............................................................................................................. 142

Figure 5.14: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 20 \( \Omega \)) at location F4 (Case 5-25). .............................................................................................................. 142

Figure 5.15: Plots of arguments and digital signals in the event of phase C-g fault (fault resistance 0.1 \( \Omega \)) at location F5 (Case 5-26). .............................................................................................................. 143

Figure 5.16: Plots of arguments and digital signals in the event of phase C-g fault (fault resistance 20 \( \Omega \)) at location F5 (Case 5-28). .............................................................................................................. 143

Figure 5.17: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 \( \Omega \)) at location F6 (Case 5-27) .............................................................................................................. 143
Figure 5.18: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 Ω) at location F4 (Case 5-29).................................................................................. 143

Figure 5.19: Plots of arguments and digital signals in the event of (resistance 20 Ω) at fault location F4 (Case 5-30). ........................................................................................................ 144

Figure 5.20: Plots of arguments and digital signals in the event of C-g fault (fault resistance 0.1 Ω) at location F5 (Case 5-31).................................................................................. 144

Figure 5.21: Plots of arguments and digital signals in the event of C-g fault (fault resistance 20 Ω) at location F5 (Case 5-32).................................................................................. 144

Figure 5.22: Plots of arguments and digital signals in the event of C-g fault (fault resistance 0.1 Ω) at location F6 (Case 5-33).................................................................................. 144

Figure 5.23: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-54)..................................................................................................................... 146

Figure 5.24: Plots of arguments and digital signals in the event of BC fault at location at F5 (Case 5-55)..................................................................................................................... 146

Figure 5.25: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-56)..................................................................................................................... 147

Figure 5.26: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-57)..................................................................................................................... 147

Figure 5.27: Plots of arguments and digital signals in the event of BC-g fault at location F5 (Case 5-58)..................................................................................................................... 147

Figure 5.28: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-59)..................................................................................................................... 147

Figure 5.29: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-60)..................................................................................................................... 148
Figure 5.30: Plots of arguments and digital signals in the event of BC-g fault at location F5 (Case 5-61) ................................................................................................................. 148

Figure 5.31: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-62) ................................................................................................................. 148

Figure 5.32: Plots of arguments and digital signals in the event of external A-g fault at location F1 (Case 5-95) .................................................................................................. 151

Figure 5.33: Plots of arguments and digital signals in the event of external BC fault at location F1 (Case 5-96) .................................................................................................. 151

Figure 5.34: Plots of arguments and digital signals in the event of external BC-g fault at location F1 (Case 5-97) .................................................................................................. 151

Figure 5.35: Plots of arguments and digital signals in the event of external ABC fault at location F1 (Case 5-98) ................................................................................................... 151

Figure 5.36: Plots of arguments and digital signals in the event of external A-g fault at location F2 (Case 5-99) .................................................................................................. 152

Figure 5.37: Plots of arguments and digital signals in the event of external BC fault at location F2 (Case 5-100) ................................................................................................. 152

Figure 5.38: Plots of arguments and digital signals in the event of external BC-g fault at location F2 (Case 5-101) ................................................................................................. 152

Figure 5.39: Plots of arguments and digital signals in the event of external ABC fault at location F2 (Case 5-102) ................................................................................................. 152

Figure A.1: Schematic diagram of two-core asymmetrical PST. ................................ 166

Figure A.2: Single-phase diagram of two-core asymmetrical PST. .......................... 167

Figure B.1: Frequency response of cosine and sine filters for sampling frequency of 1440 Hz ............................................................................................................................ 176
Figure B.2: Frequency response of cosine and sine filters for sampling frequency of 2880 Hz................................................................. 177

Figure C.1: Single line diagram of the parallel transmission network together with the phase shifting transformer................................................................. 178

Figure C.2: Schematic of a capacitive voltage transformer......................................... 182

Figure D.1: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-3)................................................................. 183

Figure D.2: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-4)................................................................. 183

Figure D.3: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-5)................................................................. 184

Figure D.4: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-6)................................................................. 184

Figure D.5: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-7)................................................................. 184

Figure D.6: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-8)................................................................. 184

Figure D.7: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-9)................................................................. 185

Figure D.8: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-10). ................................................................. 185

Figure D.9: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-11). ................................................................. 185
Figure D.10: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-12). ........................................................................................................ 185

Figure D.11: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-13). ........................................................................................................ 186

Figure D.12: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-14). ........................................................................................................ 186

Figure D.13: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-15). ........................................................................................................ 186

Figure D.14: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-16). ........................................................................................................ 186

Figure D.15: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-17). ........................................................................................................ 187

Figure D.16: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-18). ........................................................................................................ 187

Figure D.17: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-21). ........................................................................................................ 187

Figure D.18: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-22). ........................................................................................................ 187

Figure D.19: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-23). ........................................................................................................ 188

Figure D.20: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-24). ........................................................................................................ 188

Figure D.21: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-25). ........................................................................................................ 188
Figure D.22: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-26).................................................................................................................. 188

Figure D.23: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-27). .................................................................................................................. 189

Figure E.1: Plots of arguments and digital signals (Case 5-5). ....................................... 191

Figure E.2: Plots of arguments and digital signals (Case 5-6). ....................................... 191

Figure E.3: Plots of arguments and trip signals (Case 5-7). ........................................... 192

Figure E.4: Plots of arguments and trip signals (Case 5-8). ........................................... 192

Figure E.5: Plots of arguments and trip signals (Case 5-9). ........................................... 192

Figure E.6: Plots of arguments and trip signals (Case 5-10). ......................................... 192

Figure E.7: Plots of arguments and trip signals (Case 5-11). ........................................ 193

Figure E.8: Plots of arguments and trip signals (Case 5-12). ......................................... 193

Figure E.9: Plots of arguments and trip signals (Case 5-13). ......................................... 193

Figure E.10: Plots of arguments and trip signals (Case 5-14). ....................................... 193

Figure E.11: Plots of arguments and trip signals (Case 5-15). ....................................... 194

Figure E.12: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-63) ................................................................................... 196

Figure E.13: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-64) ................................................................................... 196

Figure E.14: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-65) ................................................................................... 196
Figure E.15: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-66) ................................................................. 196

Figure E.16: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-67) ................................................................. 197

Figure E.17: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-68) ................................................................. 197

Figure E.18: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-69) ................................................................. 197

Figure E.19: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-70) ................................................................. 197

Figure E.20: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-71) ................................................................. 198

Figure E.21: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-72) ................................................................. 198

Figure E.22: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-73) ................................................................. 198

Figure E.23: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-74) ................................................................. 198

Figure E.24: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-75) ................................................................. 199

Figure E.25: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-76) ................................................................. 199

Figure E.26: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-77) ................................................................. 199
Figure E.27: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-78) ................................................................. 199

Figure E.28: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-79). ................................................................................... 200

Figure E.29: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-80). ................................................................................... 200

Figure E.30: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-81) ................................................................. 200

Figure E.31: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-82) ................................................................. 200

Figure E.32: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-83) ................................................................. 201

Figure E.33: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-84) ................................................................. 201

Figure E.34: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-85) ................................................................. 201

Figure E.35: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-86) ................................................................. 201

Figure E.36: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-87) ................................................................. 202

Figure E.37: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-88) ................................................................. 202

Figure E.38: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-89) ................................................................. 202
Figure E.39: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-90) ........................................................................................................... 202

Figure E.40: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-91) ............................................................................................................. 203

Figure E.41: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-92) ............................................................................................................. 203

Figure E.42: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-93) ............................................................................................................. 203

Figure E.43: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-94) ............................................................................................................. 203

Figure E.44: Plots of phase A current, arguments and trip signals in the event of external A-g fault with CT saturation at location F1 (Case 5-103) ................................................................. 204

Figure E.45: Plots of phase B current, arguments and trip signals in the event of external BC fault with CT saturation at location F1 (Case 5-104) ................................................................. 204

Figure E.46: Plots of phase C current, arguments and trip signals in the event of external BC-g with CT saturation at location F1 (Case 5-105) ................................................................. 205

Figure E.47: Plots of phase A current, arguments and trip signals in the event of external ABC fault with CT saturation at location F1 (Case 5-106) ................................................................. 205

Figure E.48: Plots of phase A current, arguments and trip signals in the event of external A-g with CT saturation at location F1 (Case 5-107) ................................................................. 206

Figure E.49: Plots of phase B current, arguments and trip signals in the event of external BC with CT saturation at location F1 (Case 5-108) ................................................................. 206

Figure E.50: Plots of phase C current, arguments and trip signals in the event of external BC-g with CT saturation at location F1 (Case 5-109) ................................................................. 207
Figure E.51: Plots of phase C current, arguments and trip signals in the event of external ABC with CT saturation at location F1 (Case 5-110) ......................................................... 207
List of Appendices

Appendix A  Modeling of Two-Core Asymmetrical Phase Shifting Transformer……165
Appendix B  Signal Processing…………………………………………………………..173
Appendix C  Power System Simulation Models………………………………………178
Appendix D  Additional Simulation Results of Electromagnetic Differential Protection
..........................................................................................................................183
Appendix E  Additional Simulation Results of Directional Comparison-Based Protection…………………………………………………………………………191
List of Abbreviations (Acronyms)

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 Ph</td>
<td>Three Phase</td>
</tr>
<tr>
<td>CB</td>
<td>Circuit Breaker</td>
</tr>
<tr>
<td>CT</td>
<td>Current Transformer</td>
</tr>
<tr>
<td>CVT</td>
<td>Capacitor Voltage Transformers</td>
</tr>
<tr>
<td>DCB</td>
<td>Directional Comparison-Based Protection</td>
</tr>
<tr>
<td>DCMP</td>
<td>Differential Current Measuring Principle</td>
</tr>
<tr>
<td>DFT</td>
<td>Discrete Fourier transformer</td>
</tr>
<tr>
<td>DHP</td>
<td>Delta-hexagonal PST</td>
</tr>
<tr>
<td>EDP</td>
<td>Electromagnetic differential protection</td>
</tr>
<tr>
<td>EDU</td>
<td>Electromagnetic Differential Unit</td>
</tr>
<tr>
<td>EMTDC</td>
<td>Electromagnetic Transient Including DC</td>
</tr>
<tr>
<td>EMTP</td>
<td>Electromagnetic Transients Program</td>
</tr>
<tr>
<td>E-side</td>
<td>Exciting Winding Terminal</td>
</tr>
<tr>
<td>EW</td>
<td>Exciting Winding</td>
</tr>
<tr>
<td>FACTS</td>
<td>Flexible Alternating Current Transmission System</td>
</tr>
<tr>
<td>L-side</td>
<td>Load Side</td>
</tr>
<tr>
<td>OLTC</td>
<td>On-Load Tap Changer</td>
</tr>
<tr>
<td>Ph-g</td>
<td>Phase-to-Ground</td>
</tr>
<tr>
<td>Ph-ph</td>
<td>Phase-to-Phase</td>
</tr>
<tr>
<td>POW</td>
<td>Point on Wave</td>
</tr>
<tr>
<td>PSCAD</td>
<td>Power Systems Computer Aided Design</td>
</tr>
<tr>
<td>PST</td>
<td>Phase Shifting Transformers</td>
</tr>
<tr>
<td>RTDS</td>
<td>Real Time Digital Simulator</td>
</tr>
<tr>
<td>SDP</td>
<td>Standard Delta PST</td>
</tr>
<tr>
<td>SIR</td>
<td>Source Impedance Ratio</td>
</tr>
<tr>
<td>S-side</td>
<td>Source Side</td>
</tr>
<tr>
<td>SW</td>
<td>Series Winding</td>
</tr>
<tr>
<td>VT</td>
<td>Voltage Transformer</td>
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Chapter 1

Power System Protection

An electrical power system comprises a complex network of elements such as generators, transformers, transmission and distribution lines, etc. For a stable and secure operation of a power system, these elements must perform their function continuously, so that the system quantities or parameters, such as voltage, current, impedance, frequency, power and power direction, remain within tolerable limits [1]. However, faults, which are random in nature, result in the change of system parameters that can be in, or out, of the range of tolerable limits. Occurrence of faults, therefore, can occur at any time and at any location within the power system network. Although an occurrence of a fault is rare, every element of a power system endures some failure or disturbance eventually.

For a safe and secure operation, such that minimizes risk to human life and damage to expensive power system elements, it is of utmost importance that steps must be taken in order to remove the faults in a very selective and fast way [2]. To detect and disconnect the faulted element of a power system network, the provision of an adequate protection system is very important. Protective relays, together with the other elements of power system protection, e.g. breakers and fuses, serve to provide a safe operation of a power system network with minimum damage to people and property in the occurrence of any fault or disturbance.

1.1. Zones of Protection

A protection system is responsible for isolating a faulty area of a power system network so that the rest of the power system continues to operate without severe damage due to a high fault current. A protection zone defines the portion of a power system such that any fault anywhere in the zone is detected and isolated from rest of the power system by the protective system responsible for that zone. As shown in Figure 1.1, each zone represents one or more power system elements such as generator, transformer, busbar, transmission...
line and motor. On occurrence of fault, isolation of zone is done by circuit breakers, therefore circuit breaker define the boundary of the zone, each zone represents one or more power system elements such as the generator, transformer, busbar, transmission line or motor. In the event of a fault, zones are isolated by the circuit breakers. Therefore, a circuit breaker defines the boundary of the zone.

Another aspect of protection zones is that the overlapping of two neighboring zones helps in the detection of faults in the unprotected portion of the zone. In the event of a fault in the overlapping of zones, both neighboring zones are isolated, and hence a larger part of the power system, which corresponds to both zones involved in the overlap, will be isolated. Therefore, the overlapping zone is normally made as small as possible.

1.2. Aspects of the Protection System

A. Reliability

Reliability is the most important requisite of applying a protective relay. Faults are rare in nature, and therefore the relay remains inoperative for a long time, but when a fault occurs, the relays must respond instantly and correctly. Two important attributes of reliability are dependability and security [3]. Dependability implies that protection relays must operate when they are required to operate. Whereas, security implies that the relay must operate when it is not required to operate.
B. Speed

To minimize any damage to the power system equipment due to a fault, a protective system must respond quickly and isolate the faulted zone from the rest of the power system by operating the zone circuit breakers.

C. Discrimination or Selectivity

As mentioned before, a relay must respond to a fault within its zone of protection and isolate the faulted zone or element from the rest of the power system. Discrimination is mainly of two kinds: absolute and dependent. Absolute discrimination implies that the protection system detects and discriminates the fault in an out of the defined zone of protection and responds to faults that lie in its zone of protection [4]. Examples include unit protection systems such as generator, transformer or busbar protection. Dependent or relative discrimination implies that a protection system responds to faults based on a correlation or co-ordination with the other protective relays that also detect the same abnormal condition.

D. Sensitivity

Sensitivity of the relay refers to the minimum operating level of the operating quantities, such as current in over-current or differential relays and voltage in over- or under-voltage relays [2], [4]. For instance, a transformer current differential protection must be sensitive enough to detect low current faults.

1.3. Basic Protection Principles

Most of the relays can be classified based on the protection principles they present. According to reference [5], protection principles can be classified as:

A. Magnitude Relays

The operating quantity defined in these relays corresponds to the magnitude of the input measuring quantity. For example, over-voltage relay operates if the voltage magnitude
(peak or rms) exceeds the defined threshold or pickup setting defined by the protection engineer. Another common example of magnitude relay is over-current relay.

B. Directional Relays:

These relays react to a fault in the defined directions. The direction of a fault can normally be known from the phase angle between the operating and reference, or polarizing, quantity. For example, the phase angle between a current and a voltage is commonly used in directional relays, or the phase angle of one current may be compared with that of another current.

C. Ratio Relays

These relays operate by monitoring the operating quantity calculated by taking the ratio of the two input signals that are expressed in phasor quantities. Ratio relays can be designed to operate using the magnitude or phase, or a combination of both. Distance and directional comparison relays are the most common types of ratio relays.

D. Differential Relays

A differential relay is always used as a unit protection. The operating principle of the differential relay is to monitor the current entering and leaving the zone of protection. During the normal or external fault conditions, the current measured into the zone is always equal to the current leaving the zone, and therefore the vector sum of both currents is always zero (ideally). However, in the event of internal fault conditions it measures a large differential current. Differential protection is commonly used for the protection of transformers, motors, generators and short-transmission lines.

1.4. Transformer Protection

A transformer is one of the most important and expensive elements in a power system network. Transformers are available in various types, and therefore can be classified based on purpose, design and construction, number of phases, etc. However, common types of transformers are substation, distribution, autotransformer, phase shifter and
zigzag. Applications of these transformers are everywhere in the power system, and therefore a fault in a transformer can result in a whole or partial discontinuity of the power supply. In the event of a fault, if a transformer is not isolated quickly, this fault can lead to severe damage and interruption of the power supply. Thermal stress due to a high fault current can result in the deterioration of the winding insulation. To minimize damage, and for a reliable and secure power system operation, proper transformer protection – both electrical and mechanical – is very important. Features like sensitivity and security must be considered when applying a transformer protection system.

The three main objectives of transformer protection are:

1. Detection of internal faults with high sensitivity
2. High speed isolation of the transformer in the event of a fault
3. Security/stability against the external fault, or no-faulted, system conditions for which tripping of the transformer is not required.

Proper protection minimizes the cost of repair, production loss, adverse effect on the balance of the system, damage to the adjacent equipment and the period of unavailability of the damaged equipment [6]. Therefore, proper protection with a high speed of operation and sensitivity is very important, especially in the cases where there are HV power transformers involved.

Typical statistics of fault distribution over the power system network shows that transformer faults account for 12–20% of the total number of faults over the period of one full year. Transformer faults can be categorized based on the internal and external conditions. Internal faults can be categorized as: winding phase-to-phase, phase-to-ground faults; winding inter-turn faults; core insulation failure; shorted laminations; over fluxing and tank faults. Whereas, external applied conditions could result in overloads, overvoltage and over fluxing [2].

The type of protection system employed depends on the application, size and importance of the transformer. Depending on the application, transformers are normally available in a wide range of ratings – typically from a few kVA to hundreds of MVA. Primary
protection is needed against faults and overload conditions. There is no single standard available to protect all kinds of the transformers [6]. The most cost-effective schemes with a high speed and sensitivity are desirable. Transformers larger than 5 MVA are usually equipped both with electrical and mechanical types of relays. Commonly used electrical protection principles are: current differential, over-current, earth-fault and overload protections. Whereas, mechanical relays are pressure guard (Buchholz-relay), and pressure relay for the tap changer compartment and oil-level monitor. However, transformers smaller than 5MVA are usually equipped with over-current and earth-fault protections.

1.5. Phase Shifting Transformers

Phase shifting transformers are widely used for the control of power flow over parallel transmission lines. Power flow control becomes necessary in today’s deregulated power system market, when parallel transmission paths are owned or operated by different operators. PST offers a complete, reliable and more economical solution for the control of power flow as compared to FACTS devices [7]. PSTs are available in unique designs and constructions when compared to the standard power transformers. Moreover, they are among the most expensive transformer kinds in their family.

These transformers are available in various design and application types, depending on the power system application. Based on design and construction, they are available in two-core (indirect) and single-core (direct) constructions. Based on the application type, they can be categorized as symmetrical or asymmetrical. According to reference [8], a symmetrical design alters the phase angle with equal magnitudes of source- and load-side voltages, whereas an asymmetrical design alters the phase shift and voltage magnitude, which can cause changes in the reactive power flow. The advantage of the symmetrical design over asymmetrical is that the phase shift angle is the only parameter that influences the power flow.
1.6. Research Objective

Power system protection ensures a reliable and stable operation of the power system equipment. Standard and phase shifting transformers are normally protected by various protection elements and differential protection is considered as the main protection technique. Differential protection is known for its distinguished features such as speed and selectivity. However, it is also known that it has a strong association with the various traditional challenges such as magnetizing inrush current, saturation of core, CT ratio mismatch, compensation of zero-sequence current, external fault with CT saturation, etc.

A phase shifting transformer represents both magnetically coupled and electrically connected zones of protection, thus making it unique in design from the standard transformer that only represents the magnetically coupled zone. Therefore, standard current differential protection that reflects ampere-turn relation (of the magnetically connected windings) cannot offer a complete overall protection solution for a PST. Moreover, various existing proposed solutions, based on differential protection, encounter a number of various new challenges in addition to conventional ones that could result in jeopardizing the security and sensitivity of the PST current differential protection. New and traditional challenges, and the performance of existing differential-based techniques, lead and motivate us to the development of new protection approaches that ensure a solution that is not prone to these challenges.

Primarily, the scope of the research work was mainly to develop a new protection technique. However, the unavailability of the PST short circuit and simulation models that must represent an accurate mimic of the PST, leads us to the development of the modeling of the various kinds of PST for short circuit and protection studies. Therefore, this research work mainly focuses on the development of PST protection as well as modeling.

Phase I: A phase shifting transformer is categorized based on the application and construction type. Therefore, there is no standard model available that represents all kinds of PST. This work presents modeling of three kinds of PSTs: single-core standard delta, two-core symmetrical and two-core asymmetrical. The modeling approach is based on
the development of sequence (positive, negative and zero) impedance-based networks of PSTs. The established sequence-based models can be used for both balanced and unbalanced system conditions. Unlike existing PST models, the proposed model does not rely on the availability of the manufacturer’s test report data. The derived relations are used to estimate the various transformer parameters necessary to develop the simulation and short circuit models. Validation of the proposed models is done by comparing the results obtained from our proposed model and the real transformer test report data from the manufacturer. Validation results show that the presented transformer models are accurate enough and represent a good mimic of real PSTs.

Phase II: The second phase of the research work consists of the development of new protection strategies that solve the problems associated with the conventional differential protection techniques. This work considers two protection approaches applied previously for the protection of the standard transformers. These approaches are based on the electromagnetic differential protection (EDP) based method and the directional comparison-based technique. Correct implementation of these techniques for the protection of various kinds of PSTs comes across various problems, and hence leads us to the proposed solution of those issues. Both techniques solve the problems of conventional challenges such as magnetizing inrush current, core saturation, non-standard phase shift, external fault with CT saturation, etc. The electromagnetic differential protection method can only be applied to the PST it represents. However, the directional comparison-based approach can be applied to any kind of PST.

The main contributions of the thesis are:

- Performance analysis of the traditional and alternate PST current differential-based protection techniques.
- Development of short circuit and EMTP models of single-core standard-delta, and two core PSTs.
- Development of a new protection algorithm based on the electromagnetic differential protection principle for standard-delta and delta-hexagonal PSTs.
- Development of a universal protection algorithm based on the directional comparison-based technique.

1.7. Thesis Outline

Chapter 2 gives an overview of the phase shifting transformer. Various types of PSTs are discussed in more detail, and this is followed by the basic working principle of a PST. The existing available short-circuit and EMTP models are discussed based on the literature surveys. The second part of the chapter discusses the traditional and alternate current differential-based approaches in addition to the basic standard transformer current differential protection. Moreover, various differential current measuring principles are discussed, and this is followed by an outline of the limitations of the conventional differential approaches.

Chapter 3 presents the proposed mathematical modeling of standard-delta and two-core phase shifting transformers. It also presents a validation of the proposed models using the manufacturers test report data. Moreover, EMTP modeling based on the proposed mathematical models in commercially available EMTP tools – like RTDS and PSCAD/EMTDC – is also presented in chapter 3.

The development of the new protection algorithm based on electromagnetic differential protection principles for standard-delta and delta-hexagonal PSTs are presented in Chapter 4. This chapter also discusses and addresses various problems associated with these techniques – followed by the proposed solutions. Various tests are performed to check and validate the performance of the proposed algorithms in EMTP-based tool PSCAD.

Chapter 5 presents the development of the PST universal protection algorithm based on the directional comparison philosophy that can be applied for the protection of all types of PSTs. Various challenges, along with the solutions, are presented to make the proposed solution more sensitive and secure. Various tests are performed to check the performance of the proposed solution.
Chapter 7 summarizes the presented work and presents a brief performance comparison between the old and newly presented protection techniques. This chapter is followed by a list of references. Appendix A presents the proposed short-circuit modeling of the two-core asymmetrical PST. Appendix B describes the analog and digital signal processing approaches followed by phasor estimation using a discrete Fourier transformer (DFT). Appendix C lists the data and configurations of the power system simulation models used for the testing and verification of the proposed techniques. Additional simulation results are provided in Appendix D and E.

1.8. List of Publications


1.9. Summary

This chapter has briefly introduced the importance and basic concepts of power system protection. Both standard and phase shifting transformers current differential protection
principles have been reviewed. Various issues and challenges associated with the modeling and protection of phase shifting transformers have been outlined—followed by the thesis organization and list of publications. A literature review of the phase shifting transformers modeling and protection will be discussed in the following chapter.
Chapter 2

Phase Shifting Transformers - Modeling and Protection

This chapter presents a detailed review of the basic working principle and types of phase shifting transformers. A literate survey reviews the existing PSTs modeling methodologies and current differential-based protection approaches. Comparative performance analyses of the various current differential measuring principles are presented to show the importance of the thesis research work scope.

2.1. Phase Shifting Transformers

With the growth of power system networks, the control of active power over parallel transmission lines is very important. Due to the deregulation of the electricity market, today’s transmission systems are not as simple as they were in the past; the loading of the parallel transmission lines now depends on the contractual transmission path. The transfer of power flow over the parallel transmission system is achieved using power-flow control devices. These devices actually transfer power flow from an overloaded transmission line of the power system to lines with free transmission capability. Phase shifting transformers (PSTs) present an economical and reliable solution as compared with flexible alternating current transmission system (FACTS) devices, e.g., dynamic-flow controller and unified/interline power-flow controller [7], [8].

The active power flow over the transmission line is given as follows:

\[ P = \frac{|V_1||V_2|}{Z_L} \sin \alpha \]

where \( V_1 \) and \( V_2 \) are the sending- and receiving-side voltages, respectively, \( \alpha \) is the phase shift between \( V_1 \) and \( V_2 \), and \( Z_L \) is the reactance of the transmission line.
The flow of the active power over the transmission line can be achieved by controlling the voltages, but this is not a useful solution because of the greater influence of voltage on the reactive power. By lowering the reactance of the transmission line using the capacitor in series, the control of power flow can be achieved [8]. The third method is by varying the phase shift between two ends voltages using phase shifting transformers.

2.1.1. Basic Working Principle

As shown in Figure 2.1(a), with PST, the power flow is controlled by changing the phase shift angle between the PST source- and load-side voltages – \( V_S \) and \( V_L \), respectively. The subscripts S and L correspond to the PST source and load sides, respectively. Phase shift \( \delta \) can be varied by adding the varying quadrature voltage (\( \Delta V \)) between the two ends voltages, as shown in Figure 2.1(b). Assuming inductive load, the quadrature voltage must be 90° phase lag or lead to the load-side voltage (\( V_L \)). Therefore, phase shift can be advanced or retarded; advanced phase shift means that the load-side terminal voltage leads the source-side terminal voltage; retard phase shift means that the load-side terminal voltage lags the source-side terminal voltage [9].

The phase shifting transformers are available in various designs and types; however, they use the same basic technique to create the quadrature voltage. Quadrature voltage (\( \Delta V \)) can be obtained using the delta or quadrature windings. The source and load sides are connected by the secondary delta-winding (series winding); whereas primary delta-winding (exciting winding) is connected to the other two phases to obtain the delta-voltage by simply subtracting the other two phases from each other. Therefore, under load conditions, a change in \( \Delta V \) can be obtained by using the on-load tap changer (OLTC).

2.1.2. Types of Phase Shifting Transformers

Phase shifting transformers are mainly categorized into four types, each with a different design and construction. Each design uses the same basic methodology to create the quadrature voltage by simply subtracting the other two phases from each other at the exciting winding, whereas the source and load sides are connected to the series winding.
A PST can be constructed as two-core (indirect) or single-core (direct). Both types of constructions have advantages and disadvantages.

According to [8], a symmetrical design alters the phase angle with equal magnitudes of source- and load-side voltages, whereas an asymmetrical design alters the phase shift and voltage magnitude, which can cause changes in the reactive power flow. The advantage of a symmetrical design over asymmetrical is that the phase shift angle is the only parameter that influences the power flow. However, it uses two single-phase OLTCs per phase and therefore, it is more costly than the asymmetrical design. Asymmetrical design alters both phase shift and voltage magnitude. It is known from the aforementioned discussion that a variation in voltage has greater influence on reactive power than active power.

Figure 2.1: Application and working of a phase shifting transformer a) parallel transmission system with PST; b) demonstration of phase shift angle and quadrature voltage.
Figure 2.2 shows three single-core design types. The single-core design can be constructed as standard-delta symmetrical (Figure 2.2(a)), delta-hexagonal symmetrical (Figure 2.2(b)) and squashed-delta asymmetrical (Figure 2.2(c)). The single-core design is simple and economical. An on-load tap changer(s) is installed on the series winding that is connected with the system source and load sides. The two main disadvantages of this type of construction are: OLTC(s) exposure to over-voltages and through-faults; secondly, to prevent the OLTC from system over-voltages and through-fault currents, the OLTC must be selected with higher specifications; however, it’s not an economical solution. Moreover, the short-circuit impedance of the PST varies between maximum and zero, therefore influencing the contribution of fault currents in the system [10].

Figure 2.3 and Figure 2.4 show two types of commonly used two-core designs: symmetrical (Figure 2.3) and asymmetrical (Figure 2.4) [8], [9]. These types consist of

![Schematic diagrams of single-core PSTs](image)

Figure 2.2: Schematic diagrams of single-core PSTs (a) standard-delta symmetrical, (b) delta-hexagonal symmetrical, and (c) squashed-delta asymmetrical.
series and exciting units. As shown in Figure 2.3, the source and load sides are connected to the series unit primary winding, whereas primary windings of the exciting unit are connected to the system voltage level. The secondary windings of the series unit are connected with the other two phases of the secondary of the exciting unit, therefore making a delta connection to create the quadrature voltage [9]. Quadrature voltage can be controlled or changed by the OLTC installed at the secondary of the exciting unit.

The two-core construction is not as economical as the single-core, but has the advantages of a non-direct connection between the exciting unit and the system, neutral grounding, and a constant zero sequence impedance. Moreover, it offers greater flexibility in selecting the step voltage and the current of the regulating winding.

2.2. Modeling of the Phase Shifting Transformers

For the protection and short-circuit studies, it is important to have a good representation of the system, or power system element, under investigation. The transformer can be modeled either based on the core geometrical information of the windings and core, or from measured parameters (leakage inductance, resistance) at the terminal of the transformer at the manufacturer’s facility.

Modeling based on the core geometrical information requires the exact core dimensions, along with the number of turns and its magnetic characteristics. However, core information is not generally available. As shown in Figure 2.5, the core information generally required is the magnetic path length or length of the limb/yoke, the cross-sectional area of the winding limb/yoke and the permeance of the limb/yoke. Using the geometrical information, winding impedance parameters (self and mutual impedance) can be calculate to model the transformer [11].

Modeling based on the winding parameters measured from the terminal short- and open-circuit tests at the manufacturer’s facility is generally considered as more simpler and practical because of the availability of information. Nameplate information contains the total effective or apparent impedance of the transformer obtained from the short- and open-circuit tests.
Figure 2.3: Schematic diagram of a two-core symmetrical PST.

Figure 2.4: Schematic diagram of a two-core asymmetrical PST.
The leakage impedance of the windings can be approximated using the total effective impedance and number of winding turns. For instance, in a standard two windings transformer, the voltage across the windings can be represented by equations (2.1) and (2.2).

\[ V_1 = R_{11} I_1 + L_{11} \frac{d}{dt} I_1 + M_{12} \frac{d}{dt} I_2 \]  \hspace{1cm} (2.1)

\[ V_2 = M_{21} \frac{d}{dt} I_1 - R_{22} I_2 - L_{22} \frac{d}{dt} I_2 \]  \hspace{1cm} (2.2)

where

- \( V_1 \) and \( V_2 \) are the terminal voltages across winding 1 and winding 2, respectively.
- \( I_1 \) and \( I_2 \) are the terminal currents in winding 1 and winding 2, respectively.
- \( R_{11} \) and \( R_{22} \) are the resistances of winding 1 and winding 2, respectively.
- \( L_{11} \) and \( L_{22} \) are the leakage inductances of winding 1 and winding 2, respectively.
$M_{12}$ and $M_{21}$ are the mutual impedances between winding 1 and winding 2.

Mutual impedances ($M_{12}, M_{21}$) between winding 1 and winding 2 are considered equal in a linear transformer model and therefore can be replaced by $M$ [12]. The model takes into account the winding resistances ($R_{11}, R_{22}$) and the leakage inductances ($L_{11}, L_{22}$).

As shown in Figure 2.6(a), using (2.1) and (2.2), the equivalent impedance of the windings ($Z_{wdg1}, Z_{wdg2}$) can be represented as

\begin{align*}
Z_{wdg1} &= R_{11} + wL_{11} + wNM \\
Z_{wdg2} &= NwM - N^2(R_{22} - wL_{22})
\end{align*}  \tag{2.3} \tag{2.4}

where

$Z_{wdg1}$ and $Z_{wdg2}$ are the equivalent impedance of the windings 1&2, respectively.

$N$ is the turn-ratio between winding 1&2.

Equations (2.3) and (2.4) are the equivalent impedances of winding 1 and winding 2 at as seen at winding 1 of the transformer, respectively. The overall impedance of the transformer can be represented as [13].

\[ Z_{wdg12} = Z_{wdg1} + Z_{wdg2} \tag{2.5} \]

As mentioned before, impedance ($Z_{wdg12}$) is the total effective or apparent leakage impedance of the two-winding transformer. It is normally obtained from the short-circuit test of the transformer. The short-circuit test is done by making winding 2 short and applying the voltage at winding 1, as shown in Figure 2.6(b). It is justified to assume that the shunt impedance (or magnetizing branch impedance) $M$ is significantly larger than $L_2$. Therefore, from the short-circuit test, the magnetizing branch can be neglected and therefore, by measuring the current the equivalent impedance $Z_{wdg12}$ can be calculated as
Similarly, from the open circuit test, as shown in Figure 2.6(c), we can determine the magnetizing current \( I_m \) which during the open circuit test equals \( I_1 \). Therefore, the mutual impedance \( M \) can be calculated from the applied voltage and measured current.

\[
Z_{wdg12} = \frac{V_1}{I_1}
\]

Similarly, from the open circuit test, as shown in Figure 2.6(c), we can determine the magnetizing current \( I_m \) which during the open circuit test equals \( I_1 \). Therefore, the mutual impedance \( M \) can be calculated from the applied voltage and measured current.

From the above discussion, it can be concluded that to determine the winding parameters (self and mutual inductances) one must have the measurements from the short-circuit and open-circuit tests. In practice, the nameplate information, that contains \( Z_{wdg12} \) or the
equivalent impedance (positive- and/or zero-sequence) and the magnetizing current, can easily be obtained from the manufacturer. From these two parameters, we can further calculate the winding parameters.

However, due to the unique and complex designs of PSTs, the positive- and zero-sequence impedances (total apparent or effective impedances), obtained by the short-circuit tests, cannot be used in a straightforward way to approximate the impedances of the single-phase windings of the PST. In this context, the only useful relationships, that we have found, between the total effective impedance and windings’ impedances are derived in reference [12]. However, the relations are not derived as a function of tap position but are mainly useful at maximum tap position. The nameplate information of a PST only contains the positive sequence impedance (and zero-sequence impedance) at the maximum tap position. Unlike a standard transformer, the nameplate information is not enough to model the PST for all tap positions. Therefore, to approximate the windings impedances, using those relations, we require detail test report data from the manufacturer, which is not easy to obtain from the manufacturer. Secondly, in complex design types of PSTs, it is not easy to segregate total effective impedance into windings impedances.

There are a few other models suggested in this context [14]-[19]. Reference [14] gives some very brief suggestions for the short-circuit modeling of the PST but lacks in establishing the complete short-circuit model. Short-circuit modeling based on the sequence impedance of the hexagonal PST is proposed and validated with the manufacturer test data in [15]. Reference [16] suggests the winding parameter (impedance and resistance) estimation for the two-core PST using the apparent impedance measured by the manufacturer at each tap position. References [17]–[19] also suggest modeling of the two-core symmetrical and hexagonal PSTs, respectively, based on the test report data.

Moreover, most of the available models represent a balanced system. However, for short-circuit and protection studies it is important to have a model that also represents unbalanced system conditions (symmetrical component-based). Also there is no EMTP
model available in tools like PSCAD and RTDS for various kinds of PSTs. To model a PST in EMTP, existing models have to rely on detailed test report data from the manufacturer.

2.3. Protection of the Phase Shifting Transformers

2.3.1. Current Differential Protection

For many years, current differential protection has been widely used for the protection of busbars, generators, transformers and lines. Speed and selectivity are the two main advantages of differential protection, and it therefore only responds to faults within the boundary of the protected zone in a very fast manner.

As shown in Figure 2.7, the percentage differential characteristic is used to discriminate between internal and external faults by comparing the differential vs. restrain point with the defined characteristic. The differential protection technique is based on the comparison of the differential current ($I_{diff}$) with the restraining current ($I_{res}$) [6]. Differential current is measured using Kirchhoff’s law by taking the vector sum of the current entering and leaving the zone of protection. The zone of differential protection is normally defined by the positioning of the current transformers (CTs). However, the zone of protection can be the representation of either a magnetically coupled circuit (e.g. transformer) or electrically connected circuit (e.g. busbar or lines). Any change in the defined zone leads to an imbalance between the current entering and leaving the zone and, therefore, results in the differential current. Therefore, current differential protection is sensitive to most of the internal faults. However, the sensitivity of differential protection is dependent on the fault-current level.

Differential and restrain currents for a standard two winding transformer can be defined as

$$I_{diff} = |I_1 + I_2|$$

$$I_{res} = |I_1| + |I_2|$$
Figure 2.7: Standard transformer differential protection: (a) schematic diagram of a two-winding transformer with differential relay, (b) percentage differential relay characteristic.

According to the above relations, ideally in the event of an internal fault, $I_{\text{diff}}$ and $I_{\text{res}}$ are equal to the fault current, while in the event of an external fault, $I_{\text{diff}}$ is zero and $I_{\text{res}}$ is equal to double the fault current.

2.3.2. Differential Current Measuring Principles (DCMP)

As mentioned previously, differential current is measured based on Kirchhoff’s law by taking the vector sum of the current entering and leaving the circuit (zone). The differential current measuring principle (DCMP) reflects the kind of circuit it represents. Therefore, based on the circuit types and algorithms used to measure differential current, we can distinguish and categorize the differential current measuring methods as follows:
• DCMP 1: Differential current measuring principle that reflects the ampere-turn relation of the magnetically-coupled transformer windings like in a standard transformer, as shown in Figure 2.8(a).

• DCMP 2: Differential current measured by taking the vector-sum of the current entering and leaving the electrically connected circuit like in bus-bar, as shown in Figure 2.8(b).

• DCMP 3: Differential current measured by taking the vector-sum of the reference and compensated currents without knowing the type of zone it represents, as shown in Figure 2.8(c).

2.3.3. Phase Shifting Transformer Differential Protection

As with a standard transformer, biased differential protection has been used as a main form of protection for phase shifting transformers. Unlike a standard transformer, due to the unique design and construction of a PST, the current distribution inside the PST represents both magnetic and electric circuits. Therefore, various old and new differential protection-based approaches [14], [19]–[21] could be distinguished based on the differential current measuring principle that reflects the type of circuit it is representing.

Approach 1 [14]

Reference [14] proposes the current differential methods for the protection of two-core symmetrical (Approach 1A) and single-core hexagonal PST (Approach 1B).

Figure 2.8: Differential current measuring principles of: (a) magnetically-coupled circuit, (b) electrically-connected circuit, and (c) compensated two end currents.
1) **Approach 1A:** Due to the complex design of a PST, the availability of the terminal currents of all windings is not always possible, thus the PST zone of protection is divided into two sub-zones of protection. As shown in Figure 2.9, differential relay 87S protects the magnetically-couple zone of series unit windings and is extended to the secondary winding of the exciting unit. The differential current measuring principle reflects the ampere-turn (DCMP 1) relation of the magnetically-coupled series unit windings as

\[
IDIFF_{(87S_A)} = \left| \frac{1}{N_s} (I_{SC} + I_{LC}) - \frac{1}{N_s} (I_{SB} + I_{LB}) - I_{eA} \right|
\]

\[
IDIFF_{(87S_B)} = \left| \frac{1}{N_s} (I_{SA} + I_{LA}) - \frac{1}{N_s} (I_{SC} + I_{LC}) - I_{eB} \right|
\]

\[
IDIFF_{(87S_C)} = \left| \frac{1}{N_s} (I_{SB} + I_{LB}) - \frac{1}{N_s} (I_{SA} + I_{LA}) - I_{eC} \right|
\]

where \(I_{SA}, I_{SB}, I_{SC}\) and \(I_{LA}, I_{LB}, I_{LC}\) are the source- and load-side currents and \(I_{eA}, I_{eB}, I_{eC}\) are the currents in the secondary windings of the exciting unit.

Differential relay 87P protects the electrically connected zone of the series- and exciting-unit primary windings (DCMP 3). The distribution of the series winding is such that the differential current can be written as

\[
IDIFF_{(87P_A)} = \left| I_{SA} - I_{LA} - I_{EA} \right|
\]

\[
IDIFF_{(87P_B)} = \left| I_{SB} - I_{LB} - I_{EB} \right|
\]

\[
IDIFF_{(87P_C)} = \left| I_{SC} - I_{LC} - I_{EC} \right|
\]

where \(I_{EA}, I_{EB}, I_{EC}\) are the currents in the primary windings of the exciting unit.

**Approach 1B:** As shown in Figure 2.10, the differential protection of a delta-hexagonal PST comprises two electrically-connected zones of differential protection elements each protecting the electrically connected series (87M) and exciting winding (87N) zones. The
differential current measured (DCMP 2) in the electrically connected series winding zone can be presented as

\[ IDIFF^{(87M_A)} = |I_{SA} - I_{LA} + I_c - I_b| \]

\[ IDIFF^{(87M_B)} = |I_{SB} - I_{LB} + I_a - I_c| \]

\[ IDIFF^{(87M_C)} = |I_{SC} - I_{LC} + I_b - I_a| \]

where \(I_a, I_b, I_c\) are the currents in the exciting windings.

Similarly, the differential current measured (DCMP 2) in electrically connected exciting winding zone can be presented as

\[ IDIFF^{(87N_A)} = |I_a + I_a'| \]

\[ IDIFF^{(87N_B)} = |I_b + I_b'| \]

\[ IDIFF^{(87N_C)} = |I_c + I_c'| \]
Approach 2 [20]

References [20] presents the differential current measuring principle (DCMP 3) using the phase and magnitude compensation algorithm to measure the differential current from the vector sum of the source- and load-side compensated current without considering the PST type and construction. However, as in [20], the algorithm requires a tap position reading and base current at each tap position to compute the differential current. The general differential current measuring principle for both the two-core symmetrical and the delta-hexagonal PSTs is presented by [20] as

\[
\begin{bmatrix}
 IDIFF_A \\
 IDIFF_B \\
 IDIFF_C 
\end{bmatrix} = \frac{1}{I_{base}(D)} M(0^\circ)
\begin{bmatrix}
 I_{SA} \\
 I_{SB} \\
 I_{SC} 
\end{bmatrix} + \frac{1}{I_{base}(D)} M(\delta^\circ)
\begin{bmatrix}
 I_{LA} \\
 I_{LB} \\
 I_{LC} 
\end{bmatrix}
\]

where

\[
M(\delta^\circ) = \frac{1}{3}
\begin{bmatrix}
 1 + 2\cos(\delta) & 1 + 2\cos(\delta + 120) & 1 + 2\cos(\delta - 120) \\
 1 + 2\cos(\delta - 120) & 1 + 2\cos(\delta) & 1 + 2\cos(\delta + 120) \\
 1 + 2\cos(\delta + 120) & 1 + 2\cos(\delta - 120) & 1 + 2\cos(\delta) 
\end{bmatrix}
\]

where \(I_{base}(D)\) is the base current of the source- or load-side as a function of the tap-position (D) and \(\delta\) is the phase shift between the source and load side.

Approach 3 [21]

Reference [21] proposes linear and non-linear current differential techniques for the protection of a delta-hexagonal PST along with the power differential and phase comparison techniques. The differential current measuring principle (DCMP 1) reflects the ampere-turn relation between the magnetically coupled windings. Various differential current measuring principles are presented with and without the requirement of the tap position reading. The linear differential current measuring principle as a function of the tap position is
\[ IDIFF_A = \left( \frac{D+1}{2} + \frac{1}{N} \right) (I_{LC} + I_{SC}) + D(I_{LA} + I_{SB}) \]

\[ IDIFF_B = \left( \frac{D+1}{2} + \frac{1}{N} \right) (I_{LA} + I_{SA}) + D(I_{LB} + I_{SC}) \]

\[ IDIFF_C = \left( \frac{D+1}{2} + \frac{1}{N} \right) (I_{LB} + I_{SB}) + D(I_{LC} + I_{SA}) \]

where \( N \) is the series-to-exciting windings turns ratio.

2.4. Limitations of PST Differential Protection

As discussed before, PST is available in various unique designs and constructions. All of the existing techniques are based on current differential philosophy. However, most of the differential algorithms reflect the type of PST they presents. Unlike the standard transformer differential protection, the same differential current measuring principle cannot be applied to each type of PST. Problems associated with differential protection can be categorized as traditional and non-traditional.

Figure 2.10: Schematic diagram of a delta-hexagonal PST series winding (87M) and exciting winding (87N) differential relays.
2.4.1. Traditional Problems Associated with PST Differential Protection

**Category I**– In the standard current differential protection, the differential current measuring principle reflects the ampere-turn of the magnetically coupled windings. For the proper measurement of the differential current, the current entering the zone of protection must balance (or be equal to) the current leaving the zone during normal system conditions. Therefore, when applying the differential protection to a transformer, the necessary currents compensation must be done prior to the computation of the differential and restraining currents. Compensation is normally done for

- Phase shift due to winding connections across the transformer
- Magnitude mismatch between the currents due to CT ratio mismatch
- Zero-sequence current

Traditionally, phase and magnitude compensation is done by using the external interposing current transformers, as a secondary replica of the main winding connections, or by a delta connection of the main CT’s to provide phase correction only. Today’s microprocessor based relays uses the built-in algorithm which solves the dilemma of magnitude, phase and zero-sequence compensation, thus enabling most combinations of transformer winding arrangements to be catered for, irrespective of the winding connections of the primary CT’s. This avoids the additional space and cost requirements of hardware interposing CT’s. Therefore, conventional differential protection uses well-established solutions to these problems.

**Category II**– Speed and selectivity are the two main advantages of the differential protection. However, it is also known that differential protection is always prone to the conditions that jeopardize the reliability (dependability and security/stability) of the relay. These conditions include:

- Magnetizing inrush current
- External faults with current transformer saturation
- Internal fault right after current transformer saturation
- Saturation of core
**Magnetizing inrush current:** Upon energization of the unloaded transformer, significant inrush currents at the source-side of the transformer can occur, as shown in Figure 2.11(a) obtained for a hexagonal PST. Magnetizing inrush currents phenomena can result in the mal-operation of the current differential relay, as shown in Figure 2.11(b).

The differential current measuring principle that represents the electrically connected zone (Approach 1B) remains stable, whereas Approach 2 that presents DCMP 2 measures a false differential current; however, it is smaller than the differential current measuring principle that reflects the magnetic-coupled zone (Approach 3).

![Figure 2.11: Energization of an unloaded phase shifting transformer (a) magnetizing inrush currents, and (b) differential \( I_{\text{diff}} \) vs. restraining \( I_{\text{bias}} \) current characteristics.](image)
Both approaches, 2 and 3, must be complemented with a blocking or restraining unit to ensure the security of the relay. Blocking of the relay operation solves this problem; however, in the event of an internal fault while the unloaded transformer is energized, traditional differential protection can result in a delay trip operation for the internal fault due to a trip block operation of the relay. Delay in the relay trip operation depends on the magnitude of the second harmonic content. As mentioned before, modern transformers generate a lower level of second harmonic, lowering or reducing the threshold setting may result in more secure operation of the relay, however, dependability is jeopardized. As shown in Figure 2.12, the differential relay operates very slowly for the internal fault during the magnetizing of the PST.

![Graph](image1)

**a)**

![Graph](image2)

**b)**

Figure 2.12: Internal fault during magnetizing inrush currents (a) differential ($I_{\text{diff}}$) vs. restraining ($I_{\text{bias}}$) currents characteristic, and (b) demonstration of delay operation of the differential relay.
**External Fault with CT saturation:** Figure 2.13 shows the performance of the differential relay in the event of a load-side external AB fault with CT saturation. The load-side phase B CT is forced to saturate by increasing the CT secondary burden; the distorted three phase current waveforms are shown in Figure 2.13(a).

Saturation of the CT results in the computation of false differential current, as shown in Figure 2.13(b). The standard differential relay must therefore be complemented with the indicator of CT saturation to block or prevent false operation of the differential relay during an external fault with the CT saturation. However, using the relay blocking during internal fault following the CT saturation can result in the delay operation of the differential relay.

![Figure 2.13: External fault with CT saturation: (a) profiles of load-side three phase currents (b) $I_{\text{diff}}$ vs. $I_{\text{bias}}$ current characteristic.](image)
To prevent tripping due to magnetization of the transformer and saturation of the series winding, differential protection is complemented with an integrated harmonic blocking and/or flux restrained differential technique [22]. Flux restrained differential protection uses the winding currents and BH curve data. Due to the unconventional designs of PSTs, it is not possible to measure all of the winding terminal currents. Hence, an inrush blocking technique based on flux is not a practical solution. The lack of availability of BH curve data is another drawback. The widely used harmonic blocking technique uses a magnitude ratio of the 2nd and 5th harmonic to fundamental current to discriminate the fault from the CT saturation, inrush currents and transformer core saturation. Depending on the size of the transformer harmonic contents, setting is done normally between 15 and 25% of the fundamental component. However, with the new development in transformer design and materials, characteristics of the harmonics have changed in modern transformers [23], [24]. Modern transformers run at a higher flux density and hence generate low harmonic contents during inrush currents [25]. Hence, using the harmonic as an indicator of the false differential current can affect the security of the differential relay.

2.4.2. Non-Traditional Problems Associated with PST Differential Protection

Due to the unique design and construction of PSTs, there are new challenges in addition to the aforementioned traditional challenges associated with the standard transformer differential protection. The new challenges include:

- Non-standard phase shift between source and load sides
- Saturation of series-winding
- Dependence of differential and restraining current on tap-position
- Measurement of winding currents
- Replacement/repair of the buried CT
- Turn-to-turn and turn-to-ground fault detection.

**Non-standard phase shift:** In a standard transformer, the phase shift between the two ends is normally fixed and it is normally the multiple of 30 degrees leading or lagging.
As discussed before, in standard differential protection the phase shift across the transformer can be compensated externally or internally such that the differential current equals zero (ideally). In contrast, the phase shift across the phase shifting transformer is not fixed and is an increment of the non-standard phase-shift angle, and changes online as a function of the tap changer position (e.g. the maximum phase shift across the two ends of the PST is 35.1 deg with 32 steps, i.e. 1.1 deg / step). Therefore, unlike the standard differential protection of the sum of the current entering and leaving the PST, calculating the differential current is not easy or straightforward, and the conventional phase-shift compensation algorithm cannot be applied for the compensation of the phase shift.

If the standard differential protection principle is applied to a PST, a large false differential will be measured, which varies as the phase shift between two ends varies. Sensitivity of the relay will be jeopardized if the minimum pickup is increased so that the false differential current lies below the operating characteristic. Figure 2.14 illustrates the differential current as a function of the tap position.

**Saturation of series-winding:** In all of the PST types, the voltage rating of the series winding, which connects the source- and load-side terminals with the system, is lower than the voltage rating of the system connected [14]. An external fault can result in a significant increase in the terminal voltage (as shown in Figure 2.15a). If the voltage drop across the winding exceeds the volts-per-turn capability of the transformer’s iron core, that core leg can saturate (Figure 2.15(a) shows the distorted current signals due to saturation of series-winding), resulting in an over-excitation condition. This can lead to the mal-operation of the differential protection (as shown in Figure 2.15(c)) in [14]-[19].

**Dependence of differential and restraining current on tap-position:** As reported in [27], although the problem of non-standard phase shift is solved by tracking the tap-position in approaches 2 and 3, the measurement of the differential current still shows dependence on the tap position. The differential current during normal system conditions increases as the phase shift varies from maximum to minimum. A higher slope setting of the differential/restraining characteristic can solve the problem, but sensitivity is
compromised in the event of a low fault current while the PST is operating at higher tap positions.

Measurement of winding currents: The differential protection that represents the magnetically coupled windings is more sensitive to an internal fault than the one using the differential current measuring principles DCMP 2 and DCMP 3 [27]. However, PSTs are available in various unique designs and constructions. It is not always possible to measure the winding currents to calculate the differential current that represents the magnetically coupled windings. For example, a two-core PST can be constructed in one or two tanks. The secondary of the series and exciting windings are normally connected internally. Current measurements are available at the neutral of the secondary winding of the exciting unit. Therefore, conventional differential protection [14] only presents the ampere-turn of the series unit windings. However, it is not practically possible to apply the differential protection that presents the magnetically coupled winding of the exciting unit due to the unavailability of the current measurements on the secondary of the exciting unit terminals.

Figure 2.14: Differential current as a function of tap position (D).
Replacement/repair of the buried CT: The unconventional construction of a PST does not allow access to the secondary of the series and exciting units. Therefore, current transformers are installed during the manufacturing stage of the PST. These CTs are buried in the PST tank. In case of any damage to these CTs, then it is difficult to replace or repair.

Turn-to-turn and turn-to-ground fault detection: In traditional differential protection, the measuring principle of the differential current is based on an ampere-turn balance between the magnetically coupled windings. Any imbalance due to a fault is monitored by the differential protection as a differential current. The differential current produced due to an imbalance in the ampere-turn coupling of the windings depends on the level of the fault current. The level of the fault current depends on the fault resistance, and the number of shorted turns, etc. [26]. Depending on the number of shorted turns, the fault current is very high; however, the differential current is relatively very small [2].
Therefore, the current differential protection has limited sensitivity to turn-to-turn faults. Negative-sequence differential protection is the other solution to detect a turn-to-turn fault [1]. However, it is also insensitive in the event of a low-current turn-turn fault [1]. Another method commonly used is the sudden-pressure or gas-type relay [2].

As reported in [27], a differential technique [14] is not able to detect a turn-to-turn fault in a hexagonal PST and in the primary of the exciting unit of the two-core PST. Detection of the turn-to-turn fault dilemma in a hexagonal PST is solved by [21] and [20]. In a two-core PST, detection of turn-to-turn faults in the primary of the exciting winding is solved by [20] but it loses the detection of series-unit secondary winding faults [27].

2.5. Summary

This chapter presented a brief outline of the basic working principle, types, modeling and differential protection of a phase shifting transformer. The existing available modeling solutions and their limitations are described. Various current differential-based protection principles are outlined, and the traditional and non-traditional problems associated with them are described in detail.

All existing methods based on differential protection have a strong association with conventional and new challenges. These challenges influence the overall performance and proper operation of the differential protection applied to a PST. Therefore, a significant scope of research work still exists for the development of new protection techniques that provide a solution, which shows a good level of immunity to false differential current conditions in addition to internal/external fault discrimination.
Chapter 3

Modeling of Phase Shifting Transformers

This chapter presents the proposed modeling of the single-core standard delta and two-core symmetrical phase shifting transformers for protection and short-circuit studies. Validation of the derived models with the manufacturers’ testing data are presented for both types of PSTs, followed by the inter-turn and turn-to-ground fault modeling and simulation profiles of current and voltage signals during normal and faulted system conditions.

3.1. Introduction

As discussed in section 2.2, to accurately model a PST for both balanced and unbalanced system conditions, the winding impedance at each tap position is required. However, detailed test report data is seldom available from the manufacturer. The nameplate information of the PST is not enough to model the PST with varying phase shift or tap position for the models already available. Detailed test report data must include the measured values of the impedances at each tap position based on short-circuit and open-circuit tests of the actual transformer at the manufacturer’s facility.

This thesis proposes the complete modeling of standard-delta and two-core symmetrical/asymmetrical PSTs based on the approach of deriving the relations for positive-, negative- and zero-sequence impedances as a function of the tap position. Further parameters estimation is done from the derived positive-, negative- and zero-sequence impedances of the whole PST. The same approach has been used for the modeling of hexagonal PST in [15]. Unlike models already available [12], [14], [16]-[19], the presented models of PSTs do not rely on the complete test report data from the manufacturers. The symmetrical component-based model can be accurately used for the short-circuit analysis. The derived model gives us an accurate mimic of the actual PST to study protection and control. Derived winding currents and voltages are functions of the
tap position. This helps in the protection settings, and in studying the behaviors of the system and of winding currents and voltages, with a varying phase change between the source and load sides. This work also presents the modeling of PSTs in the commercially available electromagnetic transient program (EMTP) tools. A real-time digital simulator (RTDS) is used to test, validate, and check the accuracy of the derived models, and to compare this with the test report data of the actual PSTs from the manufacturers.

Additionally, EMTP-modeling of the winding internal faults (turn-to-turn and turn-to-ground) are suggested to simulate the turn-to-turn, turn-to-ground, and winding-to-winding faults for both kinds of PSTs. Phase and fault currents and voltages are of different natures, depending on the type of internal fault, span of the faulted part on the winding, and location of the fault (near or far from the neutral) [26]. Hence, the modeling of PSTs to simulate the internal faults is done keeping in mind the freedom of the varying span of the faulted part of the winding and the location of the turn-to-ground fault from neutral, i.e. close to neutral point or far from neutral point.

3.2. Modeling of Standard-Delta Phase Shifting Transformer

In this section, various expressions for the parameters are derived to accurately model the positive-, negative-, and zero-sequence impedance networks of the standard-delta PST. The accuracy of the derived model is further analyzed and validated with the manufacturer’s test report data.

3.2.1. Calculation of Positive-Sequence Winding Impedances

As shown in Figure 3.1, the tap winding with which the source (S) and load (L) are connected is called the series winding, whereas the excitation winding is connected to the other two phases, making delta connections. Hence, the quadrature voltage $\Delta V$ is developed; this, when added to the nominal voltage $V_n$, will generate the advanced (leading) or retard (lagging) phase shift between the source and the load sides [14]. Advanced phase shift means that the load-side terminal voltage leads the source-side terminal voltage; retard phase shift means that the load-side terminal voltage lags the source-side terminal voltage. As shown in Figure 3.1, on each phase two on-load tap
changers (OLTCs) are installed at source and load side terminals of series winding. Each tap changer is equipped with a change-over-switch (S) to achieve advance or retard phase shift.

As shown in Figure 3.1, tap changer position (D) can be varied between maximum (D=±1 pu) and minimum (D=0 pu) positions. Maximum positive (D=1) and negative (D=-1) tap positions corresponds to advanced and retard phase shift, respectively. The tap changer position D=1 and D=0, as shown in Figure 3.1, corresponds to maximum and minimum tap changer positions. By switching S, the tap position shown in Figure 3.1, can be changed from D=1 to D=-1.

The turn-ratio of the series and exciting windings at a particular tap position D is as follows:

\[
\frac{\Delta V_A}{\Delta V_a} = D \frac{n_A}{n_a} = DN
\]  

(3.1)

where \(\Delta V_A\) and \(\Delta V_a\) are the quadrature voltages across the series and exciting windings, respectively, whereas, \(n_A\) and \(n_a\) are the number of turns in the series and exciting windings, respectively.

Figure 3.1: Winding connections of a standard-delta PST.
The load condition should be taken into account to derive the positive-, negative-, and zero-sequence impedances of the PST as a function of the tap position. The derived equations are further used to calculate the leakage impedance of the single-phase windings of the PST.

As shown in Figure 3.2, it is assumed that the series winding (tapped winding) is equally divided into two windings (source-side and load-side). A linear model [13] of the transformer allows us to assume that the source-side series-winding leakage impedance \( Z_A' \) and the load-side series-winding leakage impedance \( Z_A'' \) are equal. Hence, \( Z_A' = Z_A'' = Z_A/2 \), where \( Z_A \) is the leakage impedance of the total series winding. From Figure 3.2, equations (3.2) and (3.3) can be written in terms of leakage impedance of the series winding as

\[
V_{SA} = V_{nA} + \frac{\Delta V_A}{2} + I_{SA} \frac{Z_A}{2} \quad (3.2)
\]

\[
V_{LA} = V_{nA} - \frac{\Delta V_A}{2} - I_{LA} \frac{Z_A}{2} \quad (3.3)
\]

Subtracting (3.3) from (3.2) and replacing \( \Delta V_A \) with \( \Delta V_a DN \), we can obtain

\[
V_{SA} = V_{LA} + \Delta V_a (D.N) + I_{LA} \frac{Z_A}{2} + I_{SA} \frac{Z_A}{2} \quad (3.4)
\]

Magnetizing branch of the transformer is ignored therefore; excitation current in the ampere-turn relation (3.5) is neglected.

\[
\frac{nA}{2} I_{SA} + \frac{nA}{2} I_{LA} = -n_a I_a \quad (3.5)
\]

where \( I_{SA}, I_{LA}, \) and \( I_a \) are the currents in the series winding at the source side, load side, and exciting winding, respectively.
Considering Figure 3.2, equation (3.6) gives us the relations of the currents in the series winding:

\[ I_{SA} + I_b = I_{LA} + I_c \Rightarrow I_{LA} = I_{SA} - j\sqrt{3}I_a \]  \hspace{1cm} (3.6)

Substituting (3-6) in (3-5) for \( I_{LA} \) and solving \( I_a \) as a function of \( I_{SA} \) we can get

\[ I_a = I_{SA} \frac{2j\sqrt{3}DN}{-2j\sqrt{3} - 3DN} \]  \hspace{1cm} (3.7)

Using the circuit of Figure 3.2, we can write the expression for the quadrature voltage developed at the exciting winding as

\[ \Delta V_A = -j\sqrt{3}V_{nA} - I_a Z_a \]  \hspace{1cm} (3.8)

Replacing \( I_a \) in (3.8) with (3.7), and substituting (3.8) in (3.4) for \( \Delta V_a \), we get

\[ V_{nA} = \left[ \frac{V_{LA}}{j\sqrt{3}DN} - \frac{V_{SA}}{j\sqrt{3}DN} + (I_{SA} + I_{LA}) \left( \frac{DN}{2j\sqrt{3}} \frac{Z_a}{2j\sqrt{3}DN} \right) \right] \]  \hspace{1cm} (3.9)
Solving $V_{LA}$ by adding (3.2) and (3.3) and substituting (3.9) for $V_{na}$, we can get

$$V_{LA} = V_{SA} e^{j\delta} - I_{SA} \left( \frac{e^{j\delta}}{3D^2N^2 + 4} \right) \left[ 4D^2N^2Z_a + Z_A(3D^2N^2 + 4) \right]$$

$$V_{LA} = V_{SA} e^{j\delta} - I_{SA} Z_1 e^{j\delta}$$

where

$$Z_1(D) = \left( \frac{1}{3D^2N^2 + 4} \right) \left[ 4D^2N^2Z_a + Z_A(3D^2N^2 + 4) \right] \quad (3.10)$$

and

$$1\angle\delta(D) = \frac{-j\sqrt{3DN - 2}}{j\sqrt{3DN - 2}}$$

Equation (3.10) represents the positive-sequence impedance of the whole PST as a function of the tap position D. The above expression represents the phase shift angle $\delta$(deg) between the source and load sides as a function of the tap position.

The derived equation (3.10) is further used to find the winding leakage impedances ($Z_A$ and $Z_a$) at the maximum tap position (D=1). Hence, the effective positive-sequence impedance of the PST at the maximum tap position will become

$$Z_{1(D=1)} = \left( \frac{1}{3N^2 + 4} \right) \left[ 4N^2Z_a + Z_A(3N^2 + 4) \right] \quad (3.11)$$

Like in the two winding transformer, winding leakage impedances ($Z_A$ and $Z_a$) can be assumed half of the effective positive sequence impedance. Hence, using equation (11), we can find the series-winding impedance as a function of the square of tap position $D$. There is no tap changer on the exciting winding, so the exciting winding leakage impedance will remain the same for all tap positions.
In large transformers, resistance is very small compared to reactance, and therefore, reactance can be taken equivalent to impedance by neglecting resistance [28]. Winding resistance and reactance can be calculated from \( Z_A \) using the positive sequence impedance angle. Parameter calculations using (3.12) and (3.13), when used back in (3.10) give us the positive-sequence impedance of the whole PST as a function of the tap position. Hence, to accurately model the PST, the manufacturer’s test report data is not required, except for the impedance at the maximum tap position given in the nameplate information.

### 3.2.2. Calculation of Negative-Sequence Winding Impedances

The negative-sequence impedance is equal to the positive-sequence impedance, and the equivalent circuit is similar, except that the phase shift will be of the same magnitude but in opposite directions. Thus, if the phase shift is \( +\delta \) degrees for the positive-sequence quantities, the phase shift for the negative-sequence quantities will be \( -\delta \) degrees.

### 3.2.3. Calculation of Zero-Sequence Winding Impedances

Taking all the phase quantities (currents and voltages) to be equal in magnitude and in-phase and rewriting (3.2), (3.3) we will get

\[
V_{SA0} = V_{nA0} + \frac{\Delta V_{A0}}{2} + I_{SA0} \frac{Z_{A0}}{2}
\]

\[
V_{LA0} = V_{nA0} - \frac{\Delta V_{A0}}{2} - I_{LA0} \frac{Z_{A0}}{2}
\]

Subtracting (3.15) from (3.14) and replacing \( \Delta V_{A0} \) with \( \Delta V_{nA0} D N \), we can obtain

\[
Z_A(D) = 0.5Z_{1(D=1)}D^2
\]

\[
Z_{a} = 0.5 \frac{3N^2 + 4}{4N^2} Z_{1(D=1)}
\]
\[ V_{SA0} = V_{LA0} + \Delta V_{a0} DN + I_{LA0} \frac{Z_{A0}}{2} + I_{SA0} \frac{Z_{A0}}{2} \] (3.16)

The ampere-turn equation can be rewritten as

\[ Dn_A I_{SA0} = -n_a I_{a0} \Rightarrow I_{a0} = DNI_{SA0} \] (3.17)

\[ I_{SA0} + I_{b0} = I_{LA0} + I_{c0} \Rightarrow I_{SA0} = I_{LA0} \] (3.18)

Using the circuit of Figure 3.2, the expression for the quadrature voltage developed at the exciting winding is

\[ \Delta V_{a0} = -I_{a0} Z_{a0} \] (3.19)

Replacing \( I_{a0} \) in (3.19) with (3.17) and substituting in (3.16) for \( \Delta V_{ao} \), we can get

\[ V_{LA0} = V_{SA0} - I_{SA0} \left( Z_{a0} D^2 N^2 + Z_{A0} \right) \]

\[ V_{LA0} = V_{SA0} - I_{SA0} Z_{eq0} \]

where

\[ Z_0(D) = Z_{a0} D^2 N^2 + Z_{A0} \] (3.20)

Equation (3.20) represents the zero-sequence impedance of the whole PST as a function of tap position \( D \).

The derived equation (3.20) is further used to find the winding leakage impedances (\( Z_{a0} \) and \( Z_{a0} \)) at the maximum tap position (\( D=1 \)). Hence, the zero-sequence impedance of the PST at the maximum tap position will become

\[ Z_{a0} = 0.5 \frac{Z_0(D=1)}{N^2} \] (3.21)

\[ Z_{A0} = 0.5 Z_{0(D=1)} D^2 \] (3.22)
The derived parameters (3.21) and (3.22), when used back in (3.20), will give us the zero-sequence impedance of the whole PST as a function of the tap position.

3.3. Validation of the Derived Positive-And Zero-Sequence Impedances Relations

The derived relations of positive- and zero-sequence impedances are validated using the manufacturer’s test report data. From the derived positive- and zero-sequence impedances relations, we calculated the positive- and zero-sequence impedances as a function of the tap position for the whole PST, and compared this with the positive- and zero sequence impedances obtained at manufacturer’s facility.

The manufacturer’s rating of the standard-delta PST is as follows: nominal power rating: $S_n=30$ MVA; nominal voltage rating: $V_n=69$ kV; maximum no-load phase shift: $\delta=\pm 30$ deg in 32 steps; positive-sequence impedance at the maximum tap position: $Z_{1(D=1)}=9.52 \ \Omega$; zero-sequence impedance at the maximum tap position: $Z_{0(D=1)}=8.8872 \ \Omega$.

Figure 3.3 shows the calculated positive-sequence impedance of the PST based on the proposed derived model (solid line) using (3.10), (3.12) and (3.13) and the manufacturer’s data (dots). Figure 3.3 also shows the calculated zero-sequence impedance of the PST based on our proposed model (solid line), using (3.20), (3.21) and (3.22), and the manufacturer’s data (dots).

The matching of the calculated positive- and zero-sequence impedance values, as based on our proposed model and the manufacturer’s test values, shows that our proposed model is accurate enough and can be used for protection and short-circuit studies. The only required data from the manufacturer are the PST ratings, including the positive- and zero-sequence impedances at the maximum tap positions. There is no need for a detailed test report and data for each tap position.

As mention before, the magnetizing branch is ignored in the presented model however; transformer protection studies do require magnetizing branch to simulate the core saturation effects on the applied protection. Saturation model of the transformer can be
obtained by adding the nonlinear inductance branch. In EMTP tools such as RTDS and PSCAD, this can be done by placing the saturation block across the excitation winding.

3.4. Modeling of the Two-core Symmetrical Phase Shifting Transformer

As in the previous section, different parameters are derived to accurately model the positive-, negative-, and zero-sequence impedance networks of the two-core symmetrical PST. The accuracy of the derived models is further analyzed and validated with the manufacturer’s test report data.

3.4.1. Calculation of Positive-Sequence Winding Impedances

As shown in Figure 3.4, source (S) and load (L) sides are connected to the primary winding of the series unit. The secondary windings of the series unit are connected to the tapped windings (secondary side) of the exciting unit, making a delta connection to create the quadrature voltage, which, when added to the nominal voltage, will generate the advanced (leading) or retard (lagging) phase shift between the source and the load sides.

Figure 3.3: Positive- and zero-sequence impedance vs. tap position: calculated values using our proposed model (solid line) and values from the manufacturer’s test report data (dots).
The primary of the exciting unit is connected to the mid-point of the primary of the series unit. Both sides of the exciting unit are Y–N connected.

As shown in Figure 3.4, the load tap changers are installed at secondary windings of the exciting unit. Each tap changer is equipped with a change-over-switch (S) to achieve advance or retard phase shift.

Figure 3.4 shows the tap changer at maximum positive tap position (D=1), whereas other end of the tapped winding corresponds to the minimum tap position (D=0). By switching S, the tap position shown in Figure 3.4 can be converted from D=1 to D=-1.

The turn ratios of the series and the exciting units at a particular tap position D are as follows:

$$\frac{\Delta V_A}{\Delta V_a} = \frac{n_{SA}}{n_{Sa}} = N_S$$  \hspace{1cm} (3.23)

$$\frac{V_{EA}}{V_{Ea}} = \frac{n_{EA}}{Dn_{Ea}} = \frac{N_E}{D}$$  \hspace{1cm} (3.24)

where $\Delta V_A$ and $\Delta V_a$ are the quadrature voltages; $V_{EA}$ and $V_{Ea}$ are the voltages across the primary and secondary of the exciting unit; $n_{SA}$ and $n_{Sa}$ are the number of turns in the primary and the secondary windings of the series unit, respectively; $n_{EA}$ and $n_{Ea}$ are the number of turns in the primary and the secondary windings of the exciting unit, respectively.

The load condition should be taken into account to derive the positive-, negative-, and zero-sequence impedances of the PST as a function of the tap position. The derived equations are further used to calculate the leakage impedance of the single-phase windings of both series and exciting units.
Considering Figure 3.5, it is assumed that the primary winding of the series unit is equally divided into two windings (source side and load side), such that the leakage impedance of the source-side winding $Z_{SA}'$ and the load-side winding $Z_{SA}''$ are equal. Hence, $Z_{SA}' = Z_{SA}'' = Z_{SA}/2$.

Equations (3.25) and (3.26) can be written in terms of leakage impedance at the primary of the series unit, as shown in Figure 3.5.

\[ V_{SA} = V_{EA} + \frac{\Delta V_A}{2} + I_{SA} \frac{Z_{SA}}{2} \]  \hspace{1cm} (3.25)

\[ V_{LA} = V_{EA} - \frac{\Delta V_A}{2} - I_{LA} \frac{Z_{SA}}{2} \]  \hspace{1cm} (3.26)
Subtracting (3.26) from (3.25) and replacing $\Delta V_a$ with $\Delta V_{aNs}$, we can obtain

$$V_{SA} = V_{LA} + \Delta V_a . N_s + I_{LA} \frac{Z_{SA}}{2} + I_{SA} \frac{Z_{SA}}{2}$$ \hspace{1cm} (3.27)

Using the circuit of Figure 3.5, we can write the expression for the quadrature voltage developed at the secondary of the series unit as

$$\Delta V_a = -j\sqrt{3}V_{EA} + I_a Z_{Sa}$$ \hspace{1cm} (3.28)

Transferring the secondary to the primary of the exciting unit, we can write the voltage and current relation as

Figure 3.5: Single-phase diagram of a two-core symmetrical PST.
\[ V_{EA} = V_{Da} \frac{N_e}{D} + I_{EA} N_{EA} - I_{Da} N_{Da} \frac{N_e}{D} \]  

The ampere-turn ratio of the series unit is

\[ I_a = \frac{N_s}{2} (I_{SA} + I_{LA}) \]  

The ampere-turn ratio of the exciting unit is

\[ \frac{I_{EA}}{I_{Da}} = \frac{Dn_{Da}}{n_{EA}} \]  

Considering Figure 3.5, equation (3.32) gives the current relation between the secondary of the series and the exciting units

\[ I_{EA} = I_c - I_b = j \sqrt{3} I_a \Rightarrow j \sqrt{3} \frac{N_s}{2} (I_{SA} + I_{LA}) \]  

The distribution of currents in the primary of the series and exciting units is

\[ I_{EA} = I_{SA} - I_{LA} \]  

Using (3.30) to (3.33), we can derive the following relations

\[ I_{LA} = I_{SA} - \frac{2N_e - j \sqrt{3} N_s D}{j \sqrt{3} N_s D - 2N_e} \]  

\[ I_a = I_{SA} - \frac{2N_e N_s}{2N_e - j \sqrt{3} N_s D} \]  

\[ I_{EA} = I_{SA} - \frac{j2 \sqrt{3} N_e N_s}{2N_e - j \sqrt{3} N_s D} \]  

\[ I_{EA} = I_{SA} - \frac{j2 \sqrt{3} N_s D}{j \sqrt{3} N_s D - 2N_e} \]
Replacing $\Delta V_a$ and $I_a$ in (3.27) with (3.28) and (3.30), respectively, and by rearranging, we can get

$$V_{EA} = \frac{V_{LA}}{j\sqrt{3}N_s} - \frac{V_{SA}}{j\sqrt{3}N_s} + \frac{(I_{SA} + I_{LA})}{j\sqrt{3}N_s} \left( Z_{Sa} \frac{N_s^2}{2} + Z_{SA} \right)$$  \hspace{1cm} (3.35)$$

Adding (3.25) and (3.26), and rearranging for $V_{LA}$, we get

$$V_{LA} = 2V_{EA} - V_{SA} + \frac{Z_{SA}}{2} (I_{SA} - I_{LA})$$  \hspace{1cm} (3.36)$$

Using (3.29) and (3.35), the expression for $V_{EA}$ can be found and used in (3.36) to get the following expression for $V_{LA}$

$$V_{LA} = V_{SA} e^{j\delta} - \frac{I_{SA}}{3N_s^2 D^2 + 4N_e^2} e^{j\delta} \left[ \frac{4N_e^2 N_s^2 Z_{Sa} + Z_{SA} (4N_e^2 + 3N_s^2 D^2)}{+ 12N_s^2 D^2 Z_{EA} + 12N_e^2 N_s^2 Z_{EA}} \right]$$

$$V_{LA} = V_{SA} e^{j\delta} - I_{SA} Z_1 e^{j\delta}$$  \hspace{1cm} (3.37)$$

where $Z_1(D)$ is the positive-sequence impedance as a function of the tap position of the PST represented by (3.38) and $\delta$(deg) denotes the phase shift between the load- and source- sides.

$$Z_1(D) = \left( \frac{1}{3N_s^2 D^2 + 4N_e^2} \right) \left[ \frac{4N_e^2 N_s^2 Z_{Sa} + Z_{SA} (4N_e^2 + 3N_s^2 D^2)}{+ 12N_s^2 D^2 Z_{EA} + 12N_e^2 N_s^2 Z_{EA}} \right]$$  \hspace{1cm} (3.38)$$

$$1\angle \delta = \frac{-2N_e - j\sqrt{3}N_s D}{j\sqrt{3}N_s D - 2N_e}$$  \hspace{1cm} (3.39)$$

The positive-sequence impedance of the series unit remains constant for any tap position. Hence, to find the winding leakage impedance of the series unit, we put $D=0$ in (3.38) such that $Z_{1(D=0)} = N_s^2 Z_{Sa} + Z_{SA}$. At $D=0$, $Z_{1(D=0)}$ is the equivalent impedance of the single-
phase series-unit transformer shown in Figure 3.5. As done in the previous section, we can find the series-unit winding leakage impedances as below

\[ Z_{Sa} = 0.5 \frac{Z_{1(D=0)}}{N_S^2} \quad (3.40a) \]

\[ Z_{SA}' = Z_{SA}'' = 0.25Z_{1(D=0)} \quad (3.40b) \]

The positive-sequence impedance of the exciting unit is the function of the tap position \( D \). The derived equation (3.38) with tap position \( D=1 \) can be used to find the positive-sequence impedance of the exciting unit at the maximum tap, \( D=1 \), which is further used to find the winding leakage-impedances (\( Z_{EA} \) and \( Z_{Ed} \)). Using (3.38) with \( D=1 \)

\[
Z_{1(D=1)} = \frac{1}{3N_S^2 + 4N_e^2} \left[ Z_{1(D=0)} \left( 4N_e^2 + 1.5N_S^2 \right) + 12N_S^2 Z_{EA} + 12N_e^2 N_s^2 Z_{Ed} \right]
\]

From the above equation, we can find the exciting-unit primary and secondary windings leakage impedances as a function of the tap position as below.

\[
Z_{EA} = \frac{0.5}{12N_S^2} \left[ Z_{1(D=1)} \left( 3N_S^2 + 4N_e^2 \right) - Z_{1(D=0)} \left( 4N_e^2 + 1.5N_S^2 \right) \right] \quad (3.41a)
\]

\[
Z_{Ed} = \frac{0.5D^2}{12N_e^2 N_s^2} \left[ Z_{1(D=1)} \left( 3N_S^2 + 4N_e^2 \right) - Z_{1(D=0)} \left( 4N_e^2 + 1.5N_S^2 \right) \right] \quad (3.41b)
\]

Parameter calculations using (3.40) and (3.41), when used back in (3.38), give us the positive-sequence impedance of the whole PST as a function of the tap position. Hence, to accurately model the PST, the manufacturer’s test report data are not required, except for the impedance at the maximum tap position and minimum tap positions that are given in the nameplate information.
3.4.2. Calculation of Negative-Sequence Winding Impedances

The negative-sequence impedance is equal to the positive-sequence impedance, and the equivalent circuits are similar except that the phase shift will be of the same magnitude but in opposite directions. Thus, if the phase shift is $\delta$ degrees for the positive-sequence, the phase shift for the negative-sequence quantities will be $-\delta$ degrees.

3.4.3. Calculation of Zero-Sequence Winding Impedances

Taking all the phasor quantities (currents and voltages) to be equal in magnitude and in-phase and rewriting (3.25), (3.26) and (3.28) we will get

$$V_{S40} = V_{E40} + \frac{\Delta V_{40}}{2} + I_{S40} \frac{Z_{S40}}{2}$$

(3.42)

$$V_{L40} = V_{E40} - \frac{\Delta V_{40}}{2} - I_{L4} \frac{Z_{S40}}{2}$$

(3.43)

$$\Delta V_{a0} = I_{a0} Z_{a0}$$

(3.44)

Subtracting (3.43) from (3.42), use (3.44) for $V_{a0}$, and take $I_{S40} = I_{L40}$.

$$V_{S40} = V_{L40} + I_{a0} Z_{a0} N_s + I_{S40} Z_{S40}$$

(3.45)

The ampere-turn equation (3.30) will become

$$n_A I_{S40} = n_a I_{a0}$$

(3.46)

Using (3.46) for $I_{a0}$ in (3.45), we can get

$$V_{L40} = V_{S40} - I_{S40} \left(Z_{a0} N_s^2 + Z_{S40} \right)$$

(3.47)

$$V_{L40} = V_{S40} - I_{S40} Z_{eq0}$$

$$Z_0 = Z_{a0} N_s^2 + Z_{S40}$$

(3.48)
Equation (3.48) represents the zero-sequence impedance of the whole PST. The zero-sequence impedance of the exciting unit \((Z_{EA0}, Z_{Ea0})\) is zero even when both sides of exciting units are grounded; this is because the secondary of the exciting unit is connected to the secondary of the series unit in delta. Hence, the zero-sequence impedance of the PST will remain constant for all tap positions.

The derived equation (3.48) is further used to find the winding leakage impedances \((Z_{SA0} \text{ and } Z_{Sa0})\).

\[
Z_{Sa0} = 0.5 \frac{Z_0}{N_s^2} \quad (3.49)
\]

\[
Z_{SA0} = 0.5 Z_0 \quad (3.50)
\]

### 3.4.4. Validation of the Derived Positive- and Zero-Sequence Impedance Relations

Derived impedance relations for the proposed model are validated using the manufacturer’s test report data. From our derived positive- and zero-sequence impedances relations we calculated the positive- and zero-sequence impedances as a function of tap position for the whole PST and compared with the positive- and zero sequence impedances obtained at manufacturer’s facility for each tap position.

The manufacturer’s rating of the two-core symmetrical PST is as follows: nominal power rating: \(S_n = 480\) MVA; nominal voltage rating: \(V_n = 230\) kV; maximum no-load phase shift: \(\delta = \pm 35.1\) deg in 32 steps; number of turns series unit: primary winding 220, secondary winding 272; number of turns exciting unit: primary winding 354, secondary winding 160; positive-sequence impedance at maximum and minimum tap positions, \(Z_{1(D=1)} = 11.44\Omega \text{ and } Z_{1(D=0)} = 7.48\Omega\), respectively; zero-sequence impedance: \(Z_0 = 7.96\Omega\).

Figure 3.6 shows the calculated positive-sequence impedance of the PST based on our proposed model (solid line), using (3.40) and (3.41), and the manufacturer’s data (dots).
The matching of the calculated positive-sequence impedance values, based on our proposed model and the manufacturer’s test values shows that our proposed model is accurate enough and can be used for protection and short-circuits studies. Figure 3.6 also shows the phase-shift angle as a function of the tap position obtained by using the derived relation and compared with the test report values.

3.5. Emtp Modeling of Phase Shifting Transformers

3.5.1. Modeling of Standard-Delta PST in EMTP

To further verify the accuracy of our proposed model, EMTP modeling is done in RTDS. As shown in Figure 3.1 and Figure 3.2, three single-phase 3-winding transformer models are used to develop the standard-delta PST in EMTP by simply connecting the terminals of series and exciting windings externally.

Single-phase transformer-windings voltage and reactance parameters are set based on the formulae derived in the previous sections.

![Figure 3.6: Positive-sequence impedance and phase-shift vs. tap position: Calculated values using our proposed model (solid line) and values from the manufacturer’s test report data (dots).](image-url)
Rated voltage, windings 1 and 2: \( V_1 = V_2 = 0.5 V_n D N \)

Rated voltage, winding 3: \( V_3 = V_n \)

Leakage reactance windings 1 and 2, ohms: \( X_1 = X_2 = 0.5 X_A (\Omega) \)

Leakage reactance winding 3, ohms: \( X_3 = X_a (\Omega) \)

Positive-sequence impedance measurements are made by making the source-side terminals of the series winding short-circuited, whereas the load-side terminals of the series winding are supplied with the three-phase voltage supply. For the validation of the zero-sequence impedance model, short-circuit tests were performed at different tap positions using the RTDS model by making the source-side terminals of the series winding short-circuited and supplied with the single-phase voltage supply (the other end of the supply is grounded), whereas the load side is short-circuited and connected with the ground.

Figure 3.7 shows the measured positive- and zero-sequence impedance of our EMTP model, validated with the measured values from the manufacturer’s data. Figure 3.7 also shows us the accuracy of our proposed EMTP model. Hence, the digital model (EMTP)
based on our proposed theoretical model has sufficient accuracy for protection and short-circuit studies.

As shown in Figure 3.7, at the maximum tap position there is a difference in the measured zero-sequence impedance of the EMTP model and the measured values from the manufacturer’s test report, which can result in values of the zero-sequence currents that are different from the actual. As recommended by [15], for the case where PST is operating at the maximum tap position, this difference in the zero-sequence impedance can be compensated by lowering the system zero-sequence impedance with the same proportion.

3.5.2. Turn-to-Turn, Turn-to-Ground, and Winding-to-Winding Faults Modeling of a Standard-Delta PST

To simulate the internal faults, the equivalent model of the standard-delta PST is suggested as in Figure 3.8. For the inter-turn and turn-ground fault modeling, the faulted winding is divided into three parts: the short-circuited part and the remaining coils in the circuit as shown in Figure 3.8. According to [2], the inter-turn fault results in an increase of the source current as the number of shorted turns increases. Therefore, modeling of the fault is done in such a way that the origin of the fault and the short-circuited part can be varied by varying the voltage rating of the faulted winding parts according to the following equations.

\[ \Delta V_a = \Delta V_{a1} + \Delta V_{a2} + \Delta V_{a3} \]

\[ \Delta V_{a2} = (1 - t_s)\Delta V_a \]

\[ \Delta V_{a3} = (1 - t_f)\Delta V_a \]

where \( t_s \) (pu) is the span of the faulted part of the winding to simulate turn-turn fault and \( t_f \) (pu) is the position of the turn-ground fault on the winding.

Fault simulation: The external faults (F1, F2, and F3) can be simulated on the source and load sides of the series winding as well as on the exciting winding, as shown in Figure.
3.8. As shown in Figure 3.8, the internal fault can be simulated as a turn-to-turn fault (S1 closed, S2 and S3 opened) and turn-to-ground fault (S2 closed, S1 and S3 opened). A fault between windings of two phases (winding-to-winding) can be simulated by closing the switch S3 while the other end of the switch is connected to the winding of other phase. For each fault point we can simulate 3-phase, phase-to-phase, and phase-to-ground faults.

3.5.3. Modeling of a Two-Core Symmetrical PST in EMTP

To further verify the accuracy of our proposed model of the two-core symmetrical PST, EMTP modeling is done in RTDS. Three single-phase 3-winding transformers are used to model the series unit, whereas one three-phase 2-winding transformer is used to model the exciting unit, as shown in Figure 3.4. The series unit and the exciting unit are connected externally to model the full two-core symmetrical PST. The windings voltage and reactance parameters are set based on the formulae derived in the previous sections.

*Series-unit parameters for a single-phase 3-winding transformer:*

Rated voltage, windings 1 & 2: \( V_1 = V_2 = (N_s D / 2 N_o) V_n \)
Rated voltage, windings 3 & 4: \( V_3 = V_4 = 2 V_1 / N_3 \)

Leakage reactance of windings 1 & 2: \( X_1 = X_2 = 0.5 X_{SA} \) (\( \Omega \))

Leakage reactance of windings 3 & 4: \( X_3 = X_4 = 2 X_{Sa} \) (\( \Omega \))

*Exciting-unit parameters for a three-phase 2-winding transformer:

Rated voltage, winding 1: \( V_1 = V_n \)

Rated voltage, winding 2: \( V_2(D) = (V_1 / N_\phi) D \)

Leakage reactance of winding 1: \( X_1 = X_{EA} = Z_{SA} \sin(\theta_{ZSA}) \) (\( \Omega \))

Leakage reactance of winding 2: \( X_2 = X_{Ea(D=1)} \) (\( \Omega \))

Positive-sequence impedance is measured by making the source-side terminals of the series unit short-circuited whereas the load side of the series winding is supplied with the with the three-phase voltage supply.

For the zero-sequence impedance model, two validation tests are performed at different tap positions. Test 1: the source-side terminals of the series unit are short-circuited and supplied with the single-phase voltage supply (the other end of the supply is grounded), whereas the load side is short-circuited and connected to the ground of the primary winding of the exciting unit (as done in the manufacturer’s test report). Test 2: the load side terminals of the series unit are short-circuited and supplied with the single-phase voltage supply (the other end of the supply is grounded), whereas the source-side terminals are short-circuited and connected to the ground of the primary winding of the exciting unit. The following values were measured from the tests.

Test 1: \( Z_0 = 7.48 \, \Omega/\text{phase} \); Test 2: \( Z_0 = 7.48 \, \Omega/\text{phase} \)

For all tap positions, the zero-sequence impedance of the PST is the same, which shows that there is no effect of the change in tap position on zero-sequence impedance.
Figure 3.9 shows the measured positive-sequence impedance of our EMTP model, which was validated with the measured values from the manufacturer’s data. The same figure shows the accuracy of our proposed EMTP model. Hence, the digital model (EMTP) based on our proposed theoretical model has sufficient accuracy for protection and short circuit studies. We also compared the positive-sequence impedance of the PST measured from our EMTP model and the EMTP model based on [17]. Figure 3.9 shows the accuracy of our model compared with the EMTP model proposed in [17].

3.5.4. Turn-to-Turn, Turn-to-Ground and Winding-to-Winding Faults Modeling of a Two-core Symmetrical PST

To simulate the internal faults, the equivalent model of the two-core symmetrical PST is suggested as in Figure 3.10. The series and exciting units are modeled both for the inter-turn, turn-ground, and winding-winding faults. The phase windings of the secondary and primary of the series and exciting units, respectively, are divided into three parts: the short-circuited part and the remaining coils in the circuit, as shown in Figure 3.10.
The winding faults are modeled in such a way that the origin of the fault and the short-circuited part can be varied by varying the voltage rating of the respected winding parts according to the following equations

\[ \Delta V_a = \Delta V_{a1} + \Delta V_{a2} + \Delta V_{a3} \]
\[ \Delta V_{a2} = (1 - t_s)\Delta V_a \]
\[ \Delta V_{a3} = (1 - t_{fs})\Delta V_a \]
\[ V_{EA} = V_{EA1} + V_{EA2} + V_{EA3} \]
\[ V_{EA2} = (1 - t_e) V_{EA} \]
\[ V_{EA3} = (1 - t_{fe}) V_{EA} \]

where \( t_s \) (pu) and \( t_e \) (pu) are the spans of the faulted part of the series and exciting unit windings, respectively, for the case of a turn-turn fault; \( t_{fs} \) (pu) and \( t_{fe} \) (pu) are turn-ground fault positions from the neutral on the series and exciting unit windings, respectively.

Fault Simulation: The external (F1, F2) and internal faults (F3, F4) can be simulated on the source and load sides of the series winding as well as on the primary and secondary sides of the exciting winding, as shown in Figure 3.10. The internal fault in both series and exciting units can be simulated as a turn-to-turn fault (S1 closed, S2 and S3 opened or S4 closed, S5 and S6 opened), turn-to-ground fault (S2 closed, S1 and S3 opened or S5 closed, S4 and S6 opened). A windings-winding in series or exciting units can be simulated by closing the switch S3 or S6, respectively, while the other end of the switch(S3 or S6) is connected to the winding of other phase. For each fault point we can simulate 3-phase, phase-to-phase, and phase-to-ground faults.
3.6. Simulation of Terminals Current and Voltage during Normal and Fault System Conditions

To test the proper working of a phase shifting transformer, this section shows terminal currents and voltages during normal and faulted power system conditions. The proposed model of a two-core symmetrical phase shifting transformer is modeled in PSCAD. Details of the PST and the power system test model are provided in Appendix C.

As per the PST nameplate information given in Appendix C, the maximum phase shift across the PST source and load sides is 35.1 deg in 32 steps (or 1.096 deg per tap position step size). Figure 3.11 shows the simulated phase shift between the source and load sides as a function of the tap position (0 to 1 per unit where 1 corresponds to tap position 32). The results illustrated in Figure 3.11 validate the proper working of the PST.
As shown in Figure 3.12, significant magnetization inrush currents are obtained when the unloaded PST is energized while the source-side phase voltages pass the zero-crossing

Figure 3.11: Phase shift as a function of the tap position.

Figure 3.12: Profiles of source- and exciting-unit primary winding terminal currents during energization of PST.

and enter into a positive half cycle.
Figure 3.13 and Figure 3.14 show profiles of currents and voltages at the source side (S-side), the load-side (L-side) and the exciting unit primary winding terminal (E-side) for tap positions (0, 0.25, 0.5 and 1). In Figure 3.13 and Figure 3.14, currents as a function of tap positions (D=0.25 corresponds to 0 – 0.25 sec, D=0.5 corresponds to 0.25–0.5 sec, D=0.75 corresponds to 0.5–0.75 sec, and D=1 corresponds to 0.75 – 1 sec).

Figure 3.13: Profiles of phase A voltages at source (S-side), load (L-side) and exciting-unit primary winding terminal (E-side) for various tap positions.

Figure 3.14: Profiles of phase A currents at source (S-side), load (L-side) and primary winding terminal of exciting-unit (E-side) for various tap positions.
Figure 3.15 and Figure 3.16 show the voltages and currents profile for a phase A to ground internal fault at location (F4 in Figure 3.10) while the PST is operating at mid-tap position.

Figure 3.15: Profiles of terminals voltages in the event of an internal phase A to ground fault at location F4.

Figure 3.16: Profile of terminal currents in the event of an internal phase A to ground fault at location F4.
3.7. Summary

This chapter presented modeling of single-core standard-delta and two-core symmetrical phase shifting transformers, which can be used for both balanced and unbalanced system conditions. The proposed modeling approach is based on the development of positive-, negative- and zero-sequence networks; derived mathematical relations are further used to develop the relations of winding terminal voltages, currents and impedances as a function of the tap position. The accuracy of the presented models is first verified mathematically with the manufacturer’s test report data. Then, EMTP modeling is done in RTDS to further test and verify the digital model. Simulation results illustrate the proper working of a PST during normal and fault system conditions.
Chapter 4

Electromagnetic Differential Protection

A single-core phase shifting transformer represents both magnetically coupled and electrically connected circuits, which makes it unique in design and construction when compared to the standard transformer. This chapter presents a new protection principle that is based on the operating principle of the standard-delta and delta-hexagonal phase shifting transformers (PSTs) using current–voltage relations, which represents electromagnetic relations of the windings. The presented current–voltage relations reflect the exact representation of the PST, and therefore remain valid during normal and external fault conditions. In contrast, in the event of an internal fault, the proposed electromagnetic differential protection will not remain valid and, therefore, can be used to detect and discriminate between the internal/external fault conditions.

4.1. Introduction

Standard single- and three-phase transformer protection methods based on electromagnetic equations (current–voltage relations) are known from [29], [30], [31], [32]. In addition to the internal/external fault discrimination, the electromagnetic equation-based technique resolves the problem of magnetization inrush current. Reference [29] uses the primary and secondary windings’ electromagnetic equations of the standard transformer (single- or three-phase) to develop the electromagnetic differential equations (EDE). During normal system conditions, EDE is valid and computes zero or a very small error (DIFF), whereas during the internal fault condition, the computed error is significantly large.
4.2. Electromagnetic Differential Protection Method- Standard Transformer

The protection technique based on the electromagnetic differential equations of a standard power transformer is known from [29]. Electromagnetic equations of the standard transformer’s primary and secondary windings are used to develop the differential method to detect the internal faults. As shown in Figure 4.1, using winding terminal voltages $v_1$ & $v_2$, currents $i_1$ & $i_2$ and flux linkages $\lambda_{12}$ & $\lambda_{21}$ of the magnetically coupled windings 1 & 2 one can obtain

$$v_1 = r_1 i_1 + l_1 \frac{d}{dt} i_1 + \frac{d}{dt} \lambda_{21} \quad (4.1)$$

$$v_2 = \frac{d}{dt} \lambda_{12} - r_2 i_2 - l_2 \frac{d}{dt} i_2 \quad (4.2)$$

where $r_1$ and $r_2$ are the resistances of winding 1 and 2, respectively and $l_1$ and $l_2$ are the inductances of winding 1 and 2, respectively.

The algorithm requires terminal currents and voltages at the primary and secondary of the transformer and uses the winding parameters. By combining and rearranging the electromagnetic equations of winding 1 and 2, an electromagnetic differential equation is achieved as given by (4.3)

![Figure 4.1: Two-winding transformer.](image)
\[ v_1 = n_1 i_1 + l_1 \frac{d}{dt} i_1 + v_2 + n_2 i_2 + l_2 \frac{d}{dt} i_2 \]  \hspace{1cm} (4.3)

Equation (4.3) is used as a differential measuring equation. During normal system conditions, magnetization inrush, core saturation and external fault conditions, the measured value of the left side and estimated value of the right side of (4.3) are equal. However, during an internal fault, equation (4.3) does not remain valid. This criterion is used for the detection and discrimination of internal/external faults.

4.3. Electromagnetic Differential Protection Method- Delta-Hexagonal PST (EDP-DHP)

This section presents two methods based on electromagnetic equations and explores the suitability of applying these techniques for the protection of a delta/hexagonal PST. Like the standard transformer, the electromagnetic differential protection method I (EDP-DHP I) obtained by combining the PST series- and exciting-winding electromagnetic equations is presented in section 4.3.1. Section 4.3.2 shows why the presented method of section 4.3.1 (EDP-DHP I) is not sufficient to provide a complete protection of PST by presenting various problems and limitations. To solve the dilemmas associated with EDP-DHP I, section 4.3.3 presents electromagnetic differential protection method II (EDP-DHP II) which exploits the unique design of a PST by combining both magnetically-coupled and electrically connected circuits to obtain the electromagnetic differential equations.

4.3.1. Proposed Electromagnetic Differential Protection Method I (EDP-DHP I)

As shown in Figure 4.2, the tap winding by which the source (S) and load (L) are connected is called the series winding, whereas the excitation winding is connected to the other two phases, making delta connections. Hence, the quadrature voltage $\Delta V$ is developed; this, when added to the nominal voltage $V_n$ will generate the phase shift between the source and the load sides [14]. Let’s assume that the PST is operating at full tap position D (when the load side leads the source side, the tap position D varies between 0 and 1, whereas when the load side lags the source side, the tap position D
varies between 0 and -1) and considering Figure 4.3, we can write electromagnetic equations for the series and exciting windings as

\[ V_A = R_A I_A + jX_A I_A + M_{12} I_a \]  
\[ V_a = M_{21} I_A - R_a I_a - jX_a I_a \]

where

\( V_A \) and \( V_a \) are phase ‘A’ voltages at the series and exciting winding terminals, respectively.

\( I_A \) and \( I_a \) are the current in the series and exciting winding of phase A, respectively.

\( R_A/X_A \) and \( R_a/X_a \) are the resistance/reactance of series- and exciting-winding, respectively.

\( M_{12} \) and \( M_{21} \) are the flux linkages contributed by the series-to-exciting winding and vice versa, respectively.

The ampere-turn equation of the magnetically coupled series and exciting winding at tap position D can be written as

\[ DNI_A I_a = 0 \Rightarrow \frac{I_A}{I_a} = \frac{1}{DN} \]

Figure 4.2: A schematic diagram of a delta-hexagonal PST.
where \( N \) is the series-to-exciting winding turn ratio.

It is known from [33] that the series and exciting windings are magnetically coupled on the same leg of the three-legged core. Therefore, for a linear transformer model, it is justified to assume that \( M_{12} = M_{21} \) [12]. By combining and rearranging the magnetically coupled series- and exciting-winding equations (4.4) and (4.5), and using (4.6), we can get

\[
V_A = R_A I_A + jX_A I_A + DN V_a + R_a I_a + jX_a I_a \tag{4.7}
\]

Considering Figure 4.3, we can replace \( V_A \) in (4.7) with the source and load side voltages, \( V_{SA} \) and \( V_{LA} \), respectively, by using the relation \( V_A = V_{SA} - V_{LA} \), hence

\[
V_{SA} - V_{LA} = I_A (R_A + jX_A) + DN V_a + DN I_a (R_a + jX_a) \tag{4.8}
\]

The left side of (4.8) is the measured value of \( V_S - V_L \), whereas the right side is the estimated value of \( V_S - V_L \). By subtracting the left and right side of (4-8), one can obtain the absolute error \(|DIFF|\) as

\[
|DIFF| = \left| (V_{SA} - V_{LA}) - \left( I_A (R_A + jX_A) + DN V_a + DN I_a (R_a + jX_a) \right) \right|
\]

where \(|DIFF|\) is the differential quantity or error between the measured (left side of (4.8)) and the estimated (right side of (4.8)) values of \( V_S - V_L \).

According to the electromagnetic differential protection method, during normal system conditions (4.8) remains valid and the relay computes a small or zero (ideally) absolute error \(|DIFF|\). However, in the event of internal fault conditions, the electromagnetic differential relay computes a significantly large error \(|DIFF|\) between the measured and estimated value of \( V_S - V_L \). The electromagnetic differential unit (EDU) will operate if the error \(|DIFF|\) is larger than the pre-specified threshold, \( THRES \).

In a similar manner, we can also derive the electromagnetic differential equations for phase B and phase C.
4.3.2. Problems and Limitations of the Proposed Electromagnetic Differential Protection Method I (EDP-DHP I)

- The method presented in section 4.3.1 works in very good agreement while the PST is operating at the maximum tap position. However, when the PST is at another tap position $0 \leq D < 1$, as shown in Figure 4.4, parts of the series-winding $Wdg.A1$ and $Wdg.A2$ remain unprotected. Therefore, (4.8) is not sufficient to provide the complete protection solution against the internal fault in the hexagonal PST.

- The technique requires the series- and exciting-windings terminal voltages. Series winding source- and load-side terminal voltages are easily available at bus and transmission levels. However, the requirement of the additional voltage measurement at the exciting-winding terminal would increase the cost of overall protection.

- The error $|DIFF|$ computed by EDP-DHP I in the event of an external fault with CT saturation or series-winding saturation of the transformer is significantly large. Increasing the threshold setting $THRES$ setting solves the problem but results in less sensitivity to the low-current faults and inter-turn faults.

- The algorithm also requires winding parameters as a function of the tap position, which are seldom available from the manufacturer. Nameplate information is easily
available; however, it only contains positive-sequence impedance at the maximum tap position.

- The magnitude of $|DIFF|$ depends on the varying phase shift. Therefore, the setting of $THRES$ cannot be fixed to maintain both the stability and sensitivity of the relay. However, a change of the threshold setting with respect to the tap position or phase shift is not a practical solution at this point.

These problems lead us to the solution by proposing the modified method as done in the following section.

4.3.3. Proposed Electromagnetic Differential Protection Method II (EDP-DHP II)

The following current, voltage and impedance notations are used in this section:

- Current: source-side ($I_{SA}/I_{SB}/I_{SC}$), load-side ($I_{LA}/I_{LB}/I_{LC}$) and exciting winding ($I_a/I_b/I_c$) currents

- Voltage: source-side ($V_{SA}/V_{SB}/V_{SC}$), load-side ($V_{LA}/V_{LB}/V_{LC}$) and exciting winding ($V_a/V_b/V_c$) voltages.

Considering Figure 4.4, and using the symmetry between the phases, we can derive the analytical equivalent of \( V_a \) as

\[
V_a = V_{SB} + V_{B1} - V_{LC} + V_{C2}
\]  

(4.9)

where \( V_{B1} \) and \( V_{C2} \) are the voltages across the windings Wdg.B1 and Wdg.C2

Assuming that the PST is operating at a particular tap position D, we can derive the equivalent of voltages \( V_{B1} \) and \( V_{C2} \)

\[
V_{B1} = I_a Z_{B1} + \left( \frac{1 - D}{2D} \right) (V_B - I_B Z_B)
\]  

(4.10)

\[
V_{C2} = I_a Z_{C2} + \left( \frac{1 - D}{2D} \right) (V_C - I_C Z_C)
\]  

(4.11)

Replacing \( V_{B1} \) and \( V_{C2} \) in (4.9) with (4.10) and (4.11), respectively, one can obtain

\[
V_a = V_{SB} + I_a Z_{B1} + \left( \frac{1 - D}{2D} \right) (V_B - I_B Z_B) - V_{LC} + I_a Z_{C2} + \left( \frac{1 - D}{2D} \right) (V_C - I_C Z_C)
\]  

(4.12)

For a symmetrical linear transformer model we can assume that

\[
Z_A = Z_B = Z_C
\]

\[
Z_{A1} = Z_{A2} = Z_{B1} = Z_{B2} = Z_{C1} = Z_{C2}
\]

\[
Z_a = Z_b = Z_c
\]

Replacing \( V_a \) in (4.8) with (4.12) and rearranging we can get

\[
V_{SA} - V_{LA} = I_a (Z_a + 2Z_{A1}) DN + (V_{SB} - V_{LC}) \left[ 1 + \left( \frac{1 - D}{2D} \right) \right] DN
\]

\[
-(V_{LB} - V_{SC}) \left( \frac{1 - D}{2} \right) N - (I_B + I_C) Z_A \left( \frac{1 - D}{2} \right) N + I_A Z_A
\]  

(4.13)
As shown in Figure 4.4, looking into the PST from the source side, the distribution of the currents in the series winding is such that

\[ I_A = I_{SA} + I_c \]
\[ I_B = I_{SB} + I_a \]
\[ I_C = I_{SC} + I_b \] (4.14)

Replacing \( I_A, I_B \) and \( I_C \) in (4.13) with the set of (4.14)

\[
V_{SA} - V_{LA} = I_a \left( Z_a DN + 2Z_{AI} DN - Z_A \left( \frac{1-D}{2} \right) N \right) + I_c Z_A - I_b Z_A \left( \frac{1-D}{2} \right) N
- (I_{SB} + I_{SC}) Z_A \left( \frac{1-D}{2} \right) N + I_{SA} Z_A + (V_{SB} - V_{LC}) \left( \frac{D+1}{2} \right) N
- (V_{LB} - V_{SC}) \left( \frac{1-D}{2} \right) N
\] (4.15)

Similarly, for the other two phases we can write

\[
V_{SB} - V_{LB} = I_b \left( Z_a DN + 2Z_{AI} DN - Z_A \left( \frac{1-D}{2} \right) N \right) + I_a Z_A - I_c Z_A \left( \frac{1-D}{2} \right) N
- (I_{SA} + I_{SC}) Z_A \left( \frac{1-D}{2} \right) N + I_{SB} Z_A + (V_{SC} - V_{LA}) \left( \frac{D+1}{2} \right) N
- (V_{LC} - V_{SA}) \left( \frac{1-D}{2} \right) N
\] (4.16)

\[
V_{SC} - V_{LC} = I_c \left( Z_a DN + 2Z_{AI} DN - Z_A \left( \frac{1-D}{2} \right) N \right) + I_b Z_A - I_a Z_A \left( \frac{1-D}{2} \right) N
- (I_{SA} + I_{SB}) Z_A \left( \frac{1-D}{2} \right) N + I_{SC} Z_A + (V_{SA} - V_{LB}) \left( \frac{D+1}{2} \right) N
- (V_{LA} - V_{SB}) \left( \frac{1-D}{2} \right) N
\] (4.17)

Using basic transformer circuit theory [13], it is justified to assume that \( Z_a = \frac{Z_A}{N^2} (\Omega) \) and the proportionate parts of the series winding (Wdg. A1 and Wdg. A2) impedances with respect to tap position D, we can write
\[ Z_a = \frac{Z_A}{N^2} (\Omega) \]
\[ Z_{A1} = Z_A \left( \frac{1-D}{2D} \right) (\Omega) \]  

Replacing \( Z_a \) and \( Z_{A1} \) in (4.15), (4.16) and (4.17) using (4.18) we can obtain

\[
V_{SA} - V_{LA} = Z_A \left[ I_a \left( \frac{1}{N} D + \frac{1-D}{2} \right) N - I_b \left( \frac{1-D}{2} \right) N \right. \\
\left. + I_c - (I_{SB} + I_{SC}) \left( \frac{1-D}{2} \right) N + I_{SA} \right] + (V_{SB} - V_{LC}) \left( \frac{D+1}{2} \right) N - (V_{LB} - V_{SC}) \left( \frac{1-D}{2} \right)
\]  

Similarly, for the other two phases we can write

\[
V_{SB} - V_{LB} = Z_A \left[ I_b \left( \frac{1}{N} D + \frac{1-D}{2} \right) N - I_c \left( \frac{1-D}{2} \right) N \right. \\
\left. + I_a - (I_{SA} + I_{SC}) \left( \frac{1-D}{2} \right) N + I_{SB} \right] + (V_{SC} - V_{LA}) \left( \frac{D+1}{2} \right) N - (V_{LC} - V_{SA}) \left( \frac{1-D}{2} \right)
\]  

\[
V_{SC} - V_{LC} = Z_A \left[ I_c \left( \frac{1}{N} D + \frac{1-D}{2} \right) N - I_a \left( \frac{1-D}{2} \right) N \right. \\
\left. + I_b - (I_{SB} + I_{SA}) \left( \frac{1-D}{2} \right) N + I_{SC} \right] + (V_{SA} - V_{LB}) \left( \frac{D+1}{2} \right) N - (V_{LA} - V_{SB}) \left( \frac{1-D}{2} \right)
\]

As shown in Figure 4.4, looking into the PST from the load side, the distribution of the currents in the series winding is such that

\[
I_A = I_{LA} + I_b \\
I_B = I_{LB} + I_c \\
I_C = I_{LC} + I_a
\]  

(4.22)
Replacing $I_a$, $I_b$ and $I_c$ in (4.15), (4.16) and (4.17) with set of (4.22) and replacing $Z_a$ and $Z_{AI}$ with (4.18), we can get

$$V_{SA} - V_{LA} = Z_A \left[ I_a \left( \frac{D}{N} + \left( \frac{1-D}{2} \right)N \right) - I_c \left( \frac{1-D}{2} \right)N \right]$$

$$+ I_b - (I_{LB} + I_{LC}) \left( \frac{1-D}{2} \right)N + I_{LA}$$

$$+ (V_{SB} - V_{LC}) \left( \frac{1+D}{2} \right)N - (V_{LB} - V_{SC}) \left( \frac{1-D}{2} \right)N$$

(4.23)

Similarly, for the other two phases we can write

$$V_{SB} - V_{LB} = Z_A \left[ I_b \left( \frac{1}{N} D + \left( \frac{1-D}{2} \right)N \right) - I_a \left( \frac{1-D}{2} \right)N \right]$$

$$+ I_c - (I_{LA} + I_{LC}) \left( \frac{1-D}{2} \right)N + I_{LB}$$

$$+ (V_{SC} - V_{LA}) \left( \frac{D+1}{2} \right)N - (V_{LC} - V_{SA}) \left( \frac{1-D}{2} \right)$$

(4.24)

$$V_{SC} - V_{LC} = Z_A \left[ I_c \left( \frac{1}{N} D + \left( \frac{1-D}{2} \right)N \right) - I_b \left( \frac{1-D}{2} \right)N \right]$$

$$+ I_a - (I_{LB} + I_{LA}) \left( \frac{1-D}{2} \right)N + I_{LC}$$

$$+ (V_{SA} - V_{LB}) \left( \frac{D+1}{2} \right)N - (V_{LA} - V_{SB}) \left( \frac{1-D}{2} \right)$$

(4.25)

Computation of the electromagnetic differential equations (4.19), (4.20) and (4.21) and (4.23), (4.24) and (4.25) requires measurements of currents (at source, load side and exciting winding) and voltages (source and load side). In practice, each end of the series and exciting winding (locations 3 to 6 in Figure 4.2) is brought out of the tank so that the connection between the exciting winding and series winding of the other two phases can be done externally [12]. Therefore, a measurement of source-side, load-side and exciting-winding currents can be obtained by locating the current transformers at locations 1, 2 and 3 in Figure 4.2. The algorithm does not require the exciting-winding voltage and only
requires the source- and load-side terminal voltages which are normally available at bus and transmission levels.

The algorithm also requires the winding impedance $Z_A$ at each tap position. Winding parameters at each tap position are seldom available from the transformer manufacturer. However, reference [15] presents the derived relations of apparent positive-sequence impedance and windings impedances as a function of tap position to establish a short-circuit model of hexagonal PST. The proposed model [15] only requires nameplate information to approximate the impedance of the windings as a function of tap position. In addition to the PST ratings, the positive-sequence impedance ($Z_{1@D=1}$) of the PST measured at the maximum tap position ($D=1$) is also given in the nameplate. Therefore, by using the positive-sequence impedance ($Z_{1@D=1}$), one can easily find the winding parameters as a function of the tap position using the derived positive sequence relation presented in [15]. Therefore, the proposed algorithm requires only $Z_{1@D=1}$ and automatically calculates $Z_A$ as a function of tap position $D$ by using the following relation

$$Z_A(D) = 0.5D^2(1 + N + N^2)Z1(\Omega)$$  \hspace{1cm} (4.26)

Moreover, the magnitude of the $|DIFF|$ has dependence on the tap-changer position or phase-shift between the two ends. Therefore, to minimize this dependence, the computed error $|DIFF|$ is made adaptive to the tap-changer position. This is be done by simply dividing the left and right sides of the (4.19), (4.20) and (4.21) and (4.23), (4.24) and (4.25) with the base quantity $|V_n D(1-1\angle\delta)|$. The base quantity is made adaptive to the tap-changer position by tracking the tap position $D$, where the nominal system voltage $V_n$ and maximum phase shift $\delta$ are the constants, which can be obtained from the PST nameplate information.

4.3.4. Fault Detection Algorithm

The left-hand sides of the equations (4.19), (4.20) and (4.21) are calculated using the measured values of the source- and load-side voltage. The right-hand sides of the equations (4.19) to (4.21) are the estimated value of the left-hand sides. During normal
system conditions, the difference of error $|DIFF|$ between the actual (left side) and estimated (right side) values of the $V_S-V_L$ in (4.19), (4.20) and (4.21) is very small. However, in the event of an internal fault, the $|DIFF|$ is significantly very large. The same is true for the (4.23), (4.24) and (4.25) set of electromagnetic differential equations.

To make the relay sensitive to all kinds of faults, the sensitivity of the relay can be increased by combining the decision from both of the relays. $RELAY_S$ and $RELAY_L$ computes the difference $|DIFF_S|$ and $|DIFF_L|$, respectively between the actual (left side) and estimated (right side) values of $V_S-V_L$ in (4.19) to (4.21) and (4.23) to (4.25), respectively. To ensure the sensitivity in the event of low internal-fault current conditions, the decisions from both of the relays are combined. To ensure a secure decision from both of the relays, two trip counters are used for each relay. The trip counter tracks the operating quantity $|DIFF|$ and increments or decrements if the $|DIFF|$ is equal/greater or less than the set threshold $THRES$. A final decision is made, when the output of either of the two trip counters reaches the set counter threshold limit. A decision from the relay is set to 1 when the trip counter reaches the threshold limit and 0 when it is less than threshold limit. Using an OR gate logic between $RELAY_S$ and $RELAY_L$, a final output is set to 1 (trip) or 0 (no trip).

4.4. Electromagnetic Differential Protection Method–Standard-Delta PST (EDP-SDP)

As shown in Figure 4.5(a), the tap winding with which the source (S) and load (L) are connected is called the series winding, whereas the excitation winding is connected to the other two phases of the series winding, making delta connections. Hence, the quadrature voltage $\Delta V$ is developed; this, when added to the nominal voltage $V_n$ will generate the phase shift between the source and the load sides.

As shown in Figure 4.5(b), the following current, voltage and impedance notations are used in this section to develop the current-voltage protection relation:

- Current: source-side ($I_{SA}/I_{SB}/I_{SC}$), load-side ($I_{LA}/I_{LB}/I_{LC}$) and exciting winding ($I_a/I_b/I_c$) currents
• Voltage: source-side \((V_{SA}/V_{SB}/V_{SC})\), load-side \((V_{LA}/V_{LB}/V_{LC})\), exciting winding \((V_a/V_b/V_c)\) and nominal voltages \((V_{na}/V_{nb}/V_{nc})\).

• \(Z_{A1/B1/C1}, Z_{A2/B2/C2}, Z_{a/b/c}\) are the impedances of windings Wdg’A1’/B/C, Wdg.A2/ B2/ C2 and Wdg a/b/c, respectively.

The turn ratio of the series and exciting winding at a particular tap position \((0 \leq D \leq 1)\) is as follows

\[
\frac{\Delta V_A}{\Delta V_a} = D \frac{n_S}{n_c} = DN
\]

(4.27)

where \(\Delta V_A (=\Delta V_{A1}+\Delta V_{A2})\) as shown in Figure 4.5(b) and \(\Delta V_a\) are the quadrature voltages across the series and exciting windings, respectively.

Using the notations of Figure 4.5(b), the voltage relation across the series and exciting windings can be written as

\[
V_{SA} = V_{nA} + \Delta V_{A1} + I_{SA} Z_{A1}
\]

(4.28)

\[
V_{LA} = V_{nA} - \Delta V_{A2} - I_{LA} Z_{A2}
\]

(4.29)

\[
V_a = \Delta V_a - Z_a I_a
\]

(4.30)

By subtracting (4.28) and (4.29), and re-arranging, we obtain

\[
V_{SA} - V_{LA} = Z_{A1} I_{SA} + Z_{A2} I_{LA} + \Delta V_A
\]

(4.31)

Equation (4.32) can be written by eliminating \(\Delta V_a\) in (4.30) by using (4.27) and solving for \(\Delta V_A\)

\[
V_a = \frac{\Delta V_A}{DN} - Z_a I_a
\]

(4.32)

As shown in Figure 4.5(a), for instance taking phase A, the exciting winding of phase A is connected with the mid-tap point of the phase B and C series winding, therefore the
voltage $V_a$ across the phase A exciting winding can be written as $V_a = V_{nB} - V_{nC}$ and hence (4.32) can be rewritten as

$$V_{nB} - V_{nC} = \frac{\Delta V_A}{D_N} - Z_a I_a$$

Solving the above equation for $\Delta V$, we can write
\[ \Delta V_A = DN(V_{nB} - V_{nC}) + DNZ_a I_a \]  

(4.33)

Replacing \( \Delta V_A \) in (4.31) with (4.33)

\[ V_{SA} - V_{LA} = \left( Z_{A1} I_{SA} + Z_{A2} I_{LA} + DN(V_{nB} - V_{nC}) + DNZ_a I_a \right) \]  

(4.34)

Similarly, for the other two phases we can write

\[ V_{SB} - V_{LB} = \left( Z_{B1} I_{SB} + Z_{B2} I_{LB} + DN(V_{nC} - V_{nA}) + DNZ_b I_b \right) \]  

(4.35)

\[ V_{SC} - V_{LC} = \left( Z_{C1} I_{SC} + Z_{C2} I_{LC} + DN(V_{nA} - V_{nB}) + DNZ_c I_c \right) \]  

(4.36)

For a symmetrical linear transformer model, we can assume that \[ Z_{A1} = Z_{A2} = Z_{B1} = Z_{B2} = Z_{C1} = Z_{C2} \]

\[ Z_a = Z_b = Z_c \]

The left side of (4.34) is the measured value of \( V_S - V_L \), whereas the right side is the estimated value of \( V_S - V_L \). By subtracting the left and right side of (4.34), one can obtain the absolute differential quantity \(|DIFF_A|\) as

\[ |DIFF_A| = \left| V_{SA} - V_{LA} - \left( Z_{A1} I_{SA} + Z_{A2} I_{LA} + DN(V_{nB} - V_{nC}) + DNZ_a I_a \right) \right| \]  

(4.37)

Similarly, for the other two phases we can write

\[ |DIFF_B| = \left| V_{SB} - V_{LB} - \left( Z_{B1} I_{SB} + Z_{B2} I_{LB} + DN(V_{nC} - V_{nA}) + DNZ_b I_b \right) \right| \]  

(4.38)

\[ |DIFF_C| = \left| V_{SC} - V_{LC} - \left( Z_{C1} I_{SC} + Z_{C2} I_{LC} + DN(V_{nA} - V_{nB}) + DNZ_c I_c \right) \right| \]  

(4.39)
Equations (4.37) to (4.39) represent the electromagnetic differential protection principle. These current and voltage relations remain valid and compute a zero (ideally) or small differential quantity $|\text{DIFF}|$ during normal or external fault conditions. However, in the event of an internal fault, a significant differential quantity is calculated between the measured and estimated value of $V_S - V_L$. Therefore, based on this criterion, the proposed protection element will operate if the $|\text{DIFF}|$ is larger than the pre-specified threshold, $\text{THRES}$.

4.4.1. Practical Issues and Their Solutions

Issue 1

The implementation of equations (4.37) to (4.39) requires three currents and three voltages at the source, load, and exciting-winding terminals. Voltages at the source and load sides are normally available at the busbar and transmission sides; however, practically it is not always possible to obtain exciting-winding voltages. This problem can be solved by finding the exact replica of the exciting voltages using the available source-and load-side currents and voltages. This can be done by considering the electrically connected circuit between the exciting winding of one phase and the other two phases of the series winding

$$V_{SA} = V_{nA} + \frac{\Delta V_A}{2} + I_{SA} Z_{A1}$$  \hspace{1cm} (4.40)

$$V_{LA} = V_{nA} - \frac{\Delta V_A}{2} - I_{LA} Z_{A1}$$  \hspace{1cm} (4.41)

Adding (4.40) and (4.41), we can get

$$V_{nA} = \frac{V_{SA}}{2} + \frac{V_{LA}}{2} - I_{SA} \frac{Z_{A1}}{2} + I_{LA} \frac{Z_{A1}}{2}$$  \hspace{1cm} (4.42a)

Similarly, for the other two phases we can write
\[ V_{nB} = \frac{V_{LB}}{2} + \frac{V_{SB}}{2} - I_{SB} \frac{Z_{A1}}{2} + I_{LB} \frac{Z_{A1}}{2} \]  \hspace{1cm} (4.42b)

\[ V_{nC} = \frac{V_{LC}}{2} + \frac{V_{SC}}{2} - I_{SC} \frac{Z_{A1}}{2} + I_{LC} \frac{Z_{A1}}{2} \]  \hspace{1cm} (4.42c)

Subtracting (4.42c) from (4.42b)

\[ V_{nB} - V_{nC} = \left( \frac{1}{2} (V_{LB} + V_{SB} - V_{LC} + V_{SC}) - \frac{Z_{A1}}{2} (I_{SB} - I_{LB} + I_{SC} - I_{LC}) \right) \]  \hspace{1cm} (4.43)

Replacing \( V_{nB} - V_{nC} \) in (4.37) using (4.43) one can obtain

\[ |DIFF_A| = (V_{SA} - V_{LA}) - \left( \begin{array}{c} Z_{A1}I_{SA} + Z_{A1}I_{LA} \\ + \frac{1}{2} DN(V_{LB} + V_{SB} - V_{LC} + V_{SC}) \\ - \frac{Z_{A1}}{2} DN(I_{SB} - I_{LB} + I_{SC} - I_{LC}) + DNZ_a I_a \end{array} \right) \]  \hspace{1cm} (4.44)

Similarly, we can write (4.45)-(4.46) for another two phases

\[ |DIFF_B| = (V_{SB} - V_{LB}) - \left( \begin{array}{c} Z_{A1}I_{SB} + Z_{A1}I_{LB} \\ + \frac{1}{2} DN(V_{LC} + V_{SC} - V_{LA} + V_{SA}) \\ - \frac{Z_{A1}}{2} DN(I_{SC} - I_{LC} + I_{SA} - I_{LA}) + DNZ_a I_b \end{array} \right) \]  \hspace{1cm} (4.45)

\[ |DIFF_C| = (V_{SC} - V_{LC}) - \left( \begin{array}{c} Z_{A1}I_{SC} + Z_{A1}I_{LC} \\ + \frac{1}{2} DN(V_{LA} + V_{SA} - V_{LB} + V_{SB}) \\ - \frac{Z_{A1}}{2} DN(I_{SA} - I_{LA} + I_{SB} - I_{LB}) + DNZ_a I_c \end{array} \right) \]  \hspace{1cm} (4.46)
Computation of the electromagnetic differential equations (4.44) to (4.46) requires the measurements of currents (at source-, load-side and exciting-winding) and voltages (source and load side).

**Issue 2**

For instance for phase A, the proposed algorithm (4.44) requires measurements of the source-side current ($I_{SA}$), load-side current ($I_{LA}$) and exciting-winding terminal current ($I_a$) available at locations 1, 2 and 3, respectively, as shown in Figure 4.6. All the winding internal faults ($F_1$, $F_2$ and $F_3$ in Figure 4.6) can be detected by the protection equation (4.44). However, (4.44) is not able to detect any fault in the zone between locations 3 and 4 as shown in Figure 4.6. The proposed relay sees fault $F_4$ out of zone and does not operate and hence loses dependability. This issue can be solved by exploiting Kirchhoff’s current relation in the series winding.

As in Figure 4.5(a), the series winding of one phase (at mid-position) is electrically connected with the other two phases of the exciting winding such that we can write the following Kirchhoff’s current relation:

\[
I_{SA} + I_b = I_{LA} + I_c \Rightarrow I_b = I_{LA} - I_{SA} + I_c \quad (4.47)
\]

\[
I_{SB} + I_c = I_{LB} + I_a \Rightarrow I_c = I_{LB} - I_{SB} + I_a \quad (4.48)
\]

\[
I_{SC} + I_a = I_{LC} + I_b \Rightarrow I_a = I_{LC} - I_{SC} + I_b \quad (4.49)
\]

![Figure 4.6: Internal faults in a standard-delta PST.](image-url)
Using (4.47)-(4.49) for $I_a$, $I_b$ and $I_c$ in (4.44)-(4.46) we can get

\[
|DIFF_A| = (V_{SA} - V_{LA}) - \left[ \begin{array}{c} 
-Z_A I_{SA} + Z_A I_{LA} \\
+ \frac{1}{2}DN(V_{LB} + V_{SB} - V_{LC} + V_{SC}) \\
-Z_A I_{LB} - I_{LA} + I_{SC} - I_{LC} + \\
DNZ_a(I_{LC} - I_{SC} + I_b) 
\end{array} \right] \quad (4.50)
\]

Similarly, we can write (4.51)-(4.52) for another two phases.

\[
|DIFF_B| = (V_{SB} - V_{LB}) - \left[ \begin{array}{c} 
-Z_A I_{SB} + Z_A I_{LB} \\
+ \frac{1}{2}DN(V_{LC} + V_{SC} - V_{LA} + V_{SA}) \\
-Z_A I_{LC} - I_{LA} - I_{SC} - I_{LC} + \\
DNZ_a(I_{LA} - I_{SA} + I_c) 
\end{array} \right] \quad (4.51)
\]

\[
|DIFF_C| = (V_{SC} - V_{LC}) - \left[ \begin{array}{c} 
-Z_A I_{SC} + Z_A I_{LC} \\
+ \frac{1}{2}DN(V_{LA} + V_{SA} - V_{LB} + V_{SB}) \\
-Z_A I_{LA} - I_{SA} - I_{SB} - I_{LB} + \\
DNZ_a(I_{LB} - I_{SB} + I_a) 
\end{array} \right] \quad (4.52)
\]

### Issue 3

The algorithm also requires the winding impedances $Z_A$ and $Z_a$ at each tap position. The winding parameters at each tap position are seldom available from the transformer manufacturer. However, one can easily acquire the PST nameplate information. In addition to the PST ratings, the positive-sequence impedance ($Z_{1@D=1}$) of the whole PST measured at the maximum tap position ($D=1$) is also given in the nameplate information. By using the derived relations, derived in Chapter 3 for standard delta PST, for positive-sequence impedance as a function of tap position, one can easily find the winding parameters as a function of the tap position. Therefore, the proposed algorithm requires
only \( Z_{l(D=1)} \) and automatically calculates \( Z_{4l} \) and \( Z_a \) as a function of the tap position \( D \) by using (4.53) to (4.54)

\[
Z_{4l}(D) = Z_{l(D=1)} D^2 \tag{4.53}
\]

\[
Z_a = 0.5 \frac{3N^2 + 4}{4N^2} Z_{l(D=1)} \tag{4.54}
\]

**Issue 4**

The magnitude of the operating quantity, \(|DIFF|\), depends on the transformer loading or tap-changer position / phase-shift between the two ends. For example, if the setting of the threshold (THRES) is done at the mid-tap position; it is likely that relay loses sensitivity to low-current faults while the PST is operating at lower tap positions, and loses security against false differential quantity, \(|DIFF|\), while the PST is operating at higher tap positions. In order to maintain the sensitivity and security of the proposed protection, the dependence of the differential quantity with respect to the tap-position is minimized by making the \(|DIFF|\) adaptive to the tap-changer position. This can be done by simply dividing the \(|DIFF|\) with the adaptive base quantity \(|V_n D(1-1\angle\delta)|\). The base quantity is made adaptive to the tap-changer position by tracking the tap position \( D \), where the nominal system voltage \( V_n \) and the maximum phase shift \( \delta \) are the constants, which can be obtained from the PST nameplate information.

**4.4.2. Fault Detection Algorithm**

The left-hand sides of the equations (4.50) to (4.52) are calculated using the measured values of the source- and load-side voltages. The right-hand sides of the (4.50) to (4.52) are the estimated values of the left-hand side. During normal system conditions, the difference or error \(|DIFF|\) between the actual (left side) and estimated (right side) values of \( V_S - V_L \) in (4.50) to (4.52) is very small. However, in the event of an internal fault, the \(|DIFF|\) is significantly very large.
To ensure a secure decision from the relay, a trip counter is used for each relay. The trip counter tracks the operating quantity, $|\text{DIFF}|$, and increments or decrements if $|\text{DIFF}|$ is equal/greater or less than the set threshold $\text{THRES}$. A final decision is made when the output of the trip counter reaches the set counter threshold limit. A decision from the relay is set to 1 when the trip counter reaches the threshold limit and 0 when it is less than the threshold limit.

4.5. CVT Transients

The capacitor voltage transformers (CVTs) are commonly known as an economical way of a voltage source for the relaying applications. However, these transformers can be a source of the error in relaying application because of the transient error [34]. In the event of a fault, the voltage at the secondary of the CVT does not replicate the primary voltage because of the energy storage elements such as coupling capacitors and compensating reactor [35]. The influence of CVT transients, particularly in the distance relaying, when the line is short can result in the zone reach error. Normally the superimposed transients have frequency of below 25Hz or above 250Hz. Therefore, to eliminate the error caused by the CVT transients, a second order mid-pass filtered tuned to nominal frequency is used.

The proposed techniques require voltages at source and load sides, therefore, it is important to analyze the impact of the CVT transients on the performance of the proposed protection technique. We have performed numerous test cases for various internal and external faults. These transients are more severe when the fault occurs at the zero crossing of the waveform; therefore, all the tests are for fault inception at zero crossing of the voltage waveform.

In order to demonstrate the influence of CVT transients on the proposed technique, performance of the proposed algorithm has been tested with conventional VTs (case A), CVTs without filter (case B) and CVTs with filter (case C).
Figure 4.7 shows the case of internal phase A-g fault at the source side of the PST while the PST is operating at a mid-tap position. Significant CVT transients can be seen for the voltage waveform of CVT without mid-pass filter, as shown in Figure 4.7(a). Figure 4.7(b) shows the waveforms of the measured $V_S-V_L$ (left side of equation (4.19)) quantity for all three cases. Figure 4.7(c) shows the computed operating quantity $|DIFF|$ for all three cases, which shows no significant difference between all three cases.

Figure 4.8 shows the case of external phase A-g fault at the source side of the PST while the PST is operating at a mid-tap position. Significant CVT transients can be seen for the voltage waveform of CVT without mid-pass filter, as shown in Figure 4.8(a). Figure 4.8
(b) shows the waveforms of the measured $V_S-V_L$ (left side of equation (4.19)) quantity for all three cases. Figure 4.8(c) shows the computed operating quantity $|DIFF|$ for all three cases, which shows no significant difference between all three cases.

Figure 4.7 and Figure 4.8 suggest that there is no significant influence of the CVT transients on the proposed method.

Figure 4.8: Performance comparison of the proposed technique with conventional VT, CVT without filter and CVT with filter for the case of an external fault.
4.6. Performance Evaluation

For various normal and fault system conditions, techniques proposed in sections 4.3 and 4.4 are tested. For a performance evaluation of the proposed algorithms of both delta-hexagonal and standard-delta PSTs, two power system simulation models (models 1 and 2) of the different ratings are simulated in PSCAD/EMTDC. Details of both models are provided in Appendix B. Model 1 contains the delta-hexagonal PST and model 2 contains the standard-delta transformer. To obtain the real representation of currents and voltages, modeling of the delta-hexagonal and standard-delta PSTs is done based on the real PSTs nameplate information.

4.6.1. Signal Processing

The proposed algorithm is based on the operating condition of the transformer; therefore, implementation of the algorithm is done in time-domain. Instantaneous values from current and voltage transformers are available at a time step of 50µs (sampling rate of 20 kHz). Prior to discretization of the continuous time signals, analog current and voltage signals are passed through a digital low-pass anti-aliasing filter with a cut-off frequency of 360 Hz (Appendix B). Computation of the algorithm mainly requires the fundamental frequency components; therefore, a fourth-order Butterworth low-pass filter is used to remove the higher frequency components. Moreover, input current signals are processed through the derivative component to remove the dc components. Phase delay in the current signal with reference to the voltage signal because of the derivative is compensated for prior to sampling. Sampling of the signals is done with a sampling frequency of 1440 Hz.

4.6.2. Selection of the Threshold Setting

Selection of the threshold setting is made to prevent the relay from insecure operation due to the computation of false differential quantity |DIFF| due to

1) any inaccuracies between the estimated and measured values of $V_S - V_L$.

2) CT saturation in the event of external fault.
As compared to the current differential relay, the proposed technique offers higher level of security against external fault with CT saturation. However, for an external fault with CT saturation in a strong system (low source impedance ratio (SIR)) it is likely that |DIFF| quantity enters the trip zone. Security of the relay can be increased by increasing the threshold setting. However, increasing the threshold setting can result in the limited sensitivity to low current faults. Therefore, to ensure higher level of security against CT saturation, while maintaining the sensitivity of the relay, it is important to complement the algorithm with the harmonic block unit.

4.6.3. Simulation Cases

A large number of tests are performed to analyse the performance of the algorithm. For various source impedance ratio, SIRs (0.2, 1, 5), fault types phase-to-ground (ph-g), phase-to-phase (ph-ph), double-phase-to-ground (ph-ph-g) and three-phase (3-ph)) were applied at various internal (F4, F5, and F8) and external (F1 and F2) locations as shown in Figure 4.9. Turn-to-turn faults (F6 and F7) and turn-to-ground faults (F3) of various spans of shorted turns were applied on the series and exciting winding. Each fault scenario is tested for various tap positions (high (0.7<D<1), mid (D=0.5) and low (0<D<0.3)). Furthermore, the proposed algorithm is also tested for conditions such as magnetizing inrush, series-winding saturation due to over-voltages, current transformer saturation, and with low- and high-fault resistances (0Ω, 20Ω).

The following description summarizes the representation of signals, labels, legends and symbols used in Figure 4.10 to Figure 4.32.

Source-, load- and exciting-winding terminal currents: S-side (A), L-side (A), E-side (A)

Source-, load- and exciting-winding terminal voltages: S-side (V), L-side (V), E-side (V)

Phase quantities: phA, phB and phC
Operating differential quantities computed by RELAY\textsubscript{S} and RELAY\textsubscript{L} : \(|\text{DIFF}_\text{S}, \text{DIFF}_\text{L}|\)

Pickup setting: THRES=1pu

Status of source-side circuit breaker: CBS

Fault inception: FLT

Combined trip signal: Trip

Figure 4.9: Fault modeling of a delta-hexagonal PST.
4.6.4. Test Results

4.6.4.1. Internal Faults

As mentioned in section 4.5.4, internal faults were simulated at various locations of the transformer. The sections below present a few cases of single phase-to-ground, phase-to-phase and three-phase faults. All the additional cases are presented in Appendix D.

4.6.4.1.1. Single Phase-to-Ground faults

Case 4-1: A phase A to ground fault of low fault resistance (0.1 ohms) was simulated at location F5 as shown in Figure 4.10 while the PST is operating at a high tap position. As shown in Figure 4.10, the inception of the fault (FLT) is at a time 0.193 sec, and both relays compute the errors |DIFF_S| and |DIFF_L| which are above the set threshold.

![Figure 4.10: Internal phase A-g fault at location F5: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-1).](image-url)
(THRES = 1pu). A combined trip signal (Trip as shown in Figure 4.10) was initiated by the relay at 0.205 sec (operating time of 12 msec) after the trip counters of both the relays reached the threshold (=1/4 cycle). The algorithm took 7.8 msec to make the decision.

Figure 4.11 shows the profiles of currents measured at the source side (S-Side), load side (L-Side) and exciting winding terminal (E-Side) for the same case (Case 4-1). Voltages measured at the source and load sides are also shown in Figure 4.11.

Figure 4.11: Internal phase A-g fault at location F5: profiles of source-side currents, load-side currents, exciting winding terminal currents, and source- and load sides terminal voltages (Case 4-1).
Case 4-2: A phase B to ground fault of high fault resistance (20 ohms) was simulated at location F5, as shown in Figure 4.12, while the PST is operating at a high tap position. As shown in Figure 4.13, the inception of the fault (FLT) is at a time 0.193 sec (POW = 0 deg). Both relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1pu). A combined trip signal (Trip) was initiated by the relay at 0.213 sec (operating time of 20 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 15.8 msec to make the decision.

Table 4-1 shows the performance of the proposed algorithm for various single-phase-to-ground faults of high and low resistances for the PST operating at high and low tap positions. The average operating time of the relay for the low- and high-resistance faults is 11.25 msec and 13.11 msec, respectively. The algorithm took an average time of 7.085 msec (low-resistance faults) and 8.95 msec (high-resistance faults) to make the decision.

Figure 4.12: Internal phase B-g fault at location F5: $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-2).
Table 4-1: Relay operating times for internal phase-to-ground faults

<table>
<thead>
<tr>
<th>Case.#</th>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 4-3</td>
<td>1</td>
<td>high</td>
<td>F4</td>
<td>0.1</td>
<td>12</td>
<td>Figure D.1</td>
</tr>
<tr>
<td>Case 4-4</td>
<td>1</td>
<td>high</td>
<td>F4</td>
<td>20</td>
<td>17</td>
<td>Figure D.2</td>
</tr>
<tr>
<td>Case 4-5</td>
<td>1</td>
<td>high</td>
<td>F5</td>
<td>0.1</td>
<td>12</td>
<td>Figure D.3</td>
</tr>
<tr>
<td>Case 4-6</td>
<td>1</td>
<td>high</td>
<td>F5</td>
<td>20</td>
<td>13</td>
<td>Figure D.4</td>
</tr>
<tr>
<td>Case 4-7</td>
<td>1</td>
<td>high</td>
<td>F4</td>
<td>0.1</td>
<td>10</td>
<td>Figure D.5</td>
</tr>
<tr>
<td>Case 4-8</td>
<td>1</td>
<td>high</td>
<td>F4</td>
<td>20</td>
<td>18</td>
<td>Figure D.6</td>
</tr>
<tr>
<td>Case 4-9</td>
<td>1</td>
<td>high</td>
<td>F5</td>
<td>0.1</td>
<td>10</td>
<td>Figure D.7</td>
</tr>
<tr>
<td>Case 4-10</td>
<td>1</td>
<td>high</td>
<td>F5</td>
<td>20</td>
<td>11</td>
<td>Figure D.8</td>
</tr>
<tr>
<td>Case 4-11</td>
<td>5</td>
<td>high</td>
<td>F4</td>
<td>0.1</td>
<td>13</td>
<td>Figure D.9</td>
</tr>
<tr>
<td>Case 4-12</td>
<td>5</td>
<td>high</td>
<td>F4</td>
<td>20</td>
<td>18</td>
<td>Figure D.10</td>
</tr>
<tr>
<td>Case 4-13</td>
<td>5</td>
<td>high</td>
<td>F5</td>
<td>0.1</td>
<td>12</td>
<td>Figure D.11</td>
</tr>
<tr>
<td>Case 4-14</td>
<td>5</td>
<td>high</td>
<td>F5</td>
<td>20</td>
<td>17</td>
<td>Figure D.12</td>
</tr>
<tr>
<td>Case 4-15</td>
<td>5</td>
<td>low</td>
<td>F3</td>
<td>0.1</td>
<td>11</td>
<td>Figure D.13</td>
</tr>
<tr>
<td>Case 4-16</td>
<td>5</td>
<td>low</td>
<td>F3</td>
<td>20</td>
<td>13</td>
<td>Figure D.14</td>
</tr>
<tr>
<td>Case 4-17</td>
<td>5</td>
<td>low</td>
<td>F5</td>
<td>0.1</td>
<td>10</td>
<td>Figure D.15</td>
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<td>Case 4-18</td>
<td>5</td>
<td>low</td>
<td>F5</td>
<td>20</td>
<td>11</td>
<td>Figure D.16</td>
</tr>
</tbody>
</table>

4.6.4.1.2. Phase-to-Phase and Double Phase-to-Ground faults

**Case 4-19:** A phase-to-phase fault (BC) of low fault resistance (0.1 ohms) was simulated at location F5 as shown in Figure 4.13 while the PST is operating at mid tap position. As shown in Figure 4.13, the inception of the fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both relays compute the errors |DIFF_S| and |DIFF_L| which are above the set threshold (THRES = 1pu). A combined trip signal (Trip) was initiated by the relay at 0.205 sec (operating time of 12 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 7.83 msec to make the decision.

**Case 4-20:** A phase-to-phase-ground fault(BC-g) of fault resistance (2 ohms) was simulated at location F4 as shown in Figure 4.14 while the PST is operating at mid tap position. As shown in Figure 4.14, the inception of fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both of the relays compute the errors |DIFF_S| and |DIFF_L| which are above the set threshold (THRES = 1pu). A combined trip signal (Trip as shown in Figure 4.14 was initiated by the relay at 0.20 sec (operating time of 17 msec) after the trip
counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 12.83 msec to make the decision.

Table 4-2, shows the performance of the proposed algorithm for various phase-to-phase and double phase-to-grounds faults for the PST operating at the mid-tap position. All the tests performed are for SIR 1 and 5. The average operating time (trip time) of the relay for all kinds of phase-to-phase and double phase-to-ground faults is 16.5 msec. The algorithm took an average time 12.335 msec to make the decision.

![Figure 4.13: Internal BC fault at location F5: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-19).](image-url)

Figure 4.13: Internal BC fault at location F5: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-19).
Figure 4.14: Internal BC-g fault at location F4: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-20).

Table 4-2: Relay operating times for ph-to-ph and double ph-to-ground faults

<table>
<thead>
<tr>
<th>Case.#</th>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>R_f(Ω)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 4-21</td>
<td>1</td>
<td>mid</td>
<td>F4(BC)</td>
<td>0.1</td>
<td>17</td>
<td>Figure D.17</td>
</tr>
<tr>
<td>Case 4-22</td>
<td></td>
<td></td>
<td>F4(BC-g)</td>
<td>2</td>
<td>17</td>
<td>Figure D.18</td>
</tr>
<tr>
<td>Case 4-23</td>
<td></td>
<td></td>
<td>F5(BC)</td>
<td>0.1</td>
<td>12</td>
<td>Figure D.19</td>
</tr>
<tr>
<td>Case 4-24</td>
<td></td>
<td></td>
<td>F5(BC-g)</td>
<td>2</td>
<td>12</td>
<td>Figure D.20</td>
</tr>
<tr>
<td>Case 4-25</td>
<td>SIR 5</td>
<td>mid</td>
<td>F4(BC)</td>
<td>0.1</td>
<td>24</td>
<td>Figure D.21</td>
</tr>
<tr>
<td>Case 4-26</td>
<td></td>
<td></td>
<td>F4(BC-g)</td>
<td>2</td>
<td>23</td>
<td>Figure D.22</td>
</tr>
<tr>
<td>Case 4-27</td>
<td></td>
<td></td>
<td>F5(BC)</td>
<td>0.1</td>
<td>14</td>
<td>Figure D.23</td>
</tr>
<tr>
<td>Case 4-28</td>
<td></td>
<td></td>
<td>F5(BC-g)</td>
<td>2</td>
<td>13</td>
<td>-</td>
</tr>
</tbody>
</table>
4.6.4.1.3. Three-Phase Faults

**Case 4-29:** A three phase fault was simulated at location F8, as shown in Figure 4.15 while the PST is operating at the mid-tap position. As shown in Figure 4.15, the inception of the fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold. A combined trip signal (Trip as shown in Figure 4.15) was initiated by the relay at 0.206 sec (operating time of 13 msec) after the trip counters of both of the relays reached the threshold ($=1/4$ cycle). The algorithm took 8.835 msec to make the decision.

**Case 4-30:** A three-phase fault of was simulated at location F5, as shown in Figure 4.16, while the PST is operating at the mid-tap position. As shown in Figure 4.16, the inception of the fault (FLT) is at a time 0.193 sec. Both of the relays compute the errors $|\text{DIFF}_S|$

![Figure 4.15: Internal ABC fault at location F8: |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-29).](image-url)
and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1pu). A combined trip signal, as shown in Figure 4.16, was initiated by the relay at 0.204 sec (operating time of 11 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 6.834 msec to make the decision.

![Figure 4.16: Internal ABC fault at location F5: $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-30).](image)

More results of three-phase faults are provided in Appendix D.
4.6.4.1.4. Turn-to-Ground Fault

Case 4-31: A turn-ground fault of low fault resistance (0.1 ohms) was simulated at location F3, as shown in Figure 4.17, while the PST is operating at a low tap position. As shown in Figure 4.17, the inception of the fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1pu). A combined trip signal (Trip as shown in Figure 4.17) was initiated by the relay at 0.205 sec (operating time of 12 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 7.83 msec to make the decision.

Figure 4.17: Turn-to-ground fault at location F3: $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-31).
4.6.4.1.5. Turn-to-Turn Fault

**Case 4-32:** A turn-to-turn fault, with a span of 5% of the exciting winding was simulated at location F6 as shown in Figure 4.18, while the PST is operating at the mid-tap position. As shown in Figure 4.18, the inception of the fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both of the relays compute the errors |DIFF_S| and |DIFF_L| which are above the set threshold (THRES = 1pu). A combined trip signal (Trip as shown in Figure 4.18) was initiated by the relay at 0.211 sec (operating time of 18 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 13.84 msec to make the decision.

![Figure 4.18: Turn-to-turn fault of fault span of 5% of exciting winding: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-32).](image-url)
**Case 4-33:** A turn-to-turn fault, with a span of 1.5% of the exciting winding, was simulated at location F6, as shown in Figure 4.19, while the PST is operating at a low tap position. As shown in Figure 4.19, the inception of the fault (FLT) is at a time of 0.193 sec. Both relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold ($\text{THRES} = 1\text{pu}$). A combined trip signal (Trip as shown in Figure 4.19) was initiated by the relay at 0.204 sec (operating time of 11 msec) after the trip counters of both of the relays reached the threshold ($=1/4$ cycle). The algorithm took 6.84 msec to make the decision.

![Figure 4.19: Turn-to-turn fault of fault span of 1.5% of exciting winding: $|\text{DIFF}|$ signals computed by RELAY\textsubscript{S} and RELAY\textsubscript{L}, and fault inception/trip signals (Case 4-33)](image-url)
**Case 4-34:** A turn-to-turn fault, with a span of 5% of the exciting winding, was simulated at location F6, as shown in Figure 4.20, while the PST is operating at the full tap position. As shown in Figure 4.20, the inception of the fault (FLT) is at a time of 0.193 sec (POW = 0 deg). Both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1pu). A combined trip signal (Trip as shown in Figure 4.20) was initiated by the relay at 0.218 sec (operating time of 25 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 20.84 msec to make the decision.

![Graph showing turn-to-turn fault of fault span of 5% of exciting winding: |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-34).](image-url)
4.6.4.2. External Faults With and Without CT Saturation

The proposed technique is also tested in the events of external phase-to-ground, phase-to-phase, and three-phase faults with, and without, CT saturation at high and low tap positions. Figure 4.21 to Figure 4.27 present the source- and load-side terminal current profiles in the events of phase-to-ground, phase-to-phase and three-phase external faults at the source side (F1) and load side (F2) of the PST. The performance of the relay is shown by the profiles of the source- and load-side electromagnetic differential protection characteristics, $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ respectively, along with the initiation of the fault signal (FLT) and the relay trip output (TRIP).

**Case 4-35:** External phase C-g fault at location F2 while the PST is operating at the full tap position. As shown in Figure 4.21 both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

**Case 4-36:** External phase C-g with CT saturation fault at location F2 while the PST is operating at the mid-tap position. As shown in Figure 4.22, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

**Case 4-37:** External phase C-g fault at location F1 while the PST is operating at the mid-tap position. As shown in Figure 4.23, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

**Case 4-38:** External phase BC fault at location F2 while the PST is operating at the mid-tap position. As shown in Figure 4.24, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

**Case 4-39:** External phase BC fault with phase B CT saturation at location F2 while the PST is operating at the mid-tap position. As shown in Figure 4.25, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).
**Case 4-40:** External ABC fault at location F2 while the PST is operating at the mid-tap position. As shown in Figure 4.26, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

**Case 4-41:** External ABC fault with phase A CT saturation at location F2 while the PST is operating at the mid-tap position. As shown in Figure 4.27, both relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are below the set threshold (THRES = 1pu).

---

**Figure 4.21:** External phase C-g fault at location F2: Profiles of source-side phase C terminal current, load-side phase C current, $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception and trip signals (Case 4-35)

**Figure 4.22:** External C-g fault with phase C CT saturation at location F2: Profiles of source-side phase C current, load-side phase C current, $|\text{DIFF}|$ signals computed by RELAYS and RELAYL, and fault inception and trip signals (Case 4-36).
Figure 4.23: External phase C-g fault at location F1: Profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception and trip signals (Case 4-37).

Figure 4.24: External BC fault at location F2: Profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception and trip signals (Case 4-38).
Figure 4.25: External BC fault with phase B CT saturation at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception and trip signals (Case 4-39).

Figure 4.26: External ABC fault at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception and trip signals (Case 4-40).
Figure 4.27: External ABC fault with phase A CT saturation at location F2: profiles of source-side phase C current, load-side phase C current, |DIFF| signals computed by RELAY s and RELAY L, and fault inception and trip signals (Case 4-41).

4.6.4.3. Energization of an Unloaded PST

Case 4-42: As shown in Figure 4.28, significant magnetization inrush currents at source-side (S-side in Figure 4.28), load-side (L-Side in Figure 4.28) and exciting winding terminal (E-Side in Figure 4.28) are obtained when the unloaded PST is energized while the source-side phase voltages pass the zero-crossing and enters into the positive half cycle. Figure 4.29 shows the profiles of the source- and load-side electromagnetic
differential protection characteristics $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ respectively. Figure 4.29 also shows the digital signals of the source-side circuit breaker (CBS) status, fault inception (FLT) and relay trip signal (Trip). Figure 4.29 shows that the proposed protection technique is immune to magnetization inrush current. RELAY$_S$ and RELAY$_L$ computes $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$, which are less than the THRES setting.

![CT Primary Side Currents](image)

Figure 4.28: Energization of an unloaded PST: profiles of source-side, load-side and exciting winding terminal currents (Case 4-42).
4.6.4.4. Internal Fault in an Unloaded PST

Case 4-43: As mentioned before, a blocking element is used to ensure the security of the differential protection (87) during inrush currents. However, in the event of an internal fault while the unloaded transformer is energized, traditional differential protection can result in a delayed trip operation for an internal fault due to the trip block operation of the relay. Delay in the relay trip operation depends on the magnitude of the second harmonic content. As mentioned before, modern transformers generate lower levels of second harmonic, lowering or reducing the threshold setting increases the security of the relay; however, dependability is jeopardized.
Our proposed solution solves this problem. As shown in Figure 4.30, both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1 pu) for an internal phase-to-ground fault at location F3 while the PST is operating at the full tap position and the system SIR=1. As shown in Figure 4.30, the circuit breaker was closed at 0.193 sec and the fault was initiated at a time of 0.225 sec.

A combined trip signal was initiated by the relay at 0.238 sec (operating time of 13 msec) after the trip counters of both of the relays reached the threshold (=1/4 cycle). The algorithm took 8.83 msec to make the decision.

**Case 4-44:** Figure 4.31 shows the relay performance for an internal phase A to ground fault at location F3 while the PST is operating at a low tap position. Both of the relays compute the errors $|\text{DIFF}_S|$ and $|\text{DIFF}_L|$ which are above the set threshold (THRES = 1 pu) and hence operate successfully by initiating the trip output.

![Figure 4.30: Internal phase-to-ground fault at location F3: $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-43).](image-url)
4.6.4.5. Saturation of the Series Winding

The voltage rating of the series winding that connects the source- and load-side terminal with the system is lower than the voltage rating of the connected system [14]. An external fault can result in a significant increase in the terminal voltage. Therefore, in the traditional differential protection, saturation of the series winding due to over-excitation can result in the mal-operation of the relay. Differential protection is usually complemented with the restraining unit. Fifth harmonic content in the inrush current is used as an indicator of the saturation of the transformer. As mentioned before, in modern transformers using the harmonic as an indicator of the false differential current can affect the security of the differential relay.
To test the proposed technique in the event of PST saturation, series winding is forced to saturate by increasing the source side voltage. As shown in Figure 4.32, source voltages are increased to the level of 150% in Case 4-45 (as shown in Figure 4.32). Saturation of the PST results in the distortion of the exciting-winding currents as shown in the corresponding figures.

The $|\text{DIFF}|$ computed by both the RELAY$_S$ and RELAY$_L$ is lower than THRES. Therefore, the proposed technique remains stable during the series-winding saturation of the PST.

Figure 4.32: Saturation of the series windings: profiles of source-side phase A voltage, exciting-winding terminal phase A current, $|\text{DIFF}|$ signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-45).
4.7. Summary

New protection principles based on the electromagnetic differential principle for both delta-hexagonal and standard-delta phase shifting transformers were presented in this chapter. The normal operating principle of the transformers can be represented by the electromagnetic equations of the windings. The electromagnetic equations of the mutually coupled windings are combined to form the electromagnetic differential protection principle. However, applying the electromagnetic differential principle based on the mutually coupled windings does not offer a complete protection solution when the PST is operating at any tap position other than the full tap position. In addition, various problems are identified, and are followed by the proposed solutions to those problems. More sensitive and reliable electromagnetic differential principles were developed for the protection of the delta-hexagonal and standard-delta PSTs.

The performance of the proposed protection principle was tested for various faulted and non-faulted power system conditions. In addition to the internal/external fault detection and discrimination capability, unlike differential protection, the proposed algorithm remains stable during a magnetization inrush current and offers a higher degree of stability in the event of an external fault with the current transformer saturation and saturation of the series winding.
A Phase Shifting Transformer Protection Technique Based on a Directional Comparison Approach

This chapter presents a new directional comparison-based internal/external fault detection and discrimination algorithm for the protection of all commonly used phase shifting transformer types. Like traditional differential protection, the proposed solution offers distinguished features such as speed and selectivity. However, unlike PST differential techniques, the proposed algorithm offers great reliability. It provides a secure operation during conditions such as current transformer (CT) saturation, magnetizing inrush, core saturation, any mismatch between CTs and zero-sequence current, etc. Moreover, unlike the differential solution, the proposed algorithm solves the problem of non-standard varying phase shift without tracking the tap-changer position. Performance analysis of the proposed algorithm shows that the algorithm provides the best overall protection solution for commonly used single/two-core symmetrical/asymmetrical PSTs. In addition, this work also explores and investigates the various problems associated with this technique when applied to a PST. Solutions to these problems are proposed by modifying the basic directional criteria and algorithm to ensure the sensitivity and security of the technique.

The concept of directional comparison-based protection techniques has already been proposed and investigated for the detection of a fault on the busbar [36], [37], [38], [39], standard transformer [40], transmission lines [41], [42], synchronous generator [43] and phase selection [44].

5.1. Superimposed or Delta Components

Figure 5.1(a) shows a single line transmission network with a PST linking source to the grid side. A pre-fault network is a purely positive-sequence network, normal system
currents and voltages measured at the source and load sides of the PST are purely pre-fault positive-sequence symmetrical voltages ($V_{S1, preFlt}$, $V_{L1, preFlt}$) and currents ($I_{S1, preFlt}$, $I_{L1, preFlt}$), respectively, as shown in Figure 5.1(b). As the network of Figure 5.1(c) shows, any fault condition results in a dynamic change in the current and voltage waveforms and thus results in post-fault voltages ($V_{S, postFlt}$, $V_{L, postFlt}$) and currents ($I_{S, postFlt}$, $I_{L, postFlt}$). Therefore, the post-fault current or voltage waveform comprises pre-fault and delta components. The delta component is zero during normal system conditions and hence represents a pure-fault positive-sequence superimposed (PSS) network, as shown in Figure 5.1(d). On the other hand, negative- and zero-sequence networks are pure representations of negative- and zero-sequence superimposed networks, respectively.

The positive-sequence superimposed or $\Delta$ components ($\Delta V_1$ and $\Delta I_1$) can be calculated using the pre- and post-fault symmetrical components as

$$\Delta V_1 = V_{1, postFlt} - V_{1, preFlt}$$

$$\Delta I_1 = I_{1, postFlt} - I_{1, preFlt}$$

There is no pre-fault negative-sequence voltage and current hence, negative-sequence superimposed or $\Delta$ components ($\Delta V_2$ and $\Delta I_2$) are simply the post-fault negative sequence voltage and current components defined as:

$$\Delta V_2 = V_{2, postFlt}$$

$$\Delta I_2 = I_{2, postFlt}$$

From $\Delta V$ and $\Delta I$ we can further calculate the delta positive $\Delta Z_1$ and negative-sequence impedances $\Delta Z_2$ as:

$$\Delta Z_1 = \frac{\Delta V_1}{\Delta I_1} = \frac{V_{1, postFlt} - V_{1, preFlt}}{I_{1, postFlt} - I_{1, preFlt}}$$

$$\Delta Z_2 = \frac{\Delta V_2}{\Delta I_2} = \frac{V_{2, postFlt}}{I_{2, postFlt}}$$
Figure 5.1: Illustration of superimposed network: (a) normal power system network, (b) pre-fault positive sequence network, (c) post-fault positive sequence network, and (d) positive-sequence superimposed network.
5.2. Fault Detection Based on Superimposed Components

5.2.1. Directional Criteria

As shown in Figure 5.1(a), two directional elements – relay S and relay L – are applied at the source and load sides of the transformer, respectively. Each element computes the delta positive-sequence/negative-sequence impedances $\Delta Z_{1S}/\Delta Z_{2S}$ and $\Delta Z_{1L}/\Delta Z_{2L}$.

Considering Figure 5.1(c), in the event of an internal fault, $F_1$, both positive-sequence relays $S_1$ and $L_1$ see the fault in the forward direction. Calculation of the superimposed impedances by both of the relays is as follows:

**Relay S1:**

Using the notations of Figure 5.1, pre- and post-fault voltages can be defined as:

\[
V_{IS_{preFlt}} = E_{Ig} - I_{IS_{preFlt}} Z_{Ig}
\]  
(5.1)

\[
V_{IS_{postFlt}} = E_{Ig} - I_{IS_{postFlt}} Z_{Ig}
\]  
(5.2)

Using equations (5.1) and (5.2), the positive-sequence delta impedance can be found as

\[
\Delta Z_{1S} = \frac{\Delta V_{1S}}{\Delta I_{1S}} = \frac{V_{IS_{postFlt}}}{I_{IS_{postFlt}}} - \frac{V_{IS_{preFlt}}}{I_{IS_{preFlt}}}
\]

\[
\Delta Z_{1S} = -Z_{1g}
\]  
(5.3)

**Relay L1:**

The pre- and post-fault voltages can be defined as:

\[
V_{IL_{preFlt}} = E_{Ig} - I_{IL_{preFlt}} (Z_{IL} + Z_{IG})
\]  
(5.4)

\[
V_{IL_{postFlt}} = E_{Ig} - I_{IL_{postFlt}} (Z_{IL} + Z_{IG})
\]  
(5.5)
Using (5.4) and (5.5), the positive-sequence delta impedance can be found as:

\[ \Delta Z_{1L} = -(Z_{1L} + Z_{1G}) \]  

(5.6)

As shown in Figure 5.1, for an external fault, \( F_2 \), relay \( S \) sees the fault in the forward direction and extracts the delta impedance similar to (5.3). On the other hand, relay \( L \) sees the external fault in the reverse direction and computes the delta impedance as:

\[ V_{1L_{preFlt}} = E_1 g e^{j\delta} + I_1 L_{preFlt} (Z_{1g} + Z_{1T}) \]  

(5.7)

\[ V_{1L_{postFlt}} = E_1 g e^{j\delta} + I_1 L_{postFlt} (Z_{1g} + Z_{1T}) \]  

(5.8)

Using (5.7) and (5.8), the positive-sequence delta impedance can be found as:

\[ \Delta Z_{1L} = Z_{1g} + Z_{1T} \]  

(5.9)

Equations (5.3) and (5.6) suggest that for an internal fault, both relays (\( S \) and \( L \)) see the fault in the forward direction and the loci of superimposed impedance computed by both relays lie in the third quadrant (as shown in Figure 5.2) such that

Forward fault: \( 180^\circ \leq \angle \Delta Z_{1} \leq 270^\circ \)
Whereas, for an external fault, one of the two relays S or L sees the fault in the forward direction and another sees the fault in the reverse direction. For example, for an external fault F2, as shown in Figure 5.1(c), relay S sees the fault in the forward direction and the locus of the delta impedance lies in the third quadrant, however, relay L sees the fault in the reverse direction and equation (5.9) suggests that locus of the impedance lies in first quadrant such that

Reverse fault: $90^\circ \leq \angle \Delta Z \leq 0^\circ$

Considering the pure-fault network, as shown in Figure 5.1(c), equation (5.3), (5.6) and (5.9) suggest that for a forward fault the sign of $\Delta V$ and $\Delta I$ are different; whereas for a reverse fault the sign of $\Delta V$ and $\Delta I$ are same.

Similarly, in the event of internal fault (F1 in Figure 5.1(b)), negative-sequence relays S2 and L2 compute the delta impedances ($\Delta Z_{2S}$ and $\Delta Z_{2L}$) that lie in the third quadrant of the impedance plan. Whereas, in the event of external fault (F1 in Figure 5.1(c)), $\Delta Z_{2S}$ and $\Delta Z_{2L}$ lie in the third and first quadrant of the impedance plane, respectively.

5.2.2. Computations

The proposed algorithm comprises the initial signal processing, extraction of the delta components and operating and blocking criteria.

5.2.2.1. Signal Processing

In this work, the superimposed components are computed using the currents and voltages in the phasor-domain. Current and voltage signals are first passed through an anti-aliasing filter to eliminate the higher frequency components, using the low-pass filter with a cut-off frequency of 960 Hz. Input current signals are then processed through the derivative component to remove the dc components. The phase delay in the current signal with reference to voltage signal because of the derivative is compensated prior to sampling.

Using the derivative, to remove the decaying dc, also results in the amplification of the harmonics and/or noises. Therefore, normally it is combined with an additional low pass...
filter to alleviate the harmonics/noises. Using the low pass filter with the derivative add $\frac{1}{4}$ cycle delay. However, in this thesis work, the low pass filter is not used because fundamental frequency phasor are estimated using the discrete Fourier transform (DFT), which mitigates the harmonics.

Sampling of the signals is done with a sampling frequency of 2880 Hz. Full-cycle discrete-Fourier transform (Appendix B) is used to compute the phasor components of the signals. The positive- and negative-sequence components are extracted using the estimated phasor components of the current and voltage signals.

5.2.2.2. Extraction of Superimposed Components

Extraction of the superimposed or delta components is based on the method employed by [37], [38], [39]. Superimposed components of currents and voltages are extracted by subtracting the latest samples of currents and voltages from the pre-fault samples of the corresponding signal stored in the memory. The delta component $\Delta x$ can be defined as

$$\Delta x = x(n) - x_m(n)$$

where

$x(n)$ is the current sample of the signal and

and $x_m(n) = 2x(n-N) - x(n-2N)$

N is total number of samples per cycle.

In this thesis work, extraction of the delta components is done in online mode using the memory buffer as implemented in [45]. Figure 5.3(a) shows the logic diagram of the delta filter. The control switch in Figure 5.3(a) plays an important role in the situation of the evolving fault. In the case of an evolving fault, the memory signal $x_m$ can be maintained by controlling the control switch. With this implementation, as soon as the change is detected (logic is shown in Figure 5.3(b)), the memory signal $x_m$ is latched to the memory register. Therefore, upon occurrence of the evolving fault the signal in the memory remains latched.
To ensure the secure operation of the algorithm, the change is detected in current or voltage signals, when output of the comparator, \textit{COMPI}, is true if the superimposed current and voltage quantities exceed a defined threshold (\textit{THRES}_V or \textit{THRES}_I) value. Therefore, the occurrence of the fault is detected if:

\[
\text{COMPA} = \begin{cases} 
  \text{True} = 2 & \text{if } \Delta V \geq \text{THRES}_V \text{ or } \Delta I \geq \text{THRES}_I \\
  \text{False} = 1 & \text{else}
\end{cases}
\]

Threshold values \textit{THRES}_I and \textit{THRES}_V are normally set as a percentage of the nominal current (~10-20%) and nominal voltage (~5-10%), respectively. However, it is important to consider here that the nominal or base value changes with the operation of the tap-changer in the PST. There is a significant change in currents over the full range of phase-shift between the two ends. Therefore, to ensure the sensitivity of the algorithm for all tap positions, the threshold values are set as a percentage of the online pre-fault or memory current and voltage signals. Therefore, \textit{THRES}_I and \textit{THRES}_V are set 20\% (=k_i) of I_{preFlt} and 10\% (=k_v) of V_{preFlt}, respectively.

Output of the relay S and L is set to 1 (=Trip) if the locus of the delta-impedance lies in the third-quadrant of the relay. The trip decision is made by combining the output of both relays using the AND logic. The same criterion is true for both positive- and negative-sequence superimposed impedances.

### 5.2.2.3. Trip Counters

To ensure a secure decision from the relay, a trip counter is used for each relay. A trip counter tracks the operating quantities (delta positive-sequence impedances \(\Delta Z_{1S}\) and \(\Delta Z_{1L}\)) and increment if the argument of the delta impedance lies in the third quadrant of the impedance plane or decrements if it lies outside of the third quadrant. A final decision is made when the output of the trip counter reaches the set counter threshold limit. A decision from the relay is set to 1 when the trip counter reaches the threshold limit and 0 when it is less than the threshold limit. The same is true for the negative-superimposed impedances.
5.3. Practical Issues and the Proposed Solutions

5.3.1. Energization of an Unloaded PST

As shown in Figure 5.4, a PST is energized by switching the source-side circuit breaker CBS while the load-side CB_L is open. The load-side relay does not measure any current, and therefore there is no computation of the superimposed impedance. If the status of the load-side breaker is open, the relay S at the source side will be responsible for the detection of any internal fault in an unloaded transformer. The following sections address two issues and the proposed solutions, in an unloaded transformer case.

A. Source-side circuit breaker operation

Considering Figure 5.4(a), prior to the closing of the source-side circuit breaker, the pre-energization currents ($I_{1S_{preE}}$, $I_{1L_{preE}}$) measured are zero. However, pre- and post-energization voltages ($V_{IS_{preE}}$, $V_{IS_{postE}}$) measured by the relay S are:

Source-side pre-energization voltage

$$V_{IS_{preE}} = Elg$$  \hspace{1cm} (5.10)
Source-side post-energization voltage

\[ V_{IS_{postE}} = E_{Ig} - IIS_{postE} Z_{Ig} \]  \hspace{1cm} (5.11)

where \( IIS_{postE} \) represents the magnetizing inrush current in the source-side of the transformer.

Since there is no pre-fault current, the superimposed current is equal to the post-energization current

\[ \Delta IIS = IIS_{postE} \]

Using (5.10) and (5.11), the positive-sequence superimposed impedance computed by the relay S is

\[ \Delta Z_{IS} = \frac{\Delta V_{IS}}{\Delta IIS} = \frac{E_{Ig} - IIS_{postE} Z_{Ig} - E_{Ig}}{IIS_{postE}} \]

\[ \Delta Z_{IS} = -Z_{Ig} \]  \hspace{1cm} (5.12)

As per (5.12), during the energization of an unloaded PST, the locus of the superimposed impedance, computed by relay S1, lies in the third quadrant and sees the energization of the PST (or source-side breaker operation) as a forward fault. As a result, this leads to the false operation of the relay. Previously, reference [40] has also addressed this dilemma in the directional comparison based protection algorithm for the standard transformer. Reference [40] also proposes a solution that is based on monitoring the significant change in the voltage ratio of at least a pair of the primary, secondary and tertiary voltages in a standard transformer (there is a significant change in the voltage ratio during the fault condition in comparison to the magnetizing inrush current).

However, the solution proposed by [40] cannot be applied for the case of the PST due to the following two reasons. Firstly, the PST differs in design from the standard transformer, the source and load sides are connected to the same winding (series winding), and therefore, using a ratio of the two end voltages does not always show a
significant change during the various fault conditions. Secondly, in the event of high-resistive or low-current faults, there is a small change in the voltage ratio which can result in no, or false, discrimination between the inrush current phenomena and the fault conditions.

The proposed solution to this issue is to relocate the voltage transformers (VTs) inside the protecting zone as shown in Figure 5.4(b). Therefore, for the case when voltage transformers are located inside the protected zone, voltages measured by the relays S and L before the transformer is energized are zero, hence the incremental current and voltage components are equal to the post-energization inrush current and voltage of the PST. There is no computation of the incremental impedance by the relay L since $I_L$ is zero. The positive-sequence superimposed impedance measured by relay S is therefore

$$
\Delta Z IS = \frac{\Delta V IS}{\Delta I IS} = Z IT
$$

(5.13)
Equation (5.13) shows that the locus of delta impedance computed by relay S during the energization of the PST, while the VT is located inside the protected zone lies in the first quadrant of the impedance plane and sees it as a reverse fault. Therefore, a secure operation of the relay can be achieved during the energization of the PST.

B. Measurement of the Spurious Negative-Sequence Current

The negative-sequence superimposed impedance is independent of the pre-fault components; therefore, the location of the voltage transformer has no effect on the $\Delta Z_{S2}$. However, during the closing operation of the source- and load-side circuit breakers, the signature of the spurious(false) negative-sequence current measured by the relay S is significant, as shown in Figure 5.6 at 0.1sec and 0.31sec. Therefore, the closing operation of the CBs (or CB_L) results in the computation of the negative-sequence incremental impedance ($\Delta Z_{S2} = -Z_{g2}$) that lies in the third quadrant of the impedance plane and leads to a false relay operation.

To ensure the security of the relay in this dilemma, two checks are made prior to the computation of $\Delta Z_{S2}$. The first check monitors the status of the load-side circuit breaker and it is true if the CB status is open. The second check is true if the negative-sequence current $I_{S2}$ or $\Delta I_{S2}$ exceeds the threshold $THRES_2$. Therefore, the computation of $\Delta Z_{S2}$ is only performed when both of these checks are true. Figure 5.5 also shows the

Figure 5.5: Measurement of the negative-sequence current during closing operation of the source- and load- side circuit breaker and phase-ground fault.
magnitude of the negative-sequence current during the high-resistive (50Ω) internal fault, which is much higher than during the circuit breaker operation, as shown at 0.5sec in Figure 5.6. It is also important to mention here that spurious negative-sequence current may reach up to 25% of the positive-sequence current. Therefore, threshold THRES2 must be set to a certain level such that the sensitivity of the relay is not affected for any switch-on fault condition.

5.3.1.1. Internal and External Faults in an Unloaded PST

Positive- and negative-sequence incremental impedances measured by the relay S during the internal fault in an unloaded PST are same as defined in section 5.2.1.

\[ \Delta Z_{IS} = -Z_1 g \]

\[ \Delta Z_{IS} = \frac{\Delta V_{IS}}{\Delta I_{IS}} = -Z_1 g \]

Therefore, for internal faults while the transformer is unloaded, the loci of the both positive- and negative-sequence incremental impedances seen by the relay S lie in the third-quadrant of the impedance plane. Since the load-side current \( I_L \) is zero, relay L does not compute any delta-component.

However, in the event of an external fault, both relays S and L compute the superimposed impedances. The directional criteria during an external fault are the same as have been shown in section 5.2.1.

5.3.2. Operation of the On-Load Tap-Changer

Operation of the tap-changer to control the desired flow of active power results in a change in the normal system current. Therefore, it is important to analyze the relays behavior during the operation of the on-load tap-changer operation.
Relay S1

The pre- and post-operation of the on-load tap-changer voltages $V_{S1 \text{pre}T}$ and $V_{S1 \text{post}T}$, respectively, can be written as:

\[ V_{IS \text{pre}T} = E_1 g - I_1 I_{S1 \text{pre}T} Z_1 g \]  \hspace{1cm} (5.14)

\[ V_{IS \text{post}T} = E_1 g - I_1 I_{S1 \text{post}T} Z_1 g \]  \hspace{1cm} (5.15)

where $I_{S1 \text{pre}T}$ and $I_{S1 \text{post}T}$ are the pre- and post-operation of on-load tap-changer source-side currents.

From (5.14) and (5.15), positive-sequence delta impedance can be found as

\[ \Delta Z_{IS} = -Z_1 g \]  \hspace{1cm} (5.16)

Relay L1

The pre- and post-operation of on-load tap-changer voltages $V_{L1 \text{pre}T}$ and $V_{L1 \text{post}T}$, respectively, can be written as:

\[ V_{IL \text{pre}T} = E_1 g + I_1 I_{L1 \text{pre}T} (Z_1 l + Z_1 g) \]  \hspace{1cm} (5.17)

\[ V_{IL \text{post}T} = E_1 g + I_1 I_{L1 \text{post}T} (Z_1 l + Z_1 g) \]  \hspace{1cm} (5.18)

Using (5.17) and (5.18), the positive-sequence delta impedance can be found as:

\[ \Delta Z_{IL} = -(Z_1 l + Z_1 g) \]  \hspace{1cm} (5.19)

The superimposed impedance (5.16) and (5.19) lies in the third quadrant of the impedance plane, resulting in the mal-operation of the relays.

Solution 1: From section 5.2.2, it is known that the computation of the superimposed impedance is only performed if $|\Delta I|$ exceeds the threshold setting $THRES _I$. However, the magnitude of the $\Delta I$ is proportional to the step size of the tap-changer. In practice,
depending on the application, PSTs are available in various phase shifts and total number of step sizes. Therefore, it must be ensured that \( \text{THRES}_I \) is set greater than the \(|\Delta I|\) per step without losing the sensitivity of the algorithm.

Solution 2: The second proposed solution is to use the source-side voltage \( V_S \) instead of the load-side voltage \( V_L \) to compute the superimposed impedance in the load-side relay \( L \), as shown in Figure 5.6. Computation of the superimposed impedance \( \Delta Z_L \) during the operation of the tap-changer and internal/external faults is as follows:

### 5.3.2.1. Operation of the tap-changer

The pre- and post-operation of the on-load tap-changer voltages \( V_{L1,preT} = V_{S1,preT} \) and \( V_{L1,postT} = V_{S1,postT} \), respectively, can be written as:

\[
V_{IS,preT} = E_I g - I I_{preT} e^{j\delta} Z_I g
\]  
\( (5.20) \)

\[
V_{IS,postT} = E_I g - I I_{postT} e^{j\delta} Z_I g
\]  
\( (5.21) \)

From (5.20) and (5.21), the positive-sequence delta impedance found can be written as:

\[
\Delta Z_{IL} = Z_I g e^{j\delta}
\]  
\( (5.22) \)

The superimposed impedance (5.22) lies in the first quadrant of the impedance plane. Therefore, the secure operation of the relay is achieved during the tap-changer operation of the PST.

Figure 5.6: Computation of delta impedance in relay \( L \) using source-side voltages.
5.3.2.2. Internal Fault

In the event of internal fault, the pre- and post-fault voltages \( VL_{preFlt} = VS_{preFlt} \) and \( VL_{postFlt} = VS_{postFlt} \), respectively, can be written as

\[
VL_{preFlt} e^{j\delta} = E_1 g - I I L_{preFlt} (Z1L + Z1G) \tag{5.23}
\]

\[
VL_{postFlt} e^{j\delta} = E_1 g - I I L_{postFlt} (Z1L + Z1G) \tag{5.24}
\]

From (5.23) and (5.24), the positive-sequence delta impedance found can be written as

\[
\Delta Z1L = -(Z1L + Z1G) e^{j\delta} \tag{5.25}
\]

The locus of the delta positive-sequence impedance seen by the relay L lie in the third quadrant of the impedance plane. Therefore, relay L sees the internal fault in the forward direction.

5.3.2.3. External Fault

The pre- and post-fault voltages \( VL_{preFlt} = VS_{preFlt} \) and \( VL_{postFlt} = VS_{postFlt} \), respectively, can be written as:

\[
VL_{preFlt} = E_1 g - I I L_{preFlt} e^{j\delta} Z1g \tag{5.26}
\]

\[
VL_{postFlt} = E_1 g I - I I L_{postFlt} e^{j\delta} Z1g \tag{5.27}
\]

From (5.26) and (5.27), the positive-sequence delta impedance can be found as:

\[
\Delta Z1L = Z1g e^{j\delta} \tag{5.28}
\]

Equation (5.28) shows that during external fault, the locus of the delta impedance lies in the first quadrant and therefore, sees the external fault in the reverse direction.

Using the source-side voltage measurement to compute the superimposed impedance, (5.22) shows that during the operation of the tap-changer, the locus of the \( \Delta ZL \) lies in the
first quadrant of the impedance hence ensuring the security of the relay. Moreover, during fault conditions, (5.25) and (5.28) show that the impedance lies in the third and first quadrant of the impedance plane for internal and external faults, respectively. However, (5.25) and (5.28) also show us that the loci of the superimposed impedance are now shifted by the phase shift, $\delta$.

Therefore, the sensitivity of the relay can be increased by proposing the modification in the basic directional criteria, such that for a forward fault, as shown in Figure 5.7.

Forward fault: $180^\circ + \delta \leq \angle \Delta Z l \leq 270^\circ + \delta$

Whereas, for a reverse fault, the loci of the superimposed impedance computed by the relays lie in the first quadrant such that

Reverse fault: $90^\circ + \delta \leq \angle \Delta Z l \leq 0^\circ + \delta$

5.4. Performance Evaluation

To demonstrate the effectiveness of the proposed protection method, several test cases of
normal and fault system conditions have been simulated for two-core symmetrical PSTs. The power system test model (Model 3 in Appendix C) was simulated in PSCAD/EMTDC. To obtain the real representation of currents and voltages, modeling of the delta-hexagonal and standard-delta PSTs is done based on the nameplate information of the real PSTs. Details of the test model and system parameters are given in Appendix C. Results of the few test cases are presented in this section; however, more test results, both in graphical and tabular forms, are given in Appendix E.

5.4.1. Simulation Cases

Tests are formed for different system conditions such as source impedance ratio, SIRs (0.2, 1, 5), PST tap positions (high (0.7<D<1), mid (D=0.5) and low (0<D<0.3)). External (F1, F2) and internal (F3, F4) faults were simulated on the source and load sides of the series winding as well as on the primary and secondary sides of the exciting winding, as shown in Figure 5.8. Winding faults in both series and exciting units were simulated as a turn-to-turn fault (S1 closed, S2 and S3 opened; or S4 closed, S5 and S6 opened), turn-to-ground fault (S2 closed, S1 and S3 opened; or S5 closed, S4 and S6 opened), and winding-to-winding fault (S3 closed, S1 and S2 opened; or S6 closed, S4 and S5 opened), as implemented in Figure 5.8.

The following description summarizes the representation of signals, labels, legends and symbols used in Figure 5.9 to Figure 5.39.

Source, load and exciting-winding terminal currents: S-side (A), L-side (A), E-side (A)
Source- and load-side voltages: S-side (V), L-side (V)
Phase quantities: phA, phB and phC
Arguments (\(\angle \Delta Z_{S1}/\angle \Delta Z_{S2}\)) computed by Relay S: Angle (Relay S1), Angle (Relay S2)
Arguments (\(\angle \Delta Z_{L1}/\angle \Delta Z_{L2}\)) computed by Relay L: Angle (Relay L1), Angle (Relay L2)
Status of source-side circuit breaker: CBS
Fault inception: internal (Int.FLT); external (Ext.FLT)
Combined trip signal: Trip
Trip signals of positive and negative sequence relays: Trip_POS and Trip_Neg

Figure 5.8: Fault modeling of two core symmetrical PST

5.4.2. Energization of the Unloaded PST

Case 5-1: As shown in Figure 5.9, significant magnetization inrush currents at the source side (S-side in Figure 5.9) are obtained when the unloaded PST is energized while the source-side phase voltages pass the zero-crossing and enter into the positive half cycle. Figure 5.9 also shows the arguments of the positive-sequence impedance ($\Delta Z_{S1}, \Delta Z_{L1}$) for relays S1 and L1 and negative-sequence impedance ($\Delta Z_{S2}, \Delta Z_{L2}$) for relays S2 and L2. The argument computed by S1 lies in the first quadrant of the impedance plane; however, the argument computed by load side relay L1 (and L2) is zero since load-side current is zero. As discussed in section 5.3.1, closing of the source-side circuit breaker (CB$_S$) results in the negative-sequence current (IS$_2$ in Figure 5.9); however, as expected there is no computation of the negative-sequence argument($\angle \Delta Z_{S2}$) due to the block criteria set to ensure the security of the relay, as shown in Figure 5.9. The figure also shows that the digital signals, the overall trip signal is zero and therefore relay remains stable during energization of the PST.
5.4.2.1. Switch-on-to Internal Fault in an Unloaded PST

Case 5-2: A phase A-g fault of low fault resistance (0.1 ohms) was simulated at location F3 as shown in Figure 5.10 while the PST is operating at the full-tap position and SIR=0.2. As shown in Figure 5.10, the inception of the fault (Int. FLT) is at a time of 0.196 sec. Since the negative-sequence current (IS2 in Figure 5.10) was greater than the threshold THRES_S2, relay S2 computed the negative-sequence argument ($\Delta Z_{S2}$) that lies in the third quadrant of the impedance plan and issues the trip signal (Trip_Neg). A combined trip signal (Trip as shown in Figure 5.10) was initiated by the relay at 0.209 sec.
Case 5-3: Figure 5.10: Switch-on-to internal phase A-g fault in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS2) and digital output signals (Case 5-2).

(operating time of 13 msec) after the trip counter of the relay S2 reached the threshold (=1/4 cycle). The algorithm took 8.835 msec to make the decision.

Case 5-3: Figure 5.11 shows the performance of the relay for the case when SIR=1; fault location is F3, CB5 operation is at 0.193 sec, fault type is phase A-g with a fault resistance of 20 ohms while the PST is operating at the mid tap position. The fault was initiated at 0.196 sec and relay S2 operated at 0.215 sec with a total operating time of 22 ms. A combined trip signal was initiated by the relay at 0.215 sec after the trip counter of relay S2 reached the threshold (=1/4 cycle). The algorithm took 17.83 msec to make the decision.
Case 5-4: Figure 5.12 shows the performance of the relay for the case when SIR=1; D=0.5, fault location is F4, CB₅ operation is at 0.193 sec, fault type is phase B-g with a fault resistance of 0.1 ohms. The fault was initiated at 0.196 sec and a combined trip signal was initiated by the relay at 0.213 sec after the trip counter of relay S2 reached the threshold (=1/4 cycle). The algorithm took 12.83 msec to make the decision.

Figure 5.11: Switch-on-to internal A-g fault in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS₂) and digital output signals (Case 5-3).

Figure 5.12: Switch-on-to B-g in an unloaded transformer: arguments computed by positive-sequence superimposed elements (S1 & L1), negative-sequence superimposed elements (S2 & L2), waveform of negative sequence current (IS₂) and digital output signals (Case 5-4).
Table 5-1 shows more switch-on internal faults in an unloaded PST, the average algorithm operating and relay tripping time is 7.33 and 11.5 msec, respectively.

**Table 5-1: Relay operating times for switch-on-to internal faults in an unloaded PST**

<table>
<thead>
<tr>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Type</th>
<th>Fault Location</th>
<th>Algorithm operating time (ms)</th>
<th>Trip time (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>high</td>
<td>C-g</td>
<td>F4</td>
<td>8.83</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BC</td>
<td>F5</td>
<td>3.83</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>turn-turn (5% of winding)</td>
<td>S1</td>
<td>7.834</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Turn-ground (1% from neutral)</td>
<td>S5</td>
<td>16.84</td>
<td>21</td>
</tr>
<tr>
<td>0.2</td>
<td>low</td>
<td>C-g</td>
<td>F4</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BC</td>
<td>F5</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>turn-turn (5% of winding)</td>
<td>S1</td>
<td>6.83</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Turn-ground (1% from neutral)</td>
<td>S5</td>
<td>15.84</td>
<td>20</td>
</tr>
<tr>
<td>5</td>
<td>high</td>
<td>B-g</td>
<td>F4</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BC</td>
<td>F5</td>
<td>4.84</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>turn-turn (5% of winding)</td>
<td>S1</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Turn-ground (1% from neutral)</td>
<td>S5</td>
<td>12.84</td>
<td>17</td>
</tr>
<tr>
<td>5</td>
<td>low</td>
<td>C-g</td>
<td>F4</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BC</td>
<td>F5</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>turn-turn (5% of winding)</td>
<td>S1</td>
<td>3.84</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Turn-ground</td>
<td>S5</td>
<td>12.84</td>
<td>17</td>
</tr>
</tbody>
</table>

5.4.2.2. Internal Fault in an Unloaded PST

Table 5-2 and Table 5-3 show the performance of the relay for various internal faults in an unloaded transformer. Single-phase-to-ground faults are tested for low (0.1 ohms) and high resistance (20 ohms). Each case is tested for SIRs (1 and 5) while the PST is operating at high and low tap positions. The fault was initiated at 0.196 sec and relay S2 operated at 0.215 sec with a total operating time of 22 ms. A combined trip signal was initiated by the relay at 0.215 sec after the trip counter of relay S2 reached the threshold (=1/4 cycle). The algorithm took 17.83 msec to make the decision.
Table 5-2: Relay operating times for internal faults in an unloaded PST for SIR 1

<table>
<thead>
<tr>
<th>Case.#</th>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Algorithm operating time(ms)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-5</td>
<td>1</td>
<td>high</td>
<td>F4(Ag)</td>
<td>0.1</td>
<td>8.83</td>
<td>13</td>
<td>Figure E.1</td>
</tr>
<tr>
<td>Case 5-6</td>
<td></td>
<td></td>
<td>F4(Ag)</td>
<td>20</td>
<td>8.83</td>
<td>13</td>
<td>Figure E.2</td>
</tr>
<tr>
<td>Case 5-7</td>
<td></td>
<td></td>
<td>F5(Cg)</td>
<td>20</td>
<td>9.83</td>
<td>14</td>
<td>Figure E.3</td>
</tr>
<tr>
<td>Case 5-8</td>
<td></td>
<td></td>
<td>F6(Ag)</td>
<td>0.1</td>
<td>7.83</td>
<td>12</td>
<td>Figure E.4</td>
</tr>
<tr>
<td>Case 5-9</td>
<td></td>
<td></td>
<td>F6(Ag)</td>
<td>10</td>
<td>13.83</td>
<td>18</td>
<td>Figure E.5</td>
</tr>
<tr>
<td>Case 5-10</td>
<td></td>
<td>low</td>
<td>F3(Cg)</td>
<td>20</td>
<td>9.83</td>
<td>14</td>
<td>Figure E.6</td>
</tr>
<tr>
<td>Case 5-11</td>
<td></td>
<td></td>
<td>F4(Ag)</td>
<td>20</td>
<td>9.83</td>
<td>14</td>
<td>Figure E.7</td>
</tr>
<tr>
<td>Case 5-12</td>
<td></td>
<td></td>
<td>F4(BC)</td>
<td>0.2</td>
<td>5.83</td>
<td>10</td>
<td>Figure E.8</td>
</tr>
<tr>
<td>Case 5-13</td>
<td></td>
<td></td>
<td>F3(BC)</td>
<td>0.2</td>
<td>2.83</td>
<td>7</td>
<td>Figure E.9</td>
</tr>
<tr>
<td>Case 5-14</td>
<td></td>
<td></td>
<td>F5(AC)</td>
<td>0.2</td>
<td>7.83</td>
<td>12</td>
<td>Figure E.10</td>
</tr>
<tr>
<td>Case 5-15</td>
<td></td>
<td></td>
<td>F5(ABC)</td>
<td>0.2</td>
<td>5.83</td>
<td>10</td>
<td>Figure E.11</td>
</tr>
</tbody>
</table>

Table 5-3: Relay operating times for internal faults in an unloaded PST for SIR 5

<table>
<thead>
<tr>
<th>Case.#</th>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Algorithm operating time(ms)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-16</td>
<td>SIR 5</td>
<td>high</td>
<td>F4</td>
<td>0.1</td>
<td>8.83</td>
<td>13</td>
</tr>
<tr>
<td>Case 5-17</td>
<td></td>
<td></td>
<td>F4</td>
<td>20</td>
<td>13.83</td>
<td>18</td>
</tr>
<tr>
<td>Case 5-18</td>
<td></td>
<td></td>
<td>F5</td>
<td>0.1</td>
<td>7.83</td>
<td>12</td>
</tr>
<tr>
<td>Case 5-19</td>
<td></td>
<td></td>
<td>F5</td>
<td>20</td>
<td>12.83</td>
<td>17</td>
</tr>
<tr>
<td>Case 5-20</td>
<td></td>
<td>low</td>
<td>F3</td>
<td>0.1</td>
<td>6.83</td>
<td>11</td>
</tr>
<tr>
<td>Case 5-21</td>
<td></td>
<td></td>
<td>F3</td>
<td>20</td>
<td>8.83</td>
<td>13</td>
</tr>
<tr>
<td>Case 5-22</td>
<td></td>
<td></td>
<td>F5</td>
<td>0.1</td>
<td>5.83</td>
<td>10</td>
</tr>
<tr>
<td>Case 5-23</td>
<td></td>
<td></td>
<td>F5</td>
<td>20</td>
<td>6.83</td>
<td>11</td>
</tr>
</tbody>
</table>

5.4.3. Internal Faults in a Loaded PST

Single Phase-to-Ground fault

Table 5-4 shows the performance of the algorithm for various single phase-to-ground faults of high and low resistances for the PST operating at high and low tap positions and with SIR=1. The average operating time (sec) of the relay for low- and high-resistance faults is 11 msec and 13 msec, respectively. The algorithm took an average time of 6.834 msec (low resistive faults) and 8.834 msec (high resistive faults) to make the decision.
Table 5-4: Relay operating times for internal phase-to-ground faults for SIR=1

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>R(Ω)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-24</td>
<td>high</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>11</td>
<td>Figure 5.13</td>
</tr>
<tr>
<td>Case 5-25</td>
<td></td>
<td>F4(A-g)</td>
<td>20</td>
<td>18</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>Case 5-26</td>
<td></td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>12</td>
<td>Figure 5.15</td>
</tr>
<tr>
<td>Case 5-27</td>
<td></td>
<td>F5(C-g)</td>
<td>20</td>
<td>17</td>
<td>Figure 5.16</td>
</tr>
<tr>
<td>Case 5-28</td>
<td></td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>11</td>
<td>Figure 5.17</td>
</tr>
<tr>
<td>Case 5-29</td>
<td>low</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>10</td>
<td>Figure 5.18</td>
</tr>
<tr>
<td>Case 5-30</td>
<td></td>
<td>F4(A-g)</td>
<td>20</td>
<td>9</td>
<td>Figure 5.19</td>
</tr>
<tr>
<td>Case 5-31</td>
<td></td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>9</td>
<td>Figure 5.20</td>
</tr>
<tr>
<td>Case 5-32</td>
<td></td>
<td>F5(C-g)</td>
<td>20</td>
<td>8</td>
<td>Figure 5.21</td>
</tr>
<tr>
<td>Case 5-33</td>
<td></td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>13</td>
<td>Figure 5.22</td>
</tr>
</tbody>
</table>

Figure 5.13: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 Ω) at location F4 (Case 5-24).

Figure 5.14: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 20 Ω) at location F4 (Case 5-25).
Figure 5.15: Plots of arguments and digital signals in the event of phase C-g fault (fault resistance 0.1 Ω) at location F5 (Case 5-26).

Figure 5.16: Plots of arguments and digital signals in the event of phase C-g fault (fault resistance 20 Ω) at location F5 (Case 5-28).

Figure 5.17: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 Ω) at location F6 (Case 5-27).

Figure 5.18: Plots of arguments and digital signals in the event of phase A-g fault (fault resistance 0.1 Ω) at location F4 (Case 5-29).
Figure 5.19: Plots of arguments and digital signals in the event of (resistance 20 Ω) at fault location F4 (Case 5-30).

Figure 5.20: Plots of arguments and digital signals in the event of C-g fault (fault resistance 0.1 Ω) at location F5 (Case 5-31).

Figure 5.21: Plots of arguments and digital signals in the event of C-g fault (fault resistance 20 Ω) at location F5 (Case 5-32).

Figure 5.22: Plots of arguments and digital signals in the event of C-g fault (fault resistance 0.1 Ω) at location F6 (Case 5-33).
Table 5-5 and Table 5-6 show more results of single phase-to-ground fault for SIR = 0.2 and 5 respectively.

Table 5-5. Relay operating times for internal phase-to-ground fault for SIR=0.2

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-34</td>
<td>high</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>9</td>
</tr>
<tr>
<td>Case 5-35</td>
<td>high</td>
<td>F4(A-g)</td>
<td>20</td>
<td>12</td>
</tr>
<tr>
<td>Case 5-36</td>
<td>high</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-37</td>
<td>high</td>
<td>F5(C-g)</td>
<td>20</td>
<td>12</td>
</tr>
<tr>
<td>Case 5-38</td>
<td>high</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>13</td>
</tr>
<tr>
<td>Case 5-39</td>
<td>high</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-40</td>
<td>high</td>
<td>F4(A-g)</td>
<td>20</td>
<td>11</td>
</tr>
<tr>
<td>Case 5-41</td>
<td>high</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-42</td>
<td>high</td>
<td>F5(C-g)</td>
<td>20</td>
<td>13</td>
</tr>
<tr>
<td>Case 5-43</td>
<td>high</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>17</td>
</tr>
<tr>
<td>Case 5-44</td>
<td>low</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-45</td>
<td>low</td>
<td>F4(A-g)</td>
<td>20</td>
<td>9</td>
</tr>
<tr>
<td>Case 5-46</td>
<td>low</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-47</td>
<td>low</td>
<td>F5(C-g)</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>Case 5-48</td>
<td>low</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>14</td>
</tr>
<tr>
<td>Case 5-49</td>
<td>low</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>7</td>
</tr>
<tr>
<td>Case 5-50</td>
<td>low</td>
<td>F4(A-g)</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-51</td>
<td>low</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>7</td>
</tr>
<tr>
<td>Case 5-52</td>
<td>low</td>
<td>F5(C-g)</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-53</td>
<td>low</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>18</td>
</tr>
</tbody>
</table>

Table 5-6: Relay operating times for internal phase-to-ground fault for SIR=5

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-44</td>
<td>high</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-45</td>
<td>high</td>
<td>F4(A-g)</td>
<td>20</td>
<td>9</td>
</tr>
<tr>
<td>Case 5-46</td>
<td>high</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-47</td>
<td>high</td>
<td>F5(C-g)</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>Case 5-48</td>
<td>high</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>14</td>
</tr>
<tr>
<td>Case 5-49</td>
<td>high</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>7</td>
</tr>
<tr>
<td>Case 5-50</td>
<td>high</td>
<td>F4(A-g)</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-51</td>
<td>high</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>7</td>
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<tr>
<td>Case 5-52</td>
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<td>F5(C-g)</td>
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</tr>
<tr>
<td>Case 5-53</td>
<td>high</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>18</td>
</tr>
<tr>
<td>Case 5-44</td>
<td>low</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-45</td>
<td>low</td>
<td>F4(A-g)</td>
<td>20</td>
<td>9</td>
</tr>
<tr>
<td>Case 5-46</td>
<td>low</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-47</td>
<td>low</td>
<td>F5(C-g)</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>Case 5-48</td>
<td>low</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>14</td>
</tr>
<tr>
<td>Case 5-49</td>
<td>low</td>
<td>F4(A-g)</td>
<td>0.1</td>
<td>7</td>
</tr>
<tr>
<td>Case 5-50</td>
<td>low</td>
<td>F4(A-g)</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-51</td>
<td>low</td>
<td>F5(C-g)</td>
<td>0.1</td>
<td>7</td>
</tr>
<tr>
<td>Case 5-52</td>
<td>low</td>
<td>F5(C-g)</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td>Case 5-53</td>
<td>low</td>
<td>F6(A-g)</td>
<td>0.1</td>
<td>18</td>
</tr>
</tbody>
</table>

5.4.3.1. Phase-to-Phase and Three-Phase Faults

Table 5-7 shows the performance of the algorithm for various phase-to-phase, double phase-to-ground, and three phase faults of high and low resistances for the PST operating
at the high, mid and low tap position and SIR=1. The average operating time (sec) of the relay for low and high resistance faults is 10.33 msec, respectively. The algorithm took an average time of 6.834 msec and 6.166 msec to make the decision.

More results for SIR = 0.2 and 5 are available in Appendix E.

Table 5-7: Relay operating times for internal phase-to-phase and 3 ph. faults, SIR=1

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Tap Position</th>
<th>Fault type</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-54</td>
<td>high</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>12</td>
<td>Figure 5.23</td>
</tr>
<tr>
<td>Case 5-55</td>
<td></td>
<td>BC-g</td>
<td>F5</td>
<td>20</td>
<td>12</td>
<td>Figure 5.24</td>
</tr>
<tr>
<td>Case 5-56</td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>9</td>
<td>Figure 5.25</td>
</tr>
<tr>
<td>Case 5-57</td>
<td>mid</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>13</td>
<td>Figure 5.26</td>
</tr>
<tr>
<td>Case 5-58</td>
<td></td>
<td>BC-g</td>
<td>F5</td>
<td>20</td>
<td>12</td>
<td>Figure 5.27</td>
</tr>
<tr>
<td>Case 5-59</td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>9</td>
<td>Figure 5.28</td>
</tr>
<tr>
<td>Case 5-60</td>
<td>low</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>8</td>
<td>Figure 5.29</td>
</tr>
<tr>
<td>Case 5-61</td>
<td></td>
<td>BC-g</td>
<td>F5</td>
<td>20</td>
<td>9</td>
<td>Figure 5.30</td>
</tr>
<tr>
<td>Case 5-62</td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>9</td>
<td>Figure 5.31</td>
</tr>
</tbody>
</table>

Figure 5.23: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-54)

Figure 5.24: Plots of arguments and digital signals in the event of BC fault at location at F5 (Case 5-55).
Figure 5.25: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-56).

Figure 5.26: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-57).

Figure 5.27: Plots of arguments and digital signals in the event of BC-g fault at location F5 (Case 5-58).

Figure 5.28: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-59).
Figure 5.29: Plots of arguments and digital signals in the event of BC fault at location F4 (Case 5-60).

Figure 5.30: Plots of arguments and digital signals in the event of BC-g fault at location F5 (Case 5-61).

Figure 5.31: Plots of arguments and digital signals in the event of ABC fault at location F6 (Case 5-62).

5.4.4. Turn-to-Turn Faults

Table 5-8 shows the performance of the algorithm for various turn-to-turn faults of different percentages of shorted turn of the corresponding winding. The average
operating time (sec) of the relay is 12.78 msec. The algorithm took an average of time 8.61 msec to make the decision.

Table 5-8: Relay operating times for turn-to-turn faults

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Tap position</th>
<th>SIR</th>
<th>Fault Location</th>
<th>Shorted turn(% of winding)</th>
<th>Trip time(ms)</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-63</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>5</td>
<td>16</td>
<td>Figure E.12</td>
</tr>
<tr>
<td>Case 5-64</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>2</td>
<td>15</td>
<td>Figure E.13</td>
</tr>
<tr>
<td>Case 5-65</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>5</td>
<td>15</td>
<td>Figure E.14</td>
</tr>
<tr>
<td>Case 5-66</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>2</td>
<td>16</td>
<td>Figure E.15</td>
</tr>
<tr>
<td>Case 5-67</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>5</td>
<td>10</td>
<td>Figure E.16</td>
</tr>
<tr>
<td>Case 5-68</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>2</td>
<td>10</td>
<td>Figure E.17</td>
</tr>
<tr>
<td>Case 5-69</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>5</td>
<td>10</td>
<td>Figure E.18</td>
</tr>
<tr>
<td>Case 5-70</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>2</td>
<td>10</td>
<td>Figure E.19</td>
</tr>
<tr>
<td>Case 5-71</td>
<td></td>
<td>High</td>
<td>SW-Primary</td>
<td>5</td>
<td>15</td>
<td>Figure E.20</td>
</tr>
<tr>
<td>Case 5-72</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>2</td>
<td>16</td>
<td>Figure E.21</td>
</tr>
<tr>
<td>Case 5-73</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>5</td>
<td>15</td>
<td>Figure E.22</td>
</tr>
<tr>
<td>Case 5-74</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>2</td>
<td>16</td>
<td>Figure E.23</td>
</tr>
<tr>
<td>Case 5-75</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>5</td>
<td>11</td>
<td>Figure E.24</td>
</tr>
<tr>
<td>Case 5-76</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>2</td>
<td>11</td>
<td>Figure E.25</td>
</tr>
<tr>
<td>Case 5-77</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>5</td>
<td>11</td>
<td>Figure E.26</td>
</tr>
<tr>
<td>Case 5-78</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>2</td>
<td>11</td>
<td>Figure E.27</td>
</tr>
<tr>
<td>Case 5-79</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>5</td>
<td>21</td>
<td>Figure E.28</td>
</tr>
<tr>
<td>Case 5-80</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>2</td>
<td>20</td>
<td>Figure E.29</td>
</tr>
<tr>
<td>Case 5-81</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>5</td>
<td>15</td>
<td>Figure E.30</td>
</tr>
<tr>
<td>Case 5-82</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>2</td>
<td>15</td>
<td>Figure E.31</td>
</tr>
<tr>
<td>Case 5-83</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>5</td>
<td>8</td>
<td>Figure E.32</td>
</tr>
<tr>
<td>Case 5-84</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>2</td>
<td>8</td>
<td>Figure E.33</td>
</tr>
<tr>
<td>Case 5-85</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>5</td>
<td>8</td>
<td>Figure E.34</td>
</tr>
<tr>
<td>Case 5-86</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>2</td>
<td>8</td>
<td>Figure E.35</td>
</tr>
<tr>
<td>Case 5-87</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>5</td>
<td>15</td>
<td>Figure E.36</td>
</tr>
<tr>
<td>Case 5-88</td>
<td></td>
<td></td>
<td>SW-Primary</td>
<td>2</td>
<td>15</td>
<td>Figure E.37</td>
</tr>
<tr>
<td>Case 5-89</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>5</td>
<td>14</td>
<td>Figure E.38</td>
</tr>
<tr>
<td>Case 5-90</td>
<td></td>
<td></td>
<td>SW-Secondary</td>
<td>2</td>
<td>14</td>
<td>Figure E.39</td>
</tr>
<tr>
<td>Case 5-91</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>5</td>
<td>8</td>
<td>Figure E.40</td>
</tr>
<tr>
<td>Case 5-92</td>
<td></td>
<td></td>
<td>EW-Primary</td>
<td>2</td>
<td>8</td>
<td>Figure E.41</td>
</tr>
<tr>
<td>Case 5-93</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>5</td>
<td>8</td>
<td>Figure E.42</td>
</tr>
<tr>
<td>Case 5-94</td>
<td></td>
<td></td>
<td>EW-Secondary</td>
<td>2</td>
<td>8</td>
<td>Figure E.43</td>
</tr>
</tbody>
</table>
5.4.5. External Faults in a Loaded PST

Table 5-9 shows the performance of the proposed algorithm in the event of external phase-to-ground, phase-to-phase, and three-phase faults with and without CT saturation. The results show that relays S and L compute positive- and negative-sequence superimposed impedance loci in the third and first quadrant, respectively. Thus, the relay remains stable during external faults. The entire test was performed at the mid-tap position of the PST for SIR = 1.

Table 5-9: Relay performance in the event of external faults

<table>
<thead>
<tr>
<th>Case.#</th>
<th>Fault Location</th>
<th>Fault type</th>
<th>With CT saturation</th>
<th>Relay Operation</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 5-95</td>
<td>F1</td>
<td>Ag</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.32</td>
</tr>
<tr>
<td>Case 5-96</td>
<td></td>
<td>BC</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.33</td>
</tr>
<tr>
<td>Case 5-97</td>
<td></td>
<td>BC-g</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.34</td>
</tr>
<tr>
<td>Case 5-98</td>
<td></td>
<td>ABC</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.35</td>
</tr>
<tr>
<td>Case 5-99</td>
<td>F2</td>
<td>Ag</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.36</td>
</tr>
<tr>
<td>Case 5-100</td>
<td></td>
<td>BC</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.37</td>
</tr>
<tr>
<td>Case 5-101</td>
<td></td>
<td>BC-g</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.38</td>
</tr>
<tr>
<td>Case 5-102</td>
<td></td>
<td>ABC</td>
<td>No</td>
<td>No Trip</td>
<td>Figure 5.39</td>
</tr>
<tr>
<td>Case 5-103</td>
<td>F1</td>
<td>Ag</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.44</td>
</tr>
<tr>
<td>Case 5-104</td>
<td></td>
<td>BC</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.45</td>
</tr>
<tr>
<td>Case 5-105</td>
<td></td>
<td>BC-g</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.46</td>
</tr>
<tr>
<td>Case 5-106</td>
<td></td>
<td>ABC</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.47</td>
</tr>
<tr>
<td>Case 5-107</td>
<td>F2</td>
<td>Ag</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.48</td>
</tr>
<tr>
<td>Case 5-108</td>
<td></td>
<td>BC</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.49</td>
</tr>
<tr>
<td>Case 5-109</td>
<td></td>
<td>BC-g</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.50</td>
</tr>
<tr>
<td>Case 5-110</td>
<td></td>
<td>ABC</td>
<td>Yes</td>
<td>No Trip</td>
<td>Figure E.51</td>
</tr>
</tbody>
</table>
Figure 5.32: Plots of arguments and digital signals in the event of external A-g fault at location F1 (Case 5-95).

Figure 5.33: Plots of arguments and digital signals in the event of external BC fault at location F1 (Case 5-96).

Figure 5.34: Plots of arguments and digital signals in the event of external BC-g fault at location F1 (Case 5-97).

Figure 5.35: Plots of arguments and digital signals in the event of external ABC fault at location F1 (Case 5-98).
Figure 5.36: Plots of arguments and digital signals in the event of external A-g fault at location F2 (Case 5-99).

Figure 5.37: Plots of arguments and digital signals in the event of external BC fault at location F2 (Case 5-100)

Figure 5.38: Plots of arguments and digital signals in the event of external BC-g fault at location F2 (Case 5-101)

Figure 5.39: Plots of arguments and digital signals in the event of external ABC fault at location F2 (Case 5-102)
5.5. Summary

This chapter presented a new phase shifting transformer protection technique based on the directional comparison principle. The proposed technique can be applied as a main or backup protection for the protection of any kind of PST. The fault detection criterion is based on the direction of the fault seen by two directional comparison elements installed at the source and load sides of the transformers. Based on the directional comparison principle, the loci of the superimposed positive- and negative-sequence impedances lie in the third quadrant of the impedance plane for the forward faults; however, in the case of a reverse fault, the loci lie in the first quadrant of the impedance plane. However, implementation of the proposed protection principle for the protection of a phase shifting transformer is not a straightforward solution. A large part of this chapter was dedicated to address the various practical issues that arise while applying the proposed protection approach. In the same context, various solutions have been proposed to achieve a more secure and sensitive solution.

To demonstrate the effectiveness of the proposed protection technique, a large number of test cases have been simulated and applied to the two-core symmetrical PST. The proposed technique is tested for various fault and non-fault conditions. The test results showed that the proposed protection method offers a more sensitive and secure protection solution as compared to protection principles based on the current differential approach.
Chapter 6

Summary and Conclusions

Phase shifting transformers are widely used for the control of power flow over parallel transmission lines. Like the standard transformer, the phase shifting transformer is mainly protected by the differential protection technique in addition to other electrical and mechanical protection elements. However, the existing differential current measuring principles are strongly associated with the conventional and unconventional challenges, which can jeopardize the security and sensitivity of the differential protection relay. To resolve the challenges associated with PST differential protection, this thesis focuses on the development of new protection technique that ensure a more reliable protection solution. However, the unavailability of the PST short-circuit and simulation models that must represent an accurate mimic of the PST, leads us to the development of the modeling of the various kinds of PST for short-circuit and protection studies. Therefore, this research mainly worked on the development of both PST modeling and protection.

6.1. Summary

The first chapter of the thesis mainly described the brief introduction of power system protection and the research objectives of the thesis. Chapter 2 presented a brief outline of the basic working principle, types, modeling and current differential protection principles of the phase shifting transformer. The existing available modeling solutions and their limitations were described followed by the traditional and non-traditional problems associated with the differential protection principles.

The proposed modeling solution of single-core standard-delta and two-core symmetrical phase shifting transformers, which can be used for both balanced and unbalanced system conditions, are presented in chapter 3. The proposed modeling approach is based on the development of positive-, negative- and zero-sequence networks; derived mathematical relations are further used to develop the relations of winding-terminal voltages, currents
and impedances as a function of the tap position. The accuracy of the presented models was first verified mathematically with the manufacturer’s test report data. Then EMTP modeling was done in RTDS to further test and verify the digital model.

Chapter 4 of the thesis presented a new protection method based on the electromagnetic differential equations for both delta-hexagonal and standard-delta PSTs. The method was tested for various faulted and non-faulted power system conditions. In addition to the internal/external fault detection and discrimination capability, unlike differential protection, the proposed algorithm remains stable during magnetization inrush current and offers a higher degree of stability in the event of an external fault with current transformer saturation and saturation of the series winding.

In Chapter 5, a directional comparison-based protection technique has been presented for the protection of phase shifting transformers of all kinds. Various practical issues associated with the algorithm are addressed, followed by the proposed solutions to these issues. The proposed technique is tested for various fault and no-fault conditions.

6.2. Conclusions

Conclusions of this thesis can be made based on (i) modeling and (ii) protection of phase shifting transformers.

Modeling of the single-core standard delta, two-core symmetrical and asymmetrical PSTs were done for the short-circuit and protection studies. Based on the test results obtained mathematically and from the suggested EMTP models it can be concluded that:

- Unlike existing available models, the proposed models do not require detailed test report data from the manufacturer.
- Symmetrical component-based modeling methodology is used, and therefore, can be accurately used for short-circuit analysis and load-flow studies.
Using the proposed models, an accurate representation of real transformers can be obtained to simulate current and voltage signals for various normal and faulted power system conditions.

Derived relations of voltage, current and impedance as a function of the tap position can be further used for the study and development of existing and new protection techniques.

To simulate inter-turn, turn-ground and winding-winding faults, the suggested equivalent models can be implemented in commonly used EMTP tools such as EMTDC/PSCAD or RTDS.

This thesis aimed to develop a new protection method that is able to resolve the challenges and problems associated with PST current differential-based protection techniques and offer a more reliable protection solution to protect the PST. Conclusions of each protection method (presented in chapters 4 and 5) can be made as follows:

**Electromagnetic differential protection**

- Without any restraining or blocking unit, the proposed algorithm remains stable during the magnetization inrush current. On the other hand, the conventional differential protection is dependent on the harmonic-based blocking unit. However, modern transformers run at a higher flux density and generate low harmonics content during inrush current, hence the relay security can be jeopardized. The purposed algorithm performs well in the event of simultaneous internal fault and magnetization inrush current. However, the conventional differential relay is not able to operate in such kinds of scenario due to the trip block by the blocking unit.

- During series-winding saturation, the proposed algorithm remains stable while the conventional differential protection measures a high differential current.

- Unlike the conventional differential protection characteristic, the non-standard varying phase-shift does not impact the sensitivity of the relay in the event of a
low fault current when the PST is operating at a high tap position, and the security in the event of any false current when the PST is operating at a low tap position. The proposed algorithm provides good sensitivity against low turn-turn faults. The test shows us that the relay performs well, even when the shorted turns are 1.5% of the winding, while the PST is operating at a low tap position. However, as mentioned in the previous section, in the event of a turn-turn fault, the conventional differential protection has a finite sensitivity and does not work for the low fault current.

• The proposed algorithm requires three currents and two voltages per phase. However, the current differential protection requires only currents to compute differential currents.

• Like the existing alternate current differential methods, the proposed algorithm also requires reading of the tap position from the PST. However, the conventional differential protection does not require any external readings, except current measurements.

**Directional comparison-based protection**

• In addition to the internal/external fault detection and discrimination, the proposed technique is completely immune and remains stable during magnetization inrush currents, winding saturation and external fault with CT saturation. Unlike the differential-based techniques, the algorithm doesn’t require any blocking or restraining element to ensure the security of the relay, and therefore performs well on occurrence of the simultaneous inrush current phenomena and internal fault.

• It solves the problem of turn-to-turn fault detection, which was previously undetectable by the conventional differential technique.
• Computation of the algorithm does not require tracking of the tap-changer position, which is normally used in differential-based techniques to solve the problem of non-standard varying phase-shift.

• The sensitivity and stability of the proposed algorithm are tested for various fault and non-fault conditions, which suggest that the proposed algorithm provides a complete solution for the protection of all kinds of commonly used PSTs.

The main contributions of this thesis are:

• Performance analysis of the traditional and alternate PST current differential-based protection techniques

• Development of short-circuit and EMTP models of single-core standard-delta and two-core PSTs

• Development of a new protection algorithm based on the electromagnetic differential protection equations for the standard-delta and delta-hexagonal PST

• Development of a universal protection algorithm based on the directional comparison principle

Further work can be done in the following areas:

• Design of the scaled-down prototype of phase shifting transformers based on the derived relations of winding parameters.

• Validation and testing of the two-core asymmetrical phase shifting transformer model presented in Appendix A.

• Performance of the proposed protection methods can be tested using the actual recorded current and voltage signals. A real prototype of phase shifting transformer can also be used to test the proposed protection methods as well.
• Hardware implementation and testing of the proposed protection techniques on a real phase shifting transformer.
References


[Available at: https://www.selinc.com/WorkArea/DownloadAsset.aspx?id=2612]


[Available at: https://www.selinc.com/WorkArea/DownloadAsset.aspx?id=2493]


Appendix A

Modeling of Two-core Asymmetrical PST

As done in section 3.4 for the two-core symmetrical PST, different parameters are derived to accurately model the positive-, negative-, and zero-sequence impedance networks of the two-core asymmetrical PST.

A.1. Calculation of the Positive-Sequence Winding Impedances

As shown in Figure A.1, the source (S) and load (L) sides are connected to the primary of the series unit. The secondary of the series unit is connected to the tapped-winding (secondary-side) of the exciting unit, making a delta connection to create the quadrature voltage, which, when added to the nominal voltage, will generate the phase shift between the source and the load sides. The primary of the exciting unit is connected to the source-side of the primary winding of series unit. Both sides of the exciting unit are Y–N connected.

The turn ratios of the series unit and exciting unit at a particular tap position D are as follows:

\[
\frac{\Delta V_A}{\Delta V_a} = \frac{n_{SA}}{n_{Sa}} = \frac{N_S}{n_{SA}} \tag{A.1}
\]

\[
\frac{V_{EA}}{V_{Ea}} = \frac{n_{EA}}{Dn_{Ea}} = \frac{N_E}{D} \tag{A.2}
\]

where \(\Delta V_A\) and \(\Delta V_a\) are the quadrature voltages; \(V_{EA}\) and \(V_{Ea}\) are the voltages across the primary and secondary of the exciting unit; \(n_{SA}\) and \(n_{Sa}\) are the number of turns in the primary and the secondary windings of the series unit, respectively; \(n_{EA}\) and \(n_{Ea}\) are the number of turns in the primary and the secondary windings of the exciting unit, respectively.
The load condition should be taken into account to derive the positive-, negative-, and zero-sequence impedances of the PST as a function of tap position. The derived equations are further used to calculate the leakage impedance of the single-phase windings of both series and exciting units.

Using notations of Figure A.2, equations (A.3) and (A.4) can be written in terms of leakage impedance at the primary of the series unit, as shown in Figure A.2.

\[ V_{SA} = \Delta V_A + (I_{SA} - I_{EA})Z_{SA} + V_{LA} \]  
(A.3)

where \( I_{SA} - I_{EA} = I_{LA} \)

Replacing \( \Delta V_A \) with \( \Delta V_aN_s \), we can obtain
Using the circuit of Figure A.2, we can write the expression for the quadrature voltage developed at the secondary of the series unit as

\[ V_{SA} = \Delta V_a \cdot N_s + (I_{SA} - I_{EA}) Z_{SA} + V_{LA} \]  

(A.4)

Using the circuit of Figure A.2, we can write the expression for the quadrature voltage developed at the secondary of the series unit as

\[ \Delta V_a = -j \sqrt{3} V_{EA} + I_a Z_{Sa} \]  

(A.5)

Transferring the secondary to the primary of the exciting unit, we can write the voltage and current relation as

\[ V_{EA} = V_{EA} \frac{N_e}{D} + I_{EA} Z_{EA} - I_{Ed} Z_{Ed} \frac{N_e}{D} \]  

(A.6)

The ampere-turn ratio of the series unit is

\[ \frac{I_a}{I_{LA}} = N_s \]  

(A.7)
The ampere-turn ratio of the exciting unit is

\[ \frac{I_{EA}}{I_{Ea}} = \frac{Dn_{Ea}}{n_{EA}} \]  

(A.8)

Considering Figure A.2, (A.9) gives us the current relation between the secondary of the series and the exciting units.

\[ I_{Ea} = I_c - I_b = j\sqrt{3}I_a \Rightarrow j\sqrt{3}N_s I_LA \]  

(A.9)

The distribution of currents in the primary of the series and exciting units is:

\[ I_{EA} = I_{SA} - I_{LA} \]  

(A.10)

Using (A.7) to (A.10), we can derive the following relations:

\[ I_{LA} = I_{SA} \left( \frac{N_e}{j\sqrt{3}DN_e + N_e} \right) \]  

(A.11a)

\[ I_a = I_{SA} \left( \frac{N_SN_e}{j\sqrt{3}DN_e + N_e} \right) \]  

(A.11b)

\[ I_{Ea} = I_{SA} \left( \frac{j\sqrt{3}N_SN_e}{j\sqrt{3}DN_e + N_e} \right) \]  

(A.11c)

\[ I_{EA} = I_{SA} \left( \frac{j\sqrt{3}DN_eN_e}{j\sqrt{3}DN_eN_e + N_e^2} \right) \]  

(A.11d)

Replacing \( \Delta V_a \) and \( I_a \) in (A.4) with (A.5) and (A.7), respectively, and rearranging, we can get

\[ V_{EA} = \frac{V_{LA}}{j\sqrt{3}N_s} - \frac{V_{SA}}{j\sqrt{3}N_s} + \frac{N_SI_{LA}Z_Sa}{j\sqrt{3}} + \frac{I_{LA}Z_{SA}}{j\sqrt{3}N_s} \]  

(A.12)

Replacing \( V_{EA} \) in (A.6) with (A.12) and using (A.8-A.10) we can get
where \( V_{EA} = V_{SA} \)

\[
V_{SA} = \begin{pmatrix}
\frac{V_{LA}}{j\sqrt{3} N_s} - \frac{V_{SA}}{j\sqrt{3} N_s}
+ \frac{I_{LA} Z_{SA}}{j\sqrt{3}} N_e
\frac{N_e}{D} + \frac{I_{LA} Z_{SA}}{j\sqrt{3}} N_e
\frac{N_e}{D} + \frac{N_e^2}{D^2} Z_{EA}
\end{pmatrix}
\]

Solving (A.13) for \( V_{LA} \) and by re-arranging we can get

\[
V_{LA} = V_{SA} e^{j\delta} - I_{SA} e^{j\delta} \left( Z_{SA} N_s^2 + Z_{SA} \right)
+ Z_{EA} \frac{j2\sqrt{3} D N_s}{N_e} + \frac{j2\sqrt{3} N_s N_e}{D} Z_{EA}
\]

\[
V_{LA} = V_{SA} e^{j\delta} - I_{SA} Z_1 e^{j\delta}
\]

where \( Z_1(D) \) is the positive-sequence impedance as a function of tap position of the PST represented by (A.15) and \( \delta \) denotes the phase shift between load- and source- sides.

\[
Z_1(D) = \begin{pmatrix}
Z_{SA} N_s^2 + Z_{SA}
+ Z_{EA} \frac{j2\sqrt{3} D N_s}{N_e} + \frac{j2\sqrt{3} N_s N_e}{D} Z_{EA}
\end{pmatrix}
\]

\[
\delta = \frac{N_e}{j\sqrt{3} D N_s + N_e}
\]

The positive-sequence impedance of the series unit remains constant for any tap position. Hence, to find the winding leakage-impedance of the series-unit, we put \( D=0 \) in (A.16) such that \( Z_1(D=0) = N_s^2 Z_{SA} + Z_{SA} \). At \( D=0 \), \( Z_1(D=0) \) is the equivalent impedance of the single-
phase series-unit transformer shown in Figure A.2. We can find the series-unit winding leakage-impedances as below.

\[
Z_{Sa} = 0.5 \frac{Z_{1(D=0)}}{N_S^2} \tag{A.17a}
\]

\[
Z_{SA} = 0.5Z_{1(D=0)} \tag{A.17b}
\]

The positive-sequence impedance of the exciting unit is the function of the tap position D. The derived equation (A.15) with tap position D=1 can be used to find the positive-sequence impedance of the exciting unit at maximum tap, D=1 which is further used to find the winding leakage-impedances (\(Z_{EA}\) and \(Z_{Ea}\)). Using (A.15) with D=1

\[
Z_1(D) = Z_{1(D=0)} + Z_{EA} \frac{j2\sqrt{3}N_S}{N_e} + j2\sqrt{3}N_SN_eZ_{Ea}
\]

From the above equation, we can find the exciting-unit windings leakage-impedances as a function of tap position as below.

\[
Z_{EA} = \frac{0.5}{12N_S^2} \left[ Z_{1(D=1)} \left( 3N_S^2 + 4N_e^2 \right) - Z_{1(D=0)} \left( 4N_e^2 + 1.5N_S^2 \right) \right]
\]

\[
\left( Z_{1(D=1)} - Z_{1(D=0)} \right) = Z_{EA} \frac{j2\sqrt{3}N_S}{N_e} + j2\sqrt{3}N_SN_eZ_{Ea}
\]

\[
Z_{EA} = \frac{0.5N_e}{j2\sqrt{3}N_S} \left( Z_{1(D=1)} - Z_{1(D=0)} \right) \tag{A.18A}
\]

\[
Z_{Ea} = \frac{0.5}{j2\sqrt{3}N_SN_e} \left( Z_{1(D=1)} - Z_{1(D=0)} \right) \tag{A.18B}
\]

Parameter calculations using (A.17) and (A.18), when used back in (A.15), gives us the positive-sequence impedance of the whole PST as a function of tap position. Hence, to accurately model the PST, the manufacturer’s test report data are not required, except for
the impedance at the maximum tap position and minimum tap positions that are given in
the nameplate information.

A.2. Calculation of Negative Sequence Winding Impedances

The negative-sequence impedance is equal to the positive-sequence impedance, and the
equivalent circuits are similar except that the phase shift will be of the same magnitude
but in opposite directions. Thus, if the phase shift is $+\delta$ degrees for positive-sequence, the
phase shift for negative-sequence quantities will be $-\delta$ degrees.

A.3. Calculation of Zero-Sequence Winding Impedances

Taking all the phasor quantities (currents and voltages) equal in magnitude and in-phase
and rewriting (A.3), (A.5) and (A.9) we will get

$$V_{SA0} = \Delta V_{A0} + (I_{SA0} - I_{EA0})Z_{SA0} + V_{LA0} \quad (A.19)$$

$$\Delta V_{a0} = I_{a0} Z_{Sa0} \quad (A.20)$$

$$I_{Ea0} = I_{c0} - I_{b0} = 0 \Rightarrow I_{Ea0} = 0 \quad (A.21)$$

The distribution of currents in the primary of the series and exciting units will be:

$$0 = I_{SA0} - I_{LA0} \Rightarrow I_{SA0} = I_{LA0} \quad (A.22)$$

The ampere-turn ratio of the series unit is

$$\frac{I_{a0}}{I_{LA0}} = \frac{I_{a0}}{I_{SA0}} = N_S \quad (A.23)$$

And

$$\Delta V_{A0} = I_{a0} Z_{Sa0} N_S \quad (A24)$$

Using (A.23) and (A.24) in (A.19) and solving for $V_{LA0}$ we can write
Equation (A.25) represents the zero-sequence impedance of the whole PST. The zero-sequence impedance of the exciting unit \((Z_{E0}, Z_{Ea0})\) is zero even when both sides of exciting units are grounded; this is because the secondary of the exciting unit is connected to the secondary of the series unit in delta. Hence, the zero-sequence impedance of the PST will remain constant for all tap positions.

The derived equation (A.25) is further used to find the winding leakage-impedances \((Z_{Sa0} \text{ and } Z_{Sa0})\).

\[
V_{L40} = V_{SA40} - I_{SA40} \left( Z_{Sa0} N_s^2 - Z_{SA0} \right)
\]

\[
V_{L40} = V_{SA40} - I_{SA40} Z_{eq0}
\]

\[
Z_0 = Z_{Sa0} N_s^2 + Z_{SA0} \tag{A.25}
\]

The derived parameters (A.26) and (A.27), when used back in (A.25), will give us the zero-sequence impedance of the whole PST as a function of the tap position.
Signal Processing

The proposed phase shifting transformer protection methods (Chapter 4 and 5) requires currents and voltages signals of fundamental frequency (50 or 60 Hz). In conventional transformer differential protection, harmonic indicators are used to detect the inrush currents. Generally, second and fifth harmonics in differential current are used to check the inrush current due to energization of transformer, CT saturation or core saturation.

Various system normal conditions (like such as switching operation of transformer) and fault conditions results in the generation of the decaying dc and higher frequencies. Therefore, for proper implementation of the proposed algorithms, extraction of fundamental frequency components is very important. The following detail illustrates the required signal processing and extraction of the voltage and current components that are used in implementing the proposed algorithms.

B.1. Anti-Aliasing Filter

According to the sampling theorem [46], a continuous-time signal can be fully recovered from its uniformly sampled version if the input signal is sampled at a sampling frequency \( f_s \) that is at least twice the highest required frequency. If this condition is not satisfied, the original continuous-time signal cannot be recovered from its sampled version because of distortion caused by aliasing.

To implement both the proposed algorithms and conventional differential approaches (with harmonic indicators) cutoff frequencies of 360Hz for electromagnetic differential protection(EDP) and 960Hz for directional comparison-based protection(DCB) are used. To avoid aliasing, sampling frequency is normally chosen twice the cut-off frequency. Sampling frequency of 1440 Hz and 2880 Hz are chosen for the implementation of electromagnetic differential protection based approach and directional comparison based approach, respectively.
In PSCAD and RTDS, current and voltage signals from current and voltage transformers, respectively are normally available with the minimum time-step of 50µsec, which corresponds to oversampling of input signals with 20kHz of sampling frequency. Therefore, decimation process is implemented to decimate the over-sampled signal into low sampling rate. Decimation process is implemented by first passing the over-sampled signal through the digital anti-aliasing filter and then down-sampling its output. For the design of anti-aliasing filter a 4th order Butterworth filter with cut-off frequencies of 360Hz and 960Hz are used in EDP and DCB, respectively.

**B.2. Phasor Estimation Using Discrete Fourier Transformer (DFT)**

For the purpose of phasor estimation (magnitude and phase) of the discrete signal, algorithm based on Discrete Fourier transformer is used. The DFT algorithm employs the sine and cosine functions, which are well known orthogonal functions, to estimate the phasor of sinusoidal waveforms. The general expression for the DFT is as follows:

$$V_h = \frac{2}{N} \sum_{n=0}^{N-1} v_n e^{-jn \frac{2\pi h}{N}}$$  \hspace{1cm} (B.1)

where

- \(v\) is the instantaneous value of the voltage
- \(n\) is the \(n\)th sample in the data window
- \(V\) is the phasor of the voltage
- \(h\) is the order of the harmonic
- \(N\) is the number of sample in a data window

The exponential term in (B1) can be converted to the sinusoidal equivalent such that (B1) becomes
\[ V_h = \frac{2}{N} \sum_{n=0}^{N-1} v_n \left( \cos \left( n \frac{2\pi h}{N} \right) - j \sin \left( n \frac{2\pi h}{N} \right) \right) \]  

(B.2)

Real and imaginary components of the phasor are given by

\[ R(V_h) = \frac{2}{N} \sum_{n=0}^{N-1} v_n \cos \left( n \frac{2\pi h}{N} \right) \]

\[ I(V_h) = \frac{2}{N} \sum_{n=0}^{N-1} v_n \sin \left( n \frac{2\pi h}{N} \right) \]

Table B-1 and Table B-2 shows the cosine and sine coefficients for a sampling frequency of 1440 Hz and 2880 Hz. Figure B.1 and Figure B.2 show the frequency response of the cosine and sine filters for a sampling frequency of 1440 Hz and 2880 Hz.

**Table B-1: Cosine and sine filter coefficients for a 24 point DFT**

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<tbody>
<tr>
<td>1.0</td>
<td>0.0</td>
</tr>
<tr>
<td>0.966</td>
<td>0.259</td>
</tr>
<tr>
<td>0.866</td>
<td>0.500</td>
</tr>
<tr>
<td>0.707</td>
<td>0.707</td>
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<tr>
<td>0.500</td>
<td>0.866</td>
</tr>
<tr>
<td>0.259</td>
<td>0.966</td>
</tr>
<tr>
<td>0.0</td>
<td>1.0</td>
</tr>
<tr>
<td>-0.259</td>
<td>0.966</td>
</tr>
<tr>
<td>-0.500</td>
<td>0.866</td>
</tr>
<tr>
<td>-0.707</td>
<td>0.707</td>
</tr>
<tr>
<td>-0.866</td>
<td>0.500</td>
</tr>
<tr>
<td>-0.966</td>
<td>0.259</td>
</tr>
<tr>
<td>-1.000</td>
<td>0.000</td>
</tr>
<tr>
<td>-0.966</td>
<td>-0.259</td>
</tr>
<tr>
<td>-0.866</td>
<td>-0.500</td>
</tr>
<tr>
<td>-0.707</td>
<td>-0.707</td>
</tr>
<tr>
<td>-0.500</td>
<td>-0.866</td>
</tr>
<tr>
<td>-0.259</td>
<td>-0.966</td>
</tr>
<tr>
<td>0.0</td>
<td>-1.0</td>
</tr>
<tr>
<td>0.259</td>
<td>-0.966</td>
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<tbody>
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<td>0.500</td>
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<tr>
<td>0.707</td>
<td>-0.707</td>
</tr>
<tr>
<td>0.866</td>
<td>-0.500</td>
</tr>
<tr>
<td>0.966</td>
<td>-0.259</td>
</tr>
</tbody>
</table>

Figure B.1: Frequency response of cosine and sine filters for sampling frequency of 1440 Hz.

Table B-2: Cosine and sine filter coefficients for a 48 point DFT

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</thead>
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<td>1.000</td>
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<td>0</td>
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<tr>
<td>0.991</td>
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</tr>
<tr>
<td>0.966</td>
<td>-0.966</td>
<td>0.2588</td>
<td>-0.2588</td>
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<tr>
<td>0.924</td>
<td>-0.924</td>
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<td>0.866</td>
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<td>-0.5</td>
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<td>0.793</td>
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<td>0.6088</td>
<td>-0.6088</td>
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<tr>
<td>0.707</td>
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<td>-0.866</td>
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Table Continued...

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<tr>
<td>0.000</td>
<td>0.000</td>
<td>1</td>
<td>-1</td>
</tr>
<tr>
<td>-0.131</td>
<td>0.131</td>
<td>0.9914</td>
<td>-0.9914</td>
</tr>
<tr>
<td>-0.259</td>
<td>0.259</td>
<td>0.9659</td>
<td>-0.9659</td>
</tr>
</tbody>
</table>

Figure B.2: Frequency response of cosine and sine filters for sampling frequency of 2880 Hz.
Appendix C

Power System Simulation Models

This appendix presents the test system models used to simulate various normal and faulted system conditions to test the proposed protection techniques discussed in Chapter 4 and Chapter 5. All the simulations were performed in PSCAD/EMTDC. In addition to the test systems configurations, parameters data of various system elements like such as sources, transmission lines, phase shifting transformers and instrument transformers are also presented in this section.

C.1. Test Models

Three test system models used to simulate the delta-hexagonal (Model 1), standard-delta (Model 2) and two-core symmetrical (Model 3) were simulated in PSCAD. To obtain the real representation of currents and voltages, modeling of all three kinds of the PSTs is done based on real PSTs nameplate information obtained from the manufacturer. Therefore, each system model rating (kV and MVA) is based on the actual transformer ratings. As shown in Figure C.1, all the three models consist of two end sources linked together through the parallel transmission lines between busbar (BUS 1 and BUS 2). Phase shifting transformer is installed on line 1 at bus 1 between the source- and load-side circuit breakers.

Figure C.1: Single line diagram of the parallel transmission network together with the phase shifting transformer.
C.2. Sources

### Table C-1: Equivalent sources’ data for Model 1

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model 1</th>
<th>Source 1</th>
<th>Source 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Voltage (Line-line, RMS)</td>
<td></td>
<td>138 kV</td>
<td>138 kV</td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
<td>60 Hz</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Phase Shift(initial)</td>
<td></td>
<td>0 deg</td>
<td>0 deg</td>
</tr>
<tr>
<td>Positive sequence impedance(SIR=1)</td>
<td></td>
<td>6.09 Ω∠85.5°</td>
<td>1.21 Ω∠85.5°</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td></td>
<td>15.91 Ω∠72.5°</td>
<td>3.18 Ω∠72.5°</td>
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</tbody>
</table>

### Table C-2: Equivalent sources’ data for Model 2

<table>
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<tr>
<th>Parameters</th>
<th>Model 2</th>
<th>Source 1</th>
<th>Source 2</th>
</tr>
</thead>
<tbody>
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<td>Rated Voltage (Line-line, RMS)</td>
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<td>69 kV</td>
<td>69 kV</td>
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<tr>
<td>Frequency</td>
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<td>60 Hz</td>
<td>60 Hz</td>
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<tr>
<td>Phase Shift(initial)</td>
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<td>0 deg</td>
</tr>
<tr>
<td>Positive sequence impedance(SIR=1)</td>
<td></td>
<td>9.52 Ω∠85.5°</td>
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<tr>
<td>Zero-sequence impedance</td>
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<td>24.65 Ω∠74.370</td>
<td>4.93 Ω∠700</td>
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### Table C-3: Equivalent sources’ data for Model 3

<table>
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<tr>
<th>Parameters</th>
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<tr>
<td>Rated Voltage (Line-line, RMS)</td>
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<td>230 kV</td>
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<td>60 Hz</td>
</tr>
<tr>
<td>Phase Shift(initial)</td>
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<td>0 deg</td>
</tr>
<tr>
<td>Positive sequence impedance(SIR=1)</td>
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<td>2.28 Ω∠85.5°</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td></td>
<td>29.62 Ω∠70 deg</td>
<td>5.92 Ω∠70 deg</td>
</tr>
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</table>
### C.3. Phase Shifting Transformers

#### Table C-4: Delta Hexagonal PST

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<th>Parameters</th>
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</thead>
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</tr>
<tr>
<td>3-phase MVA</td>
<td>150</td>
</tr>
<tr>
<td>Positive sequence impedance</td>
<td>6.096 Ω/88.4 deg</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td>21.378 Ω/87.3 deg</td>
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<tr>
<td>Maximum phase shift</td>
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<tr>
<td>No. of steps</td>
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</tbody>
</table>

#### Table C-5: Standard-Delta PST

<table>
<thead>
<tr>
<th>Parameters</th>
<th>PST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Voltage (Line-line, RMS)</td>
<td>69 kV</td>
</tr>
<tr>
<td>3-phase MVA</td>
<td>30</td>
</tr>
<tr>
<td>Positive sequence impedance</td>
<td>9.52 Ω</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td>8.8872 Ω</td>
</tr>
<tr>
<td>Maximum phase shift</td>
<td>30 deg</td>
</tr>
<tr>
<td>No. of steps</td>
<td>32</td>
</tr>
</tbody>
</table>

#### Table C-6: Two-core symmetrical PST

<table>
<thead>
<tr>
<th>Parameters</th>
<th>PST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Voltage (Line-line, RMS)</td>
<td>230 kV</td>
</tr>
<tr>
<td>3-phase MVA</td>
<td>480</td>
</tr>
<tr>
<td>Maximum phase shift</td>
<td>±35.1 deg</td>
</tr>
<tr>
<td>No. of steps</td>
<td>32</td>
</tr>
<tr>
<td>Positive sequence impedance @D=1</td>
<td>11.44 Ω</td>
</tr>
<tr>
<td>Positive sequence impedance @D=0</td>
<td>7.48 Ω</td>
</tr>
<tr>
<td>Zero-sequence impedance @D=1</td>
<td>7.96 Ω</td>
</tr>
<tr>
<td>Series Unit</td>
<td></td>
</tr>
<tr>
<td>no. of turns primary winding</td>
<td>220</td>
</tr>
<tr>
<td>no. of turns secondary winding</td>
<td>272</td>
</tr>
<tr>
<td>Exciting Unit</td>
<td></td>
</tr>
<tr>
<td>no. of turns primary winding</td>
<td>354</td>
</tr>
<tr>
<td>no. of turns secondary winding</td>
<td>160</td>
</tr>
</tbody>
</table>
C.4. Transmission Lines

Table C-7: Transmission Line Data for Model 1

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Line 1</th>
<th>Line 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>50 km</td>
<td>75 km</td>
</tr>
<tr>
<td>Positive sequence impedance</td>
<td>25.45 Ω∠85.9 deg</td>
<td>38.175 Ω∠85.9 deg</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td>68.76 Ω∠74.6 deg</td>
<td>103.14 Ω∠74.6 deg</td>
</tr>
</tbody>
</table>

Table C-8: Transmission Line Data for Model 2

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Line 1</th>
<th>Line 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>30 km</td>
<td>50 km</td>
</tr>
<tr>
<td>Positive sequence impedance</td>
<td>15.27 Ω∠85.9 deg</td>
<td>25.45 Ω∠85.9 deg</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td>41.256 Ω∠74.6 deg</td>
<td>68.76 Ω∠74.6 deg</td>
</tr>
</tbody>
</table>

Table C-9: Transmission Line Data for Model 3

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Line 1</th>
<th>Line 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>75 km</td>
<td>100 km</td>
</tr>
<tr>
<td>Positive sequence impedance</td>
<td>38.175 Ω∠85.9 deg</td>
<td>50.9 Ω∠85.9 deg</td>
</tr>
<tr>
<td>Zero-sequence impedance</td>
<td>103.14 Ω∠74.6 deg</td>
<td>137.5 Ω∠74.6 deg</td>
</tr>
</tbody>
</table>

C.5. Current Transformer

Table C-10: Current Transformers Data

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model 1</th>
<th></th>
<th>Model 2</th>
<th></th>
<th>Model 3</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CT ratio</td>
<td>CT S</td>
<td>CT L</td>
<td>CT S</td>
<td>CT L</td>
<td>CT S</td>
<td>CT L</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>50</td>
<td>50</td>
<td>320</td>
</tr>
<tr>
<td>Burden(Ω)</td>
<td>0.5-20</td>
<td>0.5</td>
<td>0.5-20</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5-20</td>
</tr>
</tbody>
</table>
C.6. Capacitive Voltage Transformer [47]

![Diagram of Capacitive Voltage Transformer]

Figure C.2: Schematic of a capacitive voltage transformer.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Model 1</th>
<th>Model 2</th>
<th>Model 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitor C1(pF)</td>
<td>5073</td>
<td>10543</td>
<td>2998</td>
</tr>
<tr>
<td>Capacitor C2(pF)</td>
<td>134952</td>
<td>134952</td>
<td>134952</td>
</tr>
<tr>
<td>VT ratio</td>
<td>41.6</td>
<td>41.6</td>
<td>41.6</td>
</tr>
<tr>
<td>Compensating inductance, Lcomp(H)</td>
<td>42</td>
<td>42</td>
<td>42</td>
</tr>
<tr>
<td>Primary inductance, Lp(mH)</td>
<td>0.47</td>
<td>0.47</td>
<td>0.47</td>
</tr>
<tr>
<td>Primary Resistance, Rp(ohm)</td>
<td>0.05</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>Secondary inductance, Ls(mH)</td>
<td>0.47</td>
<td>0.47</td>
<td>0.47</td>
</tr>
<tr>
<td>Secondary Resistance, Rs(ohm)</td>
<td>0.18</td>
<td>0.18</td>
<td>0.18</td>
</tr>
</tbody>
</table>

Table C-11: Capacitive voltage transformer Data
Appendix D

Additional Simulation Results of Electromagnetic Differential Protection

Additional test results in this appendix illustrate the performance of the electromagnetic differential protection techniques that have been presented in Chapter 4. A large number of tests are performed for various types of internal and external faults and fault locations. Tests are formed for different system conditions like such as SIRs\{0.2, 1, 5\}, PST tap positions \{high (0.7 < D < 1), mid (D = 0.5) and low (0 < D < 0.3)\}.

D.1. Single Phase-to-Ground Faults

This section contains Figure D.1 to Figure D.16 for various single phase to ground faults. Summary of same test cases are presented in Chapter 4.

![Figure D.1: Plots of |DIFF| signals computed by RELAY\_S and RELAY\_L, and fault inception/trip signals (Case 4-3).](image1)

![Figure D.2: Plots of |DIFF| signals computed by RELAY\_S and RELAY\_L, and fault inception/trip signals (Case 4-4).](image2)
Figure D.3: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-5)

Figure D.4: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-6)

Figure D.5: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-7)

Figure D.6: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-8)
Figure D.7: Plots of |DIFF| signals computed by RELAY₅ and RELAY₆, and fault inception/trip signals (Case 4-9).

Figure D.8: Plots of |DIFF| signals computed by RELAY₅ and RELAY₆, and fault inception/trip signals (Case 4-10).

Figure D.9: Plots of |DIFF| signals computed by RELAY₅ and RELAY₆, and fault inception/trip signals (Case 4-11).

Figure D.10: Plots of |DIFF| signals computed by RELAY₅ and RELAY₆, and fault inception/trip signals (Case 4-12).
Figure D.11: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-13).

Figure D.13: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-15).

Figure D.12: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-14).

Figure D.14: Plots of |DIFF| signals computed by RELAY_S and RELAY_L, and fault inception/trip signals (Case 4-16).
D.2. Phase-to-Phase and Double Phase-to-Ground Faults

Figure D.15: Plots of |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-17).

Figure D.16: Plots of |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-18).

Figure D.17: Plots of |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-21).

Figure D.18: Plots of |DIFF| signals computed by RELAYS and RELAYL, and fault inception/trip signals (Case 4-22).
Figure D.19: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-23).

Figure D.20: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-24).

Figure D.21: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-25).

Figure D.22: Plots of |DIFF| signals computed by RELAY$_S$ and RELAY$_L$, and fault inception/trip signals (Case 4-26).
Figure D.23: Plots of $|\text{DIFF}|$ signals computed by $\text{RELAY}_S$ and $\text{RELAY}_L$, and fault inception/trip signals (Case 4-27).

D.3. Three-Phase Faults

Table D-1: Relay operating times for three-phase and three phase-to-ground faults

<table>
<thead>
<tr>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Fault type</th>
<th>$R_f$(ohms)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>high</td>
<td>ABC</td>
<td>0.1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>0.1</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>ABC</td>
<td>0.1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>0.1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>high</td>
<td>ABC</td>
<td>0.1</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>0.1</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>ABC</td>
<td>0.1</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>0.1</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABCg</td>
<td>20</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>
D.4. External Faults

Table D-2: Relay performance in the event of external faults

<table>
<thead>
<tr>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault Location</th>
<th>Fault type</th>
<th>Relay operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>high</td>
<td>F1</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>ABCg</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>ABCg</td>
<td>NO</td>
</tr>
<tr>
<td>5</td>
<td>high</td>
<td>F1</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>ABCg</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>ABCg</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>F1</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F1</td>
<td>ABCg</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>Ag</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>BC</td>
<td>NO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>F2</td>
<td>ABCg</td>
<td>NO</td>
</tr>
</tbody>
</table>
Appendix E

Additional Simulation Results of Directional Comparison Based Protection Technique

Additional test results in this appendix illustrate the performance of the phase shifting transformer protection technique based on directional comparison principle presented in Chapter 5. A large number of tests are performed for various types of internal and external faults and fault locations. Tests are formed for different system conditions like such as SIRs\{0.2, 1, 5\}, PST tap positions \{high \((0.7<D<1)\), mid \((D=0.5)\) and low \((0<D<0.3)\}\).

E.1. Internal Fault in an Unloaded PST

![Figure E.1: Plots of arguments and digital signals (Case 5-5).](image1)

![Figure E.2: Plots of arguments and digital signals (Case 5-6).](image2)
Figure E.3: Plots of arguments and trip signals (Case 5-7).

Figure E.4: Plots of arguments and trip signals (Case 5-8).

Figure E.5: Plots of arguments and trip signals (Case 5-9).

Figure E.6: Plots of arguments and trip signals (Case 5-10).
Figure E.7: Plots of arguments and trip signals (Case 5-11).

Figure E.8: Plots of arguments and trip signals (Case 5-12).

Figure E.9: Plots of arguments and trip signals (Case 5-13).

Figure E.10: Plots of arguments and trip signals (Case 5-14).
Figure E.11: Plots of arguments and trip signals (Case 5-15).
### E.2. Phase-to-Phase and Three-Phase Faults in a Loaded Transformer

Table E-1: Relay operating times in the event of internal ph-ph and 3-ph faults

<table>
<thead>
<tr>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault type</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>high</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>mid</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>8</td>
</tr>
</tbody>
</table>

Table E-2: Relay operating times in the event of internal ph-ph and 3 phase faults, S

<table>
<thead>
<tr>
<th>SIR</th>
<th>Tap Position</th>
<th>Fault type</th>
<th>Fault Location</th>
<th>Rf(Ω)</th>
<th>Trip time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>high</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>mid</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>BC</td>
<td>F4</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BCG</td>
<td>F5</td>
<td>20</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ABC</td>
<td>F6</td>
<td>1</td>
<td>8</td>
</tr>
</tbody>
</table>
E.3. Turn-to-Turn Faults

Figure E.12: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-63)

Figure E.13: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-64)

Figure E.14: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-65)

Figure E.15: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-66)
Figure E.16: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-67)

Figure E.17: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-68)

Figure E.18: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-69)

Figure E.19: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-70)
Figure E.20: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-71)

Figure E.21: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-72)

Figure E.22: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-73)

Figure E.23: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-74)
Figure E.24: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-75)

Figure E.25: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-76)

Figure E.26: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-77)

Figure E.27: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-78)
Figure E.28: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-79)

Figure E.29: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-80)

Figure E.30: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-81)

Figure E.31: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-82)
Figure E.32: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-83)

Figure E.33: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-84)

Figure E.34: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-85)

Figure E.35: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-86)
Figure E.36: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-87)

Figure E.37: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit primary winding (Case 5-88)

Figure E.38: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-89)

Figure E.39: Plots of arguments and trip signals in the event of turn-to-turn fault at series unit secondary winding (Case 5-90)
Figure E.40: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-91)

Figure E.42: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-93)

Figure E.41: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit primary winding (Case 5-92)

Figure E.43: Plots of arguments and trip signals in the event of turn-to-turn fault at exciting unit secondary winding (Case 5-94)
E.4. External Faults

Figure E.44: Plots of phase A current, arguments and trip signals in the event of external A-g fault with CT saturation at location F1 (Case 5-103)

Figure E.45: Plots of phase B current, arguments and trip signals in the event of external BC fault with CT saturation at location F1 (Case 5-104)
Figure E.46: Plots of phase C current, arguments and trip signals in the event of external BC-g fault with CT saturation at location F1 (Case 5-105)

Figure E.47: Plots of phase A current, arguments and trip signals in the event of external ABC fault with CT saturation at location F1 (Case 5-106)
Figure E.48: Plots of phase A current, arguments and trip signals in the event of external A-g with CT saturation at location F1 (Case 5-107).

Figure E.49: Plots of phase B current, arguments and trip signals in the event of external BC with CT saturation at location F1 (Case 5-108).
Figure E.50: Plots of phase C current, arguments and trip signals in the event of external BC-g with CT saturation at location F1 (Case 5-109).

Figure E.51: Plots of phase C current, arguments and trip signals in the event of external ABC with CT saturation at location F1 (Case 5-110)
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