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A New ZVS-PWM Full-Bridge Boost Converter

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A thesis submitted in partial fulfillment of the requirements for the degree in Master of Engineering Science

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by

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ABSTRACT

Pulse-width modulated (PWM) full-bridge boost converters are used in applications where the output voltage is considerably higher than the input voltage. Zero-voltage-switching (ZVS) is typically implemented in these converters. The objective of this thesis is to propose, analyze, design, implement, and experimentally confirm the operation of a new Zero-Voltage-Switching PWM DC-DC full-bridge boost converter that does not have any of the drawbacks that other converters of this type have, such as a complicated auxiliary circuit, increased current stresses in the main power switches and load dependent ZVS operation. In this thesis, the general operating principles of the converter are reviewed, and the converter's operation is discussed in detail and analyzed mathematically. As a result of the mathematical analysis, key voltage and current equations that describe the operation of the auxiliary circuit and other converter devices have been derived. The steady state equations of each mode of operation are used as the basis of a MATLAB program that is used to generate steady-state characteristic curves that shows the effect that individual circuit parameters have on the operation of the auxiliary circuit and the boost converter.

Observations as to their steady-state characteristics are made and the curves are used as part of a design procedure to select the components of the converter, especially those of the auxiliary circuit. An experimental full-bridge DC-DC boost converter prototype is built based on the converter design and typically waveforms are presented to confirm the feasibility of the converter, as well as computer simulation results. The efficiency of the proposed converter operating with the auxiliary circuit is compared to that of a hard-switched PWM DC-DC full-bridge boost converter and the increased efficiency of the proposed converter is confirmed.

Keywords: Power conversion, DC-DC converter, Full-bridge converter, Boost Converter, Zero-voltage-switching, Soft-switching.

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Nomenclature

AC	Alternative Current
DC	Direct Current
EMI	Electromagnetic Interference
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1. General Introduction

1.1.1. Power Electronics

Power electronics is the field of electrical engineering related to the use of semiconductor devices to convert power from the form available from a source to that required by a load. The load may be AC or DC, single-phase or three-phase, and may or may not need isolation from the power source. The power source can be a DC source or an AC source (single-phase or three-phase with line frequency of 50 or 60 Hz), an electric battery, a solar panel, an electric generator or a commercial power supply. A power converter takes the power provided by the source and converts it to the form required by the load. The power converter can be an AC-DC converter, a DC-DC converter, a DC-AC inverter or an AC-AC converter depending on the application.

1.1.2. Switches

An important part of any power electronic converter is its semiconductor devices. The semiconductor devices that are typically used in switch-mode power converter are diodes, MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors). Diodes can be considered to be uncontrolled switches as they are on and conduct current when they are forward-biased and are off when they are reverse-biased. Current cannot be interrupted in a diode and some external action must be taken to the diode in order to divert current away from it and make it reverse biased. MOSFETs and IGBTs are controllable switches as they can be turned on and off by feeding a signal to their gate then removing it. The basic characteristics of each device are discussed in further detail below.

1.1.2.1. Power MOSFETs

A power MOSFET is a specific type of metal oxide semiconductor field-effect transistor (MOSFET) designed to handle significant power levels and is typically depicted as shown in Fig. 1.1. It has three terminals - a gate, a drain, and a source. The switch is on when current is fed to the gate and its gate-source capacitance is charged to a threshold voltage V_{th}, which creates a field that opens the drain-source channel and allows current to flow from drain to source. It has an isolated gate and current does not have to be continuously fed to the gate to keep the device on; the device is on as long as the voltage across the gate-source capacitance V_{gs} is greater than V_{th} and the field that keeps the drain-source channel open exists. A MOSFET has an intrinsic parallel body diode and can conduct reverse current even when the switch is off.

The MOSFET has three main regions of operation: triode, saturation, and cut-off. Since controllable semiconductor devices in almost all power electronics applications function as switches that are either fully on or fully off, a MOSFET in a power converter operates either in the triode region (fully on) or in the cut-off region (fully off). When the power MOSFET is in the on-state, however, it is not an ideal switch; it acts as if there is a resistor, $R_{ds(on)}$ (drain to source on-state resistance), between its drain and source terminals. This $R_{ds(on)}$ resistance contributes to energy loss when current flows through the device; the technical term for this energy loss is conduction loss.

Compared to other power semiconductor devices such as the IGBT, the MOSFET's main advantage is its high switching speed. MOSFETs can be turned on and off very quickly and are the fastest semiconductor devices in terms of switching because they are majority carrier devices and their operation is based on the generation and removal of an electric field,. They are the devices of choice in low power applications as their fast switching characteristics allows them to be implemented in converters that operate with high switching frequencies (>100kHz) to reduce the size of their magnetic elements (inductors, transformers). They are not suitable for higher power applications due to their $R_{ds(on)}$ and the conduction losses created by this parameter.

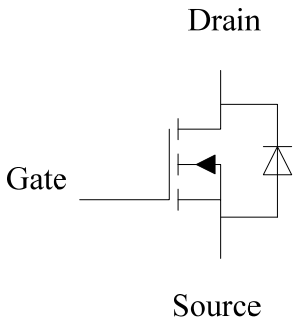


Fig. 1.1. A N-Channel power MOSFET symbol

1.1.2.2. IGBTs

The insulated gate bipolar transistor (IGBT) combines the isolated gate of a MOSFET gate with the low conduction loss of bipolar junction transistor (BJT). It has three terminals - a gate, a collector and an emitter as shown in Fig. 1.2. The term "gate" comes from the MOSFET part of the device while the terms "collector" and "emitter" come from the BJT part of the device. An IGBT may or may not be fabricated with a paralleled body diode.

The BJT has a fixed voltage drop across its collector-emitter terminals when the device is on. This is unlike the MOSFET, which has a variable voltage drop that it is equal to the product of the current flowing through the device and its $R_{ds(on)}$. This means that the BJT is, therefore, better suited for high power applications than the MOSFET because its lower voltage drop results in lower conduction losses. The BJT, however, turns on and off much slower than the MOSFET because it is a minority-carrier device that depends on the presence of a continuous base current. It cannot reach the switching speed of a MOSFET as it is more difficult to inject and remove electrons than it is to generate and remove an electric field.

It was to improve the switching frequency of the BJT that the IGBT was created by replacing the base of the BJT with the insulated gate of the MOSFET. Although the IGBT turns on and off more quickly than a BJT, its switching speed cannot match that of

the MOSFET, especially while the device is turning off as a tail in its collector current appears. Despite being a slower device, the IGBT still has the voltage drop characteristics of the BJT and is thus preferred over the MOSFET in high power applications as it has fewer conduction losses.

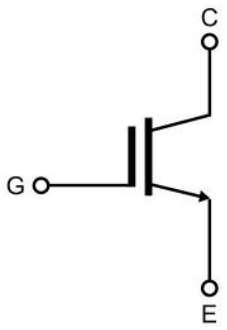


Fig. 1.2. IGBT symbol

1.1.3. High Switching Frequency Operation

A power electronic converter has energy storage elements such as inductors, capacitors and transformers that account for much of its overall size. These components are used to store and transfer energy as part of the power conversion process. As a converter's switching frequency is increased, the component values of its energy storage elements decrease, as do their physical size and weight, due to the shorter time they are required to store voltage or current. As a result, the higher the switching frequency a converter operates with, the smaller its energy storage elements (and thus its overall size) will be.

There are, however, drawbacks to operating a switch-mode power electronic converter with high switching frequency, the key one being that doing so increases the converter's switching losses. Unlike an ideal switch that would be able to turn on and off instantaneously without any overlap between the voltage across it and the current flowing through it, a real switch does have these overlaps in voltage and current whenever a switching transition from on to off or vice versa is made, as shown Fig.1.3. Fig. 1.3(a) defines the switch voltage and current as V_s and I_s respectively while Fig. 1.3(b) shows typical non-ideal switch voltage and current waveforms.

Since power is dependent on the product of voltage and current, the fact that there is voltage/current overlap during switching transitions means that there are power losses during these times. These losses are referred to as switching losses in the power electronics literature, and the higher the switching frequency that a power converter operates with, the more switching losses it will have. The main switching loss in a MOSFET occurs when it is turned on and the energy stored in its output capacitance (located between the drain and source terminals) is discharged in the switch. For an IGBT, it is the tail in the switch current that arises when the switch is turned off that is the main source of switching losses.

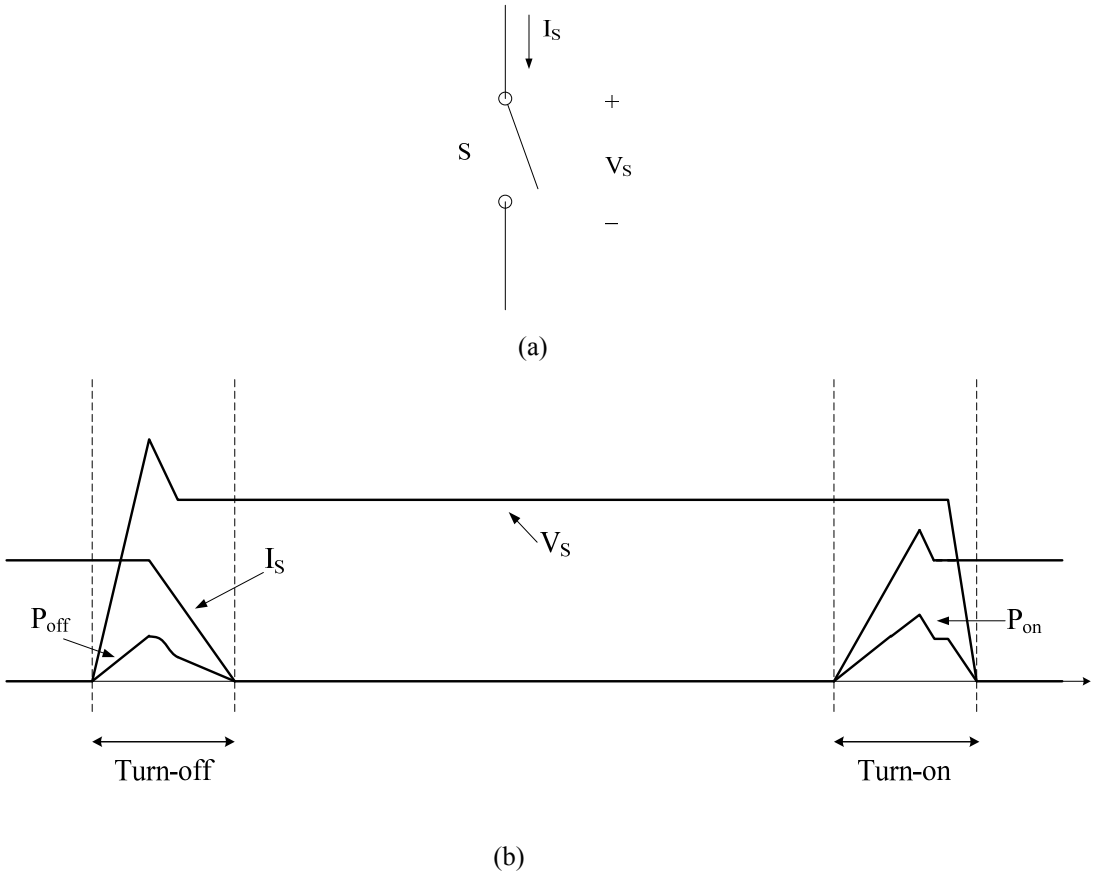


Fig. 1.3. (a) A power converter switch symbol, (b) Typical switch voltage and current waveforms

1.1.4. Soft Switching

A power converter can be operated with high switching frequencies only if the problems of switching losses can be overcome; this can be done using "soft-switching" techniques. This term "soft-switching" refers to various techniques that make the switching transitions more gradual than just simply turning a switch on or off (which is referred to as "hard-switching" in the power electronics literature) and that force either the voltage or current to be zero while the switching transition is being made. Switching losses are reduced as there is no overlap of switch voltage and switch current during a switching transition as one of the two is zero during this time. Soft-switching techniques are either zero-voltage switching (ZVS) techniques or zero-current switching (ZCS) techniques. Both ZVS and ZCS are briefly reviewed here.

ZVS techniques are techniques that force the voltage across a switch to be zero just before it is turned on or off and to keep this voltage zero while a switching transition occurs. All MOSFETs and most IGBTs have anti-parallel diodes that are built into the body of each device that allows current to flow from source to drain in a MOSFET and from emitter to collector in an IGBT. A ZVS turn-on in MOSFETs and IGBTs is therefore done by forcing current through the body-diode of the devices just before they are turned on. This clamps the voltage across the device to a single diode drop (which is a negligible voltage) during a switching transition so that turn-on switching losses are greatly reduced. A ZVS turn-off is achieved by slowing down the rate of voltage rise across a switch when it is turned off by adding some capacitance across the switch; this limits the overlap between voltage and current during the switching transition.

ZCS techniques are techniques that force the current through a switch to be zero when the switch is about to turn on or off and keep this current zero while a switching transition occurs. A ZCS turn-off is achieved by diverting current away from the switch into the rest of the power converter just before the switch is turned off. This is typically done by providing a path of negative voltage potential to the switch or by imposing a negative voltage somewhere in the current path. A ZCS turn-on can be done by adding an inductor

in series with the switch that slows down the rate of current rise when the switch is turned on; this limits the overlap in voltage and current during the switching transition.

Since MOSFETs are used in low current, high switching frequency applications and have a significant drain-source capacitance, they are usually implemented with some sort of ZVS technique. The drain-source capacitance, in combination with an external snubber capacitance, is often used to ensure that the device can be turned-off with ZVS, and negative current is used to discharge this capacitance and flow into the body-diode so that the device can turn on with ZVS. Since IGBTs are used in high current applications and have a slower turn-off due to their being minority-carrier devices, they are usually implemented with ZCS. They have smaller collector-emitter capacitances than MOSFETs and it is the turn-off losses that must be dealt with.

1.2. DC-DC Boost Converter

DC-DC converters are used whenever DC electrical power is to be changed from one voltage level to another. They are needed because unlike AC, DC cannot simply be stepped up or down using a transformer. Most DC-DC converters are power electronic converters that operate with semiconductor switches like MOSFETs and IGBTs. These switches are required to turn on and off periodically. The output DC voltage in such converters is dependent on the duty cycle D, which is defined as the length of time that the switch is on (t_{on}) over the duration of the switching cycle (T_s).

$$D = \frac{T_{on}}{T_s} \tag{1-1}$$

A basic DC-DC converter is the boost converter, which is used to step up the input voltage; its basic circuit topology (configuration) is shown in Fig. 1.4. As can be seen, the basic boost converter has four main components: Switch S, diode Q, inductor L and output filter capacitor C. The converter works as follows: When S is switched on, current flows from the input source through L and S, and energy is stored in the inductor. There is no current through Q, and the load current is supplied by the output capacitor. When S

is turned off, the current flowing in L must flow through Q as it has no other path to flow through.

In order to operate the semiconductor switch in the boost converter, a periodic pulse should be applied between gate and source terminals (V_{GS}) if the switch is a MOSFET or between gate and emitter terminals (V_{GE}) in the case that the switch is an IGBT. The duty cycle of the switch, D, which relates the width of this periodic pulse to the length of the switching period, determines the ratio of the output to the input voltage. Converters that have this property are called pulse-width modulated (PWM) converters. In the case of the boost converter, if the current through L is continuous through the switching cycle and does not drop to zero at any time, then the ratio of output voltage V_o to input voltage V_{in} can be determined to be

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{1-2}$$

where D is the duty cycle.

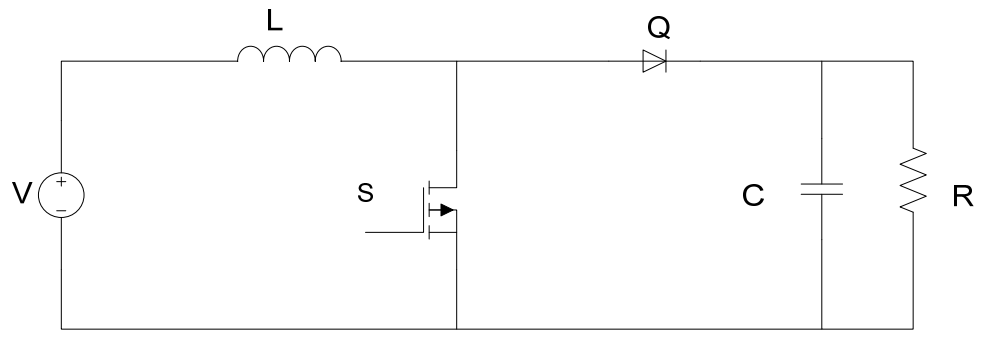


Fig. 1.4. Basic boost converter

1.3. Current-Fed Isolated PWM Full-Bridge DC-DC Boost Converter

Transformers are often used in power electronic converters to help step-up or step-down voltage and to provide electrical isolation by isolating voltages of significantly different levels or forms. This is true even for DC-DC converters, which can have transformers incorporated into their basic topologies even though a continuous DC voltage cannot be

applied across them for a lengthy period of time. In the case of DC-DC converters with transformer isolation, these converters can operate with transformers also long as care is taken to impress waveforms with zero average voltage such as AC waveforms across their input.

Current-fed PWM full-bridge isolated boost converters like the one shown in Fig. 1.5 have a transformer in their topology and are very attractive in applications where an output DC voltage that is considerably larger than the input voltage is needed. Such applications include medical power supplies and power supplies for electrostatic applications where extremely high output voltages are required, and fuel cell and photovoltaic applications where the input voltage is very low. The basic DC-DC boost converter that was discussed in the previous section is unsuitable for these applications as it requires a very large duty cycle D to produce the necessary high voltage gain. Extremely large duty cycles are to be avoided as they result in very high component stresses and inefficient converter operation as power is transferred to the output in bursts during a very small part of the switching cycle. In contrast, current-fed full-bridge boost converters contain a step-up transformer, which can do additional voltage boosting, thus avoiding operation with very large duty ratios.

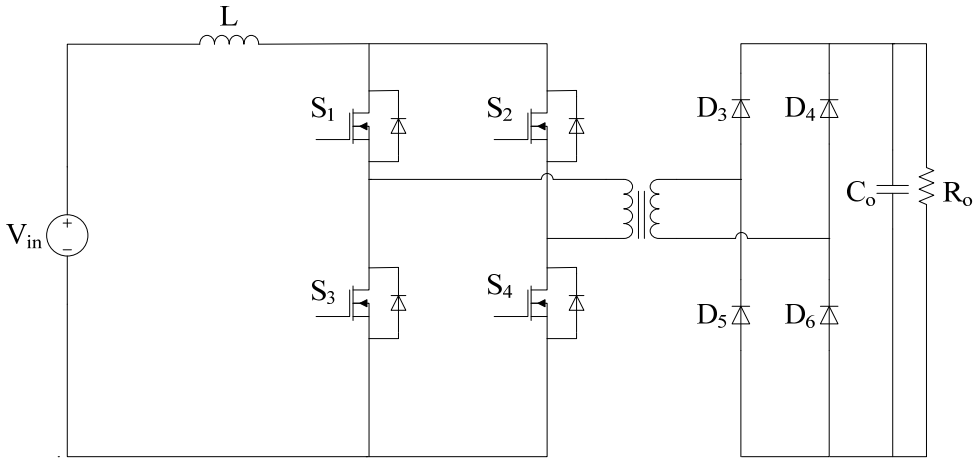


Fig. 1.5. Current-fed isolated PWM full-bridge DC-DC boost converter

The converter shown in Fig. 1.5 operates with the following sequence of gating signals during a switching cycle: S_1 and S_4 on, then all bridge switches on, then S_2 and S_3 on then all switches on. In other words, a power transfer mode when only a pair of diagonally opposed switches is on is always followed by a "boosting" mode where all the switches are on and no energy is transferred. The converter shown in Fig. 1.5 operates like a boost converter as the current in input inductor is increased in boosting mode and is decreased in power transfer mode. It should be noted that there must always be a path for the input current to flow through the full-bridge switches at all times.

The converter as shown in Fig. 1.5, however, is not a practical converter as it needs some sort of snubber or clamping circuit to snub or clamp potential voltage spikes that may occur whenever converter switches are turned off. An example of an isolated full-bridge converter with a snubber circuit is shown in Fig.1.6. In this circuit, capacitor C_c is used to clamp whatever voltage spikes may appear across the DC bus when the primary-side full-bridge switches are turned off. Some energy from C_c is transferred to input capacitor C_i through resistor R_c and is recycled.

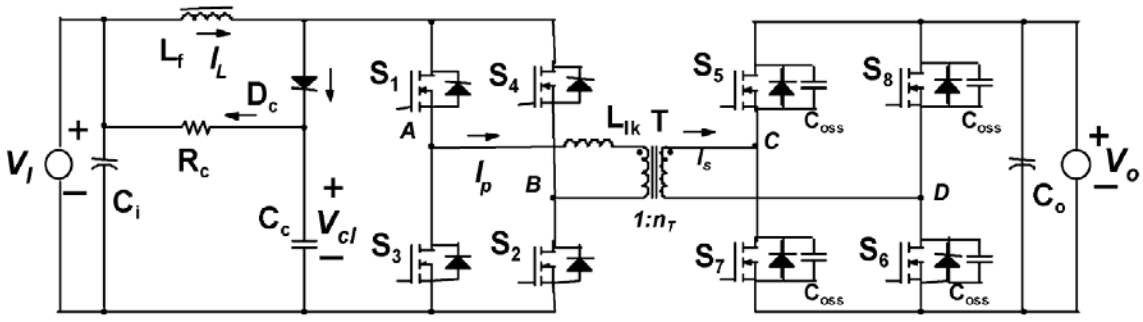


Fig. 1.6. ZVS full-bridge boost converter with an improved snubber circuit proposed in [2]

Although passive snubber circuits can help snub or clamp potential DC bus voltage spikes they do nothing to reduce switching losses or contribute to soft-switching operation. A PWM full-bridge boost converter can be implemented with either zero-voltage switching (ZVS) or zero-current switching (ZCS) depending on the application. ZVS is implemented in applications where the input voltage is high, the input current is low or medium and switch turn-on switching losses are dominant. ZCS is implemented in

applications where the input current is high and conduction losses are dominant. The focus of this thesis is on ZVS PWM full-bridge boost converters.

1.4. Literature Review

Previously proposed current-fed PWM ZVS full-bridge DC-DC converters can be categorized as follows:

- Resonant converters
- Active clamp converters
- Converters with paralleled auxiliary circuits

Each of these converter types is reviewed in this section.

1.4.1. Resonant Converters

ZVS resonant power converters [3]-[11] contain a resonant inductor-capacitor (L-C) network whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. By putting one or more components of the L-C network in parallel with the full-bridge switches, the voltage across the switches can be shaped so that they are able to turn on and off with ZVS. An example of a DC-DC resonant converter is shown in Fig. 1.7.

Although resonant converters use just a few passive components to achieve ZVS operation, they have several drawbacks. One of these is that they usually suffer from high peak voltage or current stresses in comparison to conventional PWM converters so that they generally need to be implemented with more expensive, higher voltage or current rated switches.

The most significant drawback, however, is that resonant converters operate with more conduction losses than conventional PWM converters due to an increased amount of current that circulates in the transformer primary side of the converter. This is particularly

true of a resonant converter such as the one shown in Fig. 1.7, which has resonant components that are placed parallel to the transformer primary that provide a path for current to flow through without resulting in power being transferred to the load. Such circulating current adds to the conduction losses of resonant converters so that even though they are more efficient than they would be if ZVS was not implemented, the gains in efficiency are not as much as what they could possibly be.

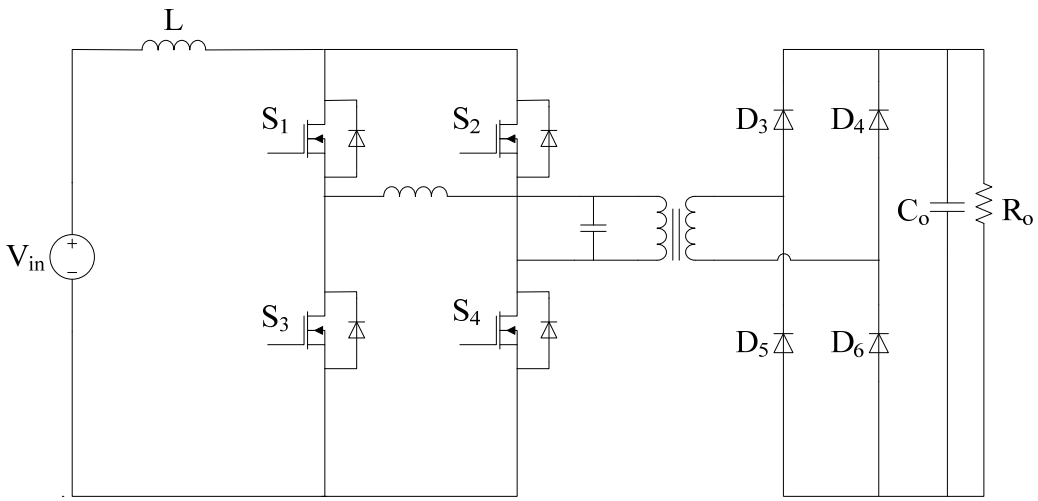


Fig. 1.7. Resonant boost converter

1.4.2. Active Clamp Converters

Another type of ZVS-PWM isolated full-bridge boost converter is the so-called active clamp converter that is shown in Fig. 1.8 [12]-[22]. This converter is the same as the conventional converter shown in Fig. 1.5 except that a simple circuit consisting of a switch and a clamp capacitor is placed across the DC bus, at the input of the full-bridge. The converter operates with power transfer and boosting modes as described above. The clamp capacitor clamps the voltage that appears across the full-bridge whenever full-bridge switches are turned off and is allowed to discharge into the full-bridge converter whenever a pair of diagonally opposed switches is on. The additional switch is always off whenever the converter is in a boosting mode and when full-bridge switches are in the process of being turned off to avoid the possibility of the capacitor being fed to

a short-circuited converter. The converter gets the name of "active clamp" as the DC bus capacitor acts as a clamp and it is in series with an active switch.

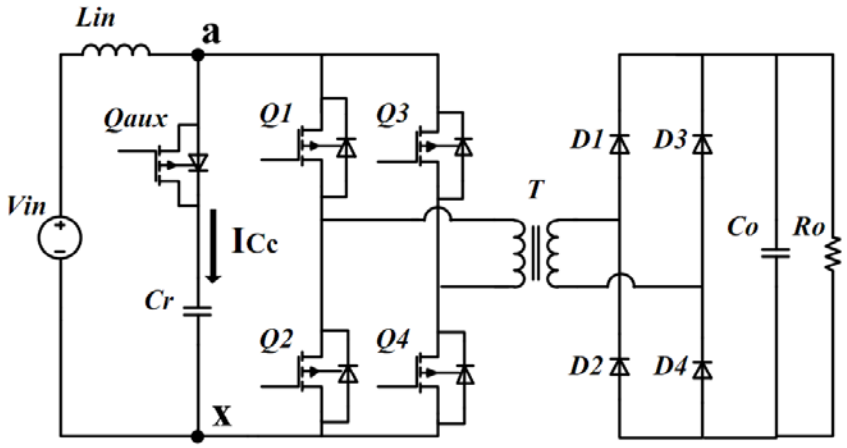


Fig. 1.8. Active clamp ZVS full-bridge boost converter

The converter's main full-bridge switches can operate with ZVS because the converter uses energy in the transformer leakage inductance to discharge the output capacitances of these switches. When the active clamp switch is on and the clamp capacitor discharges into the full-bridge, additional energy is stored in the transformer leakage inductance, which makes it easier to discharge the switch output capacitances and ensure ZVS operation. Although the converter is a fixed frequency ZVS-PWM current-fed converter that uses a very simple auxiliary circuit to create ZVS over an extended range of load, it suffers from the following disadvantages:

- Its ZVS operation is load dependent and is lost at light loads.
- The current stresses of the switches are higher than that of other PWM boost full-bridge converters as the switches must conduct current from the auxiliary circuit in addition to the input inductor current.
- The main converter switches and the active clamp switch have a significant amount of conduction losses since current flows either through the active clamp switch or

through its body diode whenever any two diagonally opposite bridge switches are on (which occurs during a significant portion of the switching cycle)

1.4.3. Converters with Paralleled Auxiliary Circuits

Most recently proposed ZVS-PWM isolated full-bridge boost converters use an auxiliary circuit placed across the primary-side DC bus to enable the main converter switches to operate with ZVS. This auxiliary circuit typically consists of an active switch and passive elements such as resistors, diodes, inductors and capacitors. The auxiliary circuit differs from the active clamp circuit as it is the turning on of the auxiliary switch that discharges the output capacitances of switches that are about to be turned on and most of the energy is stored in these capacitances is either recycled to the input or transferred to the output through a path that is parallel to the main path of power flow.

In most ZVS-PWM converters with paralleled auxiliary circuits, the auxiliary circuit operates during the turn-on of the main converter switches and only during a very small portion of the switching cycle. Since this is the case, the converter behaves like a conventional PWM converter during most of the switching cycle. The fact that the components in the auxiliary circuits handle only a small portion of the power delivered by the main switches, allows the use of lower current rated components – including auxiliary switch devices that have fewer turn-on losses than the main power devices, which must conduct more current. Although these auxiliary switch devices tend to have higher values of on-state resistance, these higher values have a minor effect on conduction losses as the auxiliary switch conducts current during only a small portion of the switching cycle.

Numerous auxiliary circuits have been proposed to achieve the ZVS operation of a full-bridge boost converter. One of the simplest is the one proposed in [23] and shown in Fig. 1.9. Although the auxiliary circuit in this converter is simple and enables the main converter switches to turn on with ZVS, a significant amount of energy has to be

dissipated in the auxiliary circuit, which limits the effectiveness of this auxiliary circuit approach.

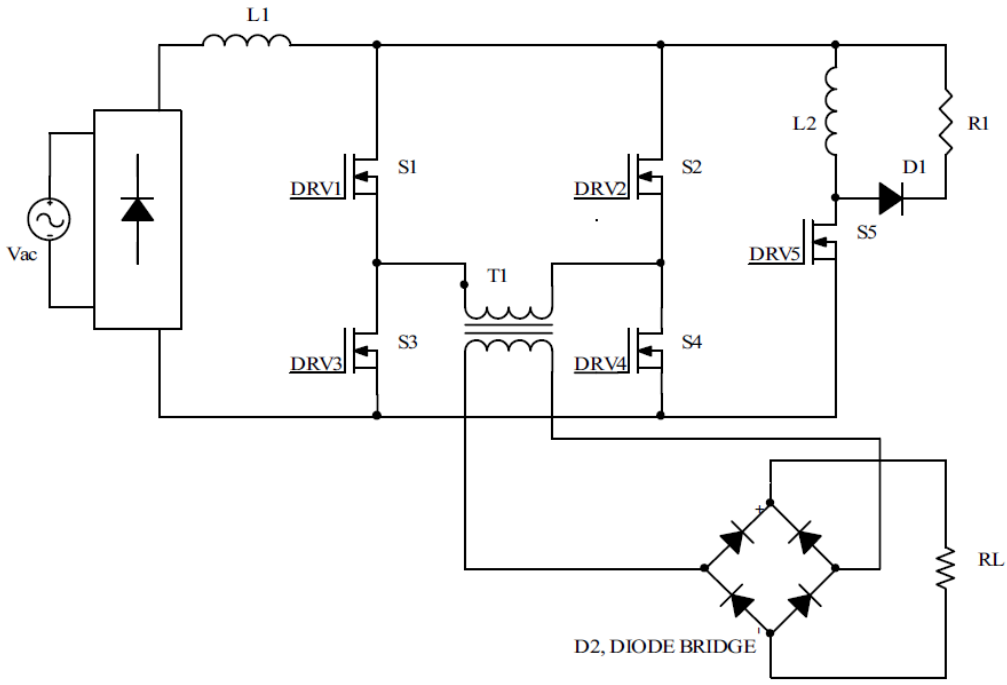


Fig. 1.9. A simple full-bridge boost converter proposed in [23]

Another proposed ZVS-PWM isolated full-bridge converter is the one proposed in [24] and shown in Fig. 1.10. Although this converter has a more sophisticated auxiliary circuit that allows for some auxiliary circuit energy to be transferred to the output instead of being dissipated, and the auxiliary switch can turn on and off softly, the auxiliary circuit pumps additional current into the full-bridge switches and some sort of dissipative snubber (not shown in diagram) has to be placed at the DC bus to suppress voltage overshoots and ringing across the switches [24]. Although there is some improvement in efficiency, the losses in the dissipative snubber minimize whatever gains in efficiency that may be achieved.

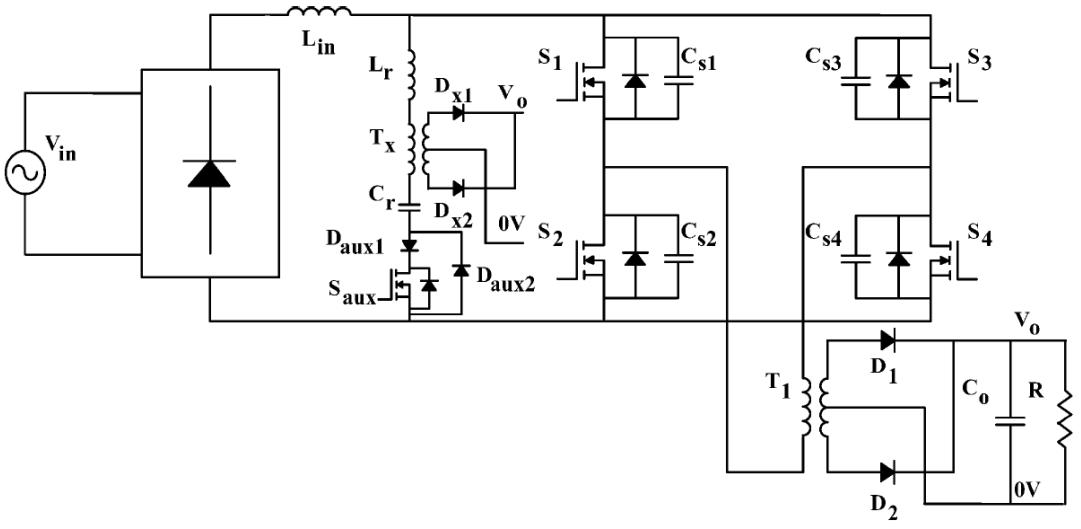


Fig. 1.10. Current-fed single-stage PWM full-bridge converter proposed in [24]

A ZVS-PWM isolated boost full-bridge converter that avoids the use of dissipative snubbers to reduce voltage spikes is the converter that is proposed in [25] and shown in Fig. 1.11. This converter uses a sophisticated passive circuit network to act as a DC bus voltage clamp and as a snubber for the auxiliary switch. Moreover, some of the auxiliary circuit energy can be transferred to the output instead to being dissipated in a resistor. The converter's auxiliary circuit, however, is very complicated and needs numerous components and the auxiliary switch does not turn off softly.

A ZVS-PWM isolated boost converter with a simpler auxiliary circuit is proposed in [26] and is shown in Fig. 1.12. This converter is implemented with an active auxiliary circuit that consists of an active switch, a capacitor, a small transformer and two diodes. The auxiliary circuit is connected parallel to the full-bridge and is used to discharge the switch output capacitances and the auxiliary circuit capacitor before the switches are to be turned on and is deactivated shortly afterwards later in the switching cycle. Although most of the auxiliary circuit energy is transferred to the input via the transformer, the active switch in the auxiliary circuit does not turn off softly and thus has turn-off losses. These losses partially offset whatever gains in efficiency that may be achieved by the reduction of the converter's turn on switching losses.

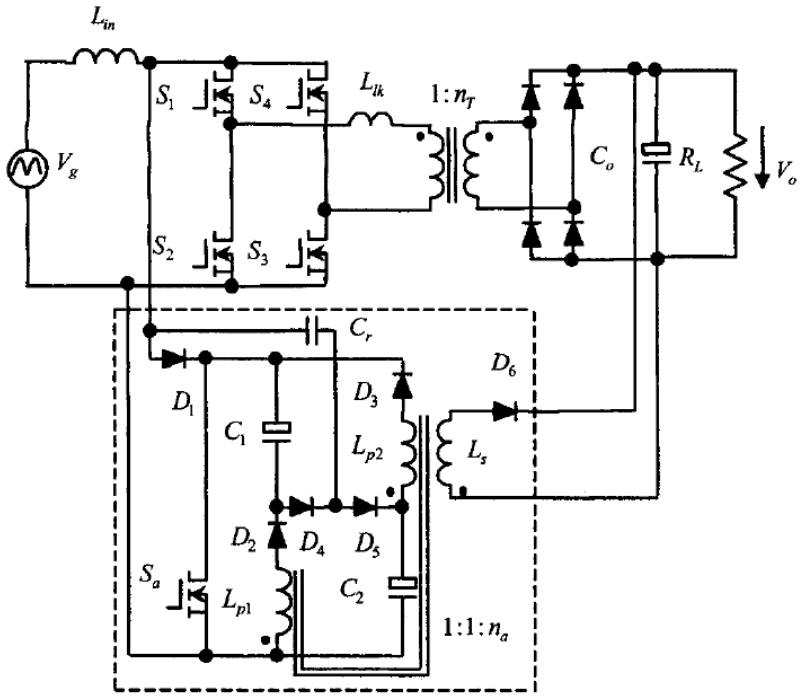


Fig. 1.11. Complicated auxiliary circuit proposed in [25]

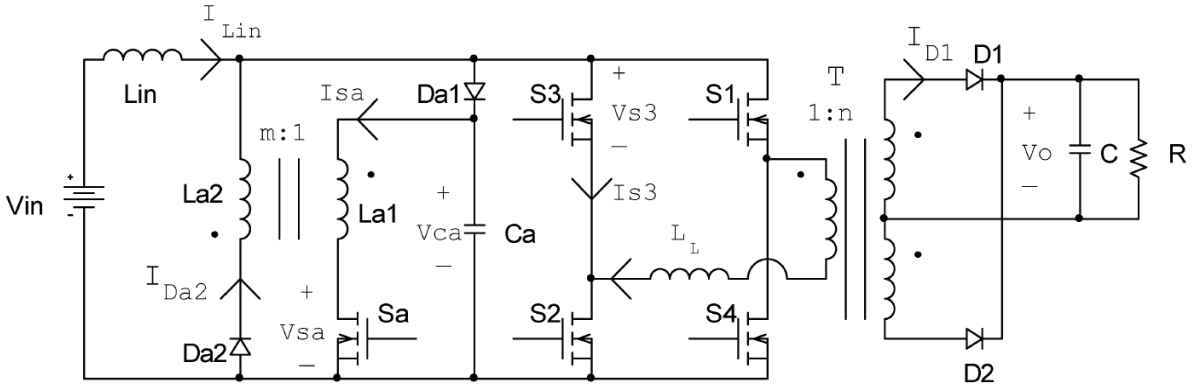


Fig. 1.12. ZVS full-bridge boost converter proposed in [26]

1.5. Thesis Objectives

The main objectives of this thesis are as follows:

- To propose a new ZVS-PWM isolated full-bridge boost converter that has fewer drawbacks than the converters reviewed in this chapter.
- To analyze the steady-state operation of the new converter so that its steady-state operating characteristics can be determined and its operation understood.
- To develop a design procedure that will allow for the proper selection of components to be implemented in the converter.
- To confirm the feasibility of the proposed converter by computer simulation and experimental work.

1.6. Thesis Outline

The thesis is organized as follows:

- In Chapter 2, the new converter is introduced, its general operation is explained, and its modes of operation are reviewed. The features of the converter are also stated in the chapter.
- In Chapter 3, the modes of converter operation that are presented in Chapter 2 are analyzed mathematically. Component voltage and current equations that describe the steady-state operation of the converter are derived, and then are used in Chapter 4 to generate graphs of converter characteristics.
- In Chapter 4, the analysis and characteristics graphs are used as part of a design procedure to select the values of key converter parameters. The design procedure is demonstrated with an example.
- An experimental prototype of the proposed ZVS full-bridge DC-DC boost converter was built and its functionality was confirmed with experimental results obtained from a 500 W prototype. The results of experimental work and computer simulation work are presented in Chapter 5.
- In Chapter 6, the contents of the thesis are summarized, the thesis contributions and conclusions are stated, and suggestions are made for future work.

Chapter 2

A New ZVS-PWM Full-Bridge Boost Converter

2.1. Introduction

A new ZVS-PWM isolated full-bridge boost converter is proposed in this chapter. The new converter achieves ZVS operation using a simple auxiliary circuit that consists of an active switch and a few passive components. It does not have the disadvantages that other previously proposed converters of the same type have such as the circulating current found in resonant type converters or the hard auxiliary switch turn-off found in converters with auxiliary circuits. In this chapter, the new converter is presented, its basic operation is explained, and its advantageous features are stated.

2.2. Proposed Converter

The proposed ZVS-PWM isolated full-bridge boost converter is shown in Fig. 2.1. It is like a conventional PWM isolated boost converter (Fig. 1.5), but with an auxiliary circuit that consists of an auxiliary switch S_{aux}, capacitor C_r, inductor L_r, and diodes D_1 and D_2.

The basic operating principle of the converter is as follows: The main full-bridge switches operate in the same way as the switches of a conventional PWM isolated boost converter. As described in Section 1.3, the gating signal of these switches is such that converter states or modes when a pair of diagonally opposed switches is on (power-transfer mode) are always followed by the turning on of all the four full-bridge switches (boosting mode).

The auxiliary circuit is activated just before a full-bridge is about to be turned on. By doing so, the output capacitances of each switch and capacitor C_r are fully discharged so that the switches can be turned on with ZVS. The energy that is stored in the output

capacitances of each switch and capacitor C_r is transferred to the input and thus recycled instead of being dissipated in the switches. The full-bridge switches can be turned off with ZVS as the output capacitances of each switch and capacitor C_r help slow down the rate of voltage rise across the switches.

The auxiliary switch S_{aux} also operates with soft-switching as it has a ZCS turn-on and turn-off. Inductor L_r helps to slow down the rate of switch current rise when S_{aux} is turned on so that it can do so with ZCS. As will be explained in the next section, S_{aux} can be turned on with ZCS as the current through this switch is naturally extinguished before it is turned off.

Diode D_1 is placed to isolate the auxiliary circuit from the main full-bridge so that the auxiliary circuit, when it is off, does not interfere with the operation of the full-bridge. Diode D_2 is used to block the internal parallel source-drain body-diode of S_{aux} so that this diode does not conduct when C_r is discharged.

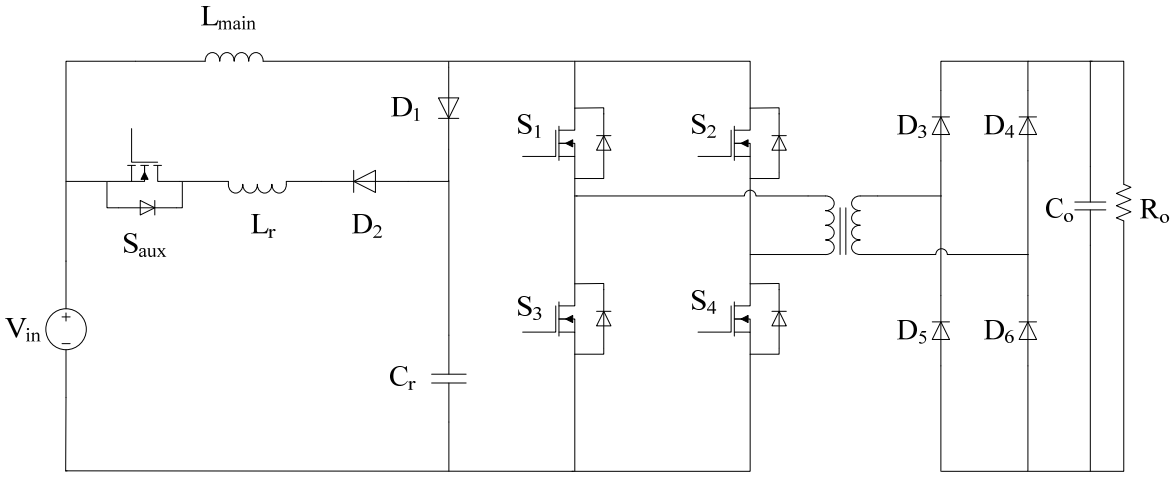


Fig. 2.1. Proposed current-fed full-bridge boost converter

2.3. Converter operation

In this section, the steady-state operation of the proposed converter is explained in detail in terms of the different states or modes that the converter goes through over a steady-state switching cycle. These modes are distinct from each other in terms of the voltage across and the current flowing through different circuit components. When the converter is in steady-state operation, the final voltage and current of each converter component are identical to its initial values for every switching cycle.

The proposed boost converter goes through ten different modes of operation over half of a steady-state switching cycle; the other half cycle is identical to the first half. Typical converter voltage and current waveforms are shown in Fig. 2.2 and equivalent circuit diagrams for each mode of converter operation are shown in Fig. 2.3. What should be especially noted about these diagrams and waveforms is how the main full-bridge switches turn on and off with ZVS and how the auxiliary switch turns on and off softly as well. The converter's modes of operation during a half switching cycle are as follows:

Mode 0 ($t < t_0$) (Fig.2.3(a)): In this mode, only switches S_1 and S_4 are on and the converter is in an energy transfer mode as energy is transferred from the input to the output through diodes D_3 and D_6. The current through L_{main} is falling throughout this mode.

Mode 1 ($t_0 < t < t_1$) (Fig.2.3(b)): This mode begins when switch S_{aux} is turned on in anticipation of the DC bus being shorted and the converter entering a boosting mode. Since the snubber capacitor voltage V_{Cr} is greater than the input voltage, current will start flowing through S_{aux}. S_{aux} turns on softly as inductor L_r is in series with this switch and limits the rise in current through it. C_r discharges into the auxiliary inductor during this mode. Since voltage V_{Cr} is higher than the bridge voltage, diode D_1 is reversed biased and does not conduct. This mode ends when C_r voltage reaches the voltage across off-state bridge switches which is $\frac{V_o}{N}$.

Mode 2 ($t_1 < t < t_2$) (Fig.2.3(c)): This mode begins when diode D_1 becomes forward biased and starts to conduct. The voltage across the bridge switches therefore follows capacitor voltage V_{Cr} which is decreasing. This voltage is also equal to the voltage across the transformer. Ideally, if the voltage across the transformer is less than $\frac{V_o}{N}$, the output diodes become reversed biased and power is not transferred to the output, but this power transfer does not in fact stop immediately because of the presence of leakage inductance in the transformer. The transformer current reaches zero at the end of this mode.

Mode 3 ($t_2 < t < t_3$) (Fig.2.3(d)): The output capacitances of switches S_2 and S_3 and capacitor C_r keep discharging during this mode. The current in the auxiliary circuit branch is equal to the sum of the current from the full-bridge caused by the discharging of the switch output capacitances and C_r, and the input current that flows through L_{main}.

Mode 4 ($t_3 < t < t_4$) (Fig.2.3(e)): At the beginning of this mode, the DC bus voltage is zero and is clamped to zero as the body-diodes of the converter switches are forward biased and start to conduct. Switches S_2 and S_3 can be turned on with ZVS sometime during this mode while current is flowing through their body-diodes. Also during this mode, the current that flows through the auxiliary circuit (and thus the current through the full-bridge) begins to decrease because the voltage across the auxiliary inductor is negative as the input voltage is at one end of the circuit and the DC bus voltage is zero. The auxiliary circuit current is equal to the current through L_{main} at the end of this mode, which makes the current flowing through the full-bridge to be zero.

Mode 5 ($t_4 < t < t_5$) (Fig.2.3(f)): At $t = t_4$, the current that was flowing through the full-bridge reverses direction and flows through the switches. The current in the auxiliary circuit continues to decrease as the input current is gradually transferred to the full-bridge. The auxiliary circuit current is zero by the end of this mode and S_{aux} can be turned off softly at any time afterwards until a diagonally pair of switches is turned off and the DC bus is no longer shorted.

Mode 6 ($t_5 < t < t_6$) (Fig.2.3(g)): The converter is in a boosting mode during this mode. It operates like a standard PWM boost converter as the DC bus is shorted, the current through L_{main} rises, and the auxiliary circuit is inactive.

Mode 7 ($t_6 < t < t_7$) (Fig.2.3(h)): At $t = t_6$, switches S_1 and S_4 are turned off. Due to the presence of their output capacitances (not shown in the figure) and C_r, these switches can be turned off with ZVS. Main switch output capacitances and C_r start charging and at the end of this mode their voltage reaches $\frac{V_o}{N}$.

Mode 8 ($t_7 < t < t_8$) (Fig.2.3(i)): At the beginning of this mode, as the DC bus voltage is rising, the transformer primary side voltage reaches a certain level that results in the output diodes becoming forward biased and thus conducting current. The main inductor current transfer from snubber capacitor C_r to the transformer primary winding is gradual and takes some time because of the leakage inductance of the transformer. During this time, the current flowing through C_r results in the capacitor being charged over and above the DC bus voltage, which results in voltage overshoots in the voltage across the main full-bridge switches that are off. At the end of this mode, the voltage across C_r reaches its maximum value and is clamped at this value as there is no current path for it to discharge. In the meantime, the main switch output capacitances and capacitor C_r start to resonate with the transformer leakage inductance at the start of this mode.

Mode 9 ($t > t_8$) (Fig.2.3(j)): After $t = t_8$, the converter is in an energy-transfer mode as switches S_2 and S_3 are conducting current, power is transferred from the input to the output, and the current in L_{main} falls. The transformer leakage inductance continues to resonate with the output capacitors of the main switches at the beginning of this mode, but this resonance eventually dies down due to parasitic resistances in the converter.

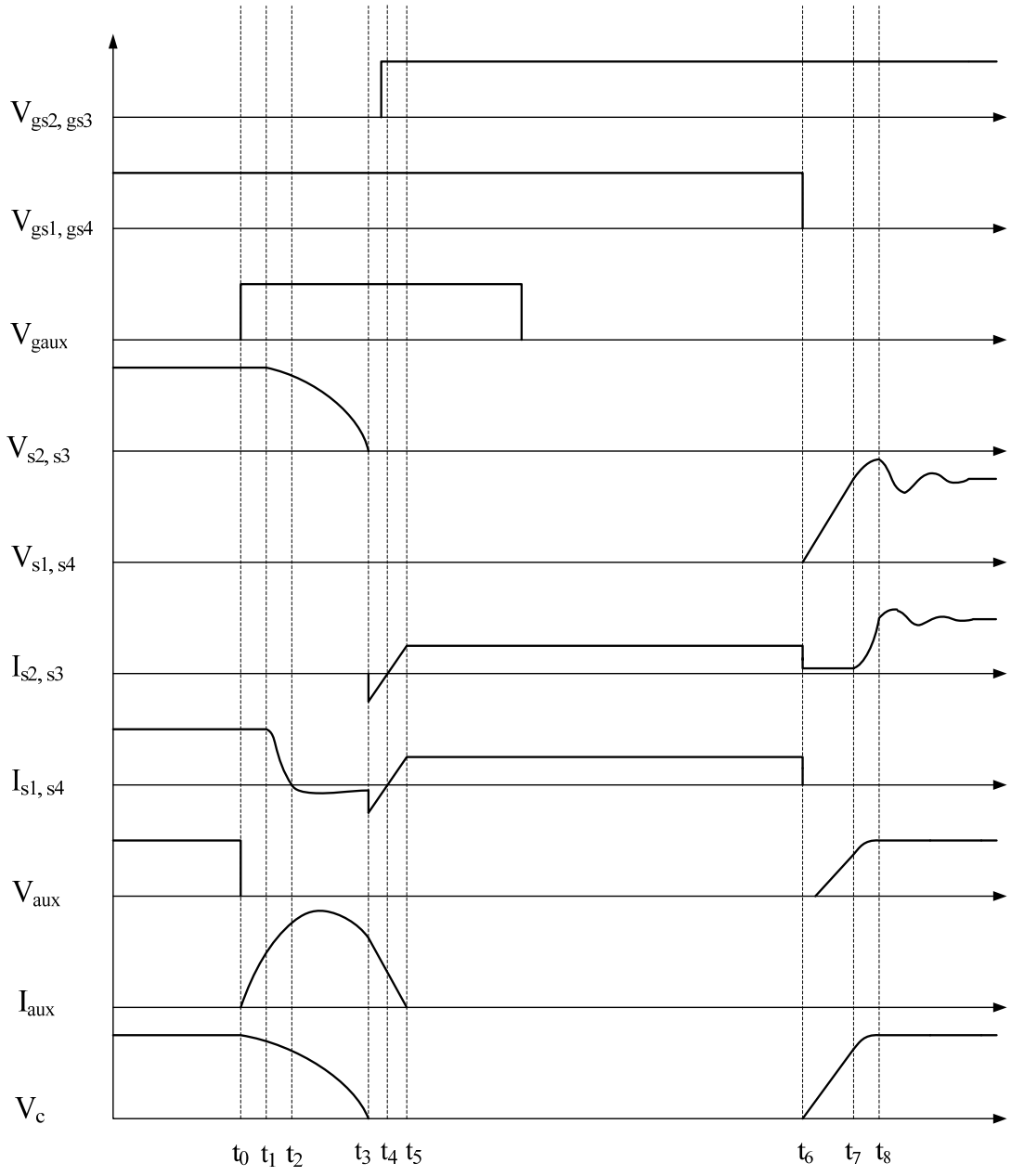
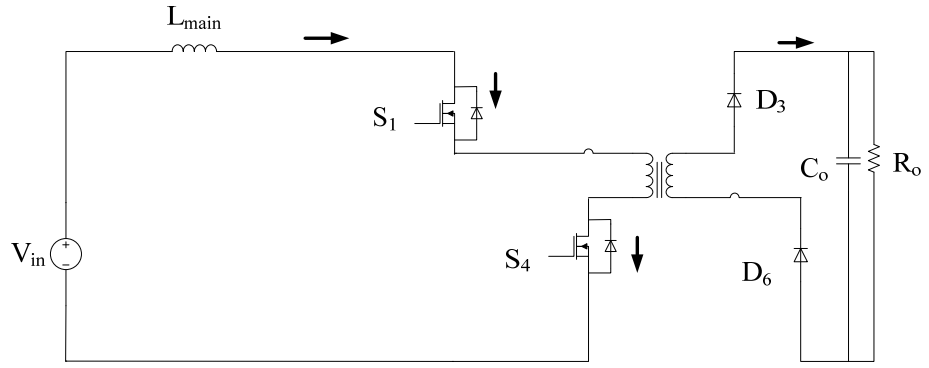
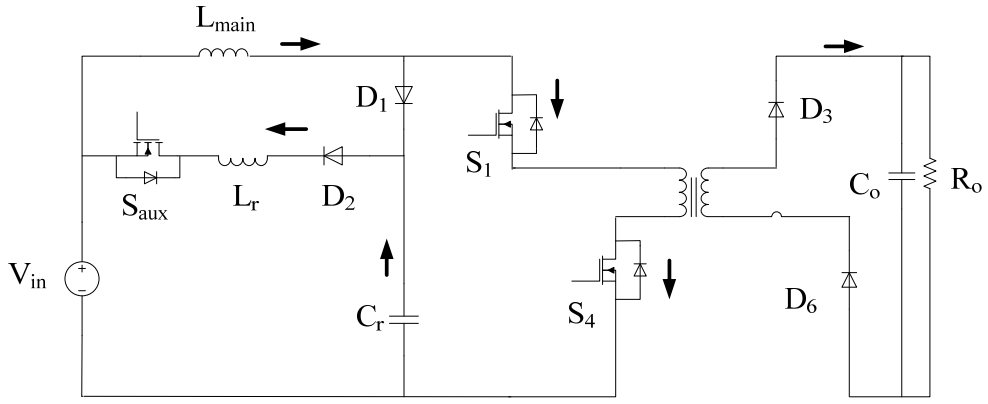


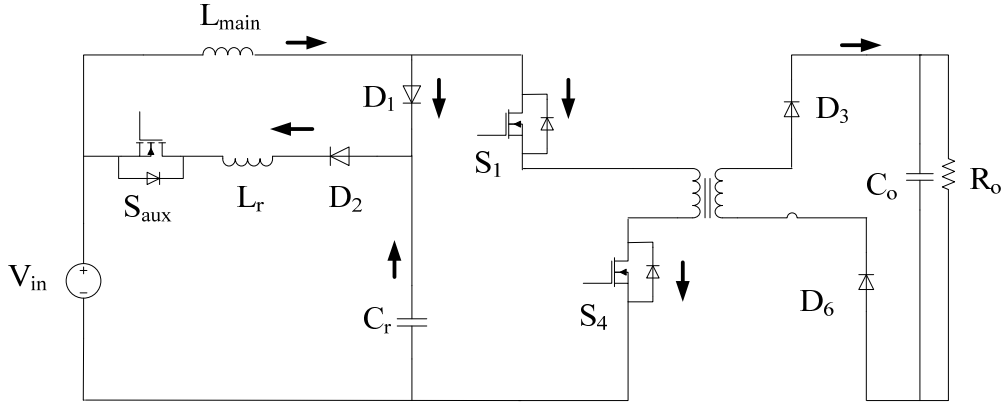
Fig. 2.2. Voltage and current of converter components in half-switching cycle



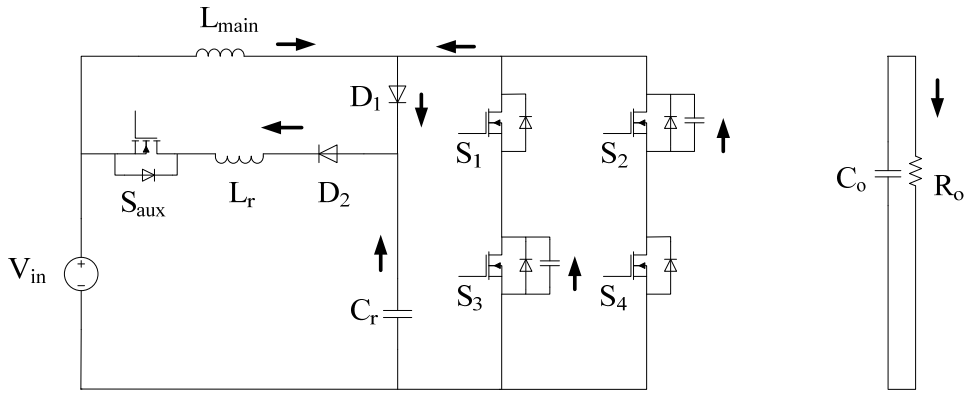
(a) Mode 0



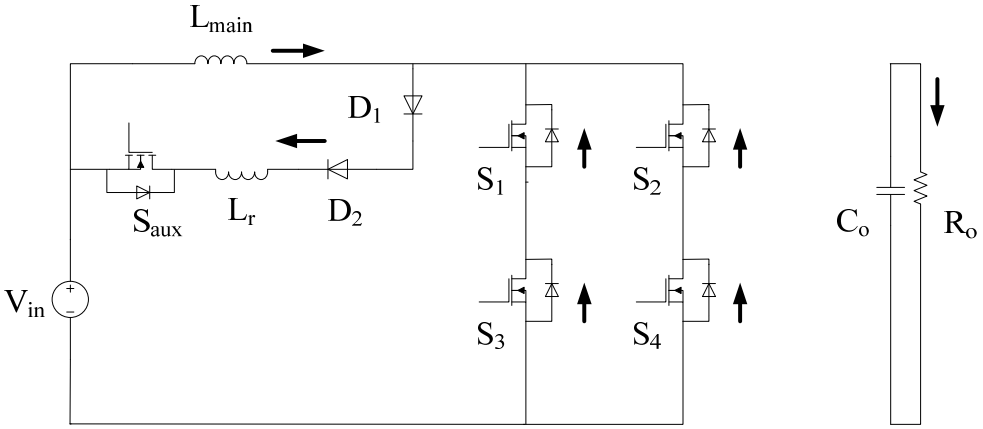
(b) Mode 1



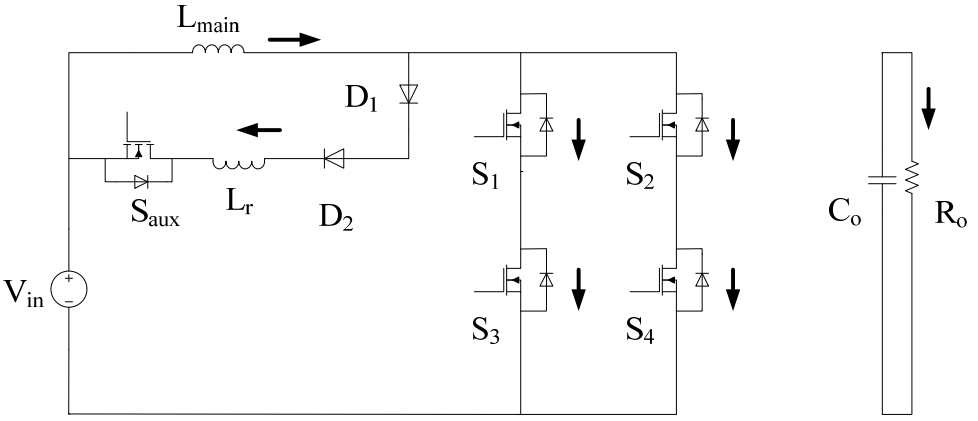
(c) Mode 2



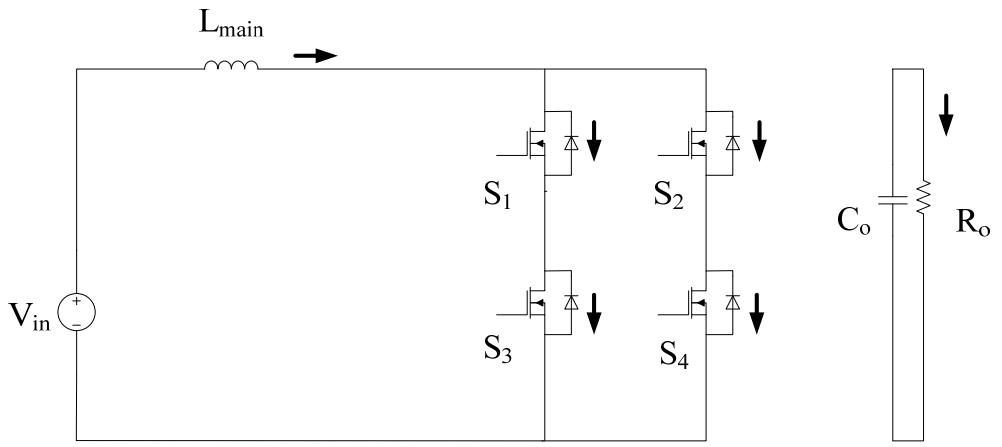
(d) Mode 3



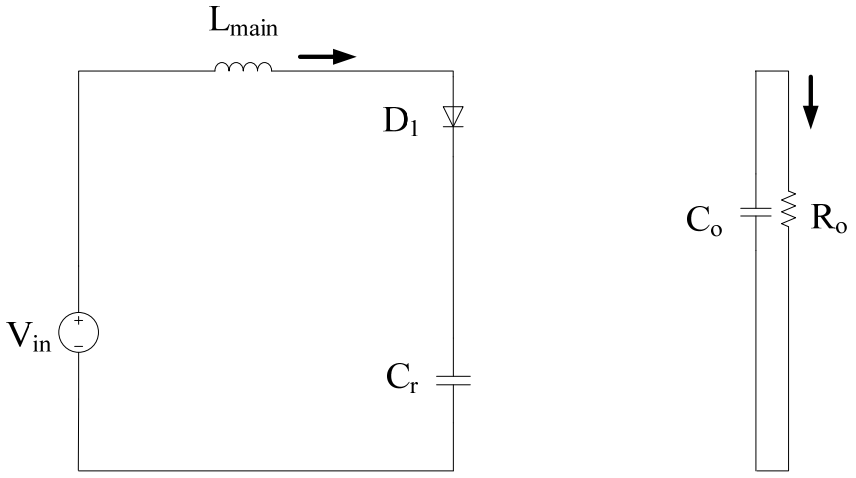
(e) Mode 4



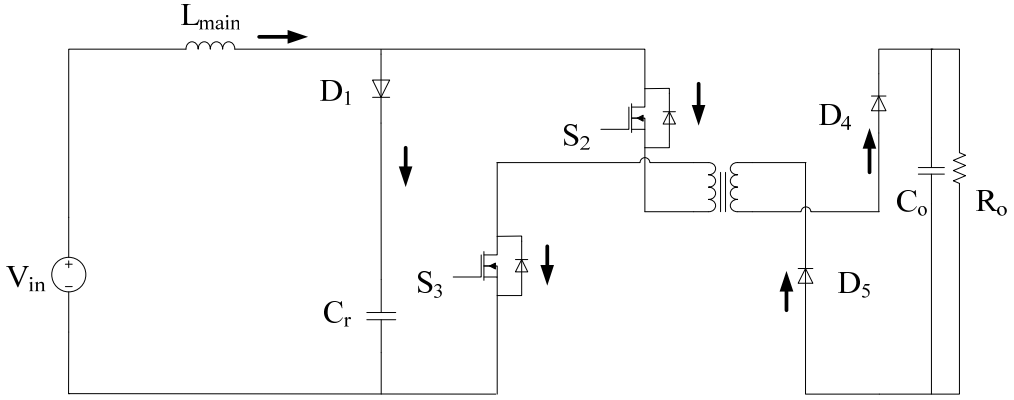
(f) Mode 5



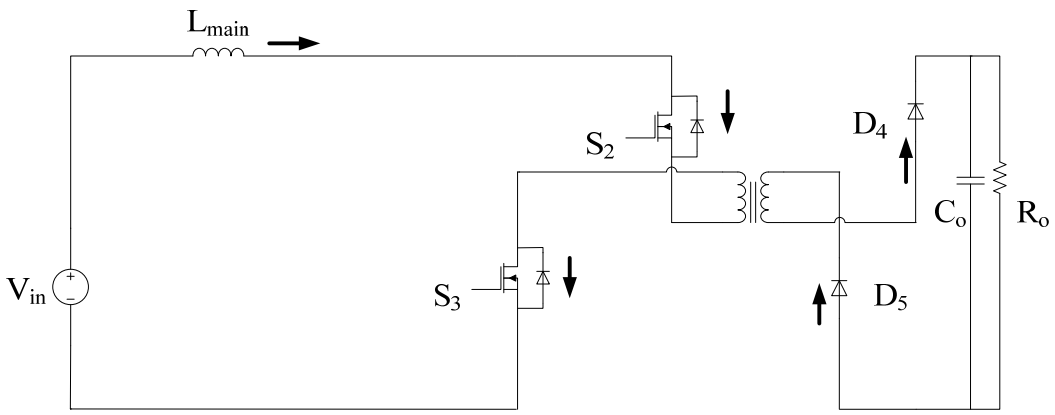
(g) Mode 6



(h) Mode 7



(i) Mode 8



(j) Mode 9

Fig. 2.3. Converter modes of operation

The proposed converter has the following features:

(i) All four main switches can turn on and off with ZVS. The auxiliary circuit operates when the switches are about to turn on and discharges the switch parallel capacitances to have zero voltage turn-on. Switches also turn off softly due to the auxiliary capacitor in parallel with them.

(ii) The auxiliary switch turns on and off softly. As it can be seen in Fig. 2.2, due to the series inductor with auxiliary switch, the current rise in the switch is gradual ("soft") and it does not have overlap with voltage across it. The turn-off of the switch occurs after the resonant interaction of L_r and C_r forces the switch current to zero, and diode D_2 keeps current from flowing through the body-diode of S_{aux}.

(iii) The auxiliary circuit is very simple as it consists of a switch, an inductor, a capacitor, and two diodes.

(iv) The timing of the turning off of the auxiliary switch is very flexible as it can be done at any time while the DC bus is shorted. This is contrast to other ZVS converters where the auxiliary switch (if it actually can be turned off softly) must do so within a narrow window of time. This feature simplifies the design of the auxiliary circuit considerably.

(v) Due to the blocking diode D_1, the auxiliary circuit does not pump additional current into the full-bridge switches so that their rms current and peak current

ratings are the same as the switches of the conventional PWM converter shown in Fig. 1.5.

(vi) One of the drawbacks of a conventional current-fed full-bridge converter is that there is no bus capacitor across the bridge. The lack of this capacitor may lead to excessive voltage spikes on the switches due to the resonance between their parasitic capacitances and transformer leakage inductance. The presence of a capacitor at the DC bus of the proposed converter prevents excessive voltage spikes from appearing across the full-bridge switches.

(vii) The auxiliary circuit does not have any unnecessary circulating current. Whatever current flows in the auxiliary circuit flows out of the circuit instead of being trapped inside, where it can contribute to conduction losses.

(viii) The converter's ZVS operation is load independent as it can ensure that its switches can turn on with ZVS from full-load to no-load. Since the operation of auxiliary circuit is dependent on the bus voltage and the bus voltage is constant from full-load to no-load, by activation of auxiliary circuit, C_r discharges and soft switching is performed at any load.

2.4. Conclusion

A new ZVS current-fed PWM full-bridge converter was introduced in this chapter. The modes of operation were studied with related circuit diagrams. Current and voltage waveforms of the converter components were provided to show soft switching operation of main switches and auxiliary switch. The advantages of the proposed converter over a conventional current-fed PWM full-bridge converter were also reviewed.

Chapter 3

Circuit Analysis of the Proposed Boost Converter

3.1. Introduction

In the previous chapter, the different modes of operation that the proposed converter goes through during half of a steady-state switching cycle were presented and explained in detail. In order to design the converter so that it can be made to operate properly, its steady-state characteristics must be known. In this chapter, a mathematical analysis of the modes of operation that were described in the previous chapter is performed to derive key equations that are needed to understand the steady-state behavior of the converter, relative to the values of certain key components. These relations will be used to develop a design procedure for the proposed converter in the next chapter of this thesis.

3.2. Circuit analysis

For the steady-state mathematical analysis presented in this chapter, the following assumptions have been made:

- Input inductor L_{main} is large enough to be considered as a constant current source.
- The output capacitor is large enough to be considered as a voltage source that is equal to the output voltage.
- All semiconductors have zero voltage drops while they are turned on.
- The transformer is ideal and has infinite magnetizing inductance.

The main objective of the mathematical analysis is to obtain equations for the auxiliary circuit capacitor voltage V_{Cr} and the auxiliary circuit inductor current i_{Lr} for each mode of operation in which the auxiliary circuit is active. With these equations, the values of V_{Cr} and i_{Lr} at the end of one mode can be used as initial values for the start of a following

mode. If the modal equations are used as part of a computer program to keep track of V_{Cr} and i_{Lr} throughout a switching cycle, analytical waveforms related to these parameters can be generated. These waveforms can then be used as part of a design procedure to design the converter so that it is possible to turn its switches on and off softly and to determine the voltages across them and the currents that flow through them so that appropriate devices can be selected. The design procedure and computer program is the focus of the next chapter of this thesis.

Mode 0

The equivalent circuit for this mode is shown in Fig. 3.1. Based on this circuit, the following Kirchhoff's Voltage Law (KVL) equation can be written at the transformer primary side:

$$\frac{V_o}{N} = (V_{in} + L\frac{di_{Lm}}{dt}) \tag{3-1}$$

where i_{Lm} is the current flowing through the input voltage source and N is the secondary to primary turns ratio of the transformer.

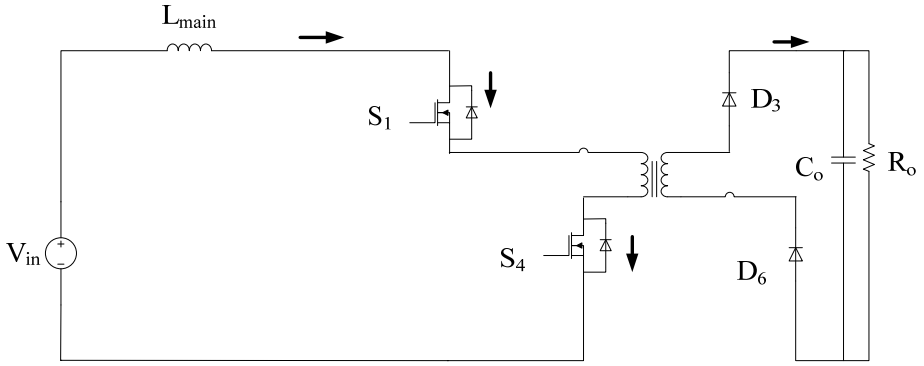


Fig. 3.1. Mode 0 of the converter operation

Mode 1

In this mode, the auxiliary switch turns on and current starts to circulate in the auxiliary circuit without any influence on the main converter operation. The equivalent circuit

shown in Fig. 3.2 is used to determine the voltage and current of the auxiliary components – specifically, the current through inductor L_r and the voltage across capacitor C_r. In this circuit, C_S is the output capacitor of one of main switches and L_{lk} is the transformer leakage inductance. The initial current of auxiliary circuit inductor L_r is zero and the initial value of snubber capacitor C_r can be expressed as

$$V_{Cr0} = I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + \frac{V_O}{N} \tag{3-2}$$

where $C_{tot} = C_r + 2C_S$.

The derivation of this equation is shown later in this chapter where the analysis of Mode 8 is performed. Mode 8 is the last mode of this half switching cycle when the auxiliary circuit is active so that the value of V_{Cr} at the end of Mode 8 can be considered to be the initial value of Mode 1, which is the first mode when the auxiliary circuit is active in the converter.

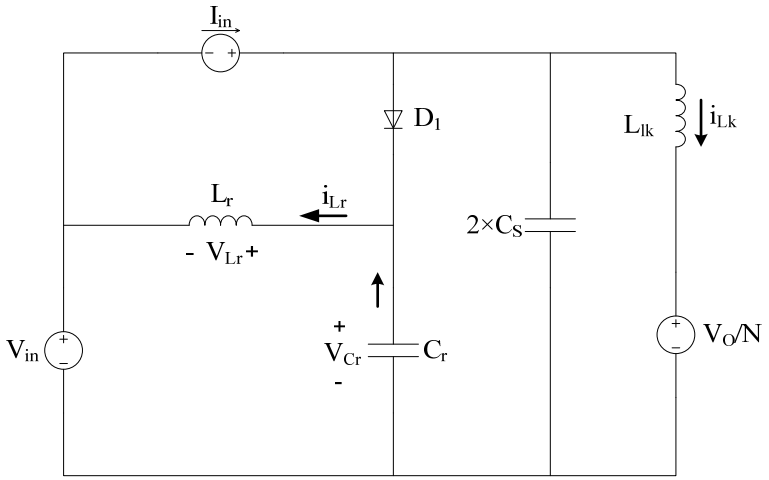


Fig. 3.2. Equivalent circuit of the converter at transformer primary side for mode 1 ($t_0 < t < t_1$)

Since diode D_1 is not actually conducting during this mode, the equivalent circuit shown in Fig. 3.2 can be simplified to the circuit shown in Fig. 3.3.

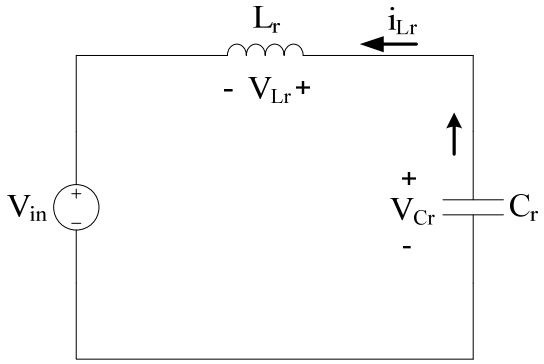


Fig. 3.3. Simplified equivalent circuit of the converter at transformer primary side for mode 1 ($t_0 < t < t_1$)

By applying KVL to the auxiliary circuit loop shown in Fig. 3.3, the following differential equation can be derived

$$-V_{Cr}(t) + L_r \frac{di_{Lr}}{dt} + V_{in} = 0 \tag{3-3}$$

This equation can be solved to give

$$V_{Cr}(t) = \left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + \frac{V_O}{N} - V_{in}\right)\cos\omega\,(t - t_0) + V_{in} \tag{3-4}$$

$$i_{Lr}(t) = C_r\omega\left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + \frac{V_O}{N} - V_{in}\right)\sin\omega\,(t - t_0) \tag{3-5}$$

where: $\omega = \frac{1}{\sqrt{L_r C_r}}$, $t_0 < t < t_1$ and with initial values of $i_{Lr}(t_0) = 0$ and $V_{Cr}(t_0)$ (equ. (3-2)) substituted into the solved equations. As described at the beginning of this section (Section 3.2), these equations can be used to determine the initial values for the next mode as these values are the same as the final values of V_{Cr} and i_{Lr} for this mode.

Equations (3-4) and (3-5) can be simplified for later steps of the analysis if V_O is substituted with

$$V_O = \frac{N}{2(1-D)}V_{in} \tag{3-6}$$

where D is the duty ratio of each main switch and N is the transformer secondary to primary turn ratio. Equ. (3-6) is an approximation of the relation between the output and

input voltages of the conventional isolated full-bridge boost converter [1], and it can be used for this analysis as the auxiliary circuit operates for only a small fraction of the converter switching cycle and thus have minimal effect on this relation. As a result of substituting equ. (3-6) into equations (3-4) and (3-5), these equations can be rewritten as

$$V_{Cr}(t) = \left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + (\frac{2D-1}{2-2D})V_{in}\right)\cos\omega\,(t - t_0) + V_{in} \tag{3-7}$$

$$i_{Lr}(t) = \sqrt{\frac{C_r}{L_r}}\left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + (\frac{2D-1}{2-2D})V_{in}\right)\sin\omega\,(t - t_0) \tag{3-8}$$

Since the snubber capacitor voltage V_{Cr} reaches $\frac{V_O}{N}$ at the end of Mode 1, at time $t = t_1$ so that

$$V_{Cr}(t_1) = \frac{V_o}{N} \tag{3-9}$$

equ. (3-7) can be written as

$$\frac{V_O}{N} = \left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + (\frac{2D-1}{2-2D})V_{in}\right)\cos\ \omega\,(\mathrm{t_1} - \mathrm{t_0}) + V_{in} \tag{3-10}$$

By substituting $\frac{V_O}{N}$ and equ. (3-6) into equ. (3-10), the following equation that expresses the duration of time for Mode 1, $\mathrm{t_1} - \mathrm{t_0}$ can be written as

$$\mathrm{t_1} - \mathrm{t_0} = \sqrt{L_r C_r}\cos^{-1}\frac{1}{1+\frac{I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}}}{(\frac{2D-1}{2-2D})V_{in}}} \tag{3-11}$$

The initial value of i_{Lr} for the next mode can be found from equ. (3-8) at time $\mathrm{t_1}$ to be

$$i_{Lr}(t_1) = \sqrt{\frac{C_r}{L_r}}\left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + (\frac{2D-1}{2-2D})V_{in}\right)\sin\omega\,(\,\mathrm{t_1} - \mathrm{t_0}) \tag{3-12}$$

Substituting equ. (3-11) into (3-12) gives the following equation for $i_{Lr}(t_1)$:

$$i_{Lr}(t_1) = \sqrt{\frac{C_r}{L_r} \times \ I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} \times \left(I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} + \left(\frac{2D-1}{1-D}\right) V_{in}\right)} = \alpha \tag{3-13}$$

$i_{Lr}(t_1)$ henceforth will be referred to as α to simplify the expression of Mode 2 equations.

Mode 2

In this mode, diode D_1 becomes forward biased and current is diverted from the main bridge switches. The equivalent circuit diagram for this mode is shown in Fig. 3.4. The output capacitors of switches S_2 and S_3 have the same voltage as capacitor C_r at the beginning of this mode, $V_{Cr}(t_1) = \frac{V_o}{N}$, therefore the primary side of the converter can be simplified to the circuit shown in Fig. 3.5 where $C_{tot} = C_r + 2C_S$.

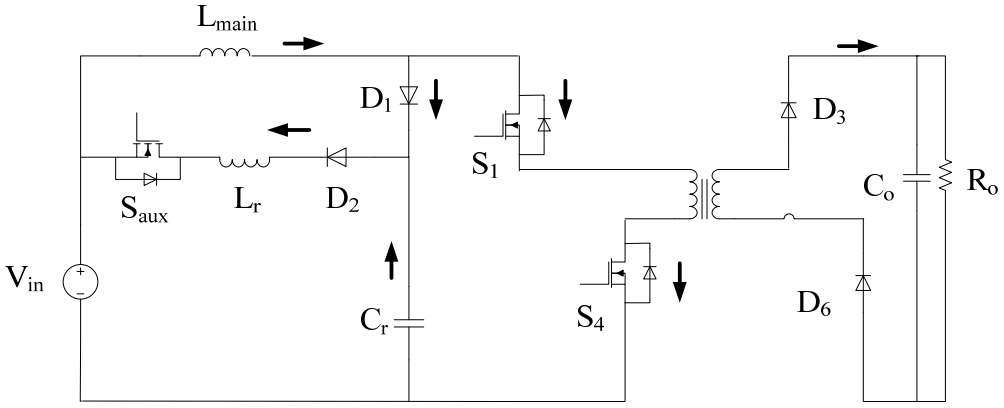


Fig. 3.4. Mode 2 of converter operation

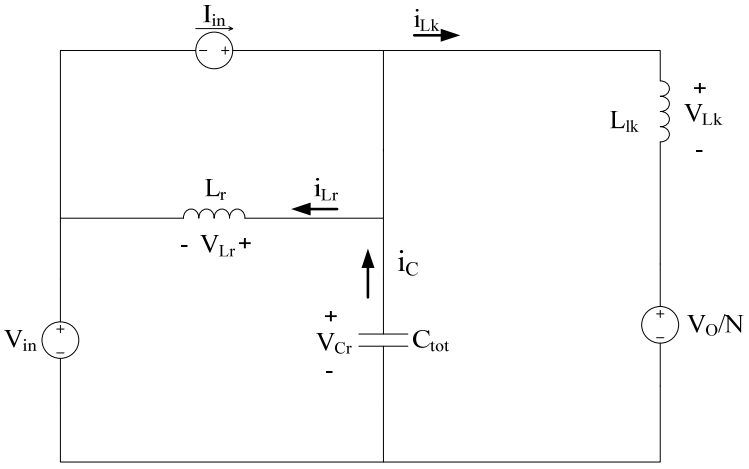


Fig. 3.5. Simplified equivalent circuit of mode 2 for $t_1 \leq t < t_2$

By applying KVL and KCL to the circuit shown in Fig. 3.5, the following equations can be derived:

$$I_{in} + i_C - i_{Lr} - i_{Lk} = 0 \tag{3-14}$$

$$V_{Cr} - V_{Lr} - V_{in} = 0 \tag{3-15}$$

$$\frac{V_o}{N} + V_{Lk} - V_{Cr} = 0 \tag{3-16}$$

These equations can be solved to give the following functions for the components:

$$V_{Cr}(t) = V_{in}\left[\frac{1}{2(1-D)} - \frac{L_{lk}+\frac{L_r}{2(1-D)}}{L_r+L_{lk}}\right]\cos\omega_1(t - t_1) - \frac{\alpha}{\omega_1 C_{tot}}\sin\omega_1(t - t_1) + V_{in} \times \frac{L_{lk}+\frac{L_r}{2(1-D)}}{L_r+L_{lk}} \tag{3-17}$$

$$i_{Lr}(t) = \frac{V_{in}}{L_r\omega_1}\left[\frac{1}{2(1-D)} - \frac{L_{lk}+\frac{L_r}{2(1-D)}}{L_r+L_{lk}}\right]\sin\omega_1(t - t_1) + \frac{\alpha}{L_r{\omega_1}^2 C_{tot}}\cos\omega_1(t - t_1) + \frac{V_{in}}{L_r+L_{lk}}\left(\frac{2D-1}{2-2D}\right)(t - t_1) - \frac{\alpha}{L_r{\omega_1}^2 C_{tot}} + \alpha \tag{3-18}$$

$$i_{Lk}(t) = \frac{V_{in}}{L_{lk}\omega_1}\left[\frac{1}{2(1-D)} - \frac{L_{lk}+\frac{L_r}{2(1-D)}}{L_r+L_{lk}}\right]\sin\omega_1(t-\ t_1) + \frac{\alpha}{L_{lk}{\omega_1}^2 C_{tot}}\cos\omega_1(t-\ t_1) -$$
$$\frac{V_{in}}{L_r+L_{lk}}\left(\frac{2D-1}{2-2D}\right)(t-\ t_1) - \frac{\alpha}{L_{lk}{\omega_1}^2 C_{tot}} + I_{in} \quad (3\text{-}19)$$

where $t_1 \le t < t_2$,

$$\omega_1 = \sqrt{\frac{1}{C_{tot}}\left(\frac{1}{L_r}+\frac{1}{L_{lk}}\right)} \quad (3\text{-}20)$$

and initial value conditions:

$$i_{Lr}(t_1) = \alpha \quad (3\text{-}21\text{-a})$$

$$V_{Cr}(t_1) = \frac{V_O}{N} = \frac{V_{in}}{2(1-D)} \quad (3\text{-}21\text{-b})$$

$$i_{Lk}(t_1) = I_{in} \quad (3\text{-}21\text{-c})$$

At the end of this mode, current in the transformer reaches zero. Due to the complexity of the above modal equations, a closed form equation for the length of time $(t_2 - t_1)$ required for the current in the leakage inductance to fall to zero $i_{Lk}(t_2) = 0$ is difficult to derive. As a result, this time will be determined by the computer program described at the start of Section 3.2.

Mode 3

At the start of this mode, the transformer primary current is zero and thus the equivalent circuit of the transformer primary side of the converter can be the one shown in Fig. 3.6, with initial values of I_0 for the inductor current and V_0 for the capacitor voltage.

Using KVL and KCL, the following equations can be derived:

$$V_{Cr} - V_{Lr} - V_{in} = 0 \quad (3\text{-}22)$$

$$I_{in} + i_C - i_{Lr} = 0 \quad (3\text{-}23)$$

By solving these equations, the following expressions for the snubber capacitor voltage $V_{Cr}(t)$ and the auxiliary circuit inductor $i_{Lr}(t)$ can be determined:

$$V_{Cr}(t) = (V_0 - V_{in})\cos\omega_2(t - t_2) + \left(\frac{I_{in} - I_0}{C_{tot}\omega_2}\right)\sin\omega_2(t - t_2) + V_{in} \qquad (3\text{-}24)$$

$$i_{Lr}(t) = C_{tot}\omega_2(V_0 - V_{in})\sin\omega_2(t - t_2) + (I_0 - I_{in})\cos\omega_2(t - t_2) + I_{in} \qquad (3\text{-}25)$$

where $\omega_2 = \frac{1}{\sqrt{L_r C_{tot}}}$ and $t_2 < t < t_3$. As with Mode 2, the length of this mode can be calculated by the computer program by determining the (t_3 - t_2) time required for V_{Cr} to fall to zero.

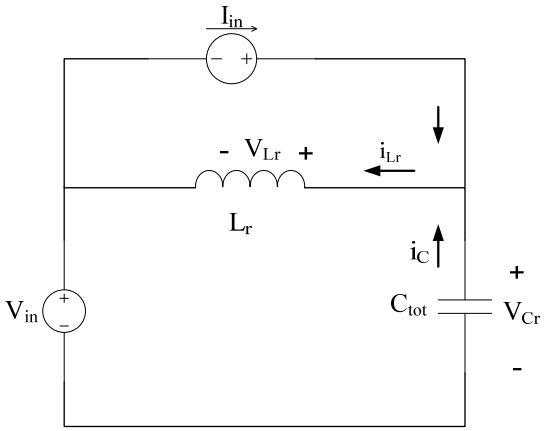


Fig. 3.6. Equivalent circuit of Mode 3 for $t_2 \leq t < t_3$

Mode 4

During this mode, the voltage across C_{tot}, V_{Cr}, is always zero and the voltage across the auxiliary circuit inductor is constant and equal to $-V_{in}$ as one end of the inductor is connected to the V_{in} input source through S_{aux} and the other end is connected to C_r (and thus 0 V) through D_2. The auxiliary circuit inductor voltage can be expressed as

$$-V_{in} = L_r \frac{di_{Lr}}{dt} \qquad (3\text{-}26)$$

By solving equ. (3-26), $i_{Lr}(t)$ can be derived:

$$i_{Lr}(t) = -\frac{V_{in}}{L_r}(t - t_3) + I_{02} \tag{3-27}$$

with the initial value of $i_{Lr}(t_3) = I_{02}$ and $t_3 < t < t_4$

Thus current linearly decreases in the auxiliary branch. From KCL, the total current flowing through bridge switches equals $I_{in} - i_{Lr}$; therefore, current in each main switch, i_S, can be written as:

$$i_S = \frac{I_{in} - i_{Lr}}{2} \tag{3-28}$$

Since $I_{in} < i_{Lr}$ in this mode, this current is considered to be negative as current is flowing through the body-diodes of the switches (Fig. 3.7).

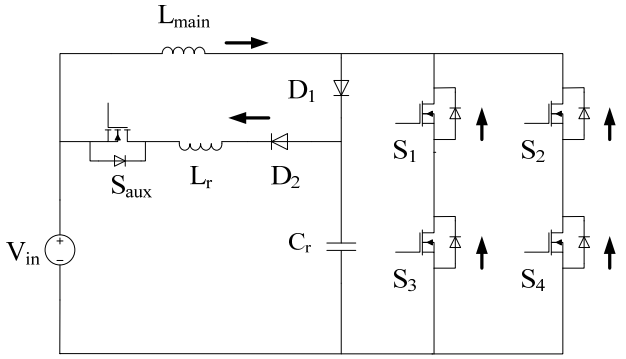


Fig. 3.7. Current flow in Mode 4

Mode 5

The only difference between this mode and Mode 4 is that current reverses in the bridge switches as shown in Fig. 3.8. The voltage across capacitor C_r stays clamped at zero as all full-bridge switches are on and the DC bus is shorted, and equations (3-26) and (3-28) that were derived for the previous mode are also valid for this mode. Equ. (3-27) can be rewritten as:

$$i_{Lr}(t) = -\frac{V_{in}}{L_r}(t - t_4) + I_{03} \tag{3-29}$$

with the initial value of $i_{Lr}(t_4) = I_{03}$ and $t_4 < t < t_5$.

At the end of this mode, the current through L_r, i_{Lr}, reaches zero and the auxiliary circuit is inactive.

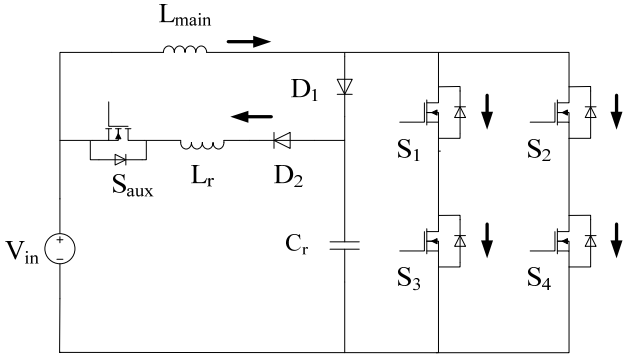


Fig. 3.8. Mode 5 equivalent circuit diagram

Mode 6

During this mode of operation, the converter is in a boosting mode as shown in Fig. 3.9 as all bridge switches are on, and the input current flows through the main switches, and the auxiliary circuit is inactive. The input inductor is magnetized according to following equation:

$$V_{in} = L_{main}\frac{di_{Lm}}{dt} \tag{3-30}$$

The auxiliary switch can turn off at anytime during this mode with zero-current switching. After the switch is turned off, the output capacitance in parallel with the auxiliary switch cannot be charged due to the blocking diode D_2; therefore voltage across this switch stays at zero until the start of the next mode. The duration of this mode is determined by the converter's duty cycle.

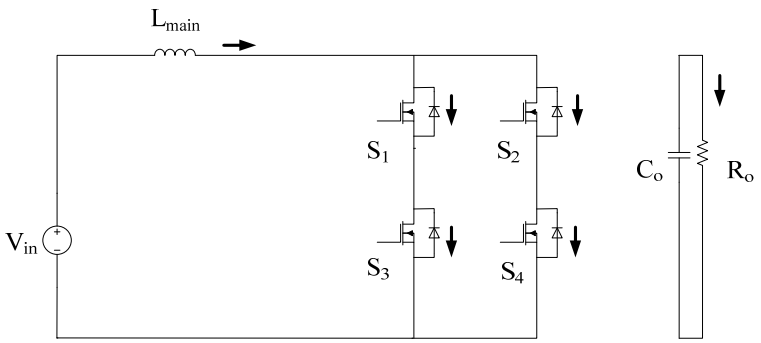


Fig. 3.9. Mode 6 of converter operation

Mode 7

This mode begins when a pair of diagonally opposed switches, S_1 and S_4, are turned off. The equivalent circuit of this mode is shown in Fig. 3.10. In this mode, the full input inductor current flows through capacitor C_r and the output capacitances of switches S_1 and S_4 (not shown in the figure) and no power is delivered to the output through the full-bridge switches.

As current flows through the auxiliary circuit, an equation is needed to define V_{Cr} (no such equation is needed for i_{Lr} because S_{aux} is off). Such an equation can be written as

$$C_{tot}\frac{dV_{Cr}}{dt} = I_{in} \tag{3-31}$$

where $C_{tot} = C_r + 2C_S$, $V_C(t_6)=0$ and $t_6 < t < t_7$. Rearranging this equation gives

$$V_{Cr}(t) = \frac{I_{in}}{C_{tot}}(t - t_6) \tag{3-32}$$

where V_{Cr} is the same as the voltage across switches S_1 and S_4. At the end of this mode, V_{Cr} reaches $\frac{V_O}{N}$, which makes the output bridge diodes D_4 and D_5 forward biased so that they can conduct current. This allows power to be transferred through them to the output.

It should be noted that the voltage across diode D_2 is V_{in}-V_{Cr}. After V_{Cr} is charged to the level of the input voltage, diode D_2 becomes forward biased and the output capacitance of the auxiliary switch voltage begins to charge. Since the capacitance is small compared to that of C_{tot}, this capacitance has been ignored in equations (3-31) and (3-32). At the end of this mode, the voltage across S_{aux}, V_{aux} is equal to

$$V_{aux} = V_{Cr} - V_{in} \tag{3-33}$$

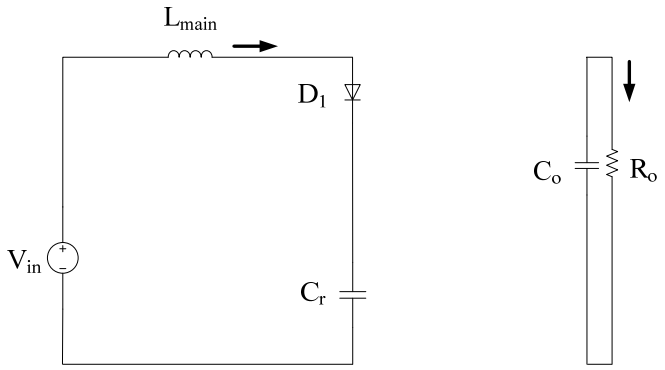


Fig. 3.10. Flow of current in mode 7 ($t_6 \leq t < t_7$)

Mode 8

During this mode, the main inductor current is gradually diverted from the snubber capacitor C_r to the transformer. While this transition is happening, input inductor current continues to charge C_r so that V_{Cr} begins to exceed $\frac{V_O}{N}$, which results in voltage overshoots appearing across switches S_1 and S_4. The amount of voltage overshoot across each switch can be determined using the equivalent circuit shown in Fig. 3.11.

According to Fig. 3.11, the following equations can be derived by using KCL and KVL

$$i_C + i_{Lk} = I_{in} \tag{3-34}$$

$$V_{Cr} - V_{Lk} - \frac{V_O}{N} = 0 \tag{3-35}$$

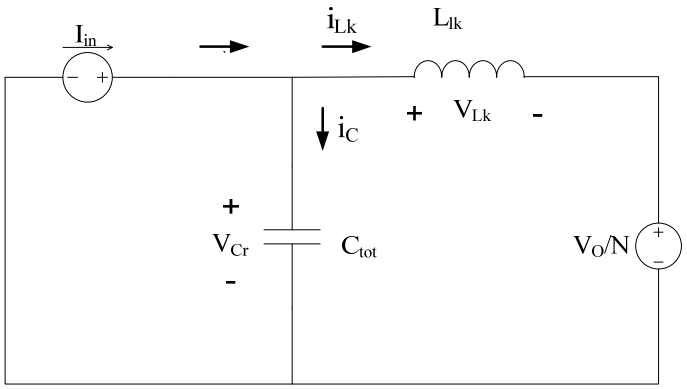


Fig. 3.11. Equivalent circuit of mode 8 ($t_7 \leq t < t_8$)

where $V_{Cr}(t_7) = \frac{V_O}{N}$ and $i_{Lk}(t_7) = 0$. By solving the equations of (3-34) and (3-35), the following expression for $V_{Cr}(t)$ can be derived.

$$V_{Cr}(t) = \frac{I_{in}}{C\omega_3} \sin \omega_3 (t - t_7) + \frac{V_O}{N} \tag{3-36}$$

where $\omega_3 = \frac{1}{\sqrt{L_{lk} C_{tot}}}$ and $C_{tot} = C_r + 2C_S$. From equ. (3-36), it can be seen that the voltage overshoot of C_r, S_1 and S_4 is

$$\Delta V_{pk} = I_{in} \sqrt{\frac{L_{lk}}{C_{tot}}} \tag{3-37}$$

so that the initial value of the snubber capacitor voltage for next mode is the maximum of V_{Cr} in equ. (3-36):

$$V_{cr,max} = I_{in} \sqrt{\frac{L_{lk}}{C_{tot}}} + \frac{V_O}{N} \tag{3-38}$$

Mode 9

During this mode, the converter is in an energy-transfer mode as switches S_2 and S_3 are conducting current, power is transferred from the input to the output, and the current in

L_{main} falls (Fig. 3.12). The transformer's leakage inductance continues to resonate with the output capacitors of the main switches at the beginning of this mode, but this resonance eventually dies down due to parasitic resistances in the converter. From a mathematical point of view, it will be assumed that voltage across the full-bridge switches eventually settles to $\frac{V_O}{N}$ sometime during this mode.

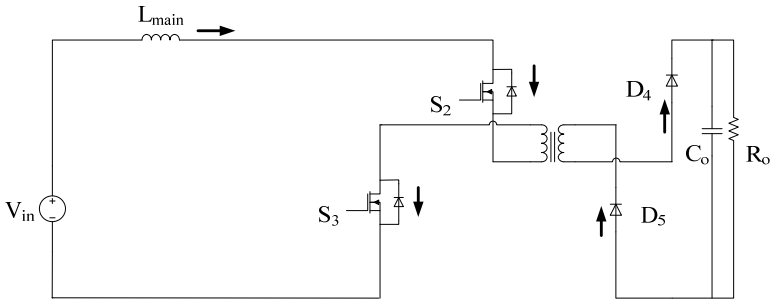


Fig. 3.12. Mode 9 of converter operation

3.3. Conclusion

In this chapter, a mathematical analysis of the modes of operation that were described in Chapter 2 was performed to derive key equations that are needed to understand the steady-state behavior of the converter, relative to the values of certain key components. These relations will be used to develop a design procedure for the proposed converter in the next chapter of this thesis.

Chapter 4

Design Procedure

4.1. Introduction

In this chapter, a procedure for the design of certain key converter parameters is presented and is demonstrated with an example. The design procedure uses the modal equations that were derived in the previous chapter and also uses graphs of steady-state relations that are based on these equations. The results of the design example were used in the implementation of an experimental prototype from which results were obtained. These results will be presented in the next chapter of this thesis.

4.2. Design Example

The design of the proposed full-bridge boost converter (Fig. 4.1) is explained with an example in this section to show the systematic design procedure for the converter. The following specifications are considered for this design:

Output Voltage:	$V_O = 300$ Volts
Output Power:	$P_O = 500$ Watts
Input Voltage:	$V_{in} = 100$ Volts
Expected efficiency at full-load	$\eta = 93$ %
Switching Frequency:	$f = 50$ KHz

The design procedure presented is iterative and requires several iterations, both theoretical and experimental, before the final design can be achieved. The general approach that is taken in the procedure is to first design the converter as a conventional

hard-switched converter without the auxiliary circuit, then to design the auxiliary circuit, and finally to confirm the design of the converter.

Equations (3-7) to (3-27) can be used to generate graphs of steady-state characteristic curves for this converter. A flowchart is shown in Appendix A of this thesis to demonstrate the procedure of creating steady-state characteristic graphs. The graphs can be generated by a computer program such as MATLAB.

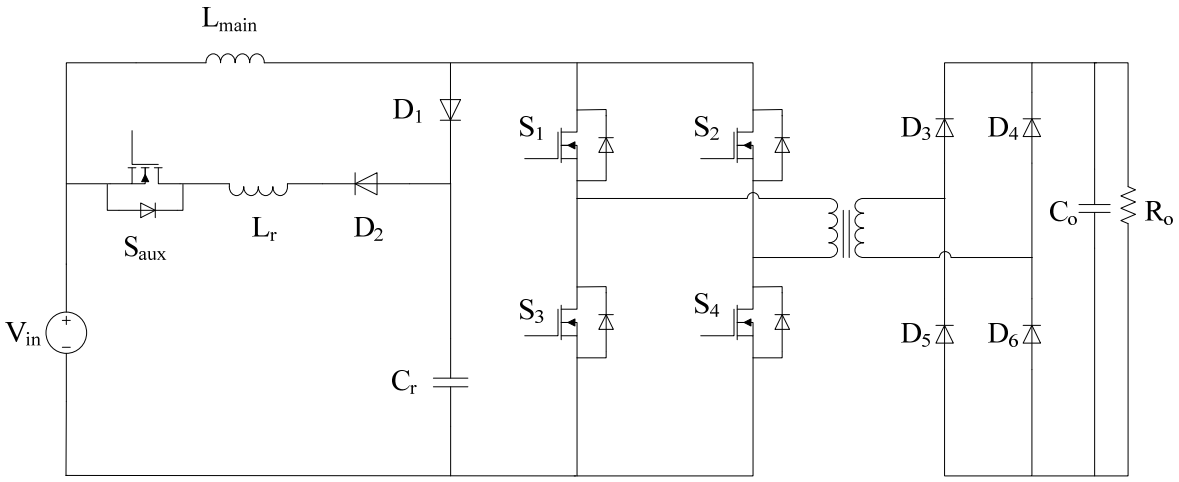


Fig. 4.1. Proposed current-fed full-bridge boost converter

4.2.1. Transformer Turns Ratio

The turns ratio of the transformer can be considered to be the most critical converter parameter as all other parameters are ultimately dependent on this one. The turns ratio, N, affects the converter's duty cycle range, which affects the selection of an input inductor value and an output capacitor value. An appropriate value of N can only be determined after several iterations; once this has been done, then the rest of the converter parameters should be designed on based on this value, and some sort of verification or "check" should be performed at the end to confirm the validity of the design.

If the input inductor current is continuous, then the relation between the output voltage V_O and the input voltage V_{in} can be expressed by the following equation, which is based on the operation of a conventional single-switch boost converter:

$$V_O = \frac{N}{1-D_c} V_{in} \tag{4-1}$$

Since there must always be a path for current to flow through in the converter, each switch must be on for at least a switch duty-cycle of D = T/2. The converter duty cycle D_c is based on the amount of overlap between the gating signals of S_1 and S_4 and those of S_2 and S_3 so that the relation between D and D_c can be expressed as

$$DT = D_c \frac{T}{2} + \frac{T}{2} \tag{4-2}$$

where D_cT represents the amount of time that there is overlap in the two pairs of gating signals (i.e. all the switches are on) during a switching cycle. Since there are two times during a switching cycle when all the converter switches are on, the term $D_c \frac{T}{2}$ is used in (4-2).

If (4-2) is substituted into (4-1), then the following equation can be derived:

$$V_O = \frac{N}{2(1-D)} V_{in} \tag{4-3}$$

and also (4-2) can be rearranged to give

$$D_c = 2D - 1 \tag{4-4}$$

For this design example, a value of N = 1, which was determined from the previous iteration will be used and the converter will be designed based on this value. With this value of N and, assuming that the input inductor current is continuous, a value of D = 0.83 can be determined as shown, based on input voltage V_{in} = 100 V and

V_O = 300 V. If D = 0.83, then D_c = 0.66 from (4-4); this value of D_c will be used in next sections to find the input inductor and the output capacitor values.

4.2.2. Input Inductor

With values of N and D determined, the design of the rest of the hard-switching converter can proceed, beginning with the input inductor in this section and the output capacitor in the next section. The main consideration to design the input inductor in an isolated full-bridge DC-DC boost PWM converter is to limit the peak-to-peak ripple of the current flowing through the inductor. There is, however, a compromise that should be considered in selecting the inductor value. If L_{main} is too large then the peak-to-peak ripple of the current will be small, but the physical size of the inductor will increase significantly, as will the size and weight of the converter. If L_{main} is too small then so too will be the physical size of the inductor, but the peak-to-peak ripple of the inductor current will be large. A 10% peak-to-peak ripple to average current ratio is a compromise that is typically made [1] and is used in this example design.

The converter operates with continuous input current. The average input current (input current without the ripple) can be found from the converter specifications:

$$I_{in} = \frac{P_O}{V_{in} \times \eta} = \frac{500}{100 \times 093} \approx 5.4 \quad \text{Amps} \tag{4-5}$$

It should be noted that the auxiliary circuit injects some current back into the input source during Modes 1-5 of operation so that the value of I_{in} when the converter has the auxiliary circuit will be different than the value of I_{in} when the converter is not operating with the auxiliary circuit. Since the average value of this current is small compared to the input current, it can be considered to be negligible compared to the average inductor current value and is thus not considered in calculating average inductor current in equ. (4-5) for the sake of simplicity.

Since the average inductor current value has been determined and it has been stated that the input inductor value should be such that the peak-to-peak ripple ΔI of the input inductor current should be 10% of the average input inductor current, then ΔI should be

$$\Delta I = 0.1 \times I_{in} = 0.54 \text{ Amps} \tag{4-6}$$

A relation between L_{main} and ΔI exists as the voltage across the input inductor when the converter is in a boosting mode and all switches are on can be expressed as

$$V_{in} = L_{main} \frac{di}{dt} \tag{4-7}$$

where V_{in} is the voltage across L_{main} when switches $S_{1,4}$ and $S_{2,3}$ are conducing. $dt = D_c \frac{T}{2}$ is the duration of the boosting mode in a half switching cycle and di = ΔI is the change in input current during that time.

The value of L_{main} , therefore, can be determined by rearranging equ. (4-7) to get

$$L_{main} = V_{in} \frac{D_c T}{2\Delta I} = 100 \times \frac{0.66 \times 20\mu s}{2 \times 0.54} = 1.22\ mH \tag{4-8}$$

4.2.3. Output Capacitor

The minimum value of the output capacitor can be determined from equ. (4-9) given in [1]:

$$C_o > \frac{D_c}{R f_o (\frac{\Delta V_o}{V_o})} \tag{4-9}$$

where D_c is the converter duty ratio determined in equ. (4-4), R is the output resistance at maximum load ($V_o^2/P_{o,max}$), f_o is the output voltage ripple frequency which is twice the switching frequency and $\frac{\Delta V_o}{V_o}$ is the percentage of peak-to-peak output voltage ripple. By assuming a 0.1 % peak-to-peak output voltage ripple, which is considered to be

acceptable for many converter applications and substituting $D_c = 0.66$, $f_o = 100$ kHz and $R = 180\ \Omega$, C_o is found to be:

$$C_o > \frac{D_c}{Rf_o(\frac{\Delta V_o}{V_o})} = \frac{0.66}{180 \times 100k \times 0.001} = 36.7\ \mu F$$

4.2.4. Snubber Capacitor

With the design of the hard-switching converter parameters N, D, L_{main} and C_o done, the next step is to consider the design of the auxiliary circuit. The first step in doing so is to consider the selection of a value for snubber capacitor C_r as the design of the other auxiliary circuit parameters are dependent on this value.

The value of C_r should be as small as possible to minimize the amount of energy that is ultimately transferred to the input after it is discharged. It should also be small to minimize the amount of time that the auxiliary circuit is in the circuit, to minimize the effect that it may have on the general operation of the converter (larger C_r means more time is needed by the auxiliary circuit to discharge it). On the other hand, however, C_r should be large enough to decrease the rate of the voltage rise across the main switches during Mode 7 in order to obtain a ZVS turn-off for the main switches and to prevent voltage spikes from appearing across the switches when they are turned off, as much as possible.

One measure of the amount of energy that is processed by the auxiliary circuit is the rms value of the current that flows through it during a switching cycle. With this in mind, a graph of auxiliary circuit rms current vs. % voltage overshoot such as the one shown in Fig. 4.2 can be generated using a MATLAB program like the one presented code in Appendix B. This graph was generated using equ. (3-37), which is reproduced here

$$\Delta V_{pk} = I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} \qquad (4\text{-}10)$$

It should be noted that voltage overshoot is dependent on the transformer leakage inductance, as shown in the description of Mode 8 of converter operation that was presented in Section 3.2. The higher the leakage inductance of the transformer is, the more voltage overshoot can appear across the main full-bridge switches. Leakage inductance, however, cannot be eliminated as it is an inherent part of any transformer. The leakage inductance of the transformer that was used in the experimental prototype was L_{lk} = 765nH.

The graph in Fig. 4.2 shows that overshoot levels higher than 20% do not have significant effect on reduction of auxiliary circuit rms current. An overshoot of 20%, therefore, is selected for this design example, and from equ. (4-10):

$$I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} = 0.2 \times \frac{V_O}{N}$$

$$\Rightarrow \quad C_{tot} = 6.2 \text{ nF}$$

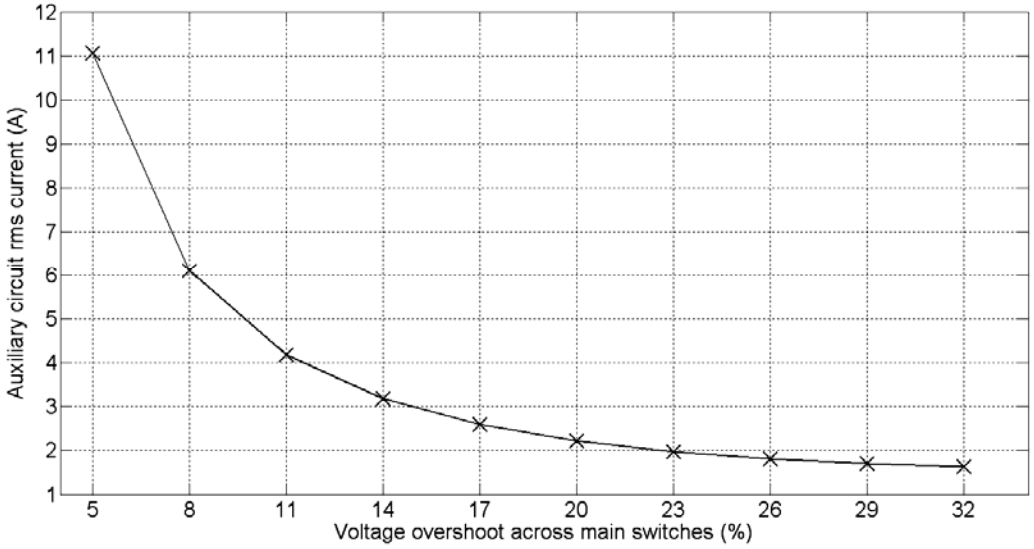


Fig. 4.2. Voltage overshoots of main switches versus auxiliary circuit rms current

According to the equation $C_{tot} = C_r + 2C_S$ where C_s is the output capacitance of a main switch. If it is assumed, based on previous iterations that IXFH52N50P2 MOSFET devices, which have an output drain-source capacitance of about 600 pF, are used as the main power switches, then the required C_r is found to be 5 nF.

4.2.5. Auxiliary inductor

Since the auxiliary switch operates with soft switching, the main concern in selecting the auxiliary inductor is to minimize the amount of rms current that flows in the auxiliary circuit (an indication of the amount of energy that is processed by the auxiliary circuit) and the peak current stress on the devices in the auxiliary circuit. An appropriate auxiliary inductor value can be selected using graphs such as the ones shown in Figs. 4.3 and 4.4.

The graph shown in Fig. 4.3 is a graph of auxiliary switch peak current vs auxiliary circuit inductor value and the graph shown in Fig. 4.4 is a graph of auxiliary switch rms current vs auxiliary circuit inductor value. These graphs were generated from the modal equations that were derived in Chapter 3 (most notably (3-8), (3-18), (3-25), (3-27) and (3-29)) and the MATLAB programs that are presented in Appendices C and D.

It can be seen from Figs. 4.3 and 4.4 that there is little change in the peak auxiliary switch current if the auxiliary circuit inductor L_r is greater than 7 μH, but that the rms current rises if L_r is greater than 7 μH. This is because the L_r current becomes flatter as L_r is increased, but it exists for a longer time as increasing L_r increases the resonant cycle between L_r and C_r. As a result, a value of L_r = 7 μH is chosen.

The validity of this value along with C_r will be confirmed in the next section as these values affect the converter's ability to operate with ZVS.

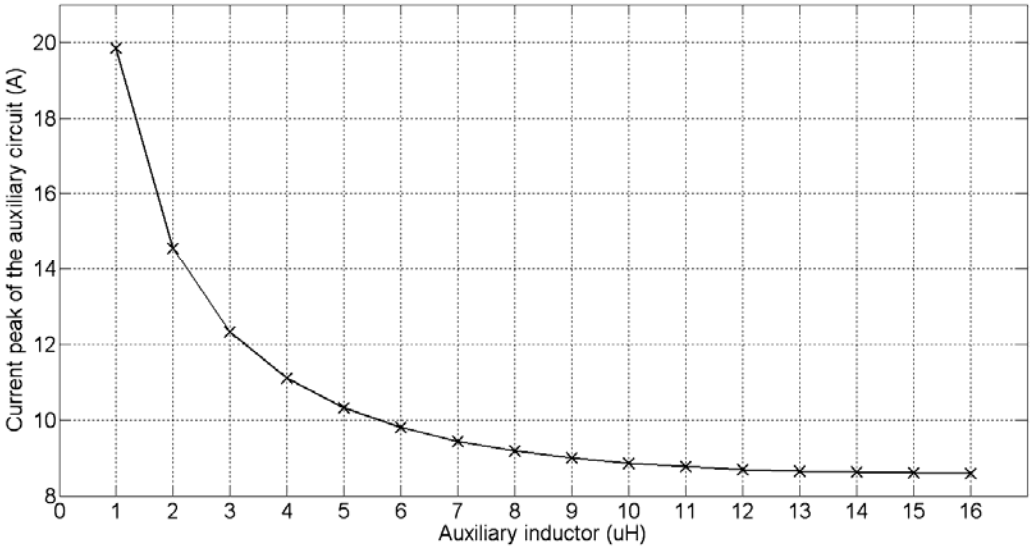


Fig. 4.3. Current peak of the auxiliary circuit

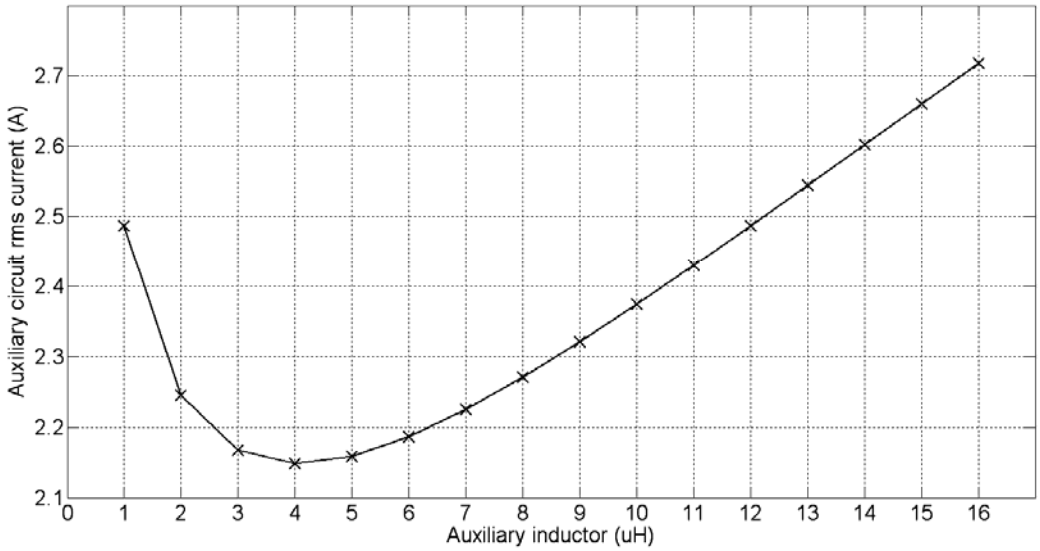


Fig. 4.4. rms of the auxiliary circuit current

4.2.6. Conditions for soft switching operation of the converter switches

In this section, the soft-switching operation of main and auxiliary switches is examined.

Due to the inductor in series with the auxiliary switch, this switch turns on softly and the current in the switch increases gradually. The auxiliary switch can be turned off with ZCS when there is no current flowing through the switch. Due to the nature of the auxiliary circuit in the converter and the fact that current flows through this circuit for only a small fraction of the switching cycle, there is no specific time window during which the auxiliary switch needs to be turned off so that it can do so with ZCS. As long as the auxiliary switch is turned off before a pair of main full-bridge switches is about to be turned off, then the auxiliary circuit will not interfere with the operation of the main full-bridge switches.

Due to the fact that the main power switches each have an output drain-source capacitance and the fact that C_r is present in the converter, the main power switches can turn off with ZVS as described above. As for the ZVS turn-on of the main switches, the snubber capacitor voltage V_{Cr} should reach zero at the end of Mode 3 of converter operation before a switch is turned on with ZVS; therefore from equ. (3-24) from Mode 3:

$$V_{Cr}(t) = (V_0 - V_{in})\cos\omega_2(t - t_2) + \left(\frac{I_{in} - I_0}{C_{tot}\omega_2}\right)\sin\omega_2(t - t_2) + V_{in} = 0 \qquad (4\text{-}11)$$

Since parameters such as ω_2 and C_{tot} and Vo are interrelated by $V_{in}, L_r, C_r, C_s, L_{lk}, I_{in}$ and D, equ. (4-11) can be rewritten as a function of D and this equation can be used to explore the converter's ZVS range with different values of D.

A graph of snubber capacitor voltage V_{Cr} vs time for different values of main switch duty cycle D is shown in Fig. 4.5, with the time axis starting from time t_2. The MATLAB program that was used to generate this graph is shown in Appendix E.

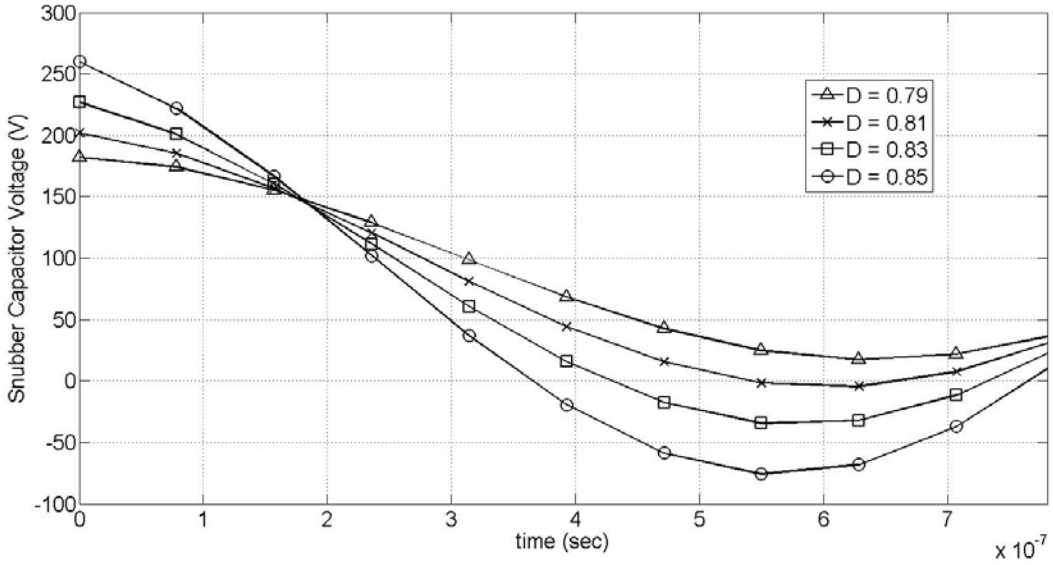


Fig. 4.5. Variation of the snubber capacitor voltage for different values of main switch duty cycle (D)

The ZVS time window (the amount of time during which a main power switch can be turned on with ZVS) is the interval that the snubber capacitor voltage is negative in Fig. 4.5. A main power switch will not turn on with ZVS unless its main switch duty cycle is at least D = 0.81 as it can be seen in Fig. 4.5. Since D was determined to be equal to 0.83 in previous steps, the main full-bridge switches can be turned on with ZVS.

4.2.7. Auxiliary and Main Switches

In order to select appropriate devices for the main full-bridge switches and the auxiliary switch, the following parameters should be considered:

- Switch rms current
- Peak current stress
- Peak voltage stress

The rms current flowing through a main power switch can be approximated by assuming that the input inductor current does not have any ripple and is thus equal to its average value. The rms current through the main switches at full-load is:

$$I_{rms} = \sqrt{\frac{1}{T}\int_{T} {i_S}^2} = \sqrt{\frac{1}{T}(2 \times \int_{D_c\frac{T}{2}} (\frac{I_{in}}{2})^2 + \int_{\frac{T}{2}-D_c\frac{T}{2}} {I_{in}}^2)} = I_{in} \times \sqrt{\left(\frac{1}{2} - \frac{D_c}{4}\right)} = 5.4 \times \sqrt{0.335}$$

$$\approx 3.1\ Amps$$

The peak current flowing through the bridge is the peak current in the main inductor. Using $I_{Lmain,avg} = 5.4$ and $\Delta I = 0.54$ from section 4.2.3, the peak switch current can be found to be

$$I_{Lmain,p} = I_{Lmain,avg} + 0.5\Delta I = 5.4 + 0.5 \times 0.54 = 5.67\ \ Amps$$

The maximum voltage across the main switches can be determined by considering an overshoot of 20% and by using equ. (3-38); this voltage is

$$V_{S1-4,max} = \frac{V_O}{N} + \ \ I_{in}\sqrt{\frac{L_{lk}}{C_{tot}}} = 360\ \ Volts$$

Based on the above considerations, IXFH52N50P2 MOSFETs can be selected for the main power switches. These devices have an output capacitance of 600 pF and since C_r was selected with this value in mind, no modification needs to be considered for C_r.

The rms and peak current through the auxiliary switch were determined from section 4.2.5 to be 2.22 and 9.45 Amps respectively.

The snubber capacitor C_r charges up to 360 volts as there is a voltage overshoot of 60 V across the main switches, as determined in Section 4.2.4; thus the maximum voltage across the auxiliary switch, which happens at Mode 0 is:

$$V_{saux,max} = V_{cr,max} - V_{in} = 360 - 100 = 260\ \ Volts$$

Based on the above considerations, a FCA36N60NF MOSFET can be selected for the auxiliary switch. These devices have an output capacitance of 140 pF, which is lower than that of the main power switches, and thus can turn-on with fewer losses than the main power switches could if they did not operate with ZVS.

The same current as that of the main switches flows through the output diodes; therefore they should have the same current ratings. The output diodes block output voltage which is designed to be 300 V. Due to these specifications, BYV29-500 devices are used for output diodes $D_{3\text{-}6}$.

Diode D_2 is in series with the auxiliary switch and has the same current ratings. This diode is exposed to its maximum voltage stress during Mode 3, when one end is connected to the input source and the other end is grounded. Based on these observations, a BYV29-300 device is selected for Diode D_2.

Diode D_1 prevents the snubber capacitor from discharging during power transfer modes. The maximum reverse voltage across this diode during these modes is 120 V (twice the main switches' voltage overshoot). This diode conducts when the auxiliary switch is activated to divert current from the bridge switches; therefore the average current flowing through this diode is less than the main inductor current. A BYV29-300 device is also selected for Diode D_2 to provide these specifications.

With the selection of appropriate devices for the main switches and the auxiliary switch, the steady-state design of the converter is complete.

4.3. Conclusion

In this chapter, a procedure for the design of certain key converter parameters was presented and was demonstrated with an example. The design procedure, which was iterative, used the modal equations that were derived in the previous chapter and also used graphs of steady-state relations that were based on these equations. As part of the

design procedure, MATLAB programs were used to generate the graphs and to solve equations. Key converter parameters that were considered in the design included the values of the input inductor, auxiliary circuit inductor and auxiliary circuit capacitor. The results of the design example were used in the implementation of an experimental prototype from which results were obtained. These results will be presented in the next chapter of this thesis.

Chapter 5

Simulation and Experimental Results

5.1. Introduction

Experimental and simulation results obtained from a prototype of the proposed ZVS PWM full-bridge DC-DC boost converter are presented in this chapter to confirm the feasibility of the converter. The converter was implemented based on the design considerations explained in previous chapter. In this chapter, typical converter waveforms are presented and the converter's efficiency is compared to that of a hard-switching converter of the same type to demonstrate efficiency improvement in the proposed converter.

5.2. Simulation and Experimental Results

The feasibility of the proposed ZVS PWM DC-DC boost converter was verified with PSIM (a commercially available software package dedicated for power electronic converter simulations [27]) and with an experimental prototype converter that was designed based on the following specifications:

Output Voltage:	V_O = 300 Volts
Output Power:	P_O = 500 Watts
Input Voltage:	V_{in} = 100 Volts
Switching Frequency:	f = 50 kHz

The prototype was implemented with the component values that were determined from the design example discussed in the previous chapter. The following components were used to implement the prototype of the proposed boost converter:

- Main bridge switches $S_{1\text{-}4}$: IXFH52N50P2
- Auxiliary switch S_{aux}: FCA36N60NF
- Diode D_1: BYV29-300
- Diode D_2: BYV29-300
- Output Diodes $D_{3\text{-}6}$: BYV29-500
- Auxiliary inductor L_r: 7 µH
- Input inductor L_{main}: 750 µH
- Resonant capacitor C_r: 5 nF
- Transformer turns ratio: 1:1
- Output capacitor: 220 µF

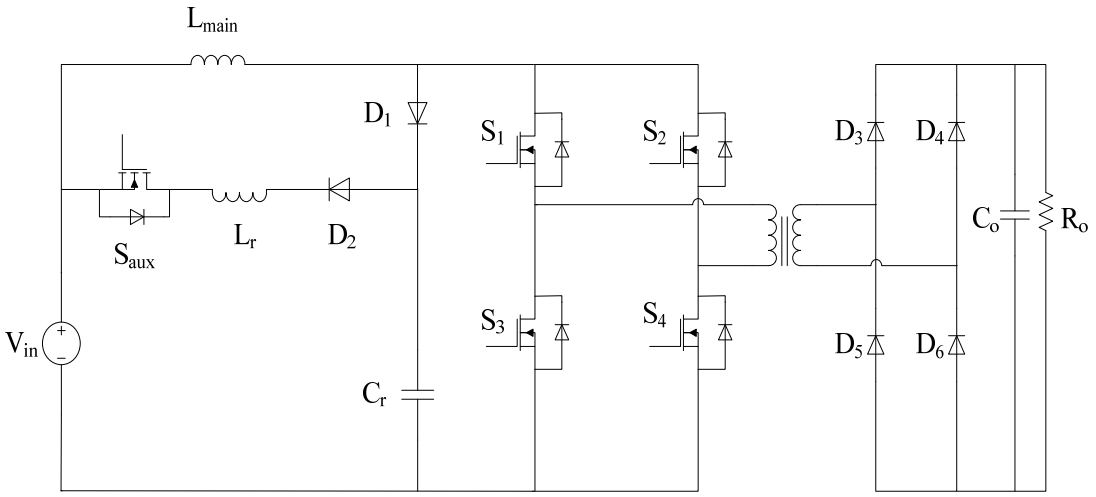


Fig. 5.1. Proposed boost converter

The ZVS operation of one of the main full-bridge switches during turn-on and turn-off are shown in Fig. 5.2 and Fig. 5.3. Typical auxiliary switch S_{aux} voltage and current waveforms are shown in Fig. 5.4 to demonstrate that this switch can turn on and off with ZCS. Gate pulse signals of the main and auxiliary switches are shown in Fig. 5.5. The input current (current flowing out of the input voltage source) is shown in Fig. 5.6 and voltage and current waveforms for the power transformer are shown in Fig. 5.7. All the waveforms presented in this chapter were taken with the converter operating at maximum load.

The following observations can be made from the waveforms presented in Fig. 5.2 - 5.7:

I. It can be seen from Fig. 5.2 that the drain-source voltage across a main switch MOSFET falls to zero before it is turned on (as indicated by the rising gate pulse). The decrease of the drain-source voltage is due to the operation of the auxiliary circuit, which discharges the output capacitance of the switch after it is activated. Since the voltage across the switch is zero before it is turned on, the waveform shows that it can be turned on with ZVS.

II. It can be seen from Fig. 5.3 that a main full-bridge switch can be turned off with ZVS. This can be seen by the fact that the drain-source voltage rises gradually after the switch's gate pulse signal has been removed. It should be noted that the voltage overshoot and ringing in the waveforms is caused by the resonance between the transformer leakage inductance and the main switches output capacitances.

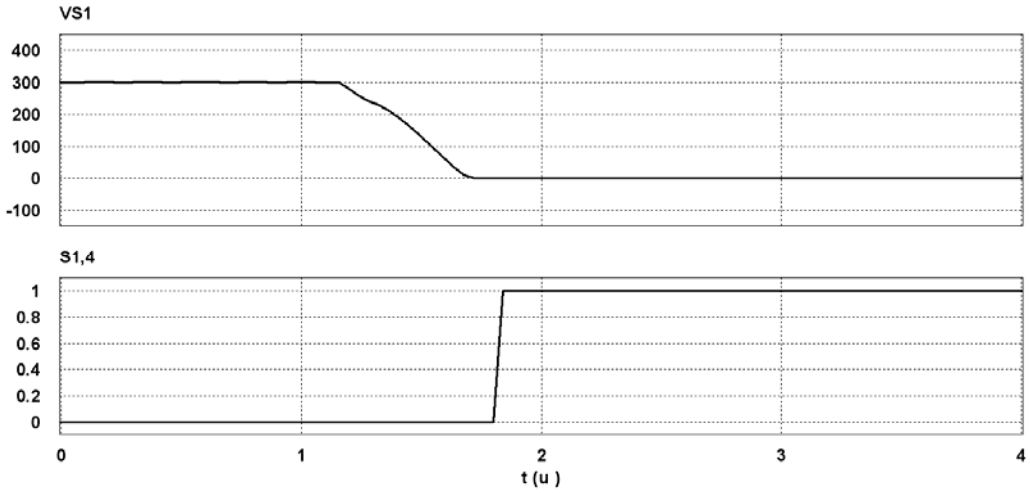
III. It can be seen from Fig. 5.4 that the auxiliary switch can turn on with ZCS. This can be seen by the fact that when the switch is turned on (as indicated by the drain-source voltage falling to zero), the current does not rise suddenly, but does so gradually. As a result, there is little overlap between switch voltage and current after the switch is turned on, and thus there are few turn-on switching losses.

IV. Fig. 5.5 shows the gating signals for all the converter switches. The top gating signal is that for the diagonally opposed switch pair S_1 and S_4. The middle gating signal is that for the diagonally opposed switch pair S_2 and S_3. The bottom gating signal is that for the auxiliary switch, S_{aux}. From these waveforms, the following can be seen: (a) The width of the auxiliary switch gating pulses is only a fraction of the width of the main switch gating pulses. This is because the auxiliary circuit needs to be active only during the time that a main switch is turned on, and then only for a short duration. (b) The frequency of the auxiliary switch gating signal is twice that of the gating signals of the other switches. This is because the auxiliary circuit is activated when the S_1 and S_4 pair of switches is about to be turned on and when the S_2 and S_3 pair of switches is about to be turned on, so that there are

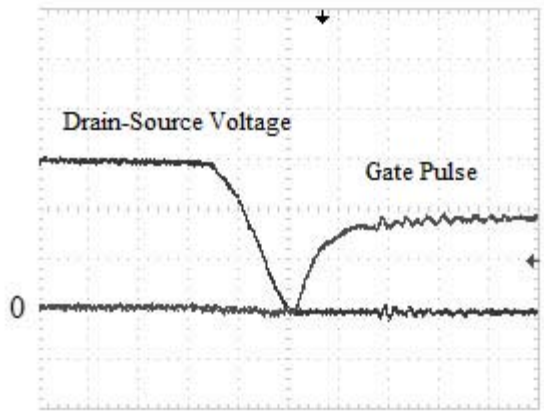
two sets of switch turn-ons during a switching cycle; thus the auxiliary switch operates at two times the converter switching frequency.

V. It can be seen from Fig. 5.6 that the current that flows in and out of the input voltage source has positive and negative portions. The positive portions are the input inductor current and the negative portions of the waveform are due to the auxiliary circuit. It can be seen from this waveform that the input current rises and falls at a rate that is twice the converter's switching cycle and that the auxiliary circuit is active for only a small portion of the switching cycle

VI. It can be seen from Fig. 5.7 that the primary transformer voltage waveform is a square wave pulse. The peak of the square wave is approximately equal to the reflected secondary voltage when current flows through the transformer primary and the converter is in an energy-transfer mode. When the transformer current is zero, the converter is in a boosting mode of operation with all its full-bridge switches on and the DC bus short-circuited so that the transformer voltage is zero.



(a)

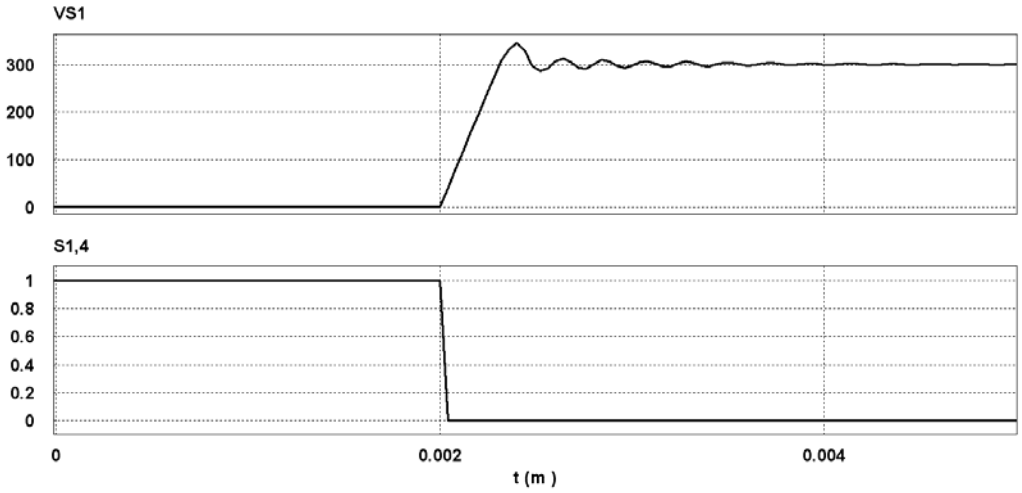


(b)

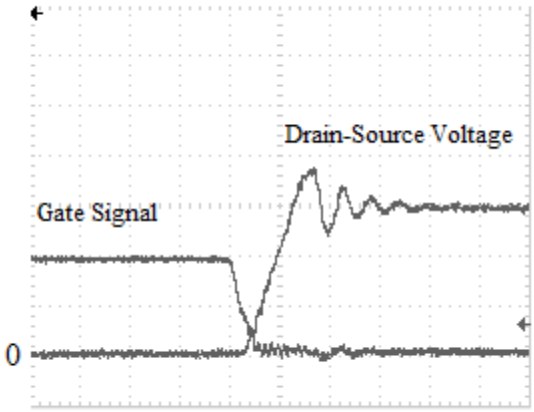
Fig. 5.2. ZVS turn-on of a main switch

(a) Simulation results (switch voltage: 100 V/div., gate pulse voltage: 0.2 V/div., t: 1 μs/div.)

(b) Experimental results (switch voltage: 100 V/div., gate pulse voltage: 5 V/div., t: 250 ns/div.)



(a)

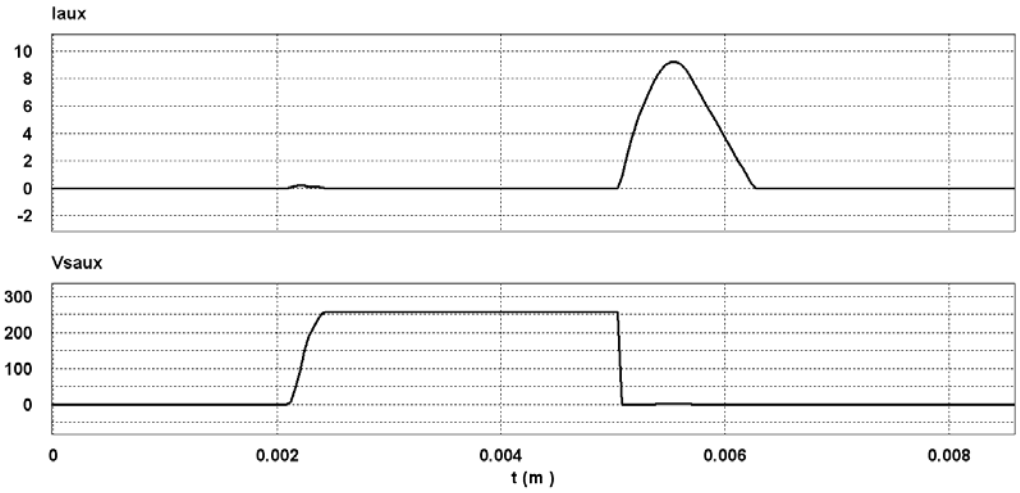


(b)

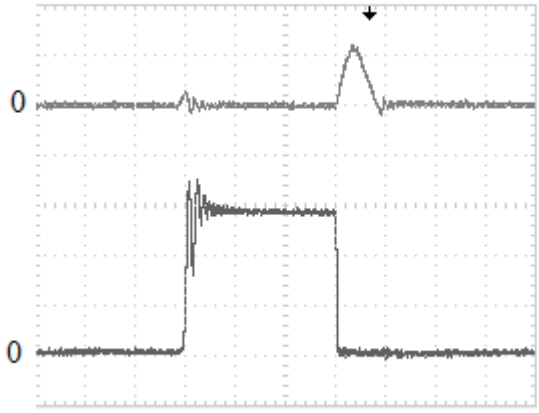
Fig. 5.3. ZVS turn-off of a main switch

(a) Simulation results (switch voltage: 100 V/div., gate pulse voltage: 0.2 V/div., t: 2 μs/div.)

(b) Experimental results (switch voltage: 100 V/div., gate pulse voltage: 5 V/div., t: 500 ns/div.)



(a)



(b)

Fig. 5.4. Auxiliary switch current (top) and auxiliary switch Drain-Source voltage (bottom)
(a) Simulation results [V: 50 V/div., I: 2 A/div., t: 2 µs/div.]
(b) Experimental results [V: 100 V/div., I: 5 A/div., t: 1 µs/div.]

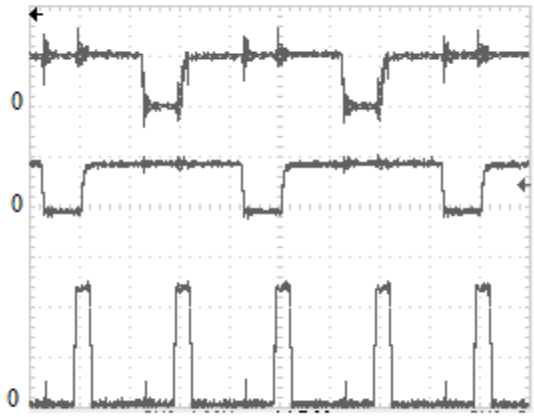
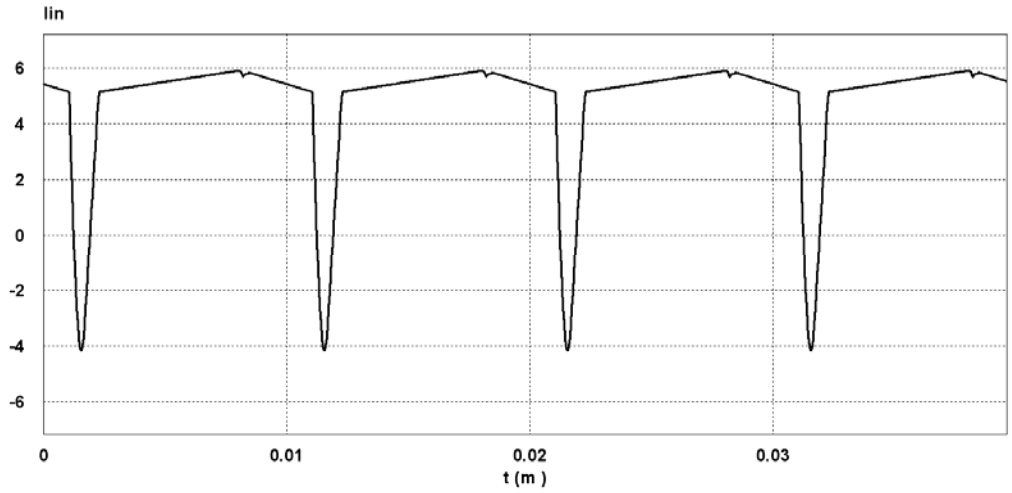
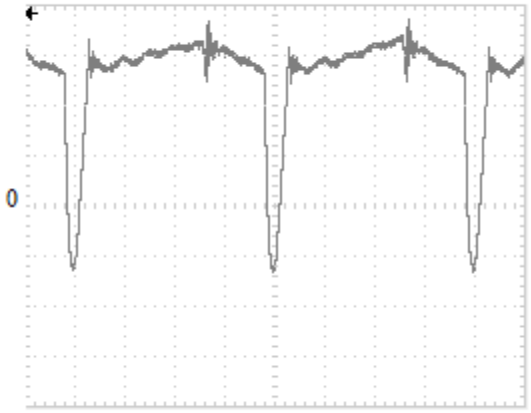


Fig. 5.5. Gate pulses of the main switches (top) and auxiliary switch (bottom) [main switch pulse voltage: 10 V/div., auxiliary switch pulse voltage: 5 V/div., t: 5 μs/div.]



(a)

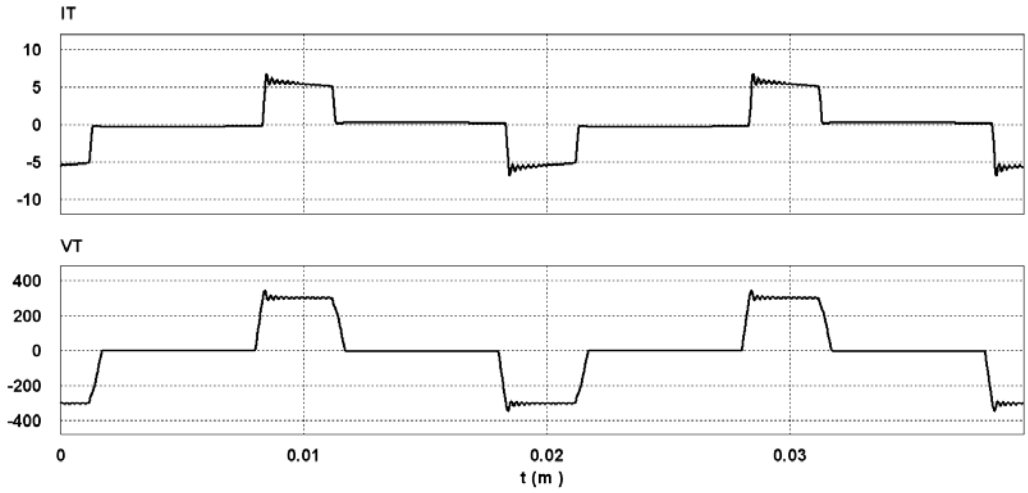


(b)

Fig. 5.6. Current flow in voltage source

(a) Simulation results (I: 2 A/div., t: 10 μs/div.)

(b) Experimental results (I: 2 A/div., t: 2.5 μs/div.)



(a)

(b)

Fig. 5.7. Transformer current (top) and voltage (bottom)
(a) Simulation results [I: 5 A/div., V: 200 V/div., t: 10 μs/div.]
(b) Experimental results [I: 5 A/div., V: 250 V/div., t: 5 μs/div.]

The efficiency of the converter prototype was measured with the auxiliary circuit (ZVS soft-switching implementation) and without (hard-switching implementation), in order to determine the effectiveness of this circuit in improving converter efficiency. If the auxiliary circuit is removed, then the hard-switching converter may have high voltage spikes across its main switches when they are turned off as the switch output capacitances are not, by themselves, sufficiently large to limit voltage rise and overshoots. As a result, a RCD snubber circuit was placed across the DC bus of the converter as shown in Fig. 5.8; the value of capacitor C of this snubber was the same as that of C_r in the auxiliary circuit of the proposed converter. The snubber works as follows: capacitor C helps clamp voltage shoots through diode D, then discharges through resistor R.

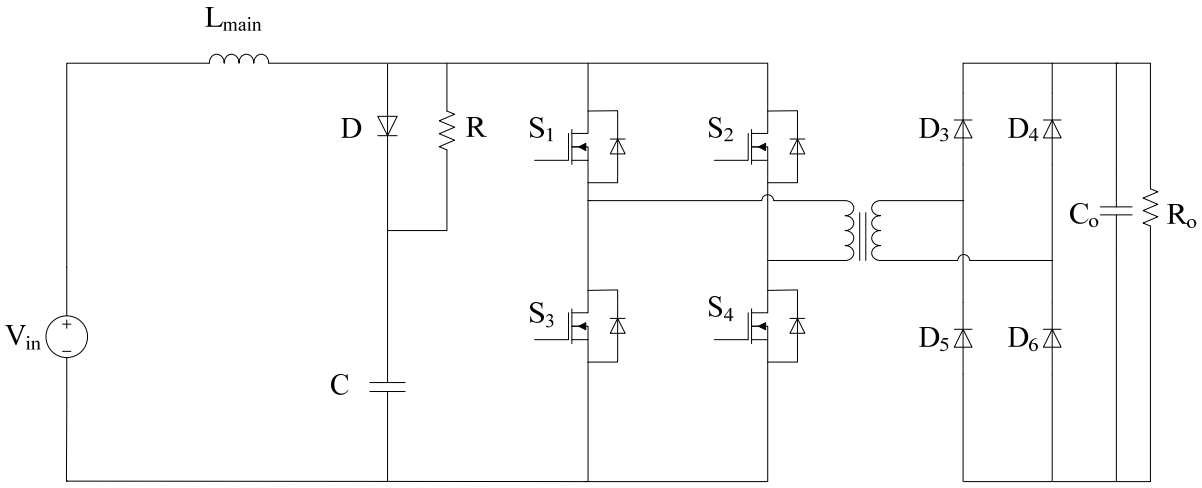


Fig. 5.8. Hard-switching PWM full-bridge boost converter, R =10 kΩ, C =5 nF

Fig. 5.9 shows the efficiency of the converter prototype with ZVS and with hard-switching. It can be seen that the proposed ZVS converter has a significantly better efficiency than the hard-switching boost converter over the load range. The efficiency improves because there are no turn-on or turn-off switching losses of the main switches and the energy used for soft-switching operation is delivered to the input. Normally, those two losses account for most of the losses of the hard-switching converter at high load.

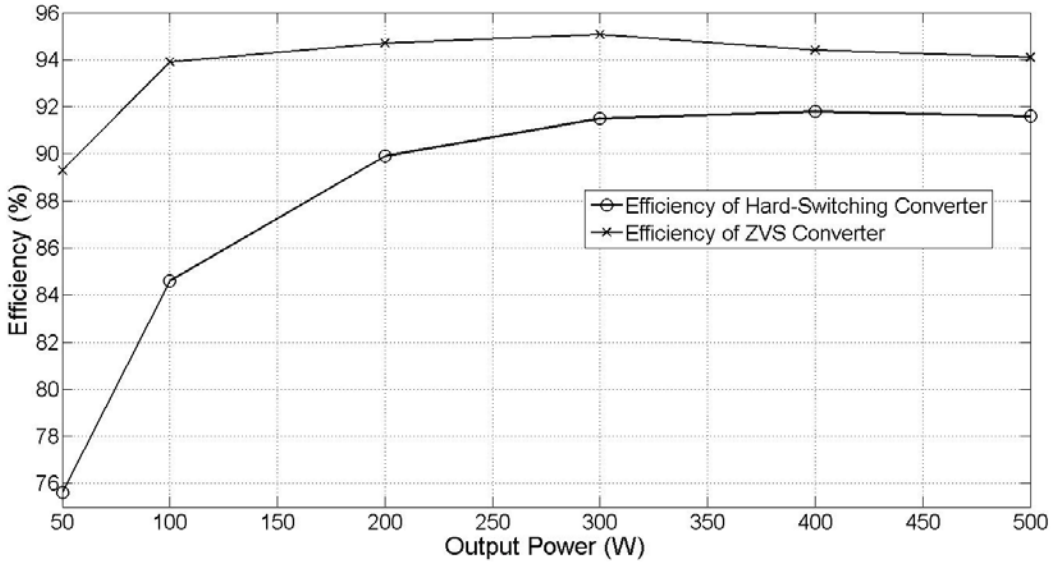


Fig. 5.9. Efficiency measurement for the proposed ZVS converter and the conventional hard-switching converter

5.3. Conclusion

Experimental results confirming the feasibility of soft-switching operation of the proposed converter were presented in this chapter. It was shown that the converter main switches operate with ZVS and the converter auxiliary switch operates with ZCS turn-on and turn-off.

The efficiency of the proposed ZVS full-bridge boost converter was compared with a conventional hard-switching full-bridge boost converter with a resistive snubber and the result shows a noticeable efficiency improvement in the proposed converter.

Chapter 6

Conclusion

6.1. Introduction

In this chapter, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work performed in thesis are presented and the main contributions of the thesis are stated. The chapter concludes by suggesting potential future research that can be done based on the thesis work.

6.2. Summary

The main objective of this thesis was to propose a new isolated PWM full-bridge DC-DC boost converter that does not have the drawbacks of previously proposed converters, such as increased peak current stress on the main power switches, excessive circulating current and auxiliary switch hard-switching operation. The contents of this thesis are summarized are follows:

In Chapter 1, basic fundamental concepts related to soft-switching such as ZVS and ZCS were introduced, previously proposed isolated DC-DC boost full-bridge converters were reviewed, and the thesis objectives were stated.

In Chapter 2, the new converter was introduced, its general operation was explained, and its modes of operation were reviewed. The features of the converter were also stated in the chapter. Some of these features include load independent soft-switching operation for all converter switches, a simple auxiliary circuit and flexible turn-off time of the auxiliary switch.

In Chapter 3, the modes of converter operation that were presented in Chapter 2 were analyzed mathematically. Component voltage and current equations that describe the steady-state operation of the converter were derived, and then were used in Chapter 4 to generate graphs of converter characteristics using a MATLAB program that showed the relationships between certain key converter parameters.

The analysis and characteristics graphs were used as part of the design procedure to select the values of key converter parameters in Chapter 4. Using the selected converter component values, the converter was simulated by PSIM circuit simulator software to confirm its feasibility.

An experimental prototype of the proposed ZVS full-bridge DC-DC boost converter was built and its functionality was confirmed with experimental results obtained from a 500 W prototype.

6.3. Conclusions

The following conclusions can be made based on the results of this thesis:

(i) The efficiency of a current-fed PWM full-bridge DC-DC boost converter can be improved by at least 2% under heavy-load conditions and more than 10% under light-load conditions by using a simple auxiliary circuit to allow the main bridge switches to operate with ZVS.

(ii) The converter has a good efficiency under light load conditions, the auxiliary switch turns off softly and there is no unnecessary circulating current flowing in the auxiliary circuit.

(iii) The maximum voltage that the main power switches are exposed to is dependent on the values of the transformer leakage inductance L_{lk} and the snubber capacitor C_r - higher the value of C_r, lower will be the peak voltage across the bridge devices for a given value of L_{lk}.

(iv) The value of L_r, in conjunction with that of C_r, is critical to the operation of the auxiliary circuit as it determines the maximum peak current stress on the auxiliary circuit components and the length of time that the auxiliary circuit is active. A trade-off must be considered in the selection of an appropriate value of L_r – L_r cannot be too low or else the peak current stress will increase nor can it be too high or else the auxiliary circuit will be active for a major portion of the switching cycle, which will stress the converter components and allow the circuit to interfere with the main converter operation.

6.4. Contributions

The principal contributions of this thesis are as follows:

(i) A new ZVS-PWM isolated full-bridge DC-DC boost converter was proposed and its operation was explained.

(ii) The steady-state operation of the new converter was analyzed and its characteristics were determined.

(iii) Guidelines for the design of the converter were given; a procedure for its design was derived and demonstrated with an example.

(iv) The feasibility of the proposed converter was confirmed by implementing a 500 W prototype. It was also shown that the new converter is more efficient than the conventional full-bridge DC-DC boost converter from light load to full load conditions.

6.5. Proposal for Future Work

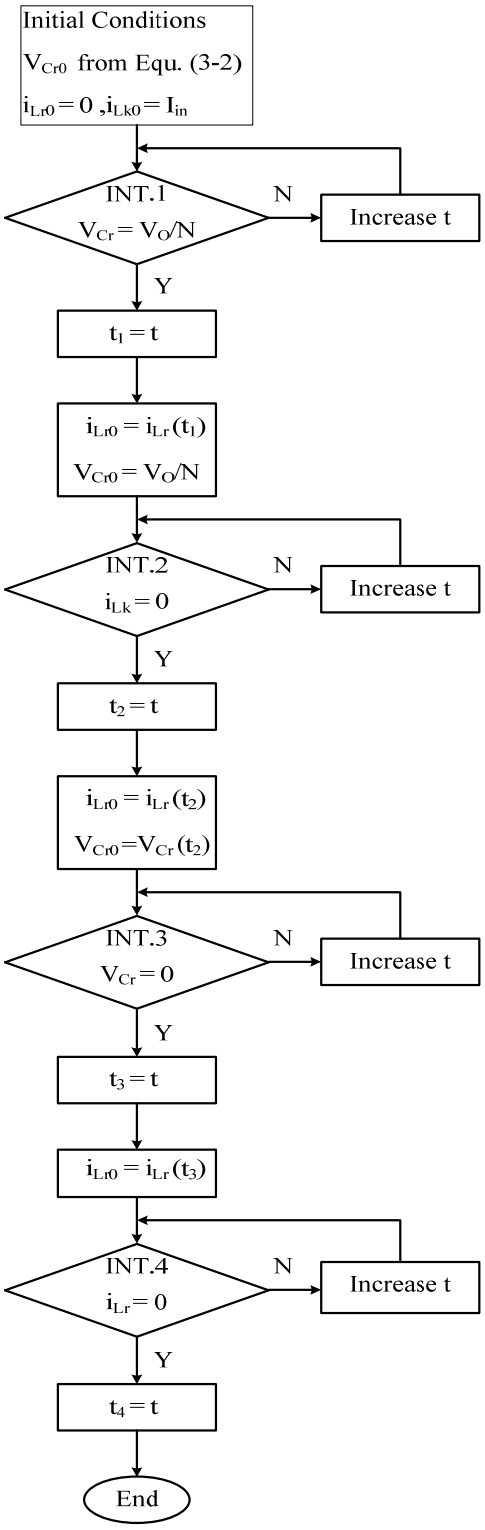
The following suggestions are made for future work:

(i) The proposed converter uses low voltage MOSFETs as its bridge switches. Research can be done to see the converter behavior if it was implemented with other switches with higher voltage and current ratings such as IGBTs, which have different properties from MOSFETs.

(ii) The proposed converter is best suited for maximum output loads of 500 W. Research can be done to see if the load range can be extended by paralleling converters and see how efficient the proposed converter approach would be.

Appendix A

The procedure of creating steady-state characteristic graphs in Chapter 4:



Appendix B

MATLAB program for generating characteristic graph in Fig. 4.2:

```
function overshootvsauxrms

% Values are from previous iteration
D=0.83;
ll=765*(10.^-9);
vi=100;
vo=300;
ii=5.4;
lr=7*(10.^-6);

% x is voltage overshoot of main switches (%)
x(1)=5;

% Calculating rms current of auxiliary circuit for ten values of
voltage overshoot
for j=1:10

    % From equ.(4-10), ctot equals:
    ctot=(10000*ii.^2*ll)/(x(j).^2*vo.^2);

    % Based on previous iterations that IXFH52N50P2 MOSFET devices,
which have an output drain-source capacitance of about 600 pF,
    % are used as the main power switches, then the required cr is
found to be:
    cr=ctot-1.2*(10.^-9);
    w=1/sqrt(lr*cr);

    % From equ.(3-11), t1 equals:
    t1 = sqrt(lr*cr)*acos(1/(1+(ii*sqrt(ll/ctot))/(vi*((2*D-1)/(2-
2*D)))));

    % From equ.(3-12), iLr(t) equals:
```

```
    iLr1=@(t)sqrt(cr/lr)*(ii*sqrt(ll/ctot)+((2*D-1)/(2-
2*D))*vi)*sin(w*t);
    a=iLr1(t1);

    % From equ.(3-20), w1 equals:
    w1=sqrt((1/lr+1/ll)/ctot);
    k=1/(2*(1-D))-(ll+lr/(2*(1-D)))/(lr+ll);

    % From equ.(3-19), iLk(t) equals:
    iLk=@(t)(vi/(ll*w1))*k*sin(w1*(t-
t1))+(a/(ll*(w1.^2)*ctot))*cos(w1*(t-t1))-(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(ll*(w1.^2)*ctot)+ii;
    t2 = fzero(iLk,t1);

    % From equ.(3-18), iLr(t) equals:
    iLr2=@(t)(vi/(lr*w1))*k*sin(w1*(t-
t1))+(a/(lr*(w1.^2)*ctot))*cos(w1*(t-t1))+(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(lr*(w1.^2)*ctot)+a;
    i0=iLr2(t2);

    % From equ.(3-17), Vcr(t2) equals:
    v0=vi*k*cos(w1*(t2-t1))-(a/(w1*ctot))*sin(w1*(t2-
t1))+vi*((ll+lr/(2*(1-D)))/(lr+ll));
    w2=1/sqrt(lr*ctot);

    % From equ.(3-24), Vcr(t) equals:
    vcr=@(t)(v0-vi)*cos(w2*(t-t2))+((ii-i0)/(ctot*w2))*sin(w2*(t-
t2))+vi;
    t3 = fzero(vcr,t2+1*(10.^-7));

    % From equ.(3-25), iLr(t) equals:
    iLr3=@(t)ctot*w2*(v0-vi)*sin(w2*(t-t2))+(i0-ii)*cos(w2*(t-t2))+ii;
    i01=iLr3(t3);
    iLr4=@(t)(-vi/lr)*(t-t3)+i01;
    t5 = fzero(iLr4,t3);

    % reproducing iLr(t) from iLr1, iLr2, iLr3 and iLr4:
```

```
    p=0:t5/100:t5;
    iLr=p;
    for i=1:101
        if p(i)<t1
            iLr(i)=iLr1(p(i));
        elseif p(i)<t2
            iLr(i)=iLr2(p(i));
        elseif p(i)<t3
            iLr(i)=iLr3(p(i));
        else
            iLr(i)=iLr4(p(i));
        end
    end

    % Creating next voltage overshoot with step of 3:
    if j<10
        x(j+1)=x(j)+3;
    end

    % Calculating rms value of iLr:
    sum=0;
    for m=1:100
        sum=sum+(t5/100)*iLr(m).^2;
    end
    % Auxiliary circuit switching frequency = 100 kHz
    rms(j)=sqrt(sum/(10*(10.^-6)));
end
plot(x,rms);
```

Appendix C

MATLAB program for generating characteristic graph in Fig. 4.3:

```
function Auxpeakcurrent

% Values are from previous iteration
cr=5*(10.^-9);
ctot=6.2*(10.^-9);
D=0.83;
ll=765*(10.^-9);
vi=100;
ii=5.4;
Lr(1)=(10.^-6);

% Calculating peak current of auxiliary circuit for 16 values of
auxiliary inductor
for j=1:16
    lr=Lr(j);
    w=1/sqrt(lr*cr);

    % From equ.(3-11), t1 equals:
    t1 = sqrt(lr*cr)*acos(1/(1+(ii*sqrt(ll/ctot))/(vi*((2*D-1)/(2-
2*D)))));

    % From equ.(3-12), iLr(t) equals:
    iLr1=@(t)sqrt(cr/lr)*(ii*sqrt(ll/ctot)+((2*D-1)/(2-
2*D))*vi)*sin(w*t);
    a=iLr1(t1);

    % From equ.(3-20), w1 equals:
    w1=sqrt((1/lr+1/ll)/ctot);
    k=1/(2*(1-D))-(ll+lr/(2*(1-D)))/(lr+ll);

    % From equ.(3-19), iLk(t) equals:
```

```
    iLk=@(t)(vi/(ll*w1))*k*sin(w1*(t-
t1))+(a/(ll*(w1.^2)*ctot))*cos(w1*(t-t1))-(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(ll*(w1.^2)*ctot)+ii;
    t2 = fzero(iLk,t1);

    % From equ.(3-18), iLr(t) equals:
    iLr2=@(t)(vi/(lr*w1))*k*sin(w1*(t-
t1))+(a/(lr*(w1.^2)*ctot))*cos(w1*(t-t1))+(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(lr*(w1.^2)*ctot)+a;
    i0=iLr2(t2);

    % From equ.(3-17), Vcr(t2) equals:
    v0=vi*k*cos(w1*(t2-t1))-(a/(w1*ctot))*sin(w1*(t2-
t1))+vi*((ll+lr/(2*(1-D)))/(lr+ll));
    w2=1/sqrt(lr*ctot);

    % From equ.(3-24), Vcr(t) equals:
    vcr=@(t)(v0-vi)*cos(w2*(t-t2))+((ii-i0)/(ctot*w2))*sin(w2*(t-
t2))+vi;
    % Finding closest zero of Vcr around t3
    if lr<10*(10.^-6)
        t3 = fzero(vcr,t2+1*(10.^-7));
        else
        t3 = fzero(vcr,t2+3*(10.^-7));
    end

    % From equ.(3-25), iLr(t) equals:
    iLr3=@(t)ctot*w2*(v0-vi)*sin(w2*(t-t2))+(i0-ii)*cos(w2*(t-t2))+ii;
    i01=iLr3(t3);
    iLr4=@(t)(-vi/lr)*(t-t3)+i01;
    t5 = fzero(iLr4,t3);

    % reproducing iLr(t) from iLr1, iLr2, iLr3 and iLr4:
    p=0:t5/100:t5;
    iLr=p;
    for i=1:101
        if p(i)<t1
```

```
            iLr(i)=iLr1(p(i));
        elseif p(i)<t2
            iLr(i)=iLr2(p(i));
        elseif p(i)<t3
            iLr(i)=iLr3(p(i));
        else
            iLr(i)=iLr4(p(i));
        end
    end

    % Creating next auxiliary inductor with step of 1uH:
    if j<16
        Lr(j+1)=Lr(j)+1*(10.^-6);
    end

    % Peak of auxiliary circuit current
    M(j)=max(iLr);
end
plot(Lr*(10.^6),M);
```

Appendix D

MATLAB program for generating characteristic graph in Fig. 4.4:

```
function rmscurrent

% Values are from previous iteration
cr=5*(10.^-9);
ctot=6.2*(10.^-9);
D=0.83;
ll=765*(10.^-9);
vi=100;
ii=5.4;
Lr(1)=(10.^-6);

% Calculating peak current of auxiliary circuit for 16 values of
auxiliary inductor
for j=1:16
    lr=Lr(j);
    w=1/sqrt(lr*cr);

    % From equ.(3-11), t1 equals:
    t1 = sqrt(lr*cr)*acos(1/(1+(ii*sqrt(ll/ctot))/(vi*((2*D-1)/(2-
2*D)))));

    % From equ.(3-12), iLr(t) equals:
    iLr1=@(t)sqrt(cr/lr)*(ii*sqrt(ll/ctot)+((2*D-1)/(2-
2*D))*vi)*sin(w*t);
    a=iLr1(t1);

    % From equ.(3-20), w1 equals:
    w1=sqrt((1/lr+1/ll)/ctot);
    k=1/(2*(1-D))-(ll+lr/(2*(1-D)))/(lr+ll);

    % From equ.(3-19), iLk(t) equals:
```

```
    iLk=@(t)(vi/(ll*w1))*k*sin(w1*(t-
t1))+(a/(ll*(w1.^2)*ctot))*cos(w1*(t-t1))-(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(ll*(w1.^2)*ctot)+ii;
    t2 = fzero(iLk,t1);

    % From equ.(3-18), iLr(t) equals:
    iLr2=@(t)(vi/(lr*w1))*k*sin(w1*(t-
t1))+(a/(lr*(w1.^2)*ctot))*cos(w1*(t-t1))+(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(lr*(w1.^2)*ctot)+a;
    i0=iLr2(t2);

    % From equ.(3-17), Vcr(t2) equals:
    v0=vi*k*cos(w1*(t2-t1))-(a/(w1*ctot))*sin(w1*(t2-
t1))+vi*((ll+lr/(2*(1-D)))/(lr+ll));
    w2=1/sqrt(lr*ctot);

    % From equ.(3-24), Vcr(t) equals:
    vcr=@(t)(v0-vi)*cos(w2*(t-t2))+((ii-i0)/(ctot*w2))*sin(w2*(t-
t2))+vi;
    % Finding closest zero of Vcr around t3
    if lr<10*(10.^-6)
        t3 = fzero(vcr,t2+1*(10.^-7));
        else
        t3 = fzero(vcr,t2+3*(10.^-7));
    end

    % From equ.(3-25), iLr(t) equals:
    iLr3=@(t)ctot*w2*(v0-vi)*sin(w2*(t-t2))+(i0-ii)*cos(w2*(t-t2))+ii;
    i01=iLr3(t3);
    iLr4=@(t)(-vi/lr)*(t-t3)+i01;
    t5 = fzero(iLr4,t3);

    % reproducing iLr(t) from iLr1, iLr2, iLr3 and iLr4:
    p=0:t5/100:t5;
    iLr=p;
    for i=1:101
        if p(i)<t1
```

```
            iLr(i)=iLr1(p(i));
        elseif p(i)<t2
            iLr(i)=iLr2(p(i));
        elseif p(i)<t3
            iLr(i)=iLr3(p(i));
        else
            iLr(i)=iLr4(p(i));
        end
    end

    % Creating next auxiliary inductor with step of 1uH:
    if j<16
        Lr(j+1)=Lr(j)+1*(10.^-6);
    end

    % Calculating rms value of iLr:
    sum=0;
    for m=1:100
        sum=sum+(t5/100)*iLr(m).^2;
    end
    % Auxiliary circuit switching frequency = 100 kHz
    rms(j)=sqrt(sum/(10*(10.^-6)));
end
plot(Lr*(10.^6),rms);
```

Appendix E

MATLAB program for generating characteristic graph in Fig. 4.5:

```
function capvoltage

% Values are from previous iteration
cr=5*(10.^-9);
ctot=6.2*(10.^-9);
lr=7*(10.^-6);
ll=765*(10.^-9);
vi=100;
ii=5.4;

% Plotting snubber capacitor voltage for 4 values of main switch duty
cycle
D=0.79;
for i=1:4
    w=1/sqrt(lr*cr);

    % From equ.(3-11), t1 equals:
    t1 = sqrt(lr*cr)*acos(1/(1+(ii*sqrt(ll/ctot))/(vi*((2*D-1)/(2-
2*D)))));

    % From equ.(3-12), iLr(t) equals:
    iLr1=@(t)sqrt(cr/lr)*(ii*sqrt(ll/ctot)+((2*D-1)/(2-
2*D))*vi)*sin(w*t);
    a=iLr1(t1);

    % From equ.(3-20), w1 equals:
    w1=sqrt((1/lr+1/ll)/ctot);
    k=1/(2*(1-D))-(ll+lr/(2*(1-D)))/(lr+ll);

    % From equ.(3-19), iLk(t) equals:
    iLk=@(t)(vi/(ll*w1))*k*sin(w1*(t-
t1))+(a/(ll*(w1.^2)*ctot))*cos(w1*(t-t1))-(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(ll*(w1.^2)*ctot)+ii;
```

```
    t2 = fzero(iLk,t1);

    % From equ.(3-18), iLr(t) equals:
    iLr2=@(t)(vi/(lr*w1))*k*sin(w1*(t-
t1))+(a/(lr*(w1.^2)*ctot))*cos(w1*(t-t1))+(vi/(lr+ll))*((2*D-1)/(2-
2*D))*(t-t1)-a/(lr*(w1.^2)*ctot)+a;
    i0=iLr2(t2);

    % From equ.(3-17), Vcr(t2) equals:
    v0=vi*k*cos(w1*(t2-t1))-(a/(w1*ctot))*sin(w1*(t2-
t1))+vi*((ll+lr/(2*(1-D)))/(lr+ll));
    w2=1/sqrt(lr*ctot);

    % From equ.(3-24), Vcr(t) equals:
    vcr=@(t)(v0-vi)*cos(w2*(t-t2))+((ii-i0)/(ctot*w2))*sin(w2*(t-
t2))+vi;

    % Plotting Vcr
    T=1.2*(pi/w2);
    t=t2:T/10:T+t2;
    Vcr=vcr(t);
    plot(t-t2,Vcr)
    hold on;
    D=D+0.02;
end
hold off;
```

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Experiences

Research Assistant **2010-2012**
University of Western Ontario (UWO) **London, Ontario**

- Designed a new ZVS-PWM isolated full-bridge DC-DC boost converter for industrial applications, tested by building a 500-Watt prototype
- Designed a new variable frequency ZCS-PWM isolated full-bridge DC-DC boost converter with improved light load efficiency, tested by building a 600-Watt prototype

Consultant **2009 – 2010**
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- Consulted in the field of CVT effects on power network harmonics in Abshar 230-kVolt substation of Isfahan regional electricity

Research Assistant **2008**

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- Designed and implemented a 1-kWatt high frequency solar battery charger using a DC-DC buck-boost converter
- Designed and implemented control circuit for the solar battery charger to operate with maximum power point tracking (MPPT)

Teaching Assistant **2004-2012**

- TA for Electronics II course at the University of Western Ontario for two semesters
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