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Investigating Performance and Reliability of Process Bus Networks for Digital Protective Relaying

Mitalkumar Kanabar, *University of Western Ontario*

Supervisor: Dr. Tarlochan S. Sidhu, *The University of Western Ontario*

A thesis submitted in partial fulfillment of the requirements for the Doctor of Philosophy degree in Electrical and Computer Engineering

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Investigating Performance and Reliability of Process Bus Networks for Digital Protective Relaying

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by

Mitalkumar Kanabar

Graduate Program in Engineering Science
Department of Electrical and Computer engineering

A thesis submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy

School of Graduate and Postdoctoral Studies
The University of Western Ontario
London, Ontario, Canada

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THE UNIVERSITY OF WESTERN ONTARIO
THE SCHOOL OF GRADUATE AND POSTDOCTORAL STUDIES

CERTIFICATE OF EXAMINATION

Supervisor

Dr. Tarlochan S. Sidhu

Examiners

Dr. Quazi Mehbubar Rahman

Dr. Mehrdad Radji Kermani

Dr. Kamran Siddiqui

Dr. Ramakrishna Gokaraju

The thesis by

Mital Kanabar

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Abstract

To reduce the cost of complex and long copper wiring, as well as to achieve flexibility in signal communications, IEC 61850 part 9-2 proposes a process bus communication network between process level switchyard equipments, and bay level protection and control (P&C) Intelligent Electronic Devices (IEDs). After successful implementation of Ethernet networks for IEC 61850 standard part 8-1 (station bus) at several substations worldwide, major manufacturers are currently working on the development of interoperable products for the IEC 61850-9-2 based process bus. The major technical challenges for applying Ethernet networks at process level include: 1) the performance of time critical messages for protection applications; 2) impacts of process bus Ethernet networks on the reliability of substation protection systems.

This work starts with the performance analysis in terms of time critical Sampled Value (SV) messages loss and/or delay over the IEC 61850-9-2 process bus networks of a typical substation. Unlike GOOSE, the SV message is not repeated several times, and therefore, there is no assurance that each SV message will be received from the process bus network at protection IEDs. Therefore, the detailed modeling of IEC 61850 based substation protection devices, communication protocols, and packet format is carried out using an industry-trusted simulation tool OPNET, to study and quantify number of SV loss and delay over the process bus.

The impact of SV loss/delay on digital substation protection systems is evident, and recognized by several manufacturers. Therefore, a sample value estimation algorithm is developed in order to enhance the performance of digital substation protection functions by estimating the lost and delayed sampled values. The error of estimation is evaluated in detail considering several scenarios of power system relaying. The work is further carried out to investigate the possible impact of SV loss/delay on protection functions, and test the proposed SV estimation algorithm using the hardware setup. Therefore, a state-of-the-art process bus laboratory with the protection IEDs and merging unit playback simulator using industrial computers on the QNX hard-real-time platform, is developed for a typical IEC 61850-9-2 based process bus network. Moreover, the proposed SV estimation

algorithm is implemented as a part of bus differential and transmission line distance protection IEDs, and it is tested using the developed experimental setup for various SV loss/delay scenarios and power system fault conditions.

In addition to the performance analysis, this work also focuses on the reliability aspects of protection systems with process bus communication network. To study the impact of process bus communication on reliability indices of a substation protection function, the detailed reliability modeling and analysis is carried out for a typical substation layout. First of all, reliability analysis is done using Reliability Block Diagrams (RBD) considering various practical process bus architectures, as well as, time synchronization techniques. After obtaining important failure rates from the RBD, an extended Markov model is proposed to analyze the reliability indices of protection systems, such as, protection unavailability, abnormal unavailability, and loss of security. It is shown with the proposed Markov model that the implementation of sampled value estimation improves the reliability indices of a protection system.

I dedicate this work to my Dearest Family and Divine God.

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List of Abbreviations

ADC	Analog to Digital Converter	MTTR	Mean Time To Repair
APDU	Application Protocol Data Unit	MU	Merging Unit
ASDU	Application Service Data Unit	OSI	Open Systems Interconnection
BER	Bit Error Rate	P&C	Protection and Control
CSMA/CD	Carrier Sense Multiple Access with Collision Detection	Ph-G	Phase-to-Ground
CT	Current Transformer	Ph-Ph	Phase-to-Phase
CVT	Capacitor Voltage Transformer	POW	Point on Waves
DFT	Discrete Fourier Transform	PSCAD	Power System Computer Aided Design
DNP	Distributed Network Protocol	PSRC	Power System Relaying Committee
EMTDC	Electro Magnetic Transient Direct Current Analysis	PTP	Precision Time Protocol
ESW	Ethernet Switch	QoS	Quality of Service
FCT	FunCTion (according to IEC 61850 standard)	RBD	Reliability Block Diagram
GOOSE	Generic Object Oriented Substation Event	RSTP	Rapid Spanning Tree Protocol
GPS	Global Positioning System	RTP	Real Time Playback
GSSE	Generic Substation Status Event	SAS	Substation Automation System
HMI	Human Machine Interface	SCL	Substation Configuration Language
IEC	International Electro technical Commission	SIR	Source Impedance Ratios
IED	Intelligent Electronic Device	SV	Sampled Values
IEEE	The Institute of Electrical and Electronics Engineers	TC	Technical Committee
IP	Internet Protocol	TCI	Tag Control Identifier
IRIG-B	Inter Range Instrumentation Group -B	TCP	Transmission Control Protocol
LAN	Local Area Network	TPID	Tag Protocol Identifier
MAC	Medium Access Control	TS	Time Synchronization source
MATLAB	MATrix LABoratory	UDP	User Datagram Protocol
MMS	Manufacturing Message Specification	VLAN	Virtual Local Area Network
MTTF	Mean Time To Failure	XML	Extensible Mark-up Language

Chapter 1

1. Introduction

This chapter provides an overview of the IEC 61850 standard, and a discussion on part-9-2 of the IEC 61850 standard to introduce the concept of process bus. Based on a detailed literature survey, the salient features, major benefits, as well as technical challenges related to the IEC 61850-9-2 based process bus for substation protection systems are also presented in this chapter. Finally, the specific research objectives inspired by these technical challenges, and research work methodology are also discussed.

1.1 IEC 61850 Standard for Substation Protection and Automation

The success of a substation protection and automation system relies on the use of an effective communication system to link various protection, control, and monitoring devices within an electric power substation. The major challenge faced by substation automation design engineers is to provide interoperability among the protection, control, and monitoring devices from the various manufacturers. Up until recently, all the manufacturers are/were using their own proprietary communication protocols for various substation protection and automation applications. Huge investment is needed to develop costly and complicated protocol converters to interface these substation intelligent devices [1]. To address this issue, the International Electro technical Commission (IEC) Technical Committee (TC)-57 has published IEC 61850 standard titled “Communication Networks and Systems in Substation” in 2003 [2]. This standard covers not only how to communicate, but also what to communicate. IEC 61850 capabilities clearly exceeded what former IEC 60870-5-103 [3] , DNP 3.0 [4], MODBUS [5] and most other proprietary protocols had to offer [6]. IEC 61850 provides the interoperability by defining the communication protocol, data format and the configuration language.

Further, this standard specifies the OSI-7 layer based Ethernet communication systems [7]. Ethernet provides high flexibility regarding communication architectures, as well as the incorporation of fast growing communication technologies [8]. The high-speed property of current Ethernet technology together with its dominant position in the LAN field, makes Ethernet an appropriate communication technology for substation automation usage [9]. IEC 61850 part-8 and part-9 propose Ethernet at station level and process level respectively. Furthermore detail on scope of the entire IEC 61850 standard is described in the following subsection.

1.1.1 Scope of IEC 61850 standard

Recent developments in communication media and networking technology have offered a wide range of new opportunities for utilities to improve their electric systems, operations, and process automation. One of the major challenges in a Substation Automation System (SAS) is the interoperability among the substation IEDs from different manufacturers. This is being addressed by the development of IEC61850 as a universal standard for SAS. IEC61850 standard is a framework for substation automation that defines the following [10],

- i. Standardized object models and naming conventions
- ii. Standardized meaning of data
- iii. Standardized services and device behavior models
- iv. Self-describing devices
- v. Common configuration language

The work on IEC 61850 started with the Electric Power Research Institute (EPRI) and the Institute of Electrical and Electronics Engineers (IEEE) working in an effort to define Utility Communications Architecture (UCA) in the early 1990s. The effort was focused towards inter-control communications architecture and communication between substations and control centers. In 1994, EPRI and IEEE started working on the next phase of the UCA (UCA 2.0 [11]), focusing on the station bus. In 1996, technical committee 57 of the IEC started work on IEC 61850 standard. In 1997 the two groups agreed to work together resulting in the IEC 61850 standards. The standard is a superset

of the UCA 2.0, with features of UCA 2.0 and more. IEC 61850 defines various aspects of the substation communications in ten major parts. Parts 3, 4 and 5 identify the different general, as well as functional requirements of the substation communication systems, and also discuss project management. Part 6 defines the Substation Configuration Language (SCL) which is based on Extensible Mark-up Language (XML) to configure different multi-vendor devices with minimal human errors and less complexity. The SCL bridges the relationship between the SAS system and the substation switchyard. Part 7-1 introduces the concepts of common data and service modeling adopted by the IEC 61850 standard. Part 7-2 defines abstract services, and various common data classes are defined in Part 7-3. Whereas, Part 7-4 defines the abstract data objects (Logical Nodes). The data objects defined in the standard contain information, such as status, measurements, etc. The concept of common data classes was introduced to build larger data objects. IEC 61850 adopts data and service abstraction, which allows the mapping of data and services to any protocol stack that meets the service requirements [12]. Part 8-1 defines the mapping of abstract data objects and services into Manufacturing Messaging Specifications (MMS). Parts 9-1 and 9-2 define the digitization of signals from instrument transformers and mapping them into sampled values packets over Ethernet layer. IEC 61850 part-9-2 proposes Ethernet based Local Area Network (LAN) to communicate substation protection and automation messages between process level switchyard devices (i.e. CTs/VTs, CBs, and other field sensors) and bay level protection and control IEDs. IEC 61850-9-2 based Ethernet communication network should facilitate the communication of time critical messages, such as Generic Object Oriented Substation Event (GOOSE) and raw data Sampled Values (SVs), within the allowable time defined in the standard [13], [14].

1.1.2 Function hierarchy and interfaces of IEC 61850

A complex substation protection, control, monitoring and recording system has a hierarchical structure as shown in Figure 1-1. The three levels in the functional hierarchy are discussed below (from bottom-up):

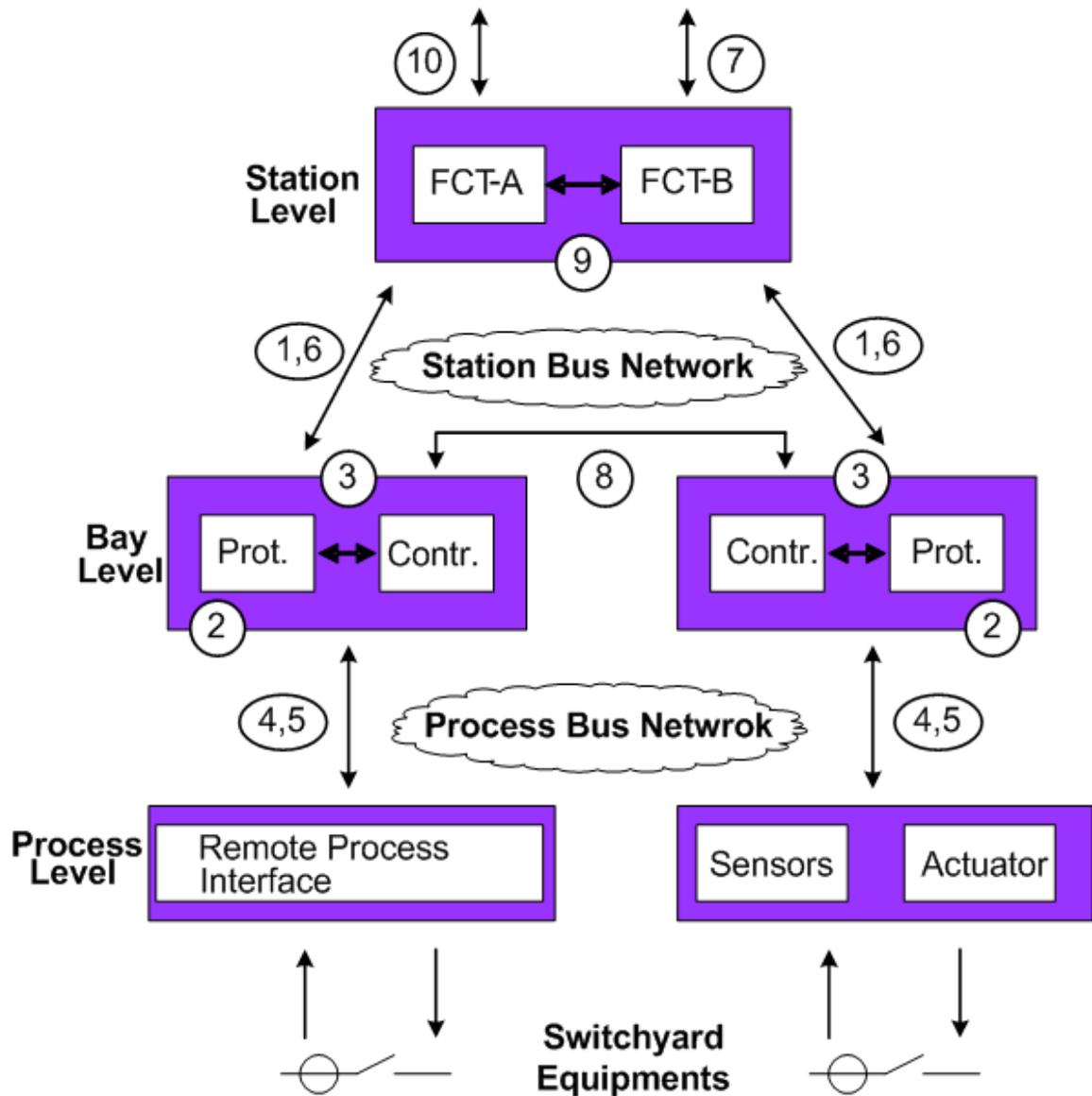


Figure 1-1 Interface model of a substation automation system with encircled interface type

Process level: It includes the primary equipment in the substation switchyard, such as analog signals from instrument transformers, binary status signals or binary control signals from actuators/sensors or other controlling devices, etc.

Bay level: Bay level is between process bus and station bus, which includes protection and control IEDs of different bays of a substation. Integrated protection and control IEDs at the bay level are connected to the process bus network. Process bus network segments of different bays may be connected through communication links.

Station level: At this level the functions are related to the overall operation of equipments in a substation. The functions using the data of more than one bay or the entire substation are implemented at this level. For example, the triggering of a breaker failure relay by a protection device, tripping multiple breakers by the breaker failure relay through the trip outputs of a bus differential protection, etc. The functions of interface numbers used in Figure 1-1 are explained in Table 1-1. It can be inferred from Figure 1-1 that a station bus network facilitates the communication between the station level and bay level. For this communication application interfaces applied between them are shown in the figure i.e. IF1, IF3, IF6, IF8 and IF9. Similarly, the process bus network is used for the purpose of data exchange between bay level and process level. Interface IF4 and IF5 are supported at this level.

Table 1-1 Interface types & their function

Sr. No.	Interface Types	Function
1	IF 1	Protection-data exchange between bay and station level
2	IF 2	Protection-data exchange between bay level and remote protection (beyond the scope of IEC 61850 standard)
3	IF 3	Data exchange within bay level
4	IF 4	CT and VT instantaneous data exchange (especially samples) between process and bay level
5	IF 5	Control-data exchange between process and bay level
6	IF 6	Control-data exchange between bay and station level
7	IF 7	Data exchange between substation (level) and a remote engineer's workplace
8	IF 8	Direct data exchange between the bays especially for fast functions such as interlocking
9	IF 9	Data exchange within station level
10	IF 10	Control-data exchange between substation (devices) and a remote control centre (beyond the scope of IEC 61850 standard)

1.1.3 OSI-7 layer based IEC 61850 communication system

IEC 61850 uses OSI-7 layer stack for communication and divides it into three groups as shown in Figure 1-2. In the standard, seven types of messages are mapped to different communication stacks. The raw data samples (type 4) and GOOSE messages (type1, 1A) are time critical and are, therefore, directly mapped to low-level Ethernet layer. This improves the performance for time critical messages by shortening the Ethernet frame (no upper layer protocol overhead), and reducing the processing time. The medium speed message (type 2), the command message with access control (type 7), the low speed message (type 3) and the file transfer functions (type 5) are mapped to MMS protocol suits, which has a TCP/IP stack on the top of the Ethernet layer. The time synchronization messages based on Simple Network Time Protocol (SNTP) (type 6) are broadcasted to all IEDs in a substation using UDP/IP.

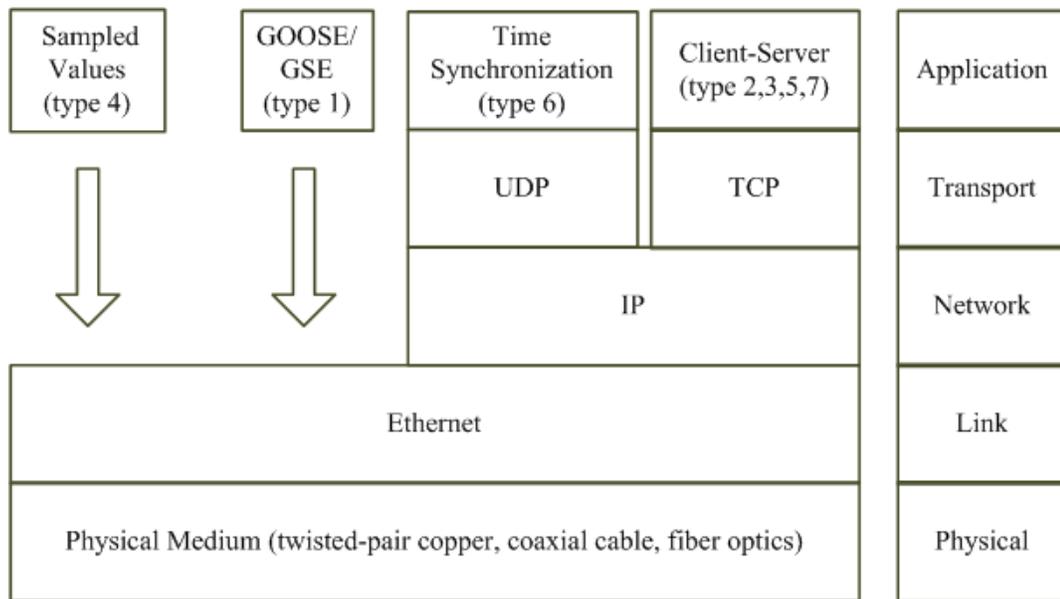


Figure 1-2 Message communication OSI-7 layer stack of IEC 61850 [2]

The features of GOOSE, SV and other (client/server) messages are discussed below:

1. GOOSE/GSE :
 1. Time critical data, e.g. trip, block, interlock, etc., using this message
 2. Does not use the TCP/IP services, and hence it is less reliable data transfer mechanism

3. A loss of GOOSE message is by multicasting (repeated transmission)
2. Sampled values
 1. Time critical data – sampled values of current / voltage signals from non-conventional instrument transformers or IEDs
 2. Continuous stream of data, rate determined by the sampling frequency of the data
 3. No measures proposed for SV loss/delay
3. Client-Server communication
 1. Predominantly information exchange, such as fault record, event record, measurement values, etc.
 2. Uses the full services of the OSI model, and hence a reliable data transfer
 3. Not time critical data

1.1.4 Advantages from IEC 61850 based implementation

The major advantages offered by IEC 61850 are listed below:

1. **Interoperability:** Different Seamless communication among multi-vendor devices.
2. **Free Configuration:** Any possible number of substation protection and control functions can be integrated and configured using Substation Configuration Language (SCL).
3. **Simple and Future-proof Architecture:** As plenty of point-to-point copper wires are reduced to just Ethernet communication links based on OSI-7, it is possible to integrate many critical functions in an IED and also have OSI-7 layer stack compatibility.

1.2 IEC 61850-9-2 Process Bus Concept

To reduce the cost of complex and long copper wiring between a switchyard and the control room, IEC 61850-9-2 has proposed Ethernet based communication network between process level switchyard devices and bay level protection and control IEDs, which is referred to as process bus. Instead of providing analog inputs to conventional

IEDs with integrated Analog-to-Digital Converters (ADCs) and binary Inputs-Outputs I/Os modules, IEC 61850-9 has specified distributed IED architecture, i.e. ADCs and binary I/Os modules are installed into the switchyard near to the signal sources. The analog signals from CTs/VTs are digitized into the Merging Units (MUs), and then digital signals are communicated to the bay level protection IEDs over Ethernet based process bus. The merging unit is the key element of the process bus [13]. As Figure 1-3 shows, MU gathers information, such as phase voltages and currents from instrument transformers, and status information from transducers using proprietary links/copper wires. All these analog values are converted to digital, and merged into a standard data packet format. This way, process bus network can carry many digital signals into a single communication cable. However, each digital stream of sampled values from various MUs should be time synchronized, so that the protection function can utilize many such digital signal streams from independent MUs. MU may have either an external time synchronization source (e.g. IRIG-B, GPS clock) or precision time synchronization protocol (IEEE 1588/IEEE C37.238), using which it provides the time stamp on each data packet. This data packet is sent to corresponding bay level protection and control IEDs using standardized Ethernet based communication links.

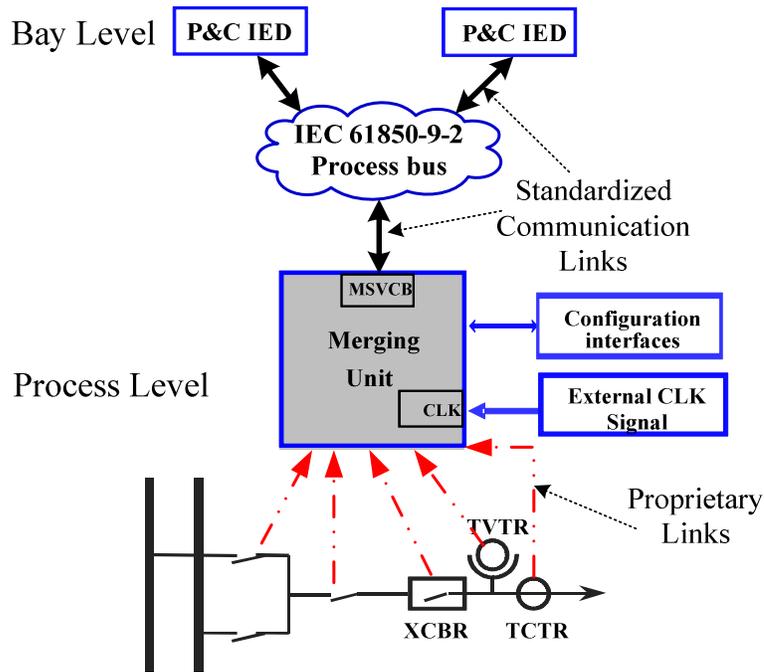


Figure 1-3 Process bus concepts

The IEC 61850-9 standard defines the Specific Communication Service Mapping (SCSM) for the transmission of sampled values in two parts. The IEC 61850-9-1 standard [15] specifies a serial unidirectional multi-drop point-to-point link carrying a fixed dataset in accordance with IEC 60044-8 [16], whereas IEC 61850-9-2 [13] proposes bidirectional multicast communication of configurable (user defined) dataset using Ethernet LANs (defined in the ISO/IEC 8802-3 or IEEE 802.3 [17]). Due to the advantages of fast growth in data rates, zero-collision, and flexible architecture, the ISO/IEC 8802-3 or ANSI/IEEE 802.3 based Ethernet switched communication (standardized in IEC 61850-9-2) is preferred over serial point-to-point standard links (IEC 61850-9-1). Currently, there are implementation guidelines (IEC 61850-9-2 LE [14]) that define a base sample rate of 80 samples per power system cycle for basic protection and control, and a high rate of 256 samples per power system cycle for high frequency applications, such as power quality and high resolution oscillography [14].

1.3 Major Benefits from Process Bus

The major benefits offered by IEC 61850-9-2 based process bus communication network are discussed below:

1.3.1 Simple wiring and flexible architecture

Millions of point-to-point copper wires are laid down from a substation switchyard to various bay level devices for the substation protection and control. In conventional protection systems, each protective relay has limited access to the few measured signals. Therefore, conventional protective functions are optimized to perform the task using minimum numbers of input signals. Besides, the substation protection and monitoring require their own instrument transformers, which allow either wide dynamic range of fault currents or accurate metering of the energy. As a result, an instrument transformer outputs cannot be shared with several devices, and thus dedicated instrument transformers and separate cables are required. The simplification of wiring can be observed by comparing Figure 1-4 (with traditional copper wires) with Figure 1-5 (with process bus communication network) for a typical transmission line protection and bay. It

can be inferred from the figures that the process bus facilitates very simple (fewer communication fibre) which can be engineered in factory itself (by configuring merging unit to corresponding subscribed IEDs). Therefore, this process bus concept can help to achieve cost savings as well.

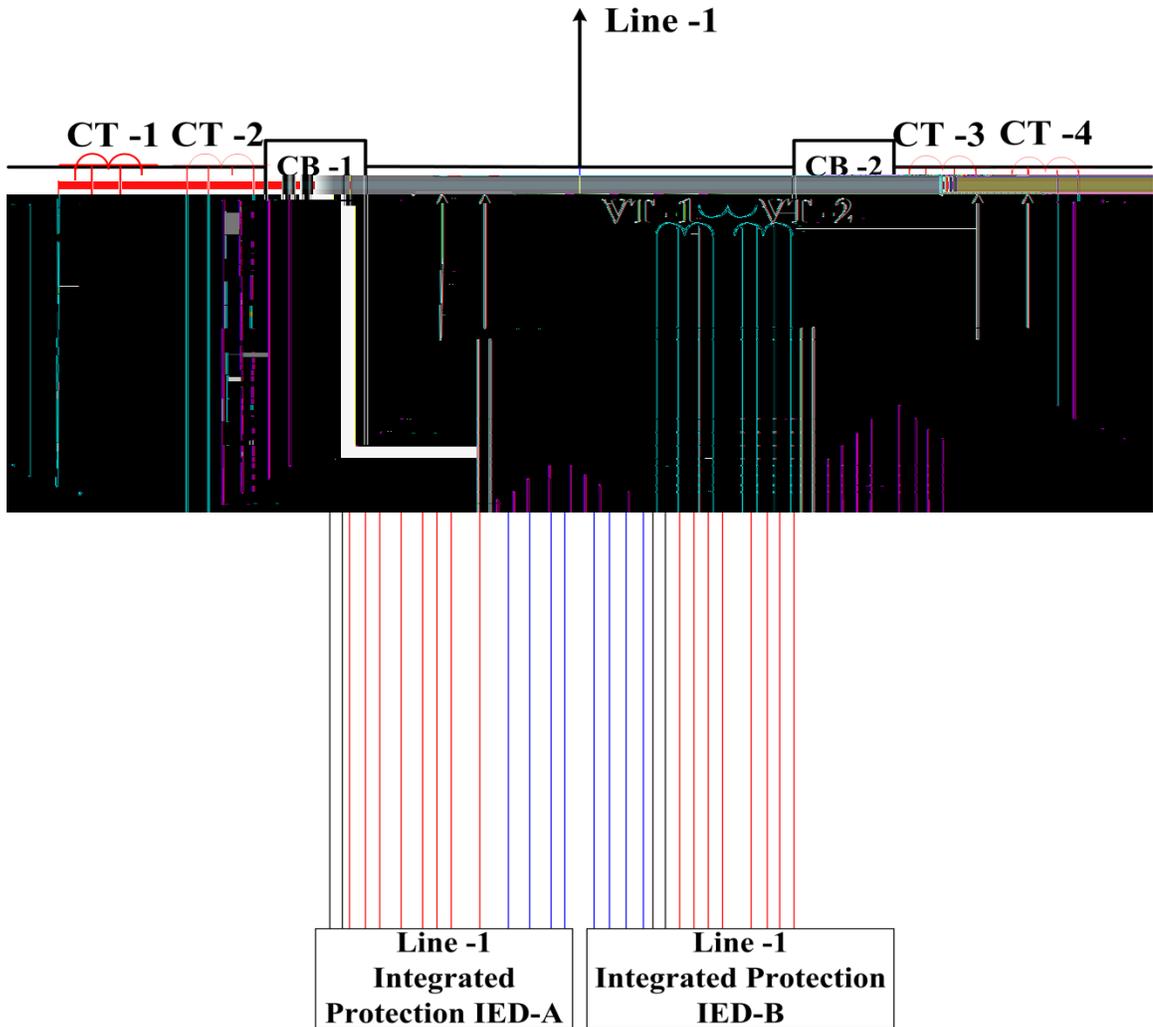


Figure 1-4 Traditional copper wiring architecture of a typical line protection

In addition to that, with traditional one-to-one copper wiring, the accessibility of current and voltage signals are only limited to connect corresponding IEDs. Whereas, in case of process bus, any IED at bay level can subscribe to any process level merging unit in order to receive SVs without additional costs. This signal flexibility in the architecture can provide opportunities to enhance protection functions, which will be discussed in the following subsections of this chapter.

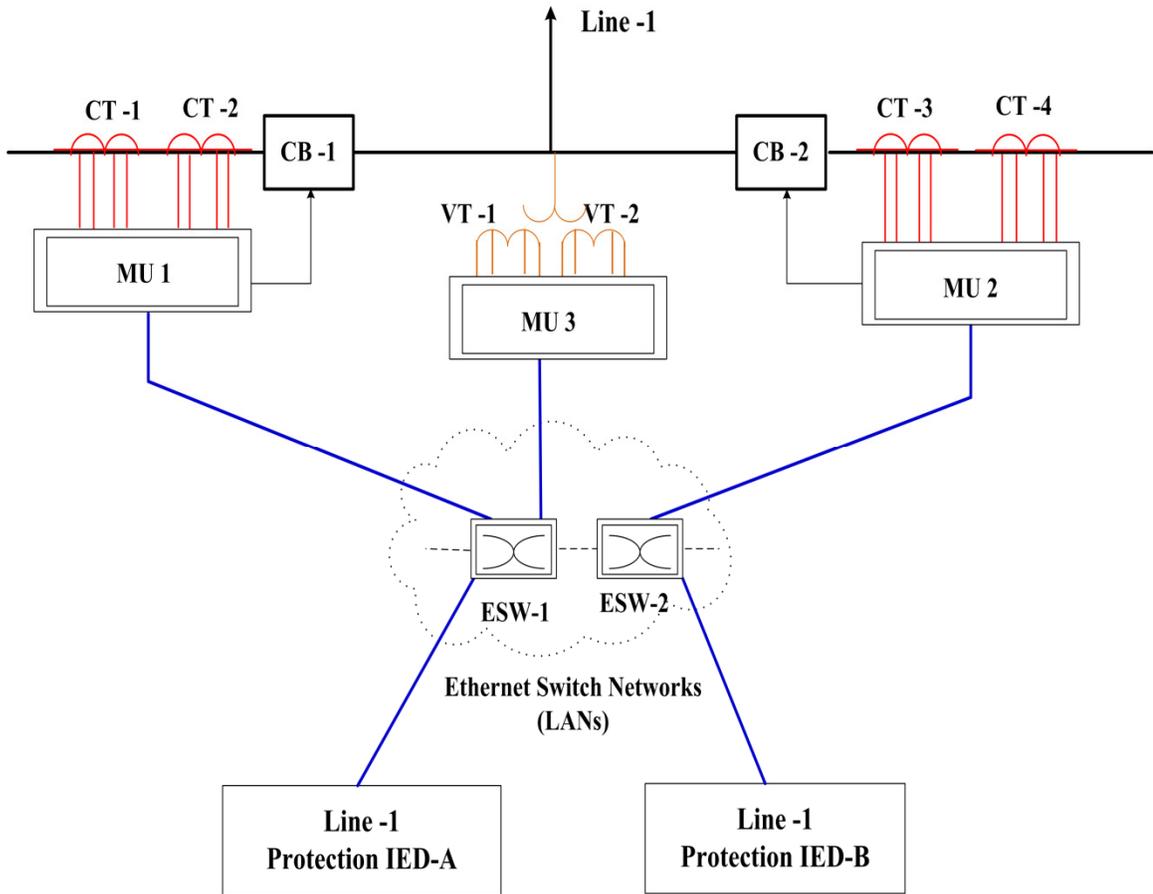


Figure 1-5 A simple and flexible architecture of a typical line protection process bus

1.3.2 Cost savings

It is the cost equation that separates what is technically possible from what is eventually manufactured by relaying vendors. The cost analysis of process bus communication has already been done in [18], [19]. Business case of applying process bus in a typical substation show that a process bus implementation can reduce the total installation cost, and savings of approx. 25% can be achieved [18]. Although material cost with process bus may increase from 27% to 42% due to the addition of communication network devices, the labour cost (which includes engineering, drafting, construction, commissioning) is expected to reduce from 73% to 34%. This is because, complex copper wiring is a major contributor of the labour cost, and pre-tested and pre-configured

process bus can provide less assembly, engineering, and commissioning at site. This can be appreciated by comparing Figure 1-4 with Figure 1-5.

1.3.3 Enhancements of protection functions

As explained in Figure 1-5, IEC 61850-9-2 process bus provides flexibility in terms of information exchange at the process level. This accessibility of any signal from the process level to any place at the bay level in a substation opens up tremendous opportunities of enhancement for substation protection functions. Enhancement of busbar protection using directional comparison concept with the help of IEC 61850-9-2 process bus is presented in [20], [21]. Moreover, IEDs could play the role of different protective relays, various control and monitoring devices and could be connected to different actuators such as circuit breakers or sectionalizers. Trip, blocking, status or any logical signals are transferred through the same network using GOOSE, and can support peer-to-peer applications in a substation [22]. In addition to that, reference [23] presents other opportunities, such as failure of any current transformer or an MU can be easily compensated by estimating lost signal from other MUs, and installing centralized back-up protection system instead of providing individual duplication of each bay level protection IED.

1.3.4 Interoperability

Different vendors are allowed to provide complete integration of protection functions among all bay level IEDs and process level MUs. An abstract representation of interoperability at the process level is shown in Figure 1-6, by showing only few of the major process bus manufacturers (to demonstrate the concept). This figure shows the capability of IEC 61850-9-2 based process bus, and the interoperability vision of this standard, i.e. seamless interface of multi-vendor devices for a common goal (or application).

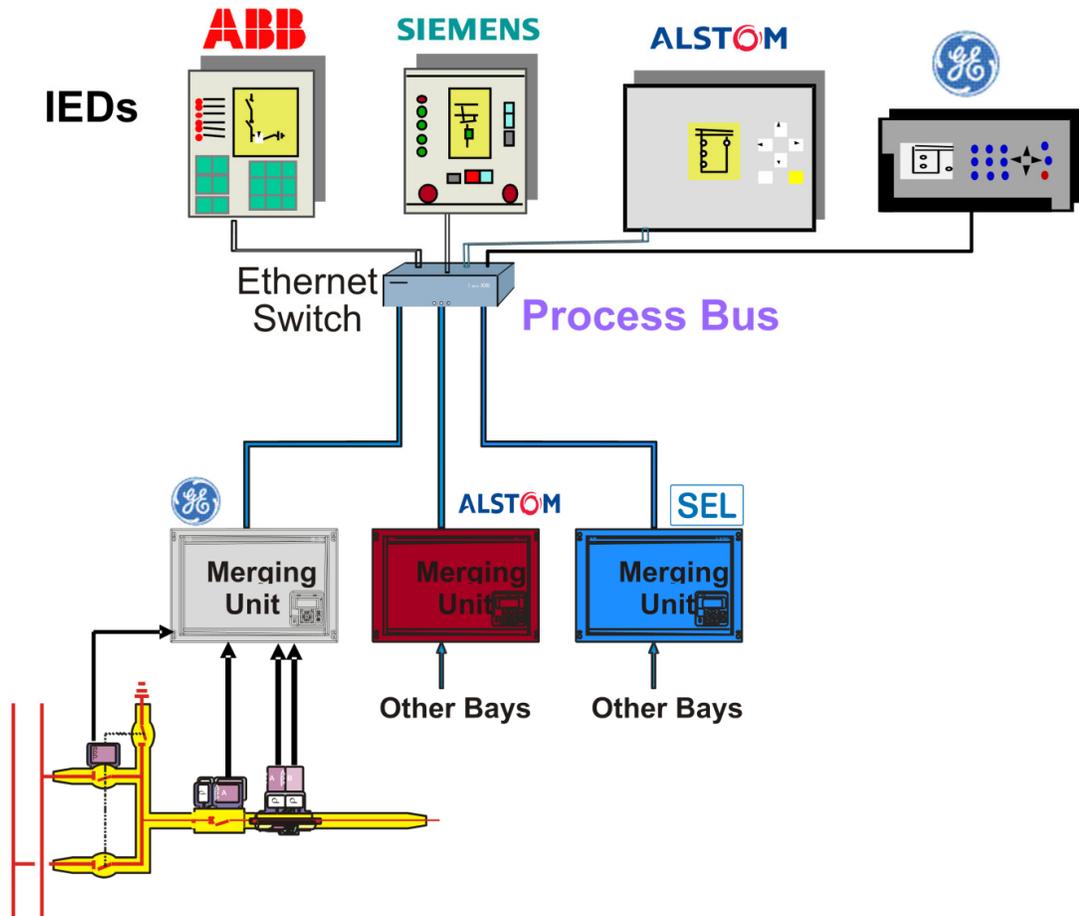


Figure 1-6 An abstract representation of interoperability at process level

1.4 Technical Challenges with Process Bus for Substation Protection

After implementation and testing of GOOSE based on the IEC 61850-8-1 standard at several substations and test facilities worldwide [24]-[26], major manufacturers are currently working on interoperable products for the time critical SV applications based on IEC 61850-9-2 [13] over the Ethernet networks to reduce labor cost and complexity of the copper wiring between switchyard and control room [27]-[30]. Major manufacturers are engaged in developing process bus devices which should be able to fit into any substation protection and automation network [31]-[34]. However, for the successful implementation of time critical substation protection application over the process bus network, the issues, such as performance of time critical messages over Ethernet communication network, as well as the reliability and availability of communication

architectures, need to be analyzed [6], [35], [36]. The technical challenges for the process bus implementation identified in literature are listed as follows:

1.4.1 Dynamic performance of communication network

The performance of a communication network is mainly dependent on the end-to-end packet delay and packet loss especially for the important piece of information. IEC 61850-5 standard [37] specifies the allowable message transmission delay requirements, and approaches that could be used to study the Substation Automation Systems (SAS) network performance. These time delay requirements have to be achieved for the time critical messages e.g. GOOSE and sampled values, independent from the network traffic load on the process bus communication network. The overall system performance and its extensibility cannot be easily solved using this standard, although it does classify the message performance class and LAN simulation method. There is no guidance available in the standard on how to characterize message delivery performance across the whole substation communication network [38]. On the other hand, although the switched Ethernet eliminates the problem of collision by making the communication full duplex (all the stations connected to the switch can send and receive packets simultaneously), the delay bounds cannot be predicted, as the queuing delay is not constant and packet buffers have limited size [39]. This results into nondeterministic message delays and/or loss. Therefore, for the dynamic performance of a physical SAS network, LAN simulation tools must be used. In IEC 61850-5, Section- I.2, an SAS network's dynamic performance was studied using COMNET III simulation program without stating how the IEDs are modeled and which worst case scenarios were considered. References [40], [41] have demonstrated preliminary simulations of overall substation automation network without modeling IEC 61850 based communication stack in OPNET [42]. OPNET is an industry-trusted commercial simulation tool for the communication networks, and the substation automation analysis using this tool is available in several literatures [38], [40], [41]. T. S. Sidhu and Y. Yin in [38], [43] have proposed IEC 61850 based models for a protection and control IED and a merging unit in OPNET. However, it is important to consider the impact of various communication network parameters, such as Ethernet

switch buffer size and packet service rate, bit error rate of communication port, etc while studying dynamic performance of the communication LANs [44], [45].

1.4.2 Loss/delay of time critical protection messages

To reduce additional time delay caused by TCP/IP (Transmission Control Protocol/Internet Protocol) layers, GOOSE and sampled value messages are directly mapped on the Ethernet link layer. However, this elimination of TCP/IP layer reduces the reliability of packet communication [46], [47]. Therefore, to enhance the transmission reliability of GOOSE, the same GOOSE message is repeated several times according to the IEC 61850-8-1 standard. GOOSE is an event triggered message, and generally sent fewer times in a second to the network; whereas, sampled value messages are time triggered and transmitted at the rate of sampling frequency. Thus, the same sampled value message is not repeated, which reduces transmission reliability of sampled value messages over the process bus. Although the priority tagging along with Virtual Local Area Network (VLAN) is applied to the sampled value packets, this does not ensure the determinism of communication delays and packet loss on the network during worst case conditions [48]. Therefore, it is important to carry out detailed dynamic analysis of IEC 61850-9-2 based process bus communication network in order to quantify the rate of SV loss or delay for various protection functions.

The SV loss or delay applies to entire the sampled value packet, which includes voltages and currents obtained at the same time stamp from the corresponding CTs/VTs. Therefore, SV loss/delay may have adverse impact on protective relaying. References [49], [50] have demonstrated the impact of SV loss on the performance of digital relaying protective functions, and presented adaptive filtering for single sampled value loss. The digital relaying algorithms of the currently deployed IEDs into the substation are not designed for the process bus contingencies, such as, SV packet delay or loss. C. Hoga in [51] has stated that the SV loss at the protection relay can have some kind of measuring blackout for the entire measuring window. In order to consider process bus communication networks for the future digital substation protection and automation, there should be a technique to alleviate impact of multiple sampled value loss/delay on

substation protection. Therefore, the process bus product developers have shown the need of smart algorithms for the treatment of lost/delayed SV data [35], and also re-sampling algorithms for the next generation IEDs [28].

1.4.3 Reliability of IEC 61850 based Ethernet architectures

IEC 61850-3 standard [52] refers IEC 60870-4 standard [53] for the details of reliability requirements, and states that there should be no single point of failure which can cause the substation to be inoperable. However, IEC 61850 does not demand for any redundancy, and it is left to substation design engineer [35]. Therefore, it is immensely important to analyze the reliability of process bus Ethernet architectures for substation protection systems. References [54], [55] presented the impact of process bus Ethernet networks on the reliability and availability of protection system using a preliminary Reliability Block Diagram (RBD). Safety related availability of an interlocking function in IEC 61850 based substation automation system was analyzed using a 3-state Markov model in [56]. References [57]-[60] have shown reliability of the different Ethernet communication configurations as applied to a substation automation system using the RBD and fault-tree methods. Furthermore, reference [61] included impact of repair rates on Mean Time To Failure (MTTF) and Mean Time To First Failure (MTTFF). However, there is no literature available to demonstrate the reliability evaluation of protection system based on IEC 61850-9-2 process bus, considering time synchronization techniques, as well as, various practical Ethernet switched architectures (according to IEEE PSRC report [8], these architectures are cascaded, ring, star-ring, and redundant-ring). Moreover, reliability analysis of process bus Ethernet architecture should be applied to a typical substation layout for the purpose of comparison.

1.4.4 Impact of process bus on reliability indices of digital protection functions

Reliability models for the traditional copper wire based protection systems are proposed in various literature sources. J. D. Grimes introduced a method to calculate the probability of failure of protective relay systems in [62]. References [63] and [64]

presented the reliability assessment of protection systems using fault-tree method; whereas, L. Castro Ferreira et al [65], [66] analyzed reliability of protection and control systems using event-tree method. The limitation of these combinatorial methods (e.g. fault-tree, event-tree, etc.) is that they cannot model more than two states (operational or failed) of the system. Additional states, such as degraded, under test, temporary failure, reconfiguration, etc., which are important for the detailed modeling of digital protection functions are not recognized in most of the cases. Therefore, Markov modeling is used for this work. A Markov model in references [67]-[70] defined the reliability indices for the protection systems, such as, unavailability of a protection system and abnormal unavailability considering various states of protection systems. This work is extended by M. F. Firuzabad et. al. in [71]-[73] by considering monitoring and self-checking features of digital protective relaying, as well as recognizing software and human errors. However, the literature has reported the Markov models of digital protection function only with traditional copper wired based protection. Therefore, it is important to extend these existing Markov models to consider IEC 61850-9-2 based process bus communication network, and also to study the impact of process bus communication networks on the proposed reliability indices of substation protection functions. There is no such Markov model available in the literature for this analysis.

1.4.5 Other Challenges

Other technical and non-technical challenges [74] related to the process bus are discussed below:

1.4.5.1 Time Synchronization issues

IEC 61850 proposes the implementation of time synchronization on LAN using Simple Network Time Protocol (SNTP). However, SNTP is able to provide accuracy of about 1 ms, which is not sufficient for raw data sampled values. One of the solutions is to use IRIG-B synchronization signal [75]. Nevertheless, IRIG-B needs an external time synchronization source, and accuracy of sampled values depends on the availability and quality of time synchronization. One of the solutions to the time synchronization problem is proposed in reference [27] using GOOSE message for sampling the analog values into

the MUs by using point-to-point communication links between IEDs and MUs. However, it is difficult to achieve interoperability using relative time synchronization method. A third potential time synchronization technique is over process bus Ethernet network using IEEE 1588 standard [76]. Next revision of IEC 61850 standard may include IEEE 1588 based time synchronization in order to achieve accuracy in the range of 1 μ s.

1.4.5.2 Data Security issues

IEC 61850-3 refers IEC 60870-4, Section-3.4 [53] for the details of security requirements. An intruder in a power substation can easily cause packet swamping, port reservation, etc. which would introduce a large time delay or data loss even for high priority messages. This may cause damage to many substation devices. Furthermore, data security is even more important while exchanging data with a control centre or other substations. Firewalls, encryption (encrypt data at sending end and decrypt data at receiving end with secured key), and authentication (authenticating user by security password or biometrics) can address data security issue to some extent [44]. Security auditing for IEC 61850 based substation automation system is carried out in [77], [78]; however, further security measures need to be studied to secure substation communication infrastructures. WT15 of TC57 works on security solutions for the substation protocol [79].

1.4.5.3 EMI immunity

Various electromagnetic interferences such as, lightning strikes, switching surges, electrostatic discharges, strokes in SF6 circuit breaker, etc. are commonly encountered in Air Insulated Substation (AIS). Hence, general EMI immunity requirements used for industry are not sufficient for AIS. IEC 61850-3 specifies only the outline of EMI immunity requirements. IEC 61850 refers to the requirements and testing procedures given in the parts of IEC 6100 series (IEC 61000-6-5 and IEC 61000-4-x) [80] or IEEE C37.90.2 [81]. All the SAS devices such as IEDs, MUs, Ethernet switches, and other communication devices must be in compliance with these EMI immunity standards especially at the process bus level.

1.4.5.4 Version upgrade issues

As discussed earlier, IEC 61850 provides free configuration, which would lead to segregation of single zone functions. Hence, single zone operation is dependent on proper hardware and software configuration of various devices installed by different manufacturers. It is also possible that a version update in any installed IED hardware or software may not support co-ordination with the existing versions from different manufacturers. This may lead to the need for updating the complete zone of functions which includes many devices of various manufacturers [35].

1.4.5.5 System expansion planning issues

IEC 61850 does not suggest any specific architecture and hence, system expansion related issues are not addressed in the standard. However, as power demand increases, power substations need to be expanded. Therefore, issues related to system expansion need to be addressed during the planning stage itself [35]. Addition of more IEDs and MUs should not create heavy traffic flows into the communication network. Proper and careful design of the process bus network is required to achieve scalability.

1.4.5.6 Manpower training issues

Communication network will be the backbone of the SAS. Hence, substation engineers will have to acquire complete networking training [35]. This is major issue with utilities to train substation engineers and keep updating them with fast growing communication technology.

1.5 Motivation

IEC 61850 based process bus communication network can offer several advantages, such as, interoperability, overall labor cost savings, and flexible architecture. However, it can be inferred from the above literature survey that some of the major technical issues, such as performance of process bus communication network, especially for time critical SV data for substation protection applications; reliability of the process bus communication

architectures, and their impact on reliability indices of protection functions are left unanswered. Although, IEC 61850-9-2 process bus has proven to be an attractive and economical technology, it is important to examine its feasibility for substation protection systems, in terms of performance of time critical SV messages over Ethernet switched process bus network, as well as, the reliability of a protection function considering process bus communication networks.

1.6 Research Objectives and Methodology

With these motivations, an exhaustive research work is carried out to investigate the impact of process bus communication network on the performance and the reliability of substation protection functions. The highlight of research objectives are listed below:

1. Detailed dynamic modeling and performance analysis of process bus communication networks for different protection functions of a typical substation.
2. Studying the number of sampled values lost/delayed at various substation protection IEDs over the process bus, and developing a sampled value estimation algorithm which can counteract adverse effects of multiple loss/delay of sampled values.
3. Development of hardware facility based on IEC61850-9-2 process bus network to demonstrate the implementation and testing of the proposed sampled value estimation algorithm as a part of some of the typical protection functions (e.g. biased-differential protection of substation busbar, and distance protection of transmission line) within a laboratory environment.
4. Evaluation of the reliability and availability of the process bus based substation protection systems, and also the comparison of the reliability and availability of various practical process bus communication networks for a typical substation layout.
5. Extension of Markov model for protection system reliability evaluation by considering process bus communication network, and studying the impact of process bus on protection reliability indices.

The specific research methodology to carry out the above listed research objectives at different stages is described below:

Stage-1. Performance of substation protection over IEC 61850-9-2 based process bus communication network

According to IEC 61850, the maximum acceptable delay for the time critical messages of substation protection, such as raw data SVs and GOOSE should be within 3 to 4 msec. Therefore, to reduce additional time delay caused by TCP/IP (Transmission Control Protocol/Internet Protocol) layers, IEC 61850 has proposed direct mapping of these time critical messages over data link layer by eliminating the TCP/IP layers. However, this elimination affects reliability of message transmission, i.e. reception of time critical messages is not guaranteed. Thus, IEC 61850 proposes repetition of the same GOOSE message several times over the communication networks. On the other hand, repetition of SV time critical messages cannot be proposed in order to limit the huge traffic over the network. Hence, there is no assurance for the SV message communication over the IEC 61850-9-2 based process bus. Thus, the detailed dynamic performance analysis of the process bus for time critical SV messages is carried out using industrial simulation tool, OPNET. The models for IEC 61850-9-2 process bus devices, such as protection IED and merging unit are developed in the OPNET. Moreover, as suggested in IEC 61850 part-9, various communication protocols such as VLAN (IEEE 802.1Q) and QoS (priority tagging based on IEEE 802.1p) are implemented in to the process bus model of the OPNET. Finally, the sample value packet loss and packet delay are studied for different process bus scenarios.

Stage-2. Sample value estimation algorithm for IEC 61850-9-2 process bus

To improve the performance of digital substation protection functions in case of SV loss/delay, a generic SV estimation algorithm is proposed which can be applicable to any digital protection system. To test the performance of the proposed algorithm for various scenarios, a typical substation is simulated in PSCAD/EMTDC software to obtain raw data SVs, and different scenarios of multiple SVs loss are created with the help of MATLAB. Finally, the error analysis is carried out, before applying to digital relaying

algorithms, to study the accuracy of proposed SV estimation algorithm by considering the effects of Source Impedance Ratio (SIR) and Point-On Wave (POW) of the fault, noise level into power signal, sampling frequency, and instance of SV loss.

Stage-3. Hardware implementation of sampled value estimation algorithm in the laboratory environment

The proposed sampled value estimation algorithm should be implemented and tested before applying to any commercial protective relaying. Therefore, hardware laboratory is setup for a typical IEC 61850-9-2 based process bus network with substation protection systems. The developed testing facility includes the development of various digital protection devices, e.g. protection IEDs, and MU real-time playback simulator over industrial embedded systems with a hard-real-time platform; implementation of IEEE 1588 based time synchronization over the process bus using the GPS signals; and configuration of IEC 61850-9-2 based Ethernet networks using the commercial Ethernet switches. The performance improvement of the busbar differential and the transmission line distance protections using the proposed sampled value estimation algorithm is analyzed with a series of experiments.

Stage-4. Reliability analysis of process bus communication architectures

To study the impacts of process bus communication network on the reliability of substation protection functions, the analysis is started with the development of Reliability Block Diagrams (RBD) for various practical process bus architectures, considering Ethernet configurations (e.g. cascaded, ring, star-ring and redundant-ring), as well as, time synchronization techniques (e.g. IRIG-B and IEEE 1588). Thereafter, the combinatorial reliability of protection system is analyzed using RBD method. Also, the failure rates of these process bus architectures obtained from RBD method can be used for the further Markov modeling.

Stage-5. Impact of process bus communication on reliability of substation protection

After obtaining the failure rates of practically possible process bus communication architectures with different time synchronization techniques using the RBD, the existing Markov models of protection system (from literature) is extended to accommodate the IEC 61850-9-2 based substation protection functions. With this proposed Markov model, the reliability indices of protection systems, such as, protection unavailability, abnormal unavailability, and loss of security are obtained to compare the traditional protection functions with the next generation IEC 61850-9-2 based protection functions. Moreover, the impact of SV loss/delay on the reliability indices of a protection system, and possibility of improvements with the help of the proposed SV estimation technique is studied using the proposed model. In addition to that, the sensitivity analysis of time synchronization techniques, process bus network reconfiguration, monitoring effectiveness, and failure rate of protection IED on protection reliability indices is carried out in detail.

1.7 Organization of the Thesis

This thesis is organized in eight chapters and five appendices.

Chapter 2 discusses salient features of the IEC 61850-9-2 based process bus communication network for substation protection systems, including time critical messages (SV and GOOSE) for protection, retransmission mechanism of a GOOSE, SV multicasting, accurate time synchronization techniques, and fast and flexible Ethernet architectures. Moreover, this chapter also provides an overview of the practical Ethernet architectures reported by IEEE PSRC Committee for process bus, as well as, potential time synchronization methods (IRIG-B and IEEE 1588).

The performance evaluation of the IEC 61850-9-2 based process bus communication network is presented in Chapter 3. Industry-trusted performance analysis tool, OPNET, is used to develop detailed models for studying the performance of a process bus. Important parameters of a communication network, such as communication link speed, bit-error-rate, background traffic, Ethernet switch buffer size and its packet service rate, priority tagging, and VLAN configuration are considered for the detailed dynamic analysis of

IEC 61850-9-2 based network. A typical substation process bus network is considered, and analysis in terms of delay and loss of SV is presented in detail.

In order to counteract the SV loss/delay in a digital protection IED, the SV estimation algorithm is proposed in Chapter 4. Moreover, the accuracy of estimated several consecutive SVs is analyzed for various Source Impedance Ratios (SIRs), and Point-On-Waves (POWs) of the power system faults, noise levels, sampling frequency, and SV loss instances. The comparison among the estimation techniques up to third order is presented with the one without estimation.

The proposed SV estimation algorithm, a corrective measure for SV loss/delay, should be implemented and tested for digital protection systems. Therefore, the work is carried out in Chapter 5 to develop IEC 61850-9-2 based process bus network as well as devices. The developed IEC 61850-9-2 enabled devices include, protection IEDs, merging unit simulator to generate SV packets in real time from the power system simulated in PSCAD/EMTDC, traffic generator, and network analyzer. Moreover, time synchronization over the network is implemented in this developed lab setup using commercial Ethernet switches in compliance with IEEE 1588 standard and GPS synchronization source. Finally, this chapter presents the implementation of the proposed SV estimation algorithm as a part of a busbar differential protection IED, as well as a transmission line distance protection IED. And, the extensive testing is carried out to examine the SV estimation algorithm performance for various SV loss/delay scenarios and power system fault conditions.

In addition to the enhancement of the performance of substation digital protection systems with SV estimation algorithm, this work also presents reliability analysis by proposing reliability models for the IEC 61850-9-2 enabled digital protection systems. Chapter 6 develops the reliability block diagrams in order to analyze combinatorial reliability (a reliability analysis method which considers series-parallel combination of the components) of the IEC 61850-9-2 based various Ethernet architectures and time synchronization techniques. The Extended Markov model of the IEC 61850-9-2 enabled protection system is proposed in Chapter 7. And, the different values of communication

architecture failure rates used in Markov model are obtained from Chapter 6. Finally, the impact of process bus communication network on substation protection functions, and sensitivity analysis is presented by comparing the reliability indices of protection systems obtained from the proposed Markov model.

The major outcomes from the research and conclusions from the entire work are highlighted in Chapter 8. This chapter also discusses possible further work from this thesis.

1.8 Summary

A brief introduction to IEC 61850 standard and its specific part-9-2 for the process bus is discussed in this chapter. Major benefits and technical challenges related to the IEC 61850-9-2 based process bus communication network is described from exhaustive literature survey. With the motivation to address the major challenges of the process bus, the specific research goals and methodology to achieve these goals are described. The next chapter will provide detailed understanding of IEC 61850-9-2 based process bus network by discussing practical Ethernet architectures, and suitable time synchronization techniques.

Chapter 2

2. IEC 61850-9-2 Based Process Bus for Digital Protection Systems

This chapter includes the salient features of IEC 61850-9-2 based process bus, such as time critical protection messages (GOOSE, SVs), retransmission of GOOSE, SV multicasting, time synchronization techniques, and Ethernet switched configurations. Thereafter, various process bus architectures considering different Ethernet switched architectures (e.g. cascaded, ring, star-ring, redundant ring, etc.), and time synchronization techniques (e.g. IRIG-B and IEEE 1588) are discussed in detail.

2.1 Features of IEC 61850-9-2 Process Bus

IEC working group TC57 has published IEC 61850 named as “Communication Networks and Systems in Substation” in 2003 [2]. Initially, IEC 61850 standard was divided into total 10 parts, which covers not only how to communicate but also what to communicate. This standard provides the interoperability between two devices of different manufacturers in the same substation by defining the communication protocol and universal modeling of logical node into SAS functions. The high-speed digital communication at process level allows replacing the traditional electrical wiring using virtual wiring, which could save a lot of time and cost while implementing substation automation system. The major features of IEC 61850-9-2 are discussed below:

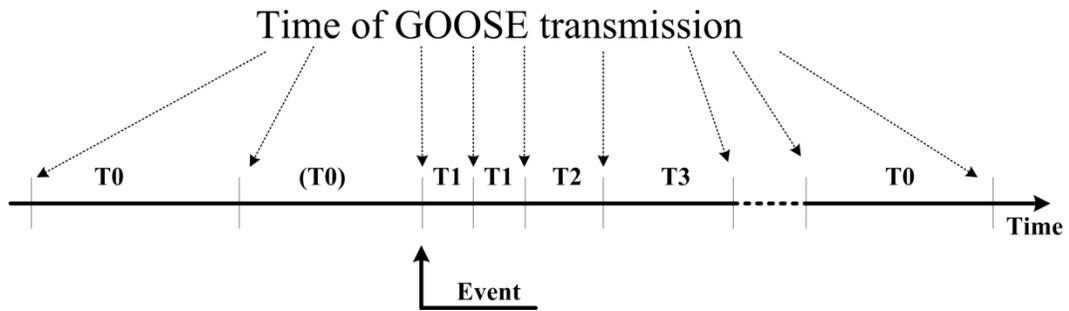
2.1.1 Time critical protection messages over process bus

There are basically two types of processes: 1) event triggered; 2) time triggered. In case of event triggered, message is sent due to occurrence of a certain event e.g. state change. The receiving node may perform operations pertaining to that event (e.g. computation of algorithms). For time triggered, message is populated at the specific predefined instance

of time. Since, the period of the time triggered SV message is normally small (approx. 0.2 msec for 4800Hz sampling frequency), the traffic over the process bus due to SVs from various MU occupies large portion of the network channel bandwidth. It may be required that the time between the event generation and the computation of the algorithm be bounded.

2.1.2 Retransmission mechanism of GOOSE

To achieve a highly dependable level of GOOSE message delivery, the IEC 61850-8-1 specifies a retransmission scheme for GOOSE messages, as shown in Figure 2-1.



T0 : Retransmission in stable conditions (no event for a long time)

(T0) : Retransmission in stable conditions may be shortened by an event

T1 : Shortest retransmission time after the event

T2, T3 : Retransmission time until achieving the stable conditions time

Figure 2-1 Transmission time of GOOSE messages

After initiation of any status change, GOOSE messages are published repeatedly. At the time of configuration, parameter called maximum time is set in each GOOSE message to wait between message publication, and the name of the data set to include in the message. In case, maximum time expires or any data set value changes, a GOOSE message is published over the network. After a change in the data set elements i.e. some event takes place, GOOSE messages are sent repeatedly with incremental periods, to make sure that all subscriber IEDs will receive them across non deterministic Ethernet. Each message includes the total time to live, which forecasts the time delay before the next message will be published so that subscribers can monitor correct data flow. When a new data set event

occurs (in this case, a binary change of state or an analog passing through a reporting dead band), a new message is created and published. The new data set event information is transmitted and repeated in the shortest T1, as shown in Figure 2-1. The retransmission time gradually increases from T2 to T3, and eventually settles at a stable retransmission time. This stable retransmission time is shortened when the next new event occurs. Subscribers constantly calculate time to wait, based on time to live within each message. The subscriber considers data “stale” when time to wait *expires* and they have not received a new replacement message from the publisher. If the subscribing IED detects expiration of the wait time, it assumes that the communication is lost and modifies its relay logic accordingly. The message retransmission scheme is necessary to perform transmission from one to many and to allow the subscriber to know that the communications channel is healthy. However, depending on the choice of final stable retransmission time, it may not be sufficient to guarantee the reliability of time-critical tasks [82].

2.1.3 Multicasting of time critical messages

The protection devices over a process bus network, such as protection IEDs and MUs should support multicasting of time critical messages (GOOSE and SV). Multicasting feature allows sending same messages to multiple destination devices. This works based on subscriber/publisher mechanism, in which an IED or an MU multicasts or publishes a message to all subscribed IEDs and MUs. Since, the time critical messages are directly mapped to data link layer 2, all IEDs and MUs should support Ethernet data link layer-2 multicasting capability. This can be achieved through Ethernet MAC (Media Access Control) source and destination addresses, which are defined in the Ethernet packet frame. These addresses have 48 bits each to identify the frames destination and source addresses. A destination address either specifies address for single receiver IED or multicast address for a group of receiver IEDs. With the help of multicasting of time critical messages, the same message need not to be repeated several times to different locations, and the traffic over the network reduces considerably.

2.1.4 Time synchronization among process bus devices

The IEC 61850-9 proposes digital process bus, which means digitization of analog signals at the switchyard into the MUs. These digital sampled values are communicated to bay level IEDs through process bus communication networks. Sampled values, generated from a MU located at different locations of a switchyard, should be synchronized to a common reference time stamp for a bay level protection IED. The two major solutions available currently to achieve accuracy in the range of 1 μ s are: 1) IRIG-B synchronization signal [75]; 2) IEEE 1588 based PTPv2 [76]. Due to time synchronization of all sampled values within a substation, any protection IED can utilize SVs from any MU, and this opens up new possibilities of digital protective relaying, as discussed in previous chapter. Furthermore details on these time synchronization techniques will be provided in following subsections of this chapter.

2.1.5 Fast and flexible Ethernet architectures

Ethernet was developed by the Xerox Corporation's Palo Alto Research Centre (known colloquially as Xerox PARC) in 1972. It is the most popular and widely deployed LAN technology in the world. Ethernet came to play in automation world in 1985. Since then, many Ethernet solutions such as Ethernet/IP, Modbus, Profinet, EtherCat are proposed and used in the industrial automation world. A modern practice is to use Ethernet switch network in substation automation systems. Ethernet switch is layer 2 or layer 3 device which has certain benefits compared to layer 1 devices i.e. a hub. Switch could read, buffer and forward frames to corresponding MAC address in full-duplex mode, as a result there is no need of CSMA/CD protocol. In addition to that, switch has following features, which are essential for the high-speed real time performance [83].

- a. **IEEE 802.3x Full-Duplex** operation on all ports ensures that no collisions can occur over the network.
- b. **IEEE 802.1p Priority Queuing** which allows frames to be tagged with different priority levels in order to ensure that a real-time critical traffic always makes it through the network even during high periods of congestion.

- c. **IEEE 802.1Q VLAN** which allows the segregation and grouping of specific ports into virtual LANs in order to isolate traffics of different applications.
- d. **IEEE 802.1w Rapid Spanning Tree Protocol** which allows for the creation of fault tolerant ring network architectures that will reconfigure in milliseconds as opposed to tens of seconds as was the case for the original Spanning Tree Protocol 802.1D.
- e. **IGMP Snooping / Multicast Filtering** that allows for multicast data frames, such as GOOSE frames, to be filtered and assigned only to those IEDs which request to listen to them.
- f. **Various combinations of 100Mbps and 1Gbps ports** which facilitate the connections between IEDs and the switch.

2.2 Ethernet Switched (ESW) Architectures for Process Bus

The basic Ethernet switched architectures include cascaded, star, and ring. The practical architectures for SAS may be hybrids of these three basic combinations. In this work, following Ethernet communication architectures are considered, as recommended by IEEE PSRC report [8] are discussed below.

2.2.1 Cascaded Ethernet architecture

A typical cascading architecture is illustrated in Figure 2-2. All four Ethernet switches (ESWs) are cascaded without having any loop.

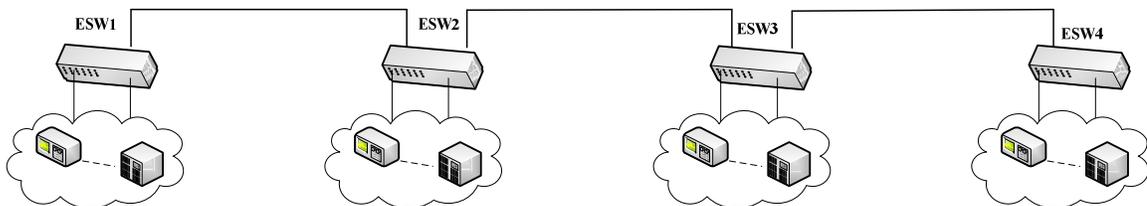


Figure 2-2 Cascaded Ethernet architecture

This architecture is simple and less expensive, as there is no need for any routing protocol in the Ethernet switches. However, the time delay (latency) of this configuration would be higher comparatively.

2.2.2 Ring Ethernet architecture

As shown in Figure 2-3, ring architecture is very similar to the cascaded architecture except that the loop is closed from the last switch to the first switch. Ethernet switches do not support loops. Therefore, it is required to employ managed switches (i.e. those with a management processor inside) with the Rapid Spanning Tree Protocol (RSTP) (IEEE 802.1w). This protocol allows switches to detect loops and internally block messages from circulating in the loop and also allows reconfiguration of the network during communication network fault within few hundreds of millisecond. This architecture has potential to offers the better reliability because it facilitates n-1 redundancy i.e. IEDs can still communicate even if any one of the ring connections and/or ESW fails. However, this architecture is costly and complex, and does not improve any network latency.

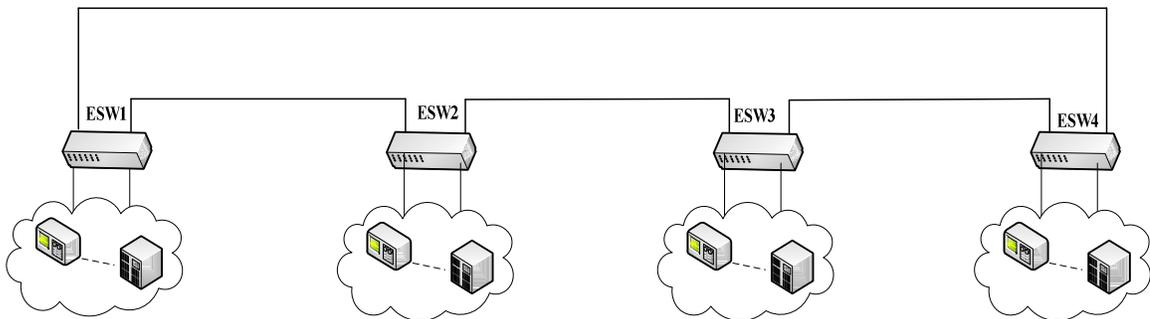


Figure 2-3 Ring Ethernet architecture

2.2.3 Star-ring Ethernet architecture

In star-ring LAN architecture as shown in Figure 2-4, each bay level Ethernet switch is connected directly to two redundant main Ethernet switches. Both these main Ethernet switches are connected in ring. This provides higher redundancy as well as low latency; however, this requires two additional switches to arrange the network in star-ring configuration.

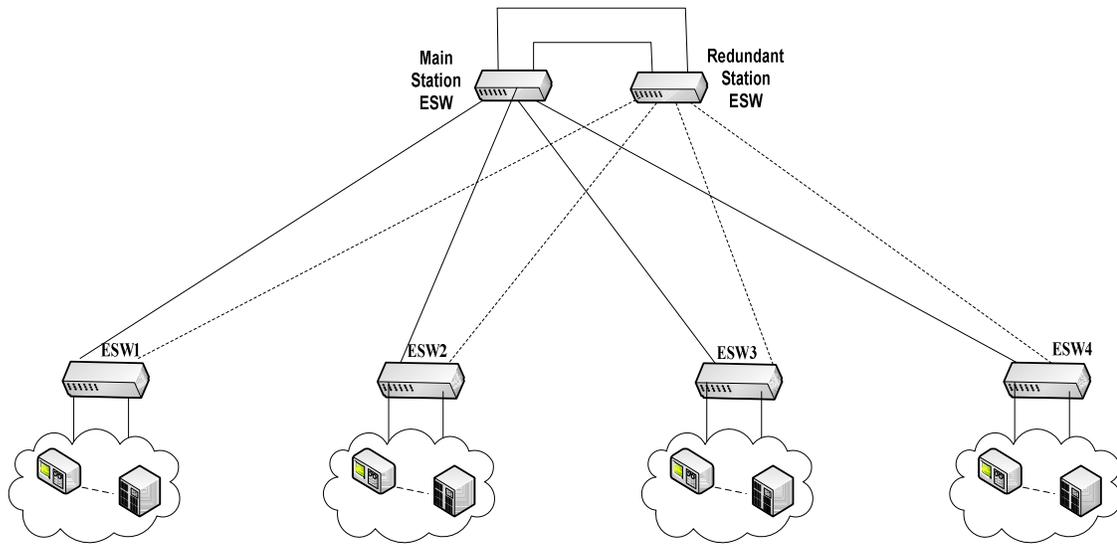


Figure 2-4 Star-ring Ethernet architecture

2.2.4 Redundant-ring Ethernet architecture

Figure 2-5 shows the redundant-ring architecture, which provides two completely redundant rings. Further, both these rings are connected again in ring of four main Ethernet switches. This kind of architecture provides complete redundant ring network with medium latency. However, this architecture requires many managed Ethernet switches with rapid spanning tree protocol (IEEE 802.1w). Moreover, all the IEDs have to have two Ethernet ports which will again increase the cost. Hence, this network provides highest reliability; on the other hand, it suffers from high cost and complexity.

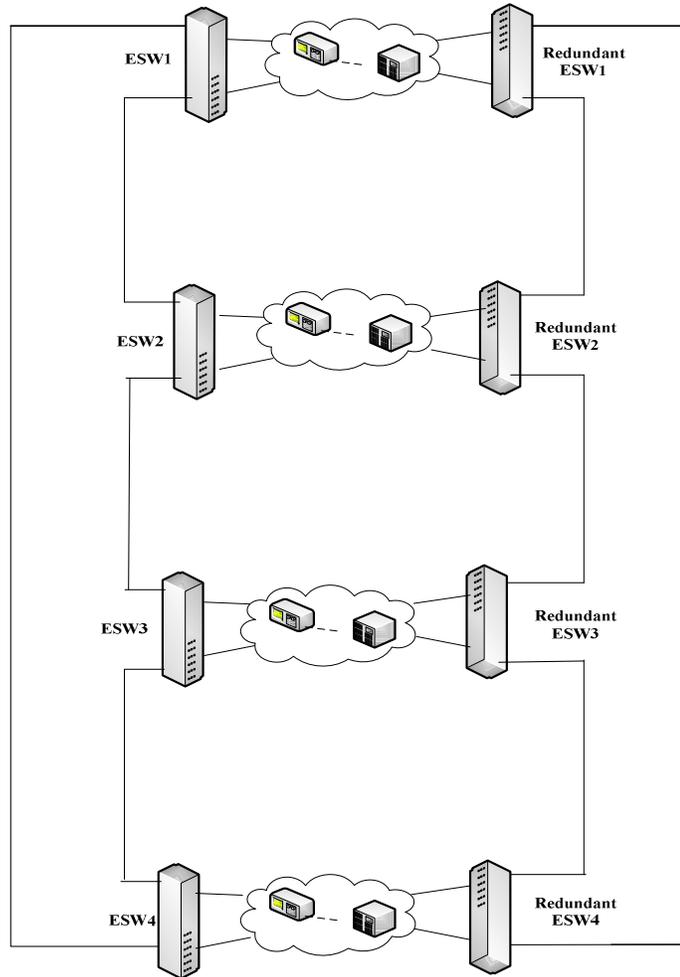


Figure 2-5 Redundant-ring Ethernet architecture

2.2.5 High redundancy protocols

Above mentioned ring based Ethernet switched architectures utilize RSTP protocol (in compliance with IEEE 802.1w) which has sub-second network recovery time. Currently, work is going on to develop process bus architectures based on IEC 62439-3 [84] to achieve highly reliable Ethernet switched networks with zero network recovery time. IEC 62439-3 proposes two protocols: 1) Parallel Redundancy Protocol (PRP) and 2) High availability Seamless Redundancy (HSR). The architecture of HSR network is almost same as ring architecture, whereas, PRP network is similar to redundant-ring architecture as discussed in previous subsection. In HSR network, the same message is circulated in two different directions, and therefore, destination receives it twice, which provides n-1

redundancy to each message transmitted over the network. However, HSR doubles the traffic over the ring network, thus speed of networking infrastructure should be very high. On the other hand, PRP circulates the same message in two different/redundant ring networks, which again result in n-1 redundancy while keeping the same speed of networking devices. However, PRP requires two separate communication network similar to presented redundant ring architecture. This way, both of these protocols are expected to provide seamless zero network recovery time, and networking infrastructure supporting this IEC 62439-3 protocol is currently under development [85].

2.3 Time Synchronization Methods for Process Bus

Currently, time synchronization with accuracy of 1 μ sec (required by protection application) can be achieved using two techniques, such as external time synchronization source based on IRIG-B protocol, and time synchronization over Ethernet data networks using IEEE 1588.

2.3.1 IRIG-B time synchronization

Currently one of the established time synchronization technologies which can satisfy the time synchronization accuracy requirements is using IRIG-B signal. The IRIG protocol was originally developed by the Inter-Range Instrumentation Group (IRIG), part of the Range Commanders Council (RCC) of the US Army [75], [86]. First time it was published in 1960 and latest version of Protocol was updated in September, 2004. IRIG – B time code is currently widely used as time synchronization protocol in substation automation system. This protocol is simple to implement, and it provides microsecond accuracy. IRIG-B time code has a pulse rate of 100 pulses-per-second with an index count of 10 milliseconds over its one second time frame. It contains time-of-year and year information in a BCD (Binary Code Decimal) format, and (optionally) seconds-of-day in SBS (straight binary seconds) [86]. The disadvantage of the IRIG –B is that, it requires dedicated/separate cabling infrastructure to implement it. All the devices requiring time synchronization are connected in daisy chain or in star topology using

coaxial cable. Also, internal optical isolation is required between devices and master clock to prevent ground loops.

The Figure 2-6 shows the process bus (Ethernet switch network) of a transmission line-1 protection bay with external Time Synchronization (TS) sources (based on IRIG-B standard) connected to all the merging units and protection IEDs. IRIG-B signal source may be connected to the individual Merging Units (MUs) and Intelligent Electronic Devices (IEDs) or shared between two closely located MUs. It can be observed that this architecture would increase the need of TS sources in a process bus. As shown in Figure 2-6, there can be complete redundancy in process bus architecture, e.g. MU-17, MU-18, and MU-29 are connected to redundant Ethernet switch (ESW-11) over the redundant network. Redundant line-1 protection IED-B is connected to redundant Ethernet switch architecture. The cloud of Ethernet switch is consist of 10 Ethernet switches connected in a ring.

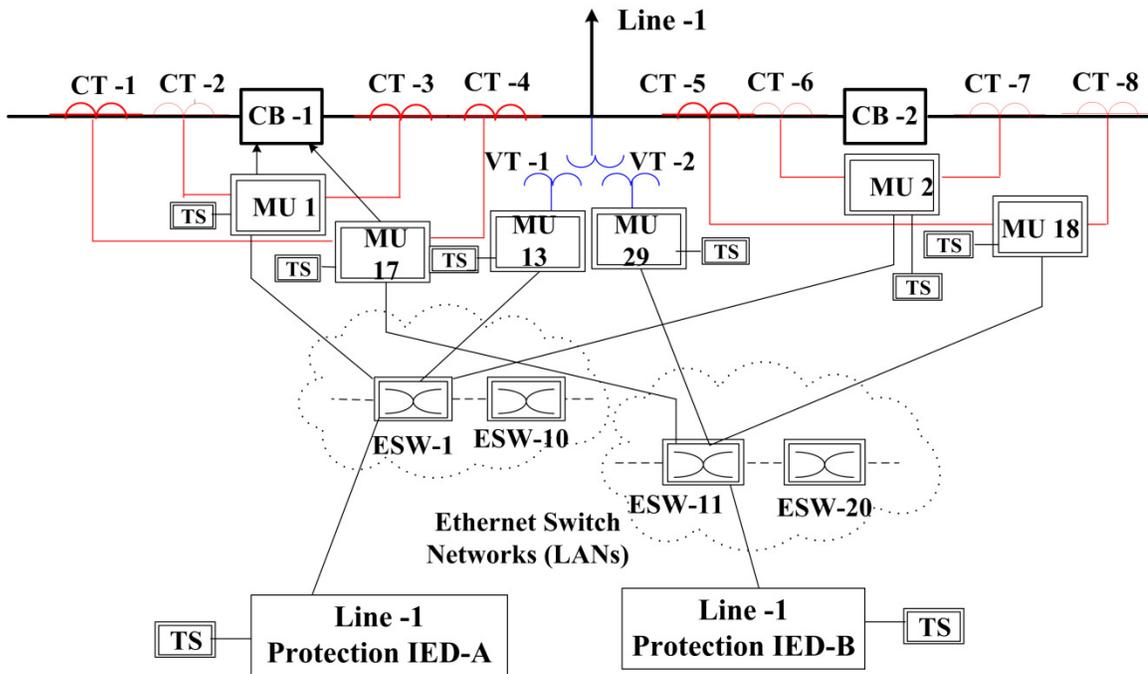


Figure 2-6 External TS using IRIG-B signal

2.3.2 IEEE 1588 based time synchronization

IEEE 1588, a standard for “Precision Clock Synchronization Protocol for Networked Measurement and Control Systems”, is modified by IEEE in March 2008, also known as

PTPv2 (Precision Time Protocol version 2) [76]. This improved protocol offer better accuracy and scalability compared to the currently used time synchronization technologies such as the Network Time Protocol (NTP) and IRIG-B (a high-precision serial protocol). It is designed to synchronize distributed clocks with an accuracy of sub-microsecond across a packet switched communication network, with relatively low network and computing capacity. Traditional synchronization technologies distribute only a common frequency, revised PTP also facilities distribution of common frequency, common phase-alignment, and common time-of-day (TOD). This IEEE 1588 PTPv2 is important for substation automation purpose, as it fulfills the timing accuracy requirements of current substation automation applications. Moreover, unlike IRIG-B, there is no need for dedicated cabling infrastructure network for time synchronization information. However, the Ethernet switches used for data communication should have IEEE 1588 PTP V2 capability.

The Ethernet switch network with IEEE 1588 based time synchronization is shown in Figure 2-7. The redundant time synchronization sources TS-1 and TS-2 basically provides the time synchronization signal in compliance with IEEE 1588 over the entire process bus using Ethernet switches. The compatibility with IEEE 1588 can be implemented in all devices using hardware and/or software.

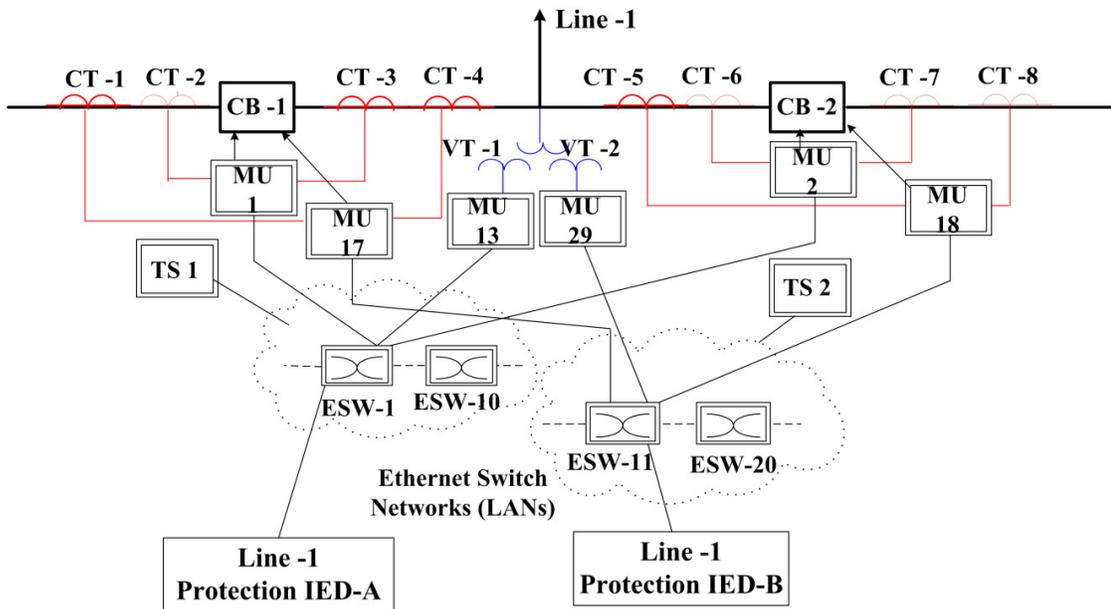


Figure 2-7 Time synchronization over the process bus network using IEEE 1588

2.4 Summary

This chapter discusses the major features of process bus proposed in IEC 61850-9-2 standard. Various process bus mechanisms, such as event and time triggered communication, GOOSE retransmission, SV multicasting, time synchronization are explained in detail. Furthermore, the flexibility of Ethernet switched architectures is presented by considering practical architectures discussed by IEEE PSRC committee report. Two potential time synchronization techniques, IRIG-B and IEEE 1588, suitable for substation protection applications (1 μ s accuracy) are described in detail. Next chapter will provide a detailed dynamic performance evaluation of the IEC 61850-9-2 based substation protection over a process bus communication network using the OPNET simulation tool.

Chapter 3

3. Performance Evaluation of IEC 61850-9-2 Process Bus Using OPNET

This chapter presents the performance analysis of substation protections over the IEC 61850-9-2 process bus network using the industry-trusted communication network simulation tool, OPNET [42]. For this, first of all the performance requirements (in terms of transfer time) suggested by the IEC 61850 standard is discussed. Thereafter, the efforts are put in this work to develop the dynamic models for several communication mechanisms and protocols, e.g. bit-error-rate on the communication channel and bit error correction mechanism at communication port; Ethernet switch packet buffer and buffer overflow mechanism; priority queuing mechanism for time critical packets, etc. In addition to that, dynamic models of Ethernet switch (ESW), fiber cables, transceiver ports, other IEC 61850 message traffics, etc. have also been developed to analyze more realistic scenarios for the IEC 61850-9-2 process bus performance evaluation. As discussed in the previous chapters, SV messages are not repeated as GOOSE, and therefore, it is important to analyze the loss/delay of SV over a process bus communication network. The results for the sampled value packet loss and delay are obtained by considering the impact of various process bus network parameters, such as, speed of the communication link, sampling frequency of the MUs, Ethernet switch buffer size and packet service rate, Bit Error Rate (BER) of the communication channel, and network background traffic.

3.1 IEC 61850 Communication Performance Requirements

As per IEC 61850, a transfer time is the time from the moment the sender (IED) puts the data content on the top of its transmission stack up to the moment the receiver (IED) extracts the data from its transmission stack. This is illustrated in Figure 3-1.

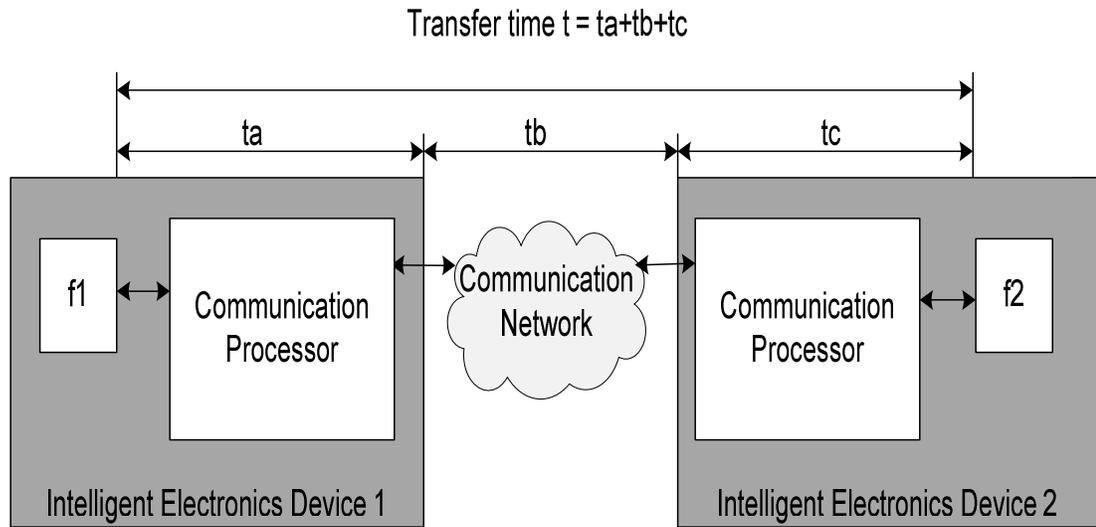


Figure 3-1 Transfer time definition

Piece of Information over Communications (PICOMs) refer to information transfer based on a single dedicated functionality, and include source and sink. The messages types are based on a grouping of the performance related PICOM attributes, and therefore, they define the performance requirements to be supported. The performance requirements are independent of the size of the substation, and are defined according to the application. According to IEC 61850-5 and IEC 61850-8, messages are classified into 7 categories based on the performance requirements. Table 3-1 summarizes these messages and transfer time requirements based on IEC 61850 standard. It can be observed from the table that the raw data samples (type 4) and GOOSE messages (type1, 1A) are time critical and are, therefore, directly mapped to data link or Ethernet layer, refer Figure 1-2. The medium speed message (type 2), low speed message (type 3), file transfer functions (type 5), and command message with access control (type 7) are not very time critical, and therefore, mapped to over TCP/IP stack above the Ethernet layer as shown in Figure 1-2. The time synchronization messages (type 6) based on NTP protocol are broadcasted to all IEDs in substation using UDP/IP. The UDP is connection-less networking protocol, whereas, TCP is connection-oriented protocol. Therefore, TCP/IP provides more reliability of message transmission, as compared to other UDP/IP or direct mapping over Ethernet [47].

Table 3-1 Message types & performance requirement in SAS

Sr. No.	Message Type	Application	Transfer Time Limit (ms)
1	Type 1 1a – Trip 1b – Others Message	Trigger	10-100
		Complex block or release	10-100
		Fast broadcast Message	1
		Process State Changed	1-10
		Trip	1
2	Type 2 Medium Speed Message	Process value in r.m.s	50-1000
		Request for syn. check interlocking	10-100
		Process State	1-100
		Calculated State	1-100
		External Condition	1-100
3	Type 3 Low Speed Message	Measured value	100-1000
		Meter value	100-1000
		Non – electrical Process value	1000-5000
		Fault value	1000-5000
4	Type 4 Raw Data Message	Process value (Sample voltage & Current)	0.1-10
5	Type 5 File Transfer	Report e.g. Energy list	1000-5000
		Mixed fault info.	1000-5000
		Mixed fault data	5000
		Event/Alarm List	100-1000
		ID data, Setting	1000-5000
		Diagnostic data	5000
6	Type 6 Time Synchronization Message	Synchronization pulse	0.1-10
7	Type 7 Command Message with Access Control Message	Command (From local to remote HMI)	1-1000

3.2 OPNET Modeler Simulation Tool

The OPNET Modeler tool facilitates the design and study of communication networks, devices, protocols, and applications with complete flexibility [42]. OPNET Modeler provides Proto-C (OPNET’s modeling language developed using C/C++) based object-oriented modeling approach, with many editors (Project editor, Node editor, Process editor, Packet editor) for detailed customization of the design as shown in Figure 3-2.

And hence, it is possible to develop any communication protocol or a device model with the OPNET code process, and node editors.

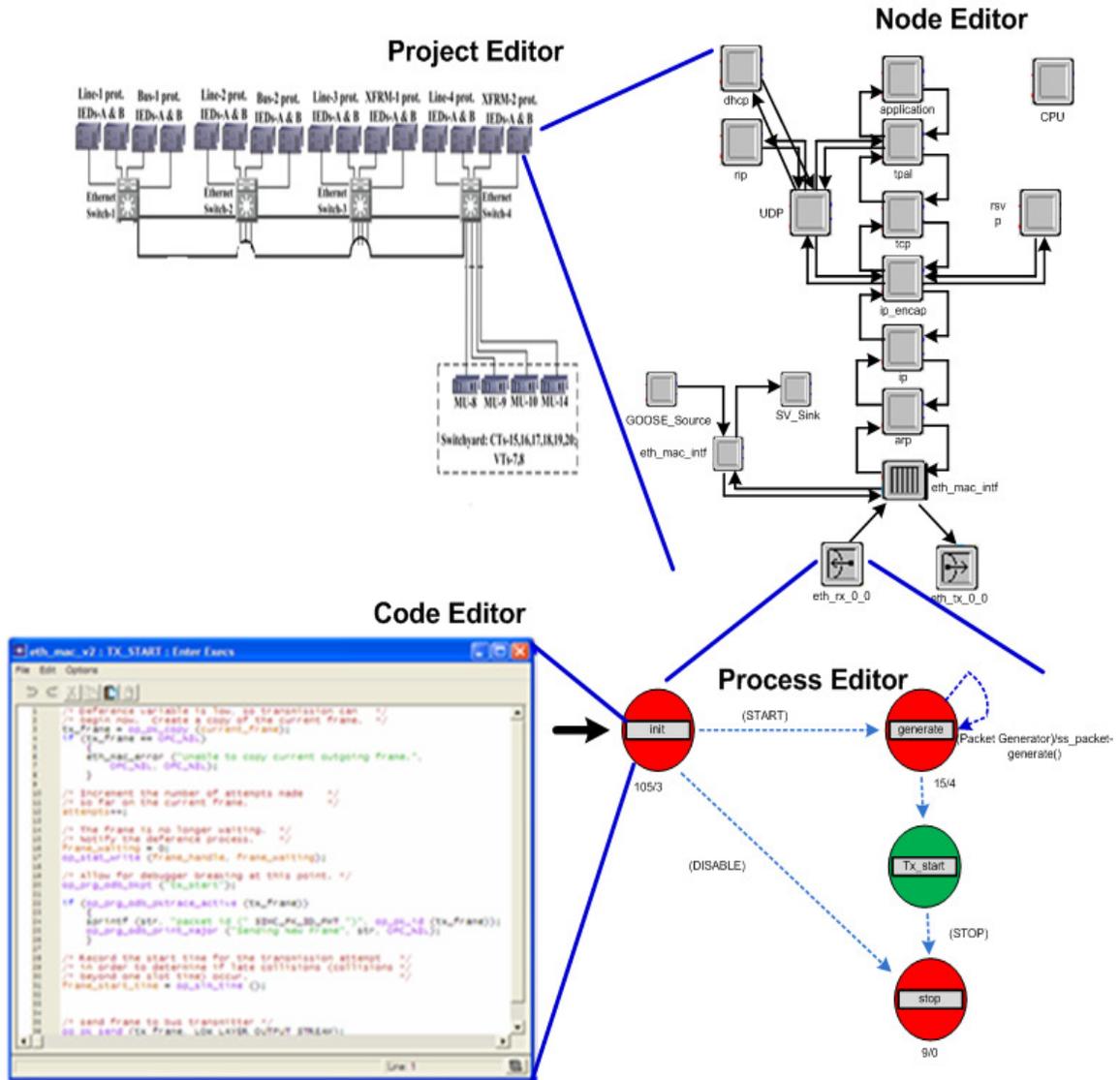


Figure 3-2 OPNET graphic editors

OPNET has four hierarchical editors as shown in the figure above:

1. Project editor: It represents the topology of a communication network using nodes
2. Node editor: It represents the architecture of network devices using modules

3. Process editor: It provides the implementation of any protocol logical flow using state-transition diagram. It defines the module process in response to events using transitional conditions and executives.
4. Code editor: It facilitates the programming environment, and can be opened from any module of the state-transition diagram in process editor.

OPNET offers the object-oriented modeling approach for the simulation of any computer network and its devices [42]. It facilitates the design and study of:

- ❖ Communication networks
- ❖ General or Vendor's devices
- ❖ Protocols

The following subsection presents modeling of IEC 61850-9-2 based process bus devices in OPNET.

3.3 Modeling of IEC 61850-9-2 Process Enabled Protection and Control Devices

3.3.1 Protection and control IED

The modeling of an IED shall be based on the communication stack specified in IEC 61850, (refer Figure 1-2). Protection and Control (P&C) IED has to communicate with MU IED, as well as other P&C IEDs. Hence, the P&C IED should have capability of interfacing directly at “mac” layer and with all the OSI-7 layer stacks. That is because, the P&C IED would send GOOSE message by directly mapping it to “mac” layer, whereas, for client-server communication (where there is no time critical-message), the P&C IED uses all the seven layers. As Figure 3-3 shows, the GOOSE message is directly mapped on the data link layer and other application messages are mapped using all 7 layers are present.

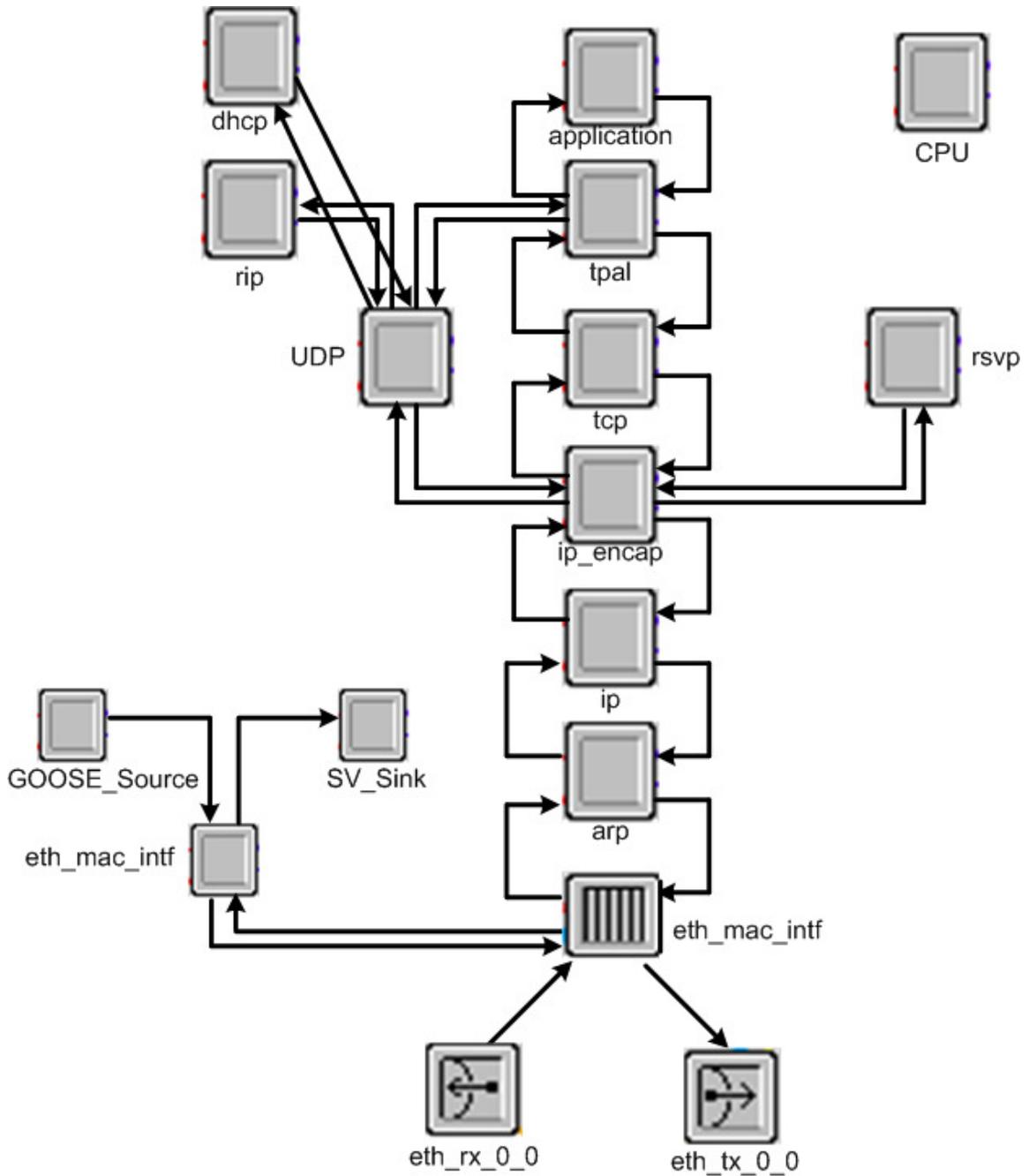


Figure 3-3 OPNET model for protection IED

3.3.2 Merging unit model

As the MU IED generate raw data packets, which are very time critical packets, the mapping of these packets is done directly on data link layer (unlike all OSI-7 layers). As Figure 3-4 shows that raw_data_source (raw packet generator), directly maps the SV

packets on mac module. *Eth_mac_intf* is the interface module between application layer and mac layer. eth_tx0 and eth_rx0 are the Ethernet transceiver, and it does the function of PHY layer.

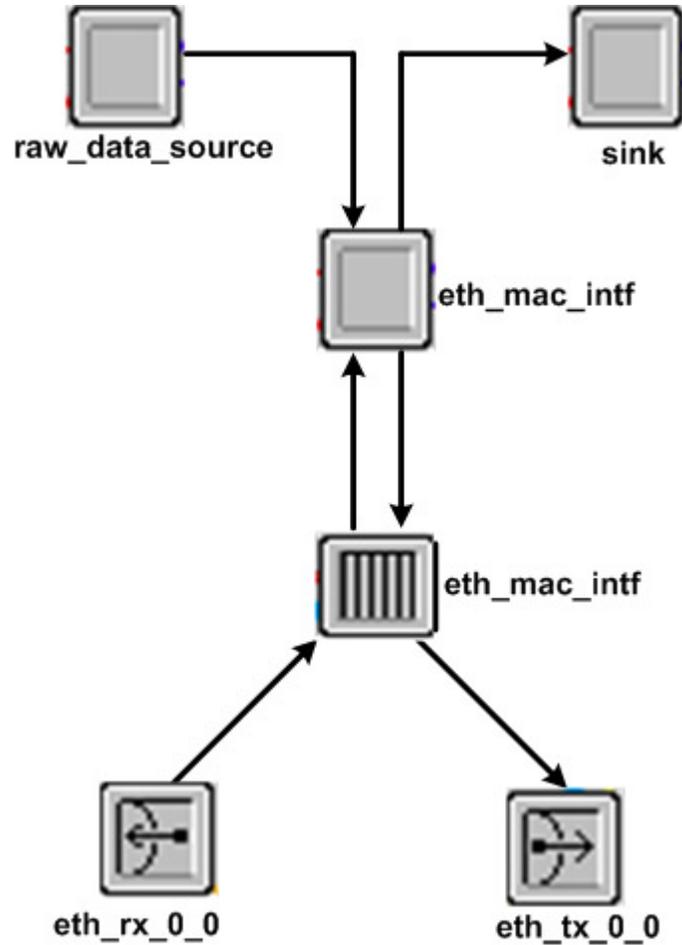


Figure 3-4 OPNET model for merging unit

Above models are used to model IEC 61850 based substation communication network in OPNET simulation environment.

3.3.3 VLANs and priority tagging

IEC 61850-9-2 recommends the implementation of VLAN/priority tagging based on the IEEE 802.1Q to achieve the Quality of Service (QoS) in process bus. As shown in Figure 3-5, the SV packets will have Tag Protocol Identifier (TPID) and Tag Control

Information (TCI) (defined in IEEE 802.1Q) fields between source MAC address and Ethertype fields. The value of TPID is 0x8100 (in hex). The 3-bits of the user priority in TCI allow total eight class of services (as defined in IEEE 802.1p), and this field can be set between 0 (i.e. lowest priority) and 7 (i.e. highest priority). The VLAN/priority tagging is implemented in SAS models with the help of Proto-C (C/C++) based object modeling using process model editor in the OPNET. The user priority field is set to higher priorities for SV and GOOSE messages, whereas, low priority for client/server based file transfer applications. Canonical Format Indicator (CFI) has 1 bit. And, 12-bits of VID (VLAN ID) allow total 4094 VLANs (excluding 0x000 and 0xFFFF as a reserved) to be implemented into a SAS network. In this SAS network, for each bay automation devices, individual VLAN is configured. This means, all devices (P&C IEDs and MUs) corresponding to same bay will have same VID, whereas, VID would be different for any two different protection function devices. This way, the broadcast domains are separated according to bays of the SAS.

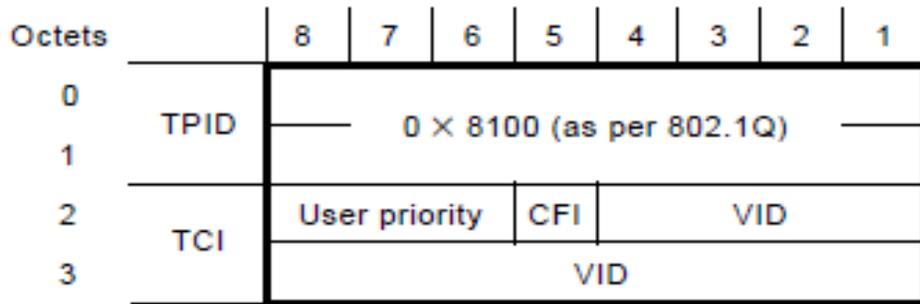


Figure 3-5 IEEE 802.1Q based VLAN/priority tagging

3.3.4 Packet format for the sampled values

The modeling of the standard sampled value packet using an OPNET packet editor is illustrated in Figure 3-6. The sampled values of three-phase-and-neutral voltages and currents, i.e. 8 signals, are merged in Application Protocol Data Unit (APDU) at the MUs. More detail on packet format fields can be found in Appendix C.

Preamble (56bits)			Start-of-Frame (8bits)
Destination_MADC_add (48bits)			
Sources_MAC_addr (48bits)			
TPID (16bits)	TCI (16bits)	Ethertype (16bits)	
APPID (16bits)	Length (16bits)	Reserved1 and 2 (32bits)	
APDU (inherited bits)			
Frame_Check_Sequence (32bits)			

Figure 3-6 Sampled value Ethernet packet format in OPNET

3.3.5 Ethernet switch model

The OPNET provides Ethernet switch models from authorized manufacturers, which are already validated with commercially available Ethernet switches [87]. Figure 3-7 shows the node model of layer-3 Ethernet switch with 10 fiber optic ports for full duplex (10Mbps and 100Mbps) communication. A layer-3 (IP layer) ESW is required to support the traffic flows among the VLANs, i.e. inter-bay communications. A “Store-and-forward” mechanism is used for this model according to Ethernet standard. Therefore, each receiving packet is stored first until the entire packet is received at the receiver of corresponding port. Then, each stored packet is checked for the data integrity (bit errors). Bit errors are corrected at certain level (according to bit error correction mechanism supported by the ports), and send to central processor module. Processor reads the destination MAC address and selects the corresponding output port for each packet at packet service rate of the ESW. Finally, the packet is queued in to the ESW buffer according to the priority tagged on the packet. Packets are transmitted from output port transmitter according to priority level of the queue, i.e. highest priority queue emptied first (strict priority algorithm).

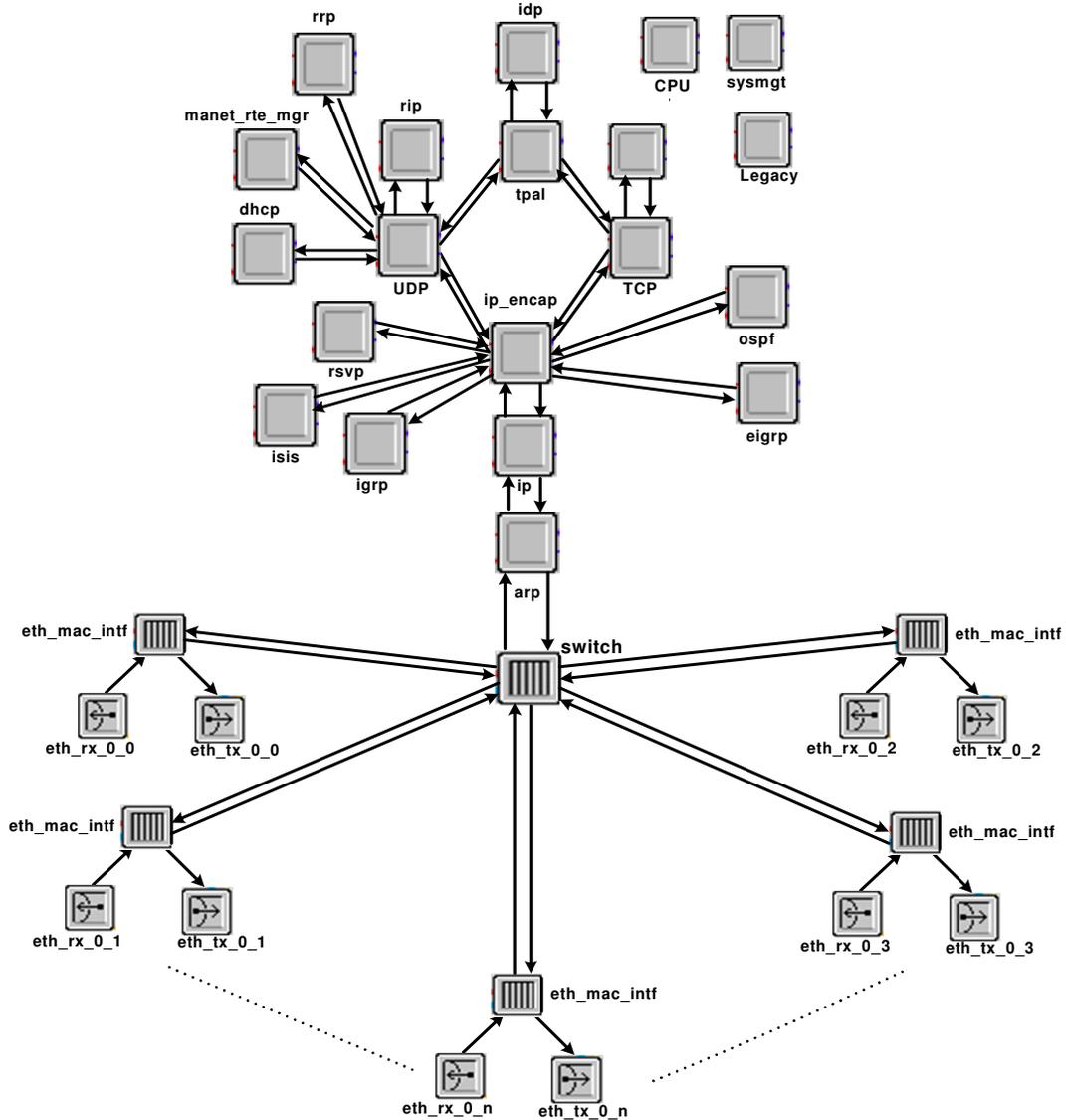


Figure 3-7 Ethernet switch node model in OPNET

3.3.6 Ethernet switch buffer size and packet service rate

Commercially available Ethernet switches has limited buffer size and packet service rate. These constraints of the practical network are modeled in Ethernet switch attributes: *Packet Service Rate (packets/sec)*, *subqueue bit and packet capacity*, as shown in Figure 3-8. Moreover, this figure also demonstrates incorporation of RSTP (IEEE 802.1W) protocol, and VLAN configuration, etc.

Attribute	Value
name	commercial switch
process model	bridge_dispatch_v2
icon name	queue
Bridge Configuration	(...)
Priority	32768
Spanning Tree Protocol	RSTP (802.1w)
QoS Parameters	(...)
QoS Support	Enabled
Default Port QoS Scheme	MWRR
Default Port Queue Configuration	(...)
Timers	(...)
BPDU Service Rate (packets/sec)	100000
Packet Service Rate (packets/sec)	500000
LACP System Priority	promoted
Port Configuration	(...)
Port Group Configuration	(...)
VLAN Configuration	(...)
Scheme	Port-Based VLAN
Spanning Tree Creation Mode	Shared
Supported VLANs	(...)
VTP Parameters	N/A
pkt_capture_mode	(...)
subqueue	(...)
Number of Rows	2
Row 0	
bit capacity (bits)	2,000,000
pk capacity (pks)	500,000
Row 1	...

Figure 3-8 Buffer size and packet service rate attributes of Ethernet switch model in OPNET

3.3.7 Communication links and ports with BER

For a process bus communication, optical fiber based communication links would be preferable, due to its EMI immunity feature. Therefore, two full duplex fiber optic communication links are considered for the process bus communication, 10 Mbps (based on 10BaseFL standard) and 100Mbps (based on 100BaseFX standard). Moreover, the bit-error-rate on the communication links should also be considered for the packet loss study. Figure 3-9 highlights the communication link model attributed with BER settings.

According to these settings, the errors in the bits transmitted through these fiber links are generated.

Attribute	Value
name	node_0 <-> node_3
model	sas_100BaseFX_BER9_100BaseT_adv
transmitter a	node_0.eth_tx_08
receiver a	node_0.eth_rx_08
transmitter b	node_3.eth_tx_09
receiver b	node_3.eth_rx_09
creation source	Object copy
creation timestamp	15:09:07 May 24 2009
creation data	Copy of node_0 <-> node_1
right-angled	disabled
label rotation	horizontal
bundle display	include in bundle
Propagation Speed	Minimum Propagation Velocity
Traffic Information	(...)
arrowheads	head and tail
ber	1E-009
color	blue
condition	enabled
cost	0.0
delay	Distance Based
ecc model	dpt_ecc_bgutil
error model	dpt_error

Figure 3-9 Models for BER of communication links in OPNET

Communication ports have capability to correct the bit errors from the packet using error correction (ecc) model, as shown in Figure 3-9. The commercially available ecc model is used in the OPNET.

3.3.8 Traffic modeling for process bus

There are basically three types of traffic models configured for IEC 61850-9-2 based process bus application: 1) high priority sporadic traffic, i.e. event triggered GOOSE messages; 2) high priority periodic traffic, i.e. time triggered raw data SV messages; 3) low priority background (or best effort) traffic, i.e. event triggered client-server applications among the IEDs. The event triggered (e.g. GOOSE, client/server) messages depends upon the number of events occurring during the simulation time, and hence, memory-less exponential distribution of an event scheduler would be more appropriate.

Whereas, for time triggered (e.g. raw data SV messages), constant packet generating source should be used.

3.4 Simulation of IEC 61850-9-2 Process Bus using OPNET

Figure 3-10 shows a dynamic Ethernet switch based process bus communication network simulated for a typical 345/230 kV substation. Detail of this substation is presented in Appendix B. According to number of IEDs and MUs, total four 10-port Ethernet switches are configured in a ring, which is one of the practical substation automation architecture [8]. Process bus configuration of total 8 bays with corresponding MUs is tabulated in Figure 3-10. To achieve a better traffic load distribution by separating the broadcast domains, total 8 VLANs are configured for this network, i.e. each protection bay has the separate VLAN, including two P&C IEDs for protection-A and B, and corresponding MUs.

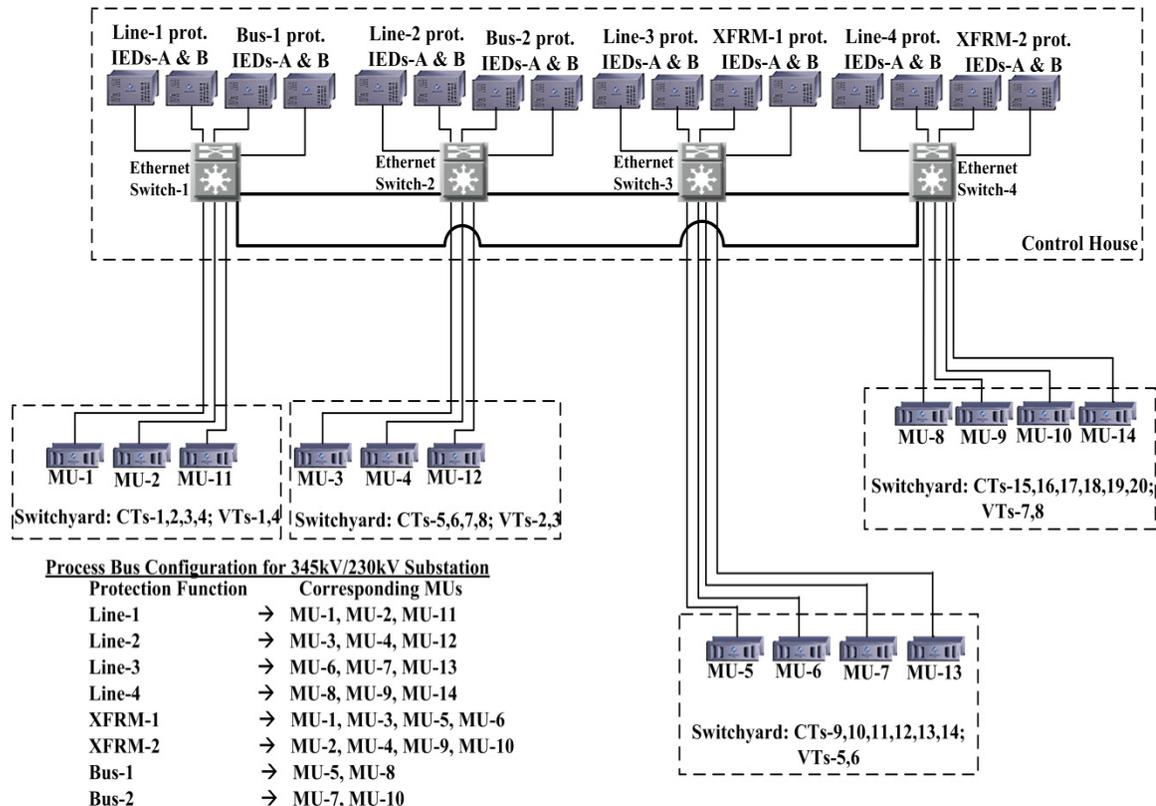


Figure 3-10 Process bus network for the sample substation simulated in OPNET

3.5 Results and Discussion

The performance of this process bus network is analyzed using various parameters, and the impacts of all these parameters are observed from the packet delay and loss of sampled value packets. To study the impact of each parameter separately, one of the parameter is varied within the commercially available range, by keeping other parameters to its nominal values, as tabulated in Table 3-2.

Table 3-2 Parameters for OPNET simulation

Parameters	Default value
Communication link Data rate	100 Mbps (Mega bits per second)
Sampling frequency	4800 Hz
BER	1.00E-09
Background Traffic	250KBps (kilo bytes per second)
Buffer size	2Mbit (Mega bits)
ESW packet service rate	0.5 Mpps (Mega packets per seconds)

The performance of sampled values is analyzed for the two different cases: the Line-3 P&C IED, which has corresponding MUs connected to the same Ethernet switch; and the Bus-1 P&C IEDs, which require sampled values from remote MUs connected to other Ethernet switches.

3.5.1 Impact of communication link data rate and MU sampling rate

The most likely used data rates for substation communication links are: 10 Mbps and 100 Mbps; and sampling frequencies are 1920 Hz and 4800 Hz. Rest of the parameters are considered same as shown in Table 3-2. It can be observed from the Table 3-3 that sampled value packet delays are high for 10 Mbps network, where as packet delays for 100 Mbps network are within the allowable range.

Table 3-3 Impact of data and sampling rates

Protection Functions	Data rate (Mbps)	Sampling rate (Hz)	Sampled value packet delay (ms)		Average number of consecutive SV loss per second
			Avg.	Max.	
Line-3	10	1920	6.4	12	3
		4800	16	25	4
	100	1920	0.7	1.1	1
		4800	1.7	3.65	2
Bus-1	10	1920	6	12.5	4
		4800	15	25.7	5
	100	1920	0.77	1.2	2
		4800	1.8	4	3

Moreover, as the sampling rate increases from 1920 Hz to 4800 Hz, the sampled value packet traffic increases. Hence, it causes more sampled value packet delays and average consecutive packet loss per second.

3.5.2 Impact of bit error rate (BER) of the communication channel

As it can be perceived from Table 3-4 that bit error rate of the communication channel has more impact on the average number of consecutive sampled value packet loss per second and almost negligible impact on the packet delays. Actually, the network interface card at the device receiver has threshold value of allowable bit-errors in the received packet. If the received packet has higher bit-errors than threshold, the packet is discarded at the receiver. Higher BER over the network causes more bit-errors into the packet communicated over the network, and hence the probability of packet rejection at the receiver increases. On the other hand, higher BER does not cause any significant impact on packet delay, and hence, it can be observed from the table that BER has negligible impact on SV delays.

Table 3-4 Impact of communication channel BER

Protection Functions	Bit Error Rate	Sampled value packet delay (ms)		Average number of consecutive SV loss per second
		Avg.	Max.	
Line-3	1.00E-08	1.72	3.9	4
	1.00E-09	1.7	3.65	2
	1.00E-10	1.7	3.9	1
Bus-1	1.00E-08	1.83	3.9	6
	1.00E-09	1.8	4	3
	1.00E-10	1.85	4.2	2

3.5.3 Impact of process bus background traffic

It can be discovered from Table 3-5 that as background traffic (client/server application packets) increases from 250 KBps (kilo bytes per second) to 350 KBps, the sampled value packet delay, as well as the average number of consecutive packet loss per second would increase, even though the sampled value packets have higher priorities as compared to the client/server applications. This is due to the fact that if the transmission of a large client/server packet has started (in the absence of higher priority packet in buffer); a higher priority packet will have to wait in a queue until this large packet has been completely transmitted [48].

Table 3-5 Impact of background traffic

Protection Functions	Background Traffic (KBps)	Sampled value packet delay (ms)		Average number of consecutive SV loss per second
		Avg.	Max.	
Line-3	250	1.7	3.65	2
	350	5	10.1	3
Bus-1	250	1.8	4	3
	350	5.5	10.3	4

3.5.4 Impact of Ethernet switch buffer size and packet service rate

Due to the “store and forward” mechanism, packets are always stored into the buffer first, and then forwarded. Therefore, as the buffer size reduces from 2Mbit to 0.5Mbit, the

sampled value packet delay increases, however, it has a negligible impact on the sampled value packet loss, as shown in Table 3-6.

Furthermore, as Ethernet switch packet service rate decreases from 0.5 Mpps (mega packets per second) to 0.15 Mpps, the sampled value packet delay is more affected because the sampled value packets have to wait more, before they are forwarded to the corresponding output port. The slow rate of packet service rate does not cause overflow of any buffer, and hence it has little impact on sampled value packet loss, as shown in Table 3-7.

Table 3-6 Impact of ESW buffer size

Protection Functions	Buffer size (Mbit)	Sampled value packet delay (ms)		Average number of consecutive SV loss per second
		Avg.	Max.	
Line-3	0.5	3.3	6.7	3
	2	1.7	3.65	2
Bus-1	0.5	3.6	6.8	3
	2	1.8	4	3

Table 3-7 Impact of ESW packet service rate

Protection Functions	ESW packet service rate (Mpps)	Sampled value packet delay (ms)		Average number of consecutive SV loss per second
		Avg.	Max.	
Line-3	0.15	6.6	10	2
	0.5	1.7	3.65	2
Bus-1	0.15	7	10.2	4
	0.5	1.8	4	3

It is also important to note that these results would change according to the size of a substation, and it may be even worse for a larger process bus communication network with the same communication parameters. Therefore, the possible corrective measures have to be taken in order to accommodate the sampled value packet delay and loss.

3.6 Summary

The performance of the IEC 61850-9-2 process bus is evaluated for the Ethernet switched ring architecture of a typical 345kV/230kV substation. Using the OPNET simulation tool, dynamic models of IEC 61850 based process bus devices and communication protocols are developed to analyze the packet delay and loss for the sampled value packets by considering various communication parameters, such as speed of the communication data link, sampling frequency of the merging units, network background traffic, Ethernet switch buffer size, packet services rate, and the communication channel bit error rate. It is demonstrated that these process bus parameters have influence on the sampled value packet loss and delays. For this particular process bus network, the observed maximum sampled value delay is up to 26 ms; whereas, the average number of consecutive sampled value loss per second are 6. This chapter has quantified the average number of SV loss and delay. Next chapter will propose a corrective measure to counteract any impact of SV loss/delay on substation protection functions.

Chapter 4

4. Proposed Algorithm to Counteract Effect of SV Loss/Delay

With the help of detailed dynamic analysis, the SV loss and delay is analyzed for a typical digital substation. This SV loss and delay have detrimental impact on different substation protection system. Reference [49], [50] have shown the impact of sampled value loss on the performance of digital relaying protective functions. This concern has also been recognized by protection devices manufacturing industry. In [51], C. Hoga has stated that the SV loss at the protection relay can have some kind of measuring blackout for the entire measuring window. Moreover, process bus product developers [28], [35] have also shown the need of a smart algorithm for the treatment of SV loss data, which also should be compatible to any (time and/or frequency based) digital relaying algorithm. This chapter presents a technique to compensate for the delayed or lost sampled values for the digital relaying algorithms. And, based on this technique, this chapter proposes a sampled value estimation algorithm which can be implemented to work with any digital protection functions. Finally, the proposed algorithm is examined for various scenarios using PSCAD/EMTDC and MATLAB simulation tools.

4.1 Corrective Measures for IEC 61850-9-2 Process Bus Performance

Traditional digital relaying algorithms are working satisfactorily since few decades using analog signals between bay level and process level over the copper wires. The performance of these tested robust relaying algorithms should not be affected by digital ESW based process bus network in any possible worst case scenarios. Hence, there is need for some kind of corrective measures which can counteract with SV packet loss.

One of the methods is to use adaptive filtering, as discussed in reference [49], [50]. However, this method has few limitations as discussed below:

1. The proposed adaptive filtering is based on phasor estimation using LES and hence, it is limited to those digital relaying algorithms which use LES.
2. Adaptive filtering is feasible only for 1 sample loss with low sampling rate (it was tested up to 32 samples per cycle). This is because it stores the filter coefficients for all possible sequence of lost samples. With multiple SV packet delay or loss and sampling rate of 80 samples per cycle, it would require large storage for the filter coefficients.

Therefore, there is need for general (applicable to all digital relaying algorithm), simple, easy to implement algorithm for next generation P&C IEDs. To achieve these qualities, this chapter proposes a numerical estimation technique for the SV loss or delay. The major requirements for the SV estimation algorithm are as follows:

1. Accurate estimation algorithm even for several consecutive sampled value losses.
2. Algorithm should be able to work for almost all the digital relaying algorithm already existing in the multi-vendor protection IEDs of the SAS.
3. Simple and easy to implement into the protection IEDs.

The SV estimation algorithm to enhance process bus performance by satisfying all above mentioned requirements is explained in the following section.

4.2 Numerical Theories for Estimation

There are several numerical theories available for the estimation or approximation in the reference books on numerical analysis [88], [89]. Some of the key methods are listed as follows:

1. Curve-fitting techniques
2. Polynomial approximation
3. Piecewise spline

Curve fitting techniques (e.g. using least square method) may not be appropriate to apply for SV estimation. This is because curve fitting techniques give a best fitted curve

function which may not necessarily passing through all the given sampled values. These techniques are more suitable for data smoothing problem to obtain the function, which is not the case with SV estimation problem. Another suitable method is polynomial approximation, which is also referred to as polynomial interpolation technique. It is basically used to obtain polynomial (of any desired degree) passing through the given set of values. And then, this polynomial function can be used to obtain a set of values at any desired point. Polynomial approximation is simple; however, the estimation error should be analyzed. Similar goal can be achieved using piecewise spline technique, which further divides set of values into many intermediate values and obtain sub-polynomials from all the intermediate points. Hence, piecewise spline has higher accuracy as compared to polynomial approximation technique. However, the computations requirements for piecewise spline is quite higher than the polynomial approximation technique, and hence, piecewise spline is more suitable for highly dispersed set of given points. For SV estimation, the given sets of SVs would be uniform in time (as all the SV has time stamp or sample count into the each SV packet) and also due to the fact that the sampling frequency would be as high as 4800 Hz, polynomial approximation technique can give sufficient accuracy. Moreover, as mentioned earlier, the SV estimation algorithm has to be easily accommodated in existing processor with least additional processing requirements. Therefore, SV estimation algorithm based on polynomial approximation technique is selected for this work.

4.3 Sampled Value Estimation Technique

There are several numerical methods available for the estimation e.g. polynomial approximation, spline techniques, curve fitting, etc. [88]. However, implementations of any of these complex numerical methods require additional computational capability. This chapter provides the coefficients for estimation techniques using the Lagrange polynomial method, which is easy to implement as compared to other available methods, and also applicable to any digital relaying algorithm.

According to Lagrange polynomial method, a unique polynomial, $p_n(t)$ of degree $\leq n$, can be obtained from the given $n+1$ distinct sampled values. SV estimation techniques utilize

this polynomial function to estimate the lost or delayed sampled values at a given time t_k , as shown below:

$$f_{k,est} = p_n(t_k) = \sum_{i=0}^n f_i C_{i,n}(t_k) \quad (4-1)$$

$$C_{i,n}(t_k) = \prod_{\substack{j=0 \\ j \neq i}}^n \left[\frac{t_k - t_j}{t_i - t_j} \right] \quad (4-2)$$

$$f_i = f(t_i), \quad i = 0, 1, 2, \dots \quad (4-3)$$

where, $f_{k,est}$ is the estimated sampled value at k^{th} instant; $C_{i,n}$ is the coefficient of n -order polynomial at i^{th} instant; f_i is the sampled value at i^{th} instant; t_i is the time at i^{th} instant.

4.3.1 First order (linear) SV estimation

The simplest form of polynomial is linear in which two SVs need to be known (t_0, f_0) and (t_1, f_1) as shown in Figure 4-1. The following equation (derived from (4-1)) can be used to obtain SV at time t_k , with known SVs (t_0, f_0) and (t_1, f_1).

This equation can also be re-arranged in the Lagrangian form as follows:

$$f_{k,est} = p_1(t_k) = C_{01} f_0 + C_{11} f_1 \quad (4-4)$$

where,

$$C_{01} = \frac{(t_k - t_1)}{(t_0 - t_1)}; \quad C_{11} = \frac{(t_k - t_0)}{(t_1 - t_0)}$$

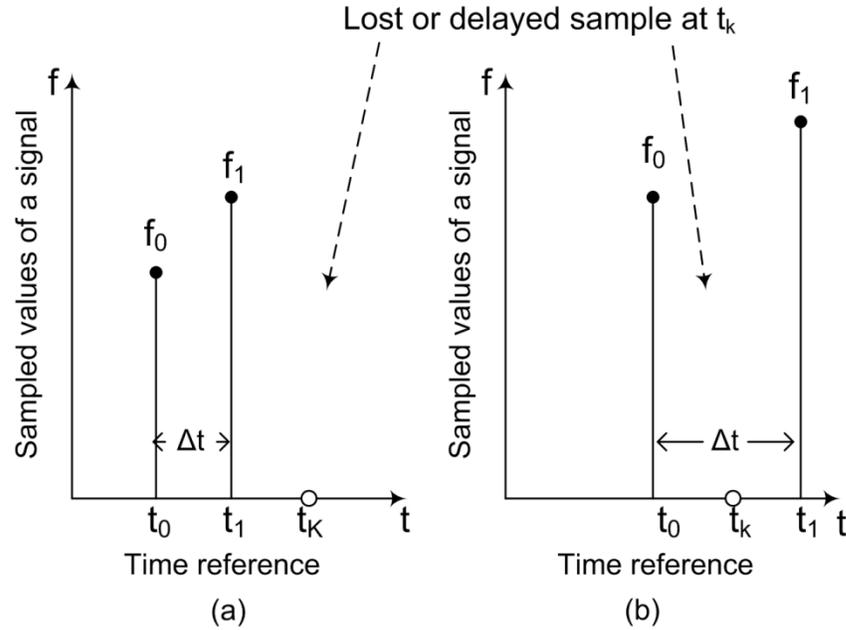


Figure 4-1 Sampled values for linear SV estimation technique: scenario-(a) next sample is not available; scenario-(b) next sample is available

As illustrated in Figure 4-1, there are two possible conditions for the SV loss: 1) next sample at t_1 (i.e. sampled at $k+1$) has not arrived; 2) next sample at t_1 (i.e. sample at $k+1$) has arrived. According to these two scenarios, both the coefficients (C_{01} and C_{11}) can be obtained for (4-4). The values of these coefficients are tabulated in Table 4-1. The set-1 coefficients belong to the scenario when next sample has not arrived (as shown in Figure 4-1 (a)); whereas, set-2 coefficients are derived for the scenario when next sample is available (as shown in Figure 4-1 (b)).

Table 4-1 Sets of coefficients for linear SV estimation method

Sets of Coefficients	C_{01}	C_{11}
set-1	-1	2
set-2	$\frac{1}{2}$	$\frac{1}{2}$

4.3.2 Second order (quadratic) SV estimation

Second order SV estimation technique is explained as follows. Second order polynomial, i.e. $p_2(t_k)$ as shown in (4-5), can be used to estimate the lost or delayed sampled value by selecting three appropriate known sampled values f_0, f_1 and f_2 , for a given set of stored coefficients C_{02}, C_{12} , and C_{22} .

$$f_{k,est} = p_2(t_k) = C_{02}f_0 + C_{12}f_1 + C_{22}f_2 \quad (4-5)$$

where,

$$C_{02} = \frac{(t_k - t_1)(t_k - t_2)}{(t_0 - t_1)(t_0 - t_2)} ; C_{12} = \frac{(t_k - t_0)(t_k - t_2)}{(t_1 - t_0)(t_1 - t_2)} ; C_{22} = \frac{(t_k - t_0)(t_k - t_1)}{(t_2 - t_0)(t_2 - t_1)}$$

The set of second order SV estimation technique coefficients (C_{02}, C_{12}, C_{22}) need to be derived by considering all the appropriate scenarios. As demonstrated in Figure 4-2, there are total three possible scenarios for the second order SV estimation technique: a) next samples have not arrived (set-1); b) next one sample at $k+1$ (i.e. t_2) has arrived (set-2); c) next two samples at $k+1$ (t_1) and $k+2$ (t_2) and t_{k+2} have arrived (set-3). Three sets of coefficients corresponding to each scenario of Figure 4-2 can be obtained for second order SV estimation, as tabulated in Table 4-2.

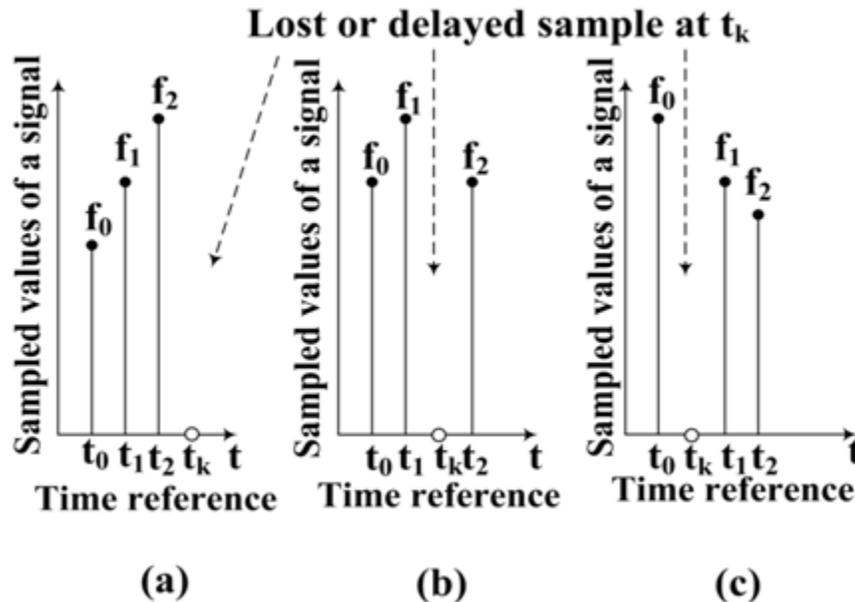


Figure 4-2 Sampled values for second order SV estimation technique: scenario-(a) next samples are not available; scenario-(b) only one next sample is available; scenario-(c) two next samples are available

Table 4-2 Sets of coefficients for second order SV estimation method

Sets of Coefficient	Selected sampled values	C ₀₂	C ₁₂	C ₂₂
set-1	$f_0=f_{k-3};$ $f_1=f_{k-2};$ $f_2=f_{k-1}$	+1	-3	+3
set-2	$f_0=f_{k-2};$ $f_1=f_{k-1}$ $f_2=f_{k+1}$	$-\frac{1}{3}$	+1	$\frac{1}{3}$
set-3	$f_0=f_{k-1};$ $f_1=f_{k+1}$ $f_2=f_{k+2}$	$\frac{1}{3}$	+1	$-\frac{1}{3}$

As the order of polynomial (n) increases, accuracy of the estimated sampled value increases, however, the computational complexity increases too. The implementation of quadratic SV estimation algorithm in conjunction with already existing traditional digital relaying algorithm is explained in the following subsection.

4.3.3 Third order (cubic) SV estimation

If manufacturers are interested in increasing further accuracy of SV estimation by providing additional processing speed, cubic polynomial coefficients can be obtained as follows:

$$f_{k,est} = p_3(t_k) = C_{03}f_0 + C_{13}f_1 + C_{23}f_2 + C_{33}f_3 \quad (4-6)$$

where,

$$C_{03} = \frac{(t_k - t_1)(t_k - t_2)(t_k - t_3)}{(t_0 - t_1)(t_0 - t_2)(t_0 - t_3)}; \quad C_{13} = \frac{(t_k - t_0)(t_k - t_2)(t_k - t_3)}{(t_1 - t_0)(t_1 - t_2)(t_1 - t_3)}$$

$$C_{23} = \frac{(t_k - t_0)(t_k - t_1)(t_k - t_3)}{(t_2 - t_0)(t_2 - t_1)(t_2 - t_3)}; \quad C_{33} = \frac{(t_k - t_0)(t_k - t_1)(t_k - t_2)}{(t_3 - t_0)(t_3 - t_1)(t_3 - t_2)}$$

It is important to note here that there will be a total of four possibilities for SV loss, and hence, there will be a total of four sets of coefficients that need to be derived using above equations as shown in Table 4-3.

Table 4-3 Sets of coefficients for cubic SV estimation method

Sets of Coefficients	C_{03}	C_{13}	C_{23}	C_{33}
set-1	- 1	- 4	- 6	4
set-2	$\frac{1}{4}$	-1	$\frac{3}{2}$	$\frac{1}{4}$
set-3	$-\frac{1}{6}$	$\frac{2}{3}$	$\frac{2}{3}$	$-\frac{1}{6}$
set-4	$\frac{1}{4}$	$\frac{3}{2}$	- 1	$\frac{1}{4}$

4.4 The Proposed Sampled Value Estimation Algorithm

Figure 4-3 shows the flow diagram of second order SV estimation algorithm, it starts with the loop when the processor of P&C IED is expecting the sampled value packet for the corresponding MU at k^{th} instant. If sampled value packet arrives, it will be stored into the buffer and traditional digital relaying algorithms will use it from the buffer. However, if the sampled value packet does not arrive, IED is supposed to wait for short duration, i.e. t_{wait} . The value of t_{wait} can be set around two to three sampling intervals, i.e. 0.417 ms to 0.625 ms for 4800 Hz sampling frequency. Even after waiting, if sampled value packet does not arrive, SV estimation will be initiated, and check for the conditions whether next samples have arrived or not. According to the availability of next samples, the set of coefficients (C_{02} , C_{12} , and C_{22}) will be selected from the Table 4-2, and the assignment of corresponding sampled values to the f_0, f_1, f_2 will be done accordingly. The selection of these values in the algorithm is carried out in order to minimize the estimation error. These selected values (C_{02}, f_0, C_{12}, f_1 , and C_{22}, f_2) will be used in (4-5) to solve for $f_{k,\text{est}}$. The counter *count* calculates the total number of consecutive sampled value packets lost or delayed.

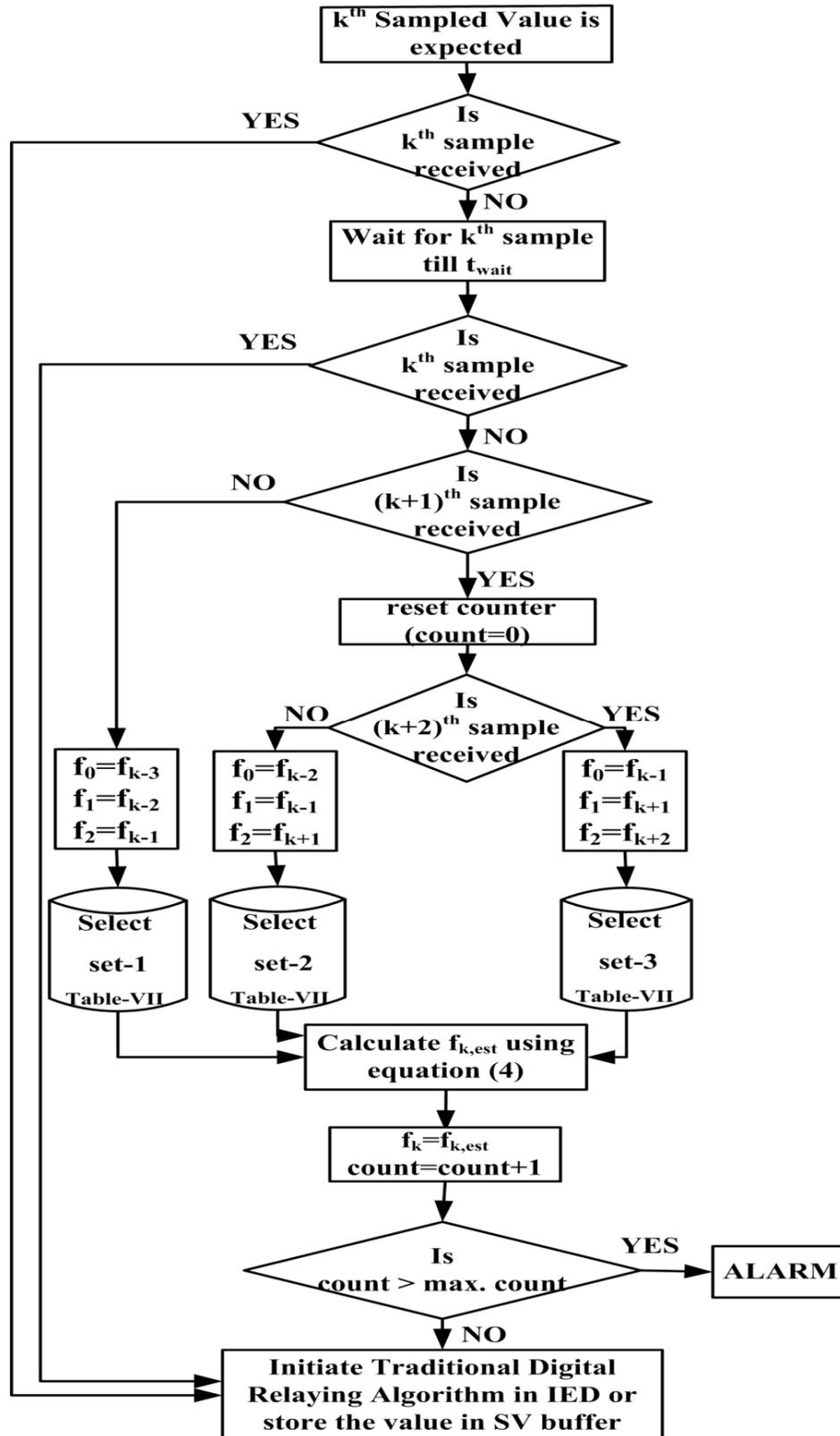


Figure 4-3 Flow diagram of proposed second order SV estimation algorithm

The utilization of estimated sampled value for the consecutive packet loss should be within some limit (*max. count*). Therefore, if the number of consecutive packet loss is higher than *max. count*, IED should ALARM the condition, as this may be due to failure of communication link, Ethernet switch, merging unit, or any damage in process bus LAN network. Furthermore, the value of *max. count* also depends upon the required estimation accuracy, which is explained in following subsection. Finally, if the consecutive SV estimation is less than the *max. count*, it will store the estimated value into the sampled value buffer, so that traditional digital relaying algorithm can utilize this value. If delayed sample value packets arrive at any time, the estimated sampled value should be replaced with the actual value arrived in the buffer. Moreover, if protection is executed at every few sets of sampling interval, this estimation procedure should also be carried out with same set of sampling interval in order to achieve higher estimation accuracy by utilizing the latest sampled values.

It can be noticed that SV estimation algorithm can be implemented to work with any traditional digital relaying algorithm from any IED manufacturer. Furthermore, it is comparatively easy to implement in the IEDs and requires very less computations and memory space. Figure 4-3 shows SV estimation using second order estimation technique, however, the same concept of SV estimation algorithm can be applied to any order SV estimation techniques by including the corresponding sets of coefficients and known sampled values.

4.5 Estimation Accuracy Analysis of the Proposed Algorithm

To analyze the overall performance of SV estimation algorithm, a typical 345kV/230kV substation (as shown in Figure B-1) is simulated using PSCAD/EMTDC simulation tool. The proposed SV estimation algorithms for the substation P&C IEDs are developed using MATLAB simulation tool. The COMTRADE recorder in PSCAD/EMTDC resembles the function of MU at process level, as it samples the analog signal collected from the secondary of CTs/CCVTs. The MATLAB extracts the sampled value streams of each

signal from corresponding COMTRADE file. The MATLAB code has also been developed to incorporate various sampled value losses and delay scenarios obtained from the OPNET. It can be observed from Table 3-3 to Table 3-7 that the maximum number of SV packet loss occurring is 6 and sampled value packet delay varies between 16 ms to 26 ms. Therefore, in order to analyze the worst case scenario, up to 10 simultaneous sampled values packet loss are examined coinciding with the time of fault inception (A-G fault created at in line-3 of the Figure B-1). This worst case scenario (up to 10 simultaneous SV packets loss coinciding with the time of fault inception) is examined on A-phase CT secondary current by considering various source impedance ratios, point-on-wave for faults, noise level in the signal, sampling frequency, and different instances on the wave. For all these different scenarios, the maximum absolute errors in estimating simultaneous SV loss from first, second, and third order SV estimation algorithms are compared with the actual values, which is the maximum absolute error incurred without SV estimation algorithm. Since estimation of each SV has some error from actual value, the maximum absolute error shows the maximum out of all multiple lost/delayed SVs estimation errors.

4.5.1 Effect of SIR of the system and POW of the fault

Table 4-4 shows the comparison of maximum absolute error in CT secondary current with different SV estimation algorithms and the actual values of the lost samples (or the maximum absolute error incurred without SV estimation algorithms) for various system SIR and fault POW by considering different number of sampled values loss at the fault inception. The POW at zero, mid and peak refers to the points at 0° , 45° , and 90° respectively, on the A-phase voltage. It can be observed from the table that for the overall maximum absolute error of 14.806 A, the second order SV estimation technique estimates the sampled values with maximum absolute error of 0.9541A (6.5%), whereas, first order and third order techniques have error of 2.179A (14.71%) and 3.617 A (24.43%) respectively. For 10 consecutive SV loss scenario, the errors of estimation are high, and it does not drop as SV estimation technique order increases. Although, the maximum absolute error for first, second, and third order techniques varies with SIRs and POW, these maximum sampled value estimation errors are considerably less compared to

the error incurred without estimating the sampled values, i.e. actual value of the lost sample.

Table 4-4 Effect of various SIRs and POW

No. of consecut-ive sample loss	SIR	POW	Actual value of the lost sample	Max. absolute $\Delta I_{\text{sec.}}$ (Amp)		
				First order	Second order	Third order
2	0.2	Zero	1.4015	0.0154	0.008	0.0347
		Mid	6.2553	0.0499	0.0034	0.0113
		Peak	8.5656	0.0973	0.0885	0.0326
	1	Zero	0.3463	0.0181	0.0044	0.0189
		Mid	5.6964	0.0379	0.0013	0.0011
		Peak	7.0156	0.0713	0.0132	0.0148
5	0.2	Zero	1.4015	0.0776	0.1132	0.3634
		Mid	9.0387	0.4607	0.0057	0.2993
		Peak	10.2597	0.8684	0.7804	0.3378
	1	Zero	0.9821	0.0656	0.071	0.2179
		Mid	7.8944	0.3708	0.005	0.0106
		Peak	8.8497	0.7641	0.0512	0.3501
10	0.2	Zero	2.7074	0.103	1.0561	0.6125
		Mid	13.0562	1.8414	0.4154	0.7682
		Peak	14.806	2.179	0.9541	3.617
	1	Zero	2.8882	0.1768	1.4416	1.1479
		Mid	11.8434	1.3423	0.349	0.2304
		Peak	11.9592	2.37	0.8526	1.6402

4.5.2 Effect of noise in the power signal

It is also important to examine the effect of possible noise levels present in the received sampled values. Figure 4-4 presents the maximum estimation error incurred from the SV estimation algorithms and compares with the maximum absolute error without estimating SV. for different Signal-to-Noise Ratios (SNRs) in dB. The noise is added on the actual values used for the estimation using MATLAB, and then SVs are estimated using these previous sampled values. The figure demonstrate that the error incurred from SV estimation is around 0.05 A with 3.8 A actual values at 2 consecutive SV loss; whereas, estimation error is around 0.4 A for 5.7 A of actual values. It can be seen from the figure that even for 10 consecutive sampled values loss with 40 dB SNR, the maximum absolute

error without sampled value estimation is 9.466 A; whereas, the maximum percentage errors from first, second and third order estimation techniques are 16.11% (1.52 A) , 6% (0.567 A), and 0.7% (0.06 A) respectively. If further higher levels of noise are expected, it is recommended to use a specific filter to attenuate the noise before the SV estimation.

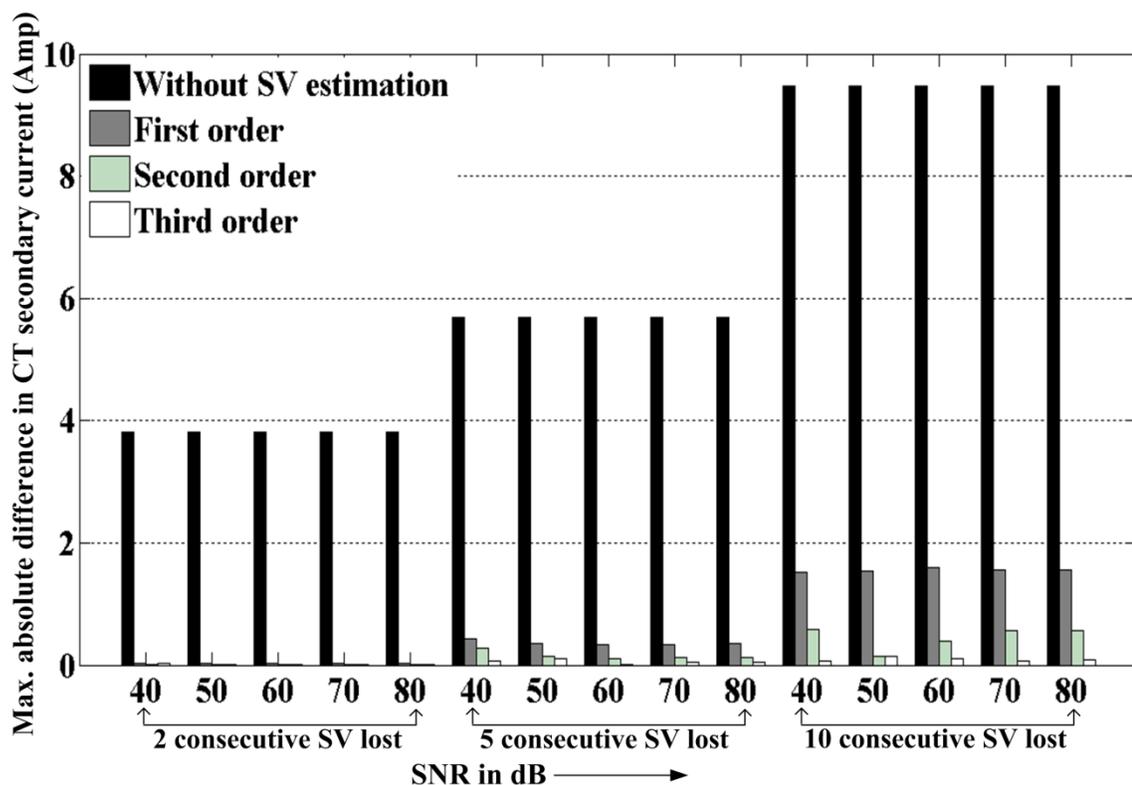


Figure 4-4 Effect of different noise levels (SNR)

4.5.3 Effect of sampling frequency

The effect of different sampling rate of the MUs on the proposed estimation algorithm for 1920 Hz and 4800 Hz is tabulated in Table 4-5. The tabulated result shows that for 1920 Hz sampling frequency with 10 consecutive sampled value loss, the first, second and third order estimation techniques have maximum estimation error as high as 27%, 21%, and 8% respectively. Whereas, for 4800 Hz sampling frequency, the maximum absolute error using first, second and third order estimation techniques are 15%, 2.5%, and 9% respectively. Therefore, it is recommended that the allowable maximum number of sampled values for the estimation should be selected based on sampling frequency too.

Table 4-5 Effect of various sampling frequencies

No. of consecutive sample loss	Sampling Freq.	Actual value of the lost sample	Max. absolute ΔI_{sec} (Amp)		
			First order	Second order	Third order
2	1920	5.0273	0.1473	0.1213	0.0916
	4800	4.3978	0.0383	0.0092	0.0029
5	1920	10.6647	1.913	1.6529	1.0588
	4800	6.3998	0.3825	0.0912	0.0579
10	1920	18.1478	4.8479	3.7811	1.388
	4800	10.2637	1.5765	0.2656	0.9644

4.5.4 Effect of actual value of signal at particular instance on the wave

Figure 4-5 shows the different instances considered to calculate the maximum absolute error incurred using SV estimation technique.

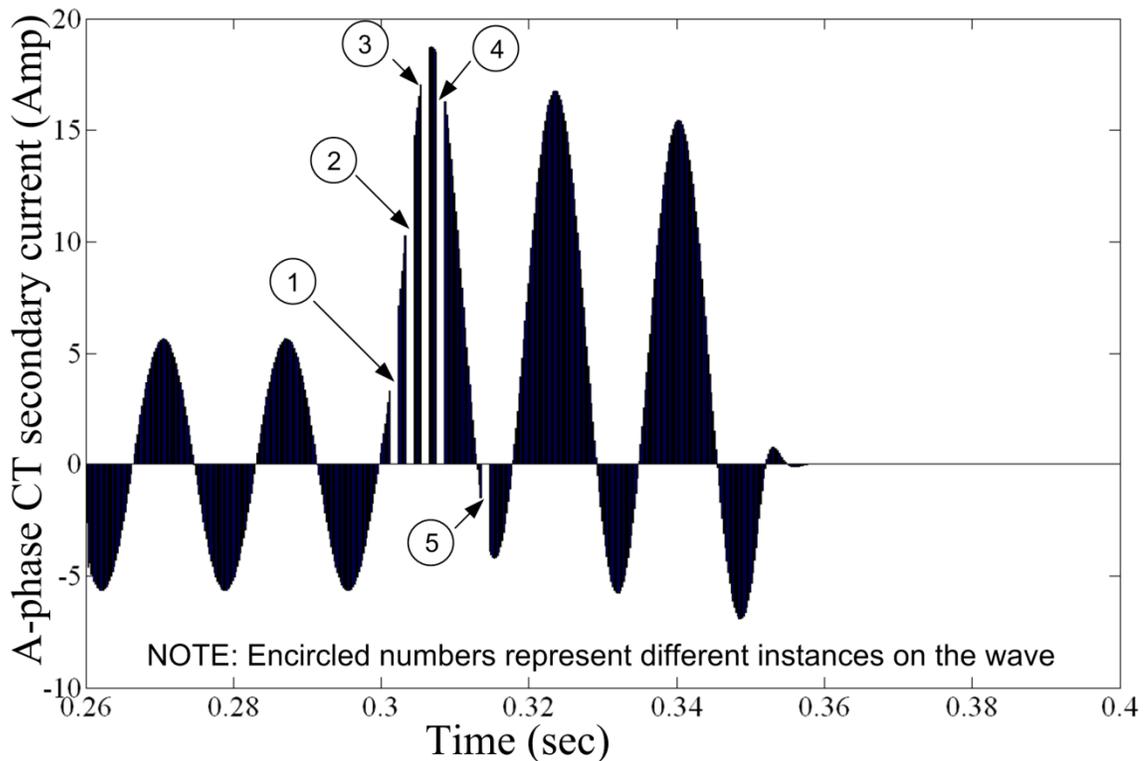


Figure 4-5 Sampled value loss at different instances during the fault

Figure 4-6 shows that maximum absolute error incurred due to sampled values loss also depends upon the actual value of the signal at particular instant. This is because the wave-shape of the voltages and currents (immediately after the fault) are close to linear at zero crossings (especially at the instance of fault) and non-linear (curvature) at the peak, as shown in the figure. The estimation error reduces as the order increases up to 5 consecutive SVs estimation. However, for the ten consecutive SVs loss, the estimation error may not reduce with the order. For example, at instant-1 the estimation error with second order technique is less than third order technique. This is may be due to the fact that wave-shape is close to linear at instant-1, and third-order polynomial accumulates more error for ten consecutive SVs estimation. The estimated sampled values using second and third order SV estimation techniques have low maximum absolute error as compared to the first order for 10 consecutive sampled value losses.

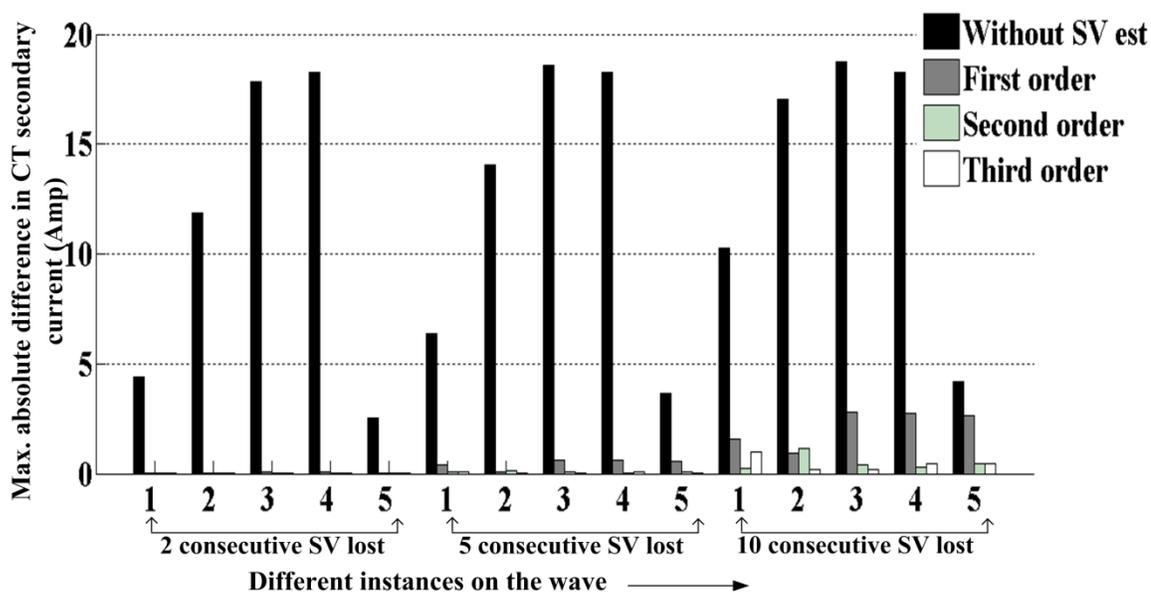


Figure 4-6 Effect of different instances on the wave

The above tabulated results from various scenarios show that the accuracy of estimated sampled value does not improve always with the higher order of the SV estimation techniques in all cases. This is due to the non-linear characteristic of voltage and current signals with decaying DC component and/or noise at the time of fault inception. If more accuracy is required or large number of consequent sampled value packet loss is

expected, the higher order or other more complex estimation techniques, such as spline, curve fitting, etc. have to be used by adding more processing power.

4.6 Summary

In order to alleviate the impacts of the lost and delayed sampled values on a digital protective relaying, the corrective measure, i.e. sampled value estimation technique has been presented in this chapter. Using this SV estimation technique, this work proposes the SV estimation algorithm with the sets of coefficients. To examine the accuracy of the proposed SV estimation algorithm, the same 345kV/230kV substation is simulated in PSCAD/EMTDC, and the sampled value estimation algorithm is programmed in the MATLAB, for the various scenarios, such as system SIRs, fault POW, noise levels in the received signal, and instances on the wave. Moreover, the rare worst case scenarios are presented by considering up to 10 consecutive sampled values loss, coinciding with the fault inception. For various SIRs and POW scenarios, the maximum estimation errors are 8.5%, 7.6%, and 3.2% incurred to estimate up to 5 consecutive sampled values lost or delayed of the maximum actual value using first, second, and third order SV estimation techniques, respectively. In case of different noise levels, the maximum absolute errors from first, second and third order SV estimation are 7%, 5% and 1.1% respectively, up to 5 consecutive samples lost. Moreover, if the sampling frequency reduces from 4800 Hz to 1920 Hz, the maximum absolute error would increase up to 17% for 5 consecutive sampled values lost. For the same scenarios with 10 consecutive sampled values lost, the maximum estimation errors are 25% or more. However, up to 5 consecutive sampled values loss at 4800 Hz sampling frequency, the proposed sampled value estimation algorithm not only offers the reasonable accuracy, but also less computational requirements, and compatibility with any traditional digital relaying algorithm. If even more estimation accuracy is needed, higher order SV estimation techniques or more complex numerical methods can be implemented using the same concept of SV estimation algorithm presented here. It is recommended that the corrective measure techniques (first order, second order, third order, or any other techniques) should be selected considering required estimation accuracy (selectivity constraints) and available processing capability (speed and cost constraint) for a particular protection IED.

Investigation of the proposed SV estimation technique using a laboratory hardware setup is presented in the next chapter.

Chapter 5

5. Laboratory Investigation of the Proposed Algorithm

One of the concerns raised by the protection devices developers from the process bus communication network is the impact of SV loss and delay on protection functions. Therefore, SV estimation algorithm is proposed, and the error analysis is demonstrated in the previous chapter. In addition to SV estimation accuracy analysis, it is also important to carry out hardware testing of the proposed algorithm as a part of substation protection functions, and investigate its performance over a digital process bus network in a laboratory environment. Thus, this chapter starts with the hardware development of the protective relaying over a process bus communication network, which includes protection IEDs, merging units, Ethernet switches, traffic generator, network analyzer, etc. to test the sampled value estimation algorithm as a part of two important substation protection functions: 1) biased differential of busbar, and 2) transmission line distance protection IEDs. Thereafter, the detailed testing of these protection functions over the process bus network is carried out considering various SV loss/delay scenarios and power system fault conditions.

5.1 Development of Process Bus Lab Devices

The hardware implementation of process bus devices is achieved using hard-real time operating system, QNX platform [90] over the industrial embedded computer system. Moreover, the process bus communication network devices used for this investigation are commercially available, and designed for substation environment, from Ruggedcom [91].

5.1.1 Merging unit simulator

Merging unit is implemented as a real time data playback using QNX. Figure 5-1 illustrates the real time data playback functional diagram. Various scenarios of a typical power system can be simulated using the PSCAD/EMTDC simulation tool to obtain signals of 3-phase to neutral currents and voltages using the COMTRADE recorder. Special file conversion code is developed using C/C++ programming, which converts 20 kHz COMTRADE data to the IEC 61850-9-2 compliant SV messages at 4800 Hz in a SV data file. This SV data file is sent to a real time data playback, working as a merging unit, in offline. With the help of the hard-real time timers of the operating system [90], the IEC 61850-9-2 compliant sampled value messages are sent to all subscribed protection IEDs over a process bus network at a regular interval (according to 4800 Hz sampling frequency). Moreover, this developed MU has capability to create various SV loss and delay scenarios over the IEC 61850-9-2 process bus, as well as to capture and read configured IEC 61850 GOOSE messages. The SV loss or delay applies to entire the sampled value packet, which includes voltages and currents obtained at the same time stamp from the corresponding CTs/VTs.

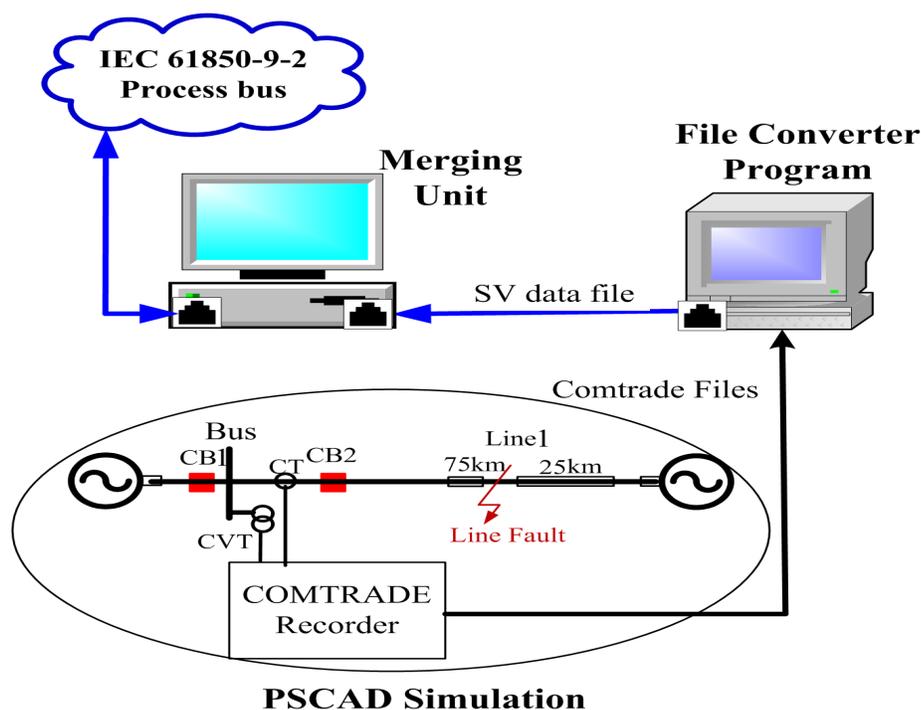


Figure 5-1 Merging unit implementation as a real-time data playback developed in a laboratory

5.1.2 Protection IED

Figure 5-2 shows the basic function block diagram of an implemented protection IED using industrial embedded systems with the real time operating system. The hard-real time operation of the protection IED is achieved with the help of various capabilities of the real time platform, such as, hard-real time timers, multi-threads, input/output packet (io-pkt), etc. To avoid complexity, the figure only illustrates the major function blocks related to digital relaying. It is desired that the SV estimation algorithm should work independent of a digital protection function. Therefore, functions related to SV capturing and buffering are grouped as independent process-1; and traditional protection functions (logical nodes as per IEC 61850) with GOOSE messaging are grouped as independent process-2. Real-time multi-threads are used to perform protection functions simultaneously with the SV packet buffering by executing both independent process threads in parallel. As the SV estimation algorithm is implemented as a part of SV buffer, it is independent of protection functions. This way, SV estimation can be implemented in an IED to work with any traditional digital relaying algorithm. Although, the SV estimation algorithm is simple and easy to implement in digital protection IEDs, it will require additional processing.

As illustrated in Figure 5-2, IEC 61850-9-2 enabled protection IED receives and filters various types of messages from Ethernet network port. *SV data dissect* function is developed to read voltage and current values from the standard IEC 61850-9-2 packet format; as well as to store these values in a circular SV buffer. The sampled value buffer is filled in sequence. The delayed or lost sampled value packets will be estimated using the proposed SV estimation algorithm, as explained in Appendix. The protection IED also has capability to configure, encapsulate and multicast the IEC 61850-8-1 GOOSE messages to the subscribed MUs and other IEDs.

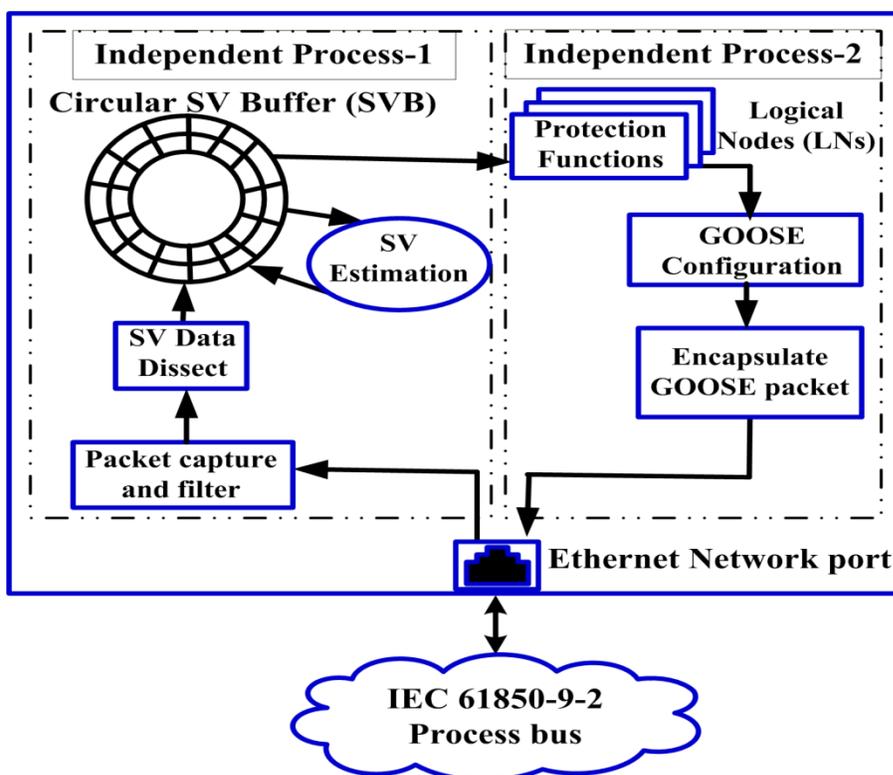


Figure 5-2 Function block diagram of the IEC 61850-9-2 enabled protection IED developed in a laboratory

5.1.3 Implementation of the SV estimation algorithm

The implementation of a first order SV estimation technique is discussed in this appendix to avoid complexity. Figure 5-3 shows the flow diagram of the SV estimation algorithm for the IEC 61850-9-2 enabled protection IED.

The digital values of voltage and current signals obtained from the SV packet are stored in the Sampled Value Buffer (SVB), as shown in Figure 5-2. To store received sampled values in sequence and to detect sample value loss in SVB, the sampled value estimation algorithm uses two pointers: 1) sampled value buffer pointer (SVB_ptr); and 2) previous sampled value buffer pointer (SVB_ptr_prev). The value of SVB_ptr would be the same as the value of *Sample Count* data field defined in IEC 61850-9-2 standard. If the received sampled value is the delayed one, the previously estimated sampled value is replaced by this received actual value in the SVB. In case, if difference between SVB_ptr and SVB_ptr_prev is higher than maximum count, this condition will initiate ALARM without estimating sampled values and this may be due to loss of communication link. If

the lost/delayed SV packets are less than the maximum count, which implies that there is SV loss or delay, and therefore, the algorithm selects coefficients as well as estimates the lost sampled values. Further details can be obtained from reference [92].

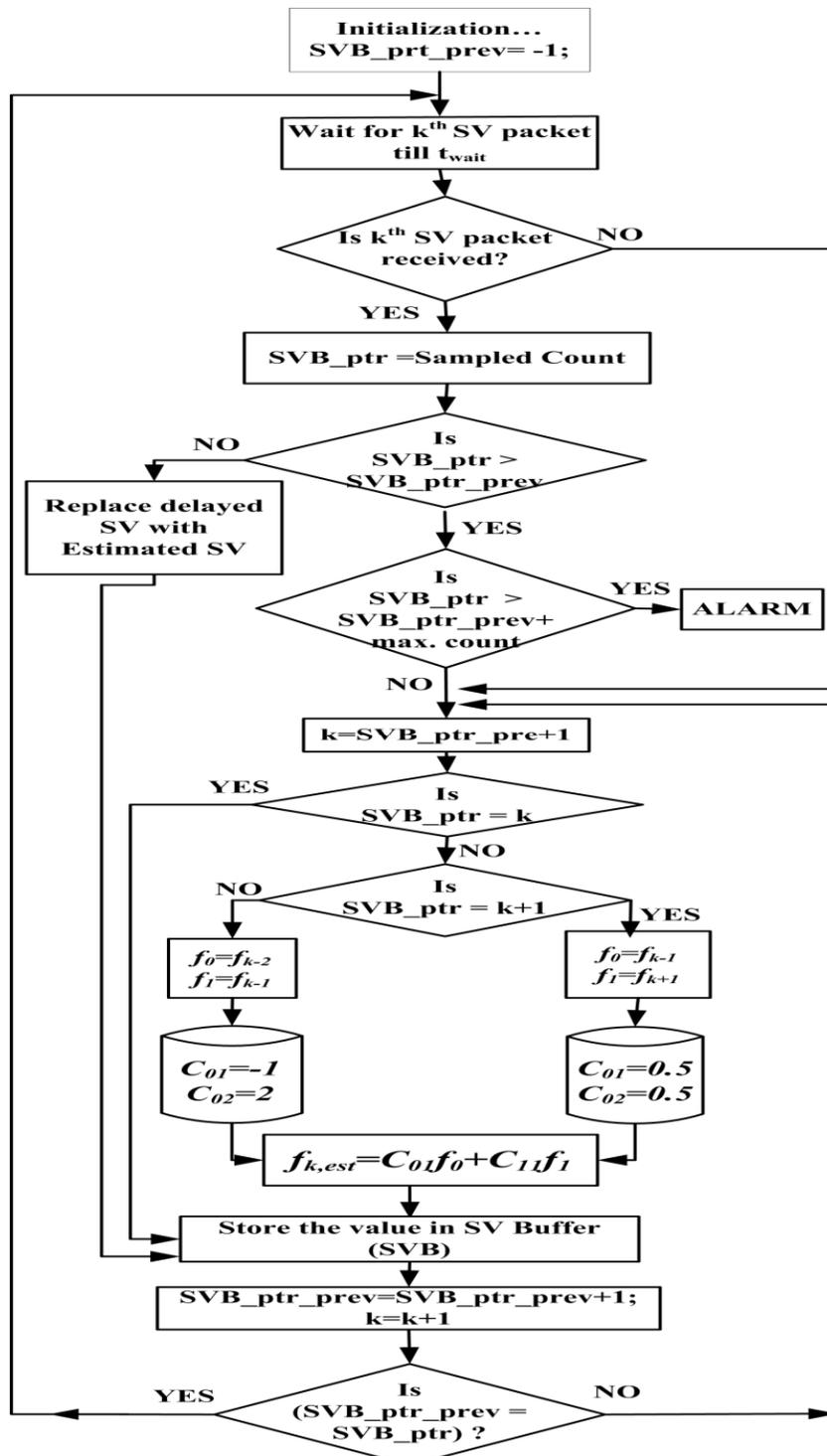


Figure 5-3 Implementation of sampled value estimation algorithm

5.1.4 Traffic generator

A traffic generator is implemented to generate different types of IEC 61850 traffic within the Virtual LAN (VLAN) of a particular protection system using the real time platform. In this work, the traffic streams used over the process bus are GOOSE, GSSE (Generic Substation Status Event), and client server applications. The traffic configuration with total traffic in Mbps is listed in Table 5-1.

Table 5-1 Traffic generator configuration

Sr. No.	Types of Messages	Ethernet Interfaces	Packet size (byte)	Inter-arrival time	Total Traffic (Mbps)
1	GOOSE	2	162	500 μ sec	5.184
2	GSSE	2	281	1 msec	4.49
3	Client/server applications	2	1456	1 msec	23.296
Total					32.97

5.1.5 Network analyzer

WireShark software is used as a network analyzer in a windows PC [93]. The network analyzer is configured in promiscuous mode to sniff all the packets from the entire IEC 61850-9-2 process bus network. It captures all the data packets from the network, and displays the content/structure of a packet in detail. In this hardware set-up, network analyzer is used to confirm the number of lost or delayed SVs, as well as to analyze the total traffic on the process bus.

5.2 IEEE 1588 based Precision Time Protocol (PTP) in a Laboratory

In order to implement IEEE 1588 [76] based PTP in a laboratory environment, SEL 2407 GPS receiver with antenna is used to connect it with process bus Ethernet switches. Ruggedcom Ethernet switches RSG 2288 has IEEE 1588-2008 capabilities to act as various clocks defined in the standard. Figure 5-4 illustrates the IEEE 1588 configuration in IEC 61850 process bus laboratory.

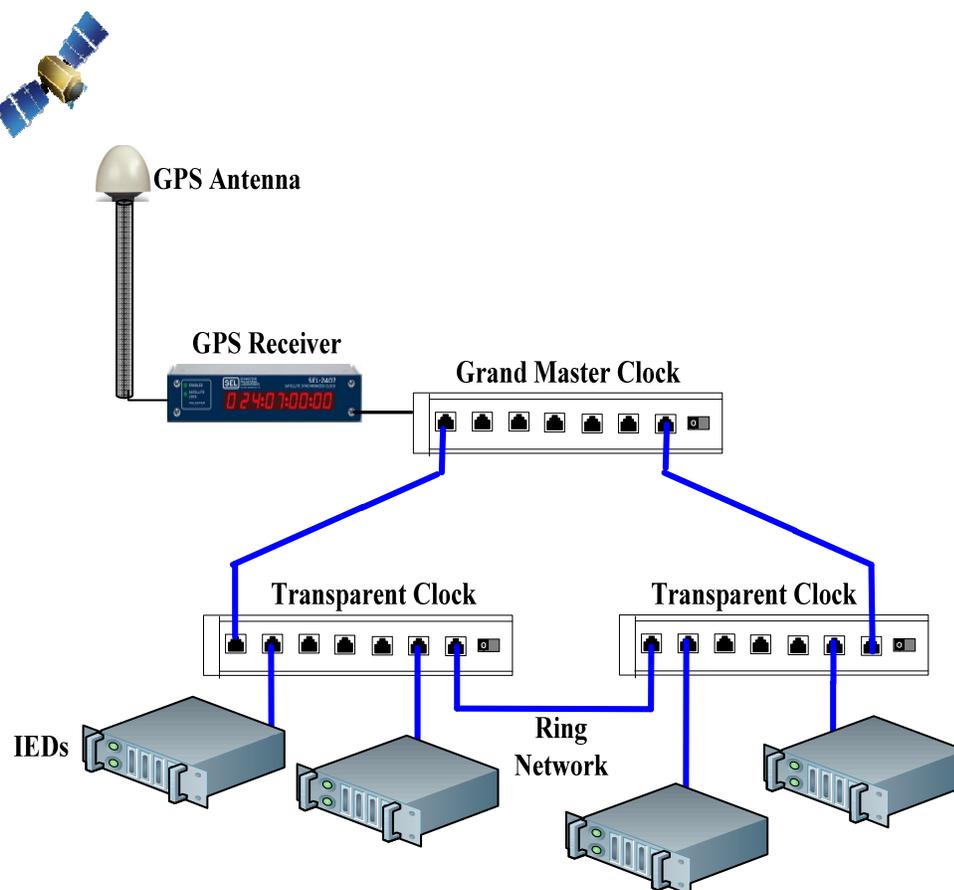


Figure 5-4 IEEE 1588-2008 over process bus network

Figure 5-5 shows the basic function block diagram of the IEC 61850-9-2 enabled protection IED with IEEE 1588-2008 (PTPv2) based time synchronization feature [76]. Protection IEDs are basically end nodes in the process bus network, and these devices receive IEEE 1588 defined time synchronization packets, as explained in Appendix D. Packet capture and filter receives these time synchronization packets from IEC 61850-9-2 network, and this function identifies IEEE 1588 packets (EtherType field of IEEE 1588 packet is 0x88F7 in hexa) and sends it to *Independent Process-3* as shown in the figure. Process-3 is responsible for synchronizing hard-real time clock of the QNX operating system. Since, all process are independent, they all are running simultaneously.

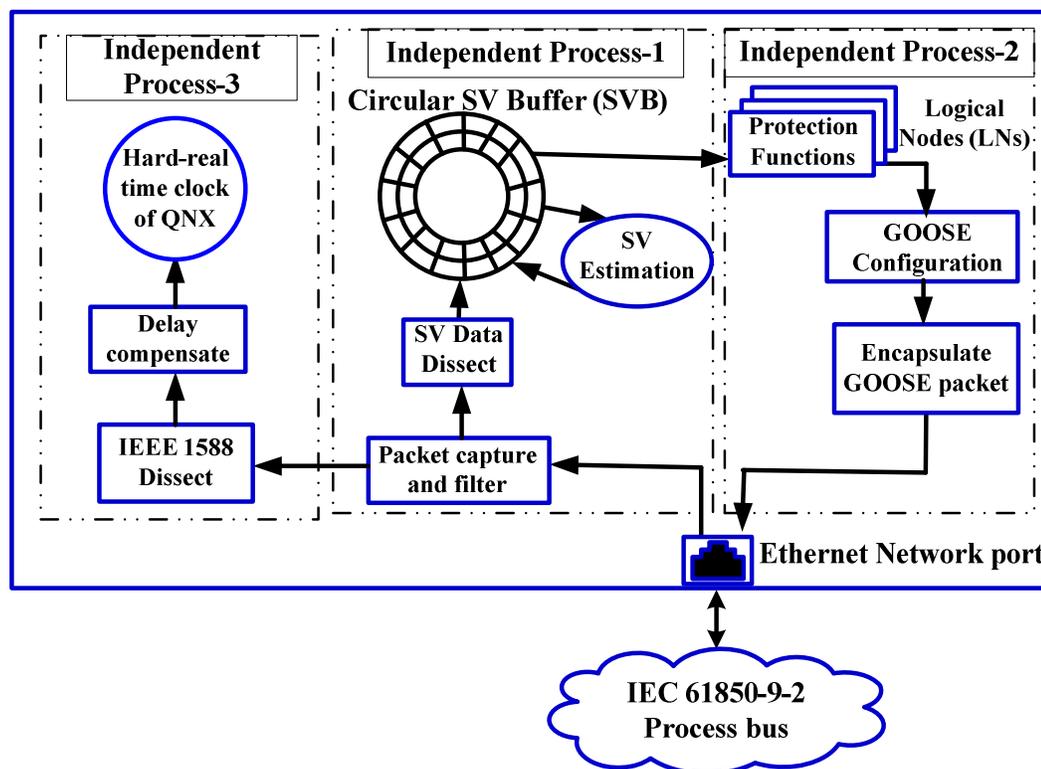


Figure 5-5 Implementation of IEEE 1588 in developed IEC 61850-9-2 enabled protection IED

IEEE 1588 Dissect function identifies the message types, and also obtains precision time stamp (10 byte) information from the appropriate packet field. Thereafter, this precision time information is sent to *delay compensate* function block. This function compensates all delays incurred over the IEC 61850-9-2 process bus network. Network delays on the path can be compensated using the working principle of IEEE 1588 standard, which is explained in Appendix D. Since the independent process-3 utilizes the time stamp at the Ethernet network port, the receiving packet time is accurate.

5.3 Laboratory Set-up

To examine the impact of SV loss/delay on bus differential and line distance protection functions, a typical 230 kV four feeder power system model is simulated using PSCAD/EMTDC, as shown in Figure 5-6. Bus differential protection is implemented for four feeders, as two feeders is too simple, and four feeders allow to study effectiveness of the SV algorithm in identifying feeder with lost and/or delayed SVs. More than four feeders may result in unnecessary complexity. A bus differential protection function

requires currents from all connected feeders (COMTRADE recorders 1 to 4); whereas, a distance protection function needs voltages and currents from corresponding feeder (COMTRADE recorder-5 for Line-3). The signal values collected in COMTRADE file are used in the merging unit simulator as shown in Figure 5-1.

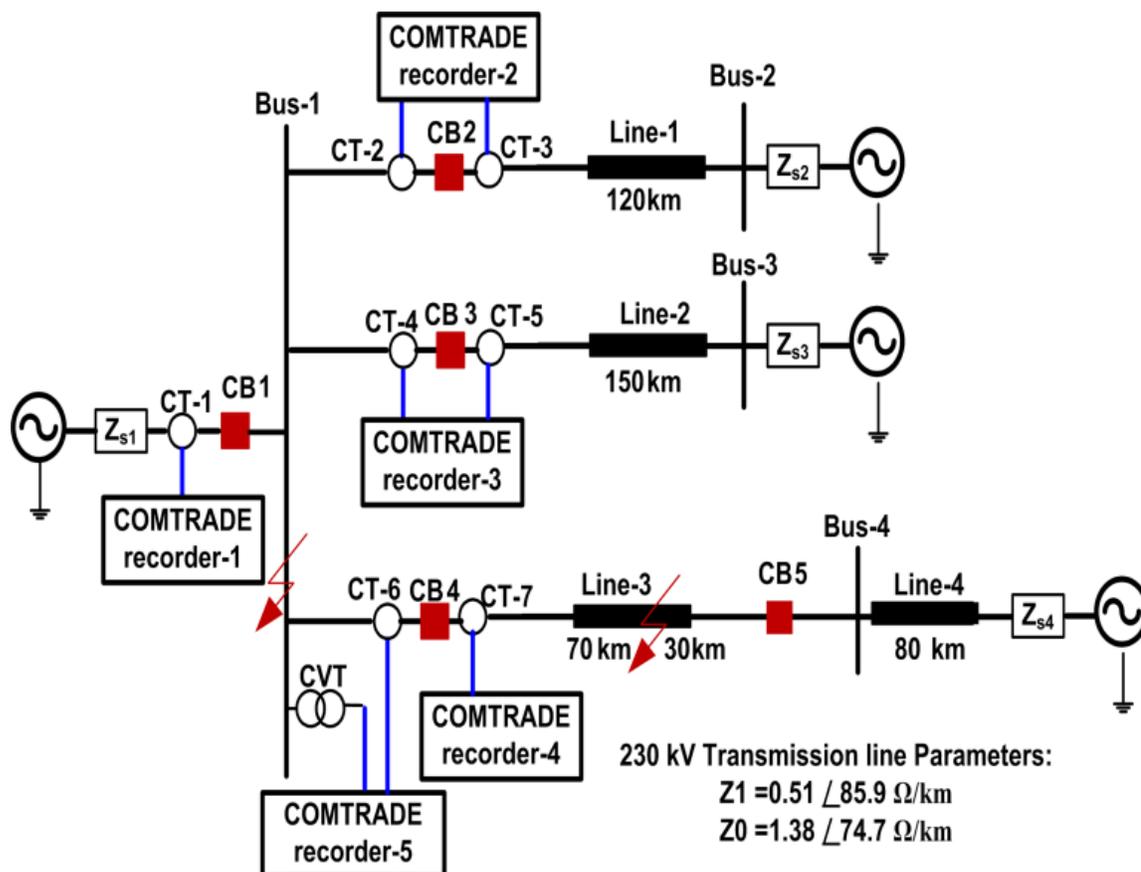


Figure 5-6 A typical power system simulated in PSCAD/EMTDC

Figure 5-7 shows the hardware test set-up of IEC 61850-9-2 based process bus communication network for the typical power substation (illustrated in Figure 5-6). All four merging units for the bus differential protection are implemented in a single embedded platform using a quad-port network interface card to avoid requirements of synchronization without compromising hard-real-time requirements. Commercial Ethernet switches designed for the substation environment are used for laboratory set-up. A single Ethernet switch is connected to station PC at station level to configure and monitor protection IEDs for various testing scenarios. The protection IEDs, merging units, traffic generator, and network analyzer are connected to two cascaded Ethernet

switches at the process level. The traffic generator injects various types of IEC 61850 messages over the process bus network. And, the network analyzer sniffs all kinds of packets in process bus using a port mirroring, and confirms a SV lost/delayed testing scenario for a particular IED [93]. The priority tagging and Virtual-LAN (VLAN) are setup in Ethernet switches to achieve a better quality of service. VLAN IDs used for distance protection system is 100 and for busbar differential, it is 200. Three bits of user priority in the TCI (Tag Control Information) field of the SV packet allow for eight classes of services (as defined in IEEE 802.1p), and this field can be set between 0 (i.e. lowest priority) to 7 (i.e. highest priority).

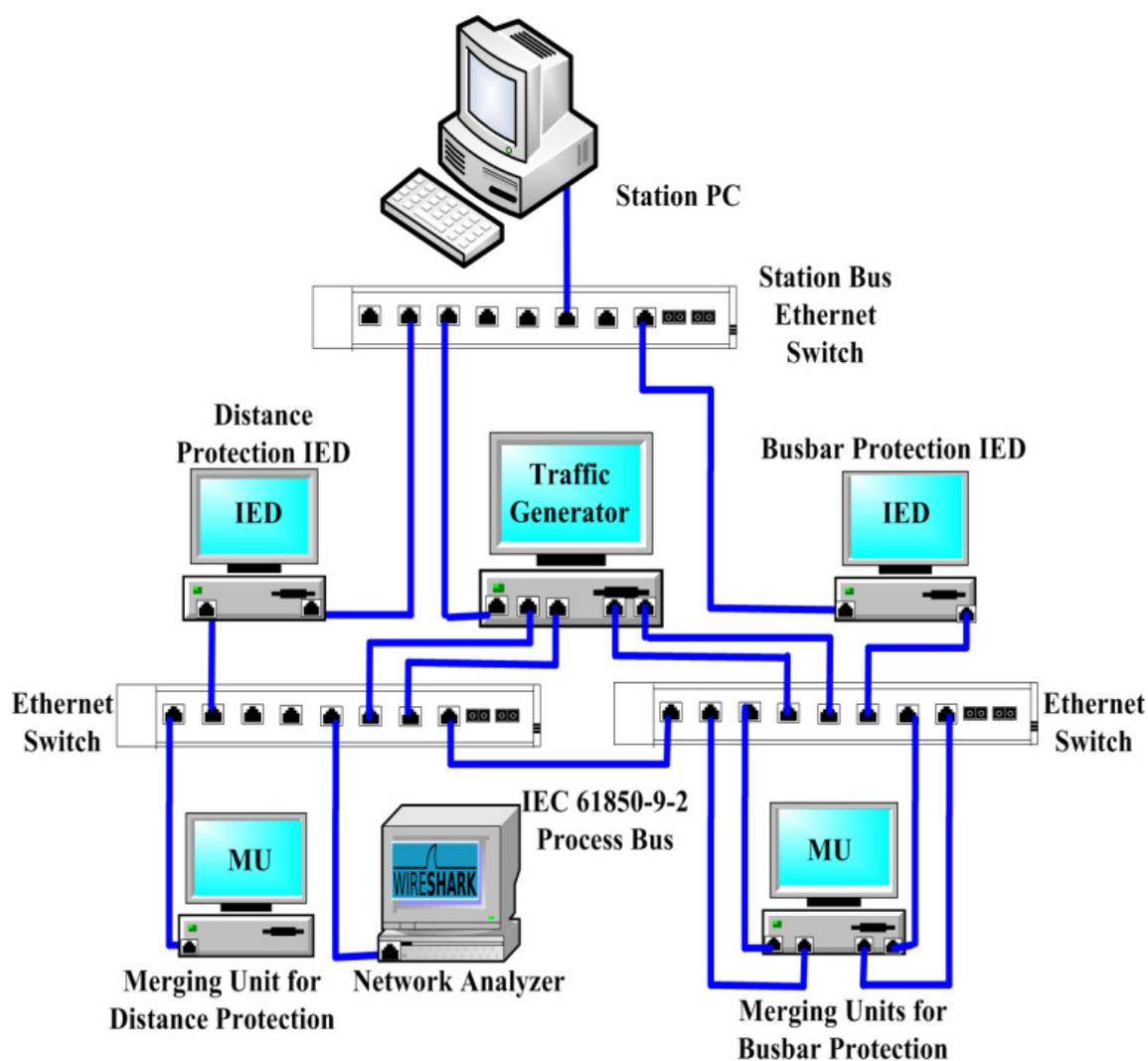


Figure 5-7 Laboratory set-up

Table 5-2 below shows the user priority levels considered in this setup. GOOSE messages are event triggered and therefore given higher priority, compared to time triggered SV messages. GSSE and other TCP/IP packets are given lower priority respectively, as they are less time critical messages comparatively.

Table 5-2 Priority levels of IEEE 802.1Q for IEC 61820-9-2

Sr. No.	Types of Messages	User priority level
1	GOOSE	7
2	Sampled value	6
3	GSSE	4
4	Client/server application packets over TCP/IP	1

5.4 Impact of SV Loss on Phasor Estimation

A DFT-based phasor estimation algorithm [94] is developed using MATLAB tool to understand the impact of SV loss. The MATLAB extracts the sampled value streams of each signal from the corresponding COMTRADE file. Figure 5-8 shows the window of CT-6 for A-phase secondary current during an A-G fault on Line-3 at 0.3 sec with 70 km distance from the relay location (as illustrated in Figure 5-6). With the help of a detailed dynamic simulation of IEC 61850-9-2 based process bus communication network in Chapter 3, it is shown that on average 1 to 6 consecutive SVs can be lost over the IEC 61850-9-2 based Ethernet switched process bus. In addition to the total number of SV loss, another parameter, i.e. number of sampling intervals between each SV loss is also considered (as shown in Figure 5-8) to understand the impact of SV loss in furthermore details. The figure shows the total of 4 SVs loss with a 3 sampling interval between each SV loss. The phasor magnitude of CT secondary current samples estimated using the full-cycle DFT technique is depicted in Figure 5-9.

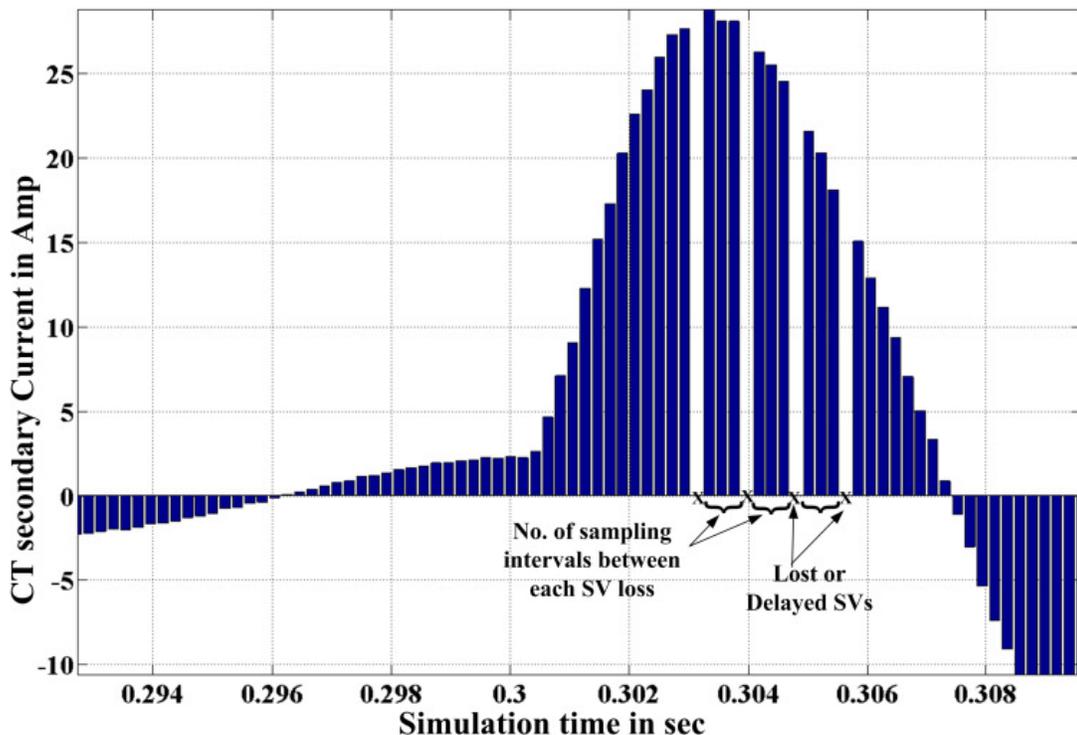


Figure 5-8 CT secondary current for the total 4 SVs loss with 3 sampling interval between each SV loss

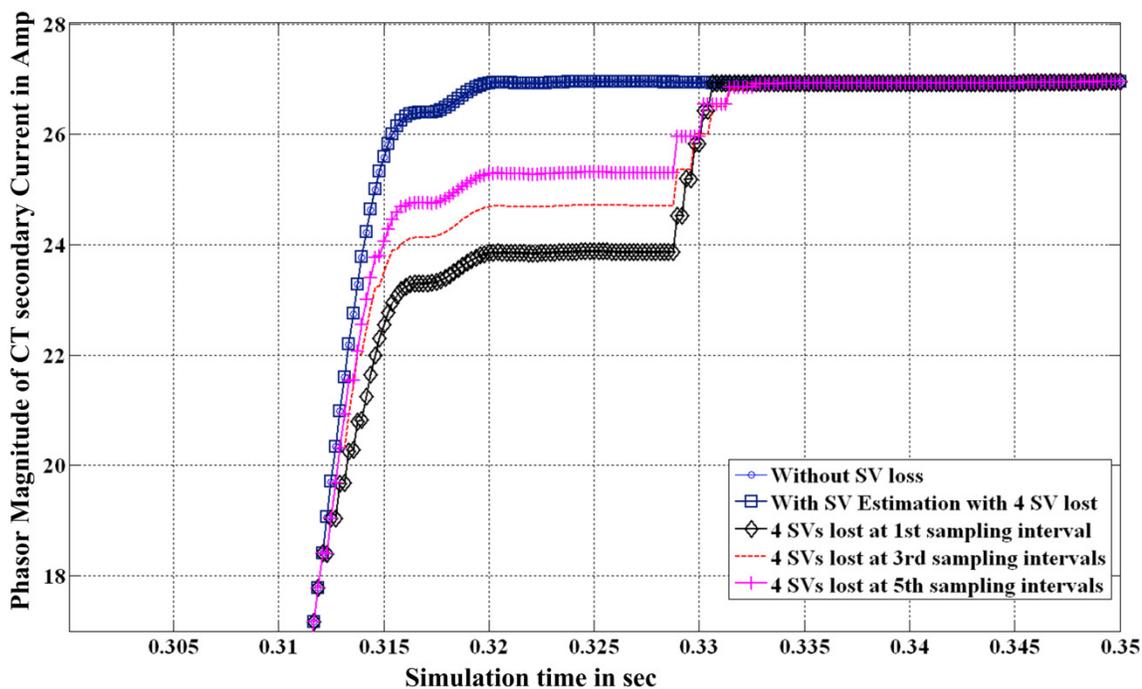


Figure 5-9 A-phase phasor magnitude with and without SV estimation

With the help of the MATLAB tool, the loss of total four SVs is simulated with 1, 3, and 5 sampling intervals between each SV loss, after a half cycle of fault inception. The

figure also shows the phasor magnitudes without SV loss/delay, as well as with the SV estimation algorithm. Traditional protection IEDs are not equipped with any corrective measures for SV loss/delay, and therefore, lost or delayed samples are neglected considering their values to be zero for the phasor estimation. Figure 5-9 shows that the magnitude of the phasor can be affected by the number of total SVs loss, as well as number of sampling intervals between each SV loss. On the other hand, the simple SV estimation algorithm can estimate the lost or delayed SV using few additional computations with enough accuracy. It can be observed from the Figure 5-9 that the value of phasor magnitude exactly follows the original value without SV loss. The detailed analysis on the accuracy the SV estimation technique is presented in Chapter 4.

5.5 Laboratory Testing Results and Discussion

Two protection functions are considered for the testing: 1) bus differential element; and 2) line distance element. The SV estimation algorithm is implemented as a part of the SV buffer, as explained in Figure 5-2. Merging units playback the SV packets in real time, and also, simulate various scenarios of SV loss/delay, as illustrated in Figure 5-1. Two parameters are selected to study various SV loss/delay conditions: 1) total number of SVs loss, and 2) number of sampling intervals between each SV loss, as explained in Figure 5-8. In Chapter 3, loss of up to 6 SVs is observed considering various dynamic scenarios; on the other hand, less than 3 SVs loss/delay may not have significant impact on a protection element. Therefore, the loss/delay of 3 to 6 SVs are considered at various sampling intervals after a half cycle (8.333 msec) from fault inception, and tested with and without SV estimation algorithm implementation. SV delay scenarios of 3 msec and 12 msec (less than a cycle) are tested to analyze the capability of SV estimation algorithm to substitute estimated values with the delayed one. This replacement may enhance accuracy of SV estimation for any further SV loss/delay. Furthermore, the testing is carried out considering low, medium, and high Source Impedance Ratios (SIRs) {0.2, 1, 5}; L-G (with fault resistance of 10 Ω) and L-L (without fault resistance) faults; different Points-on-Wave (POWs) {zero, mid, peak} with respect to A-phase voltage. The testing results and discussion on the protection elements are presented as follows:

5.5.1 Busbar differential protection element

Biased differential element of the busbar protection based on full-cycle DFT is developed using [94], [95] and implemented in the protection IED. For biased differential characteristic, the sum of the current magnitudes from all corresponding CTs is considered for restraint; whereas, the magnitude of the geometric sum of currents from all corresponding CTs is used for operation. The value of biased factor/slope (k) is set to 0.6, and the threshold of pick-up is fixed at 1 p.u. of CT secondary current rating. Figure 5-10 and Figure 5-11 show the performance of biased differential protection element for an external L-G fault (on Line-3) with total 3 SVs loss (at five sampling intervals between each SV loss) and total 5 SVs loss (at one sampling interval between each SV loss) respectively, from merging unit corresponding to CT-1. The SV loss causes drop in the magnitude of CT-1 current, which results in not only the rise of operating current, but also fall of the restraining current. The operating current with 3 SVs loss at 5 sampling intervals between each SV loss is not high enough to pick-up the element; whereas, with 5 SVs loss at one sampling interval between each SV loss, the locus of points enters into the operating region, and stays there for almost one cycle, which results into mis-operation of the busbar differential protection element. Operating time of the busbar differential protection is shown in Table 5-3. With the help of the SV estimation, the lost SVs are estimated, and the magnitude of the CT-1 current is maintained. As a result, restraining current remains higher and operating current is almost negligible during the external fault, which can be observed in the figures.

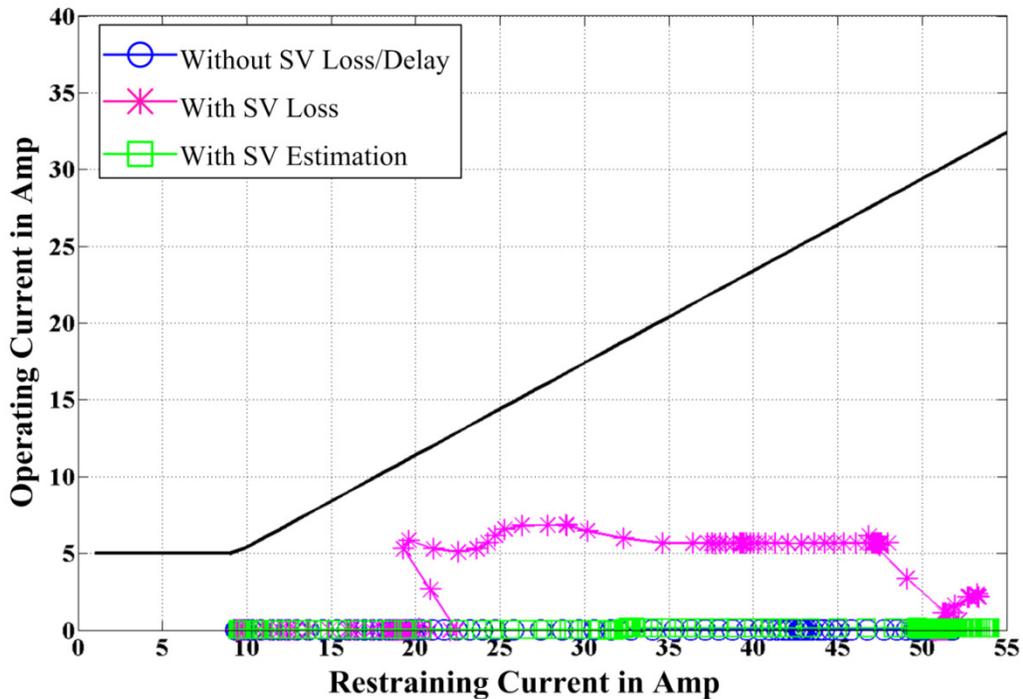


Figure 5-10 Biased differential element performance during an external fault with total of 3 SVs loss at five sampling intervals between each SV loss

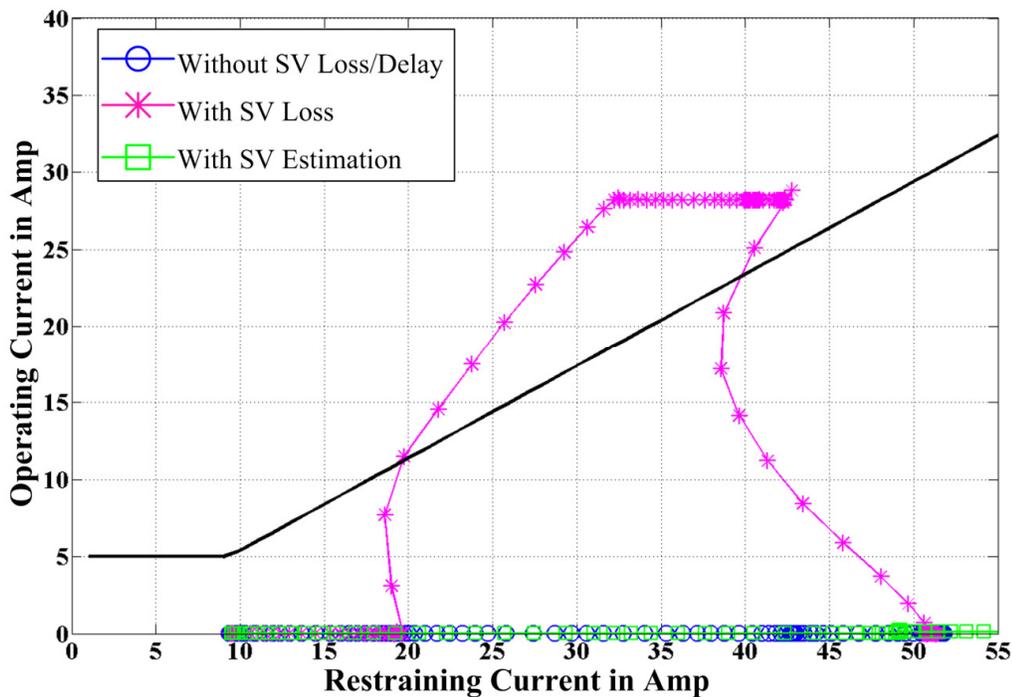


Figure 5-11 Biased differential element performance during an external fault with total of 5 SVs loss at one sampling interval between each SV loss

Table 5-3 depicts the operating time of busbar biased differential protection element for various SV loss scenarios, considering cases with and without the SV estimation algorithm. SV loss is carried out in one of the four merging units, and SV loss conditions include loss of 3 to 6 SVs at an interval of 1, 3 and 5 sampled values. Both, L-G and L-L faults are simulated on the Bus-1 (internal fault) as well as on the Line-3 (external fault).

Table 5-3 Bus differential operating times for various SV loss scenarios

Total No. of SV Loss	No. of sampling interval between each SV loss	Bus Differential Relay Operating Time (in msec)					
		LG Fault ($R_f=10 \Omega$)				LL Fault ($R_f=0 \Omega$)	
		Internal Fault (on Bus-1)		External Fault (on Line-3)		External Fault (on Line-3)	
		Without SV Esti.	With SV Esti.	Without SV Esti.	With SV Esti.	Without SV Esti.	With SV Esti.
3	1	10.52	9.05	13.80	NO	15.47	NO
	3	10.13	8.87	14.20	NO	NO	NO
	5	10.05	8.52	NO	NO	NO	NO
4	1	10.34	9.14	13.9	NO	14.60	NO
	3	10.11	8.94	14.80	NO	16.07	NO
	5	10.01	8.68	14.70	NO	NO	NO
5	1	10.48	9.11	14.10	NO	16.51	NO
	3	10.13	8.56	14.40	NO	16.74	NO
	5	10.12	8.41	15.64	NO	25.73	NO
6	1	10.67	9.21	13.40	NO	15.21	NO
	3	10.41	8.73	14.00	NO	16.84	NO
	5	10.12	8.58	16.8	NO	26.35	NO
NO : No Operation of protection element							

Normally, the operating time of busbar differential relay without any SV loss is observed around 8-10 msec. It can be observed from the table that even due to SV loss busbar protection IED clears fault in 8-10 msec for L-G fault at the Bus-1 which is same as the operating times without any SV loss/delay. It is tested that the busbar differential element does not pick-up for any external faults during normal operating condition. However, in case of sampled value loss at different sampling intervals, the biased differential element mis-operates for the Line-3 (external) fault within 13-26 msec as shown in the table. Further, it can be observed from the table that biased differential relay remains secure

(did not operate for any external fault), if the SV estimation algorithm is implemented in the protection IED.

The performance of the biased differential element during the external fault with 6 SVs delayed by 12 msec is shown in Figure 5-12. The figure shows that with six sampled value delay, the operating current increases enough to mis-operate the protection. Furthermore detailed testing results for various SV delay scenarios are tabulated in Table 5-4.

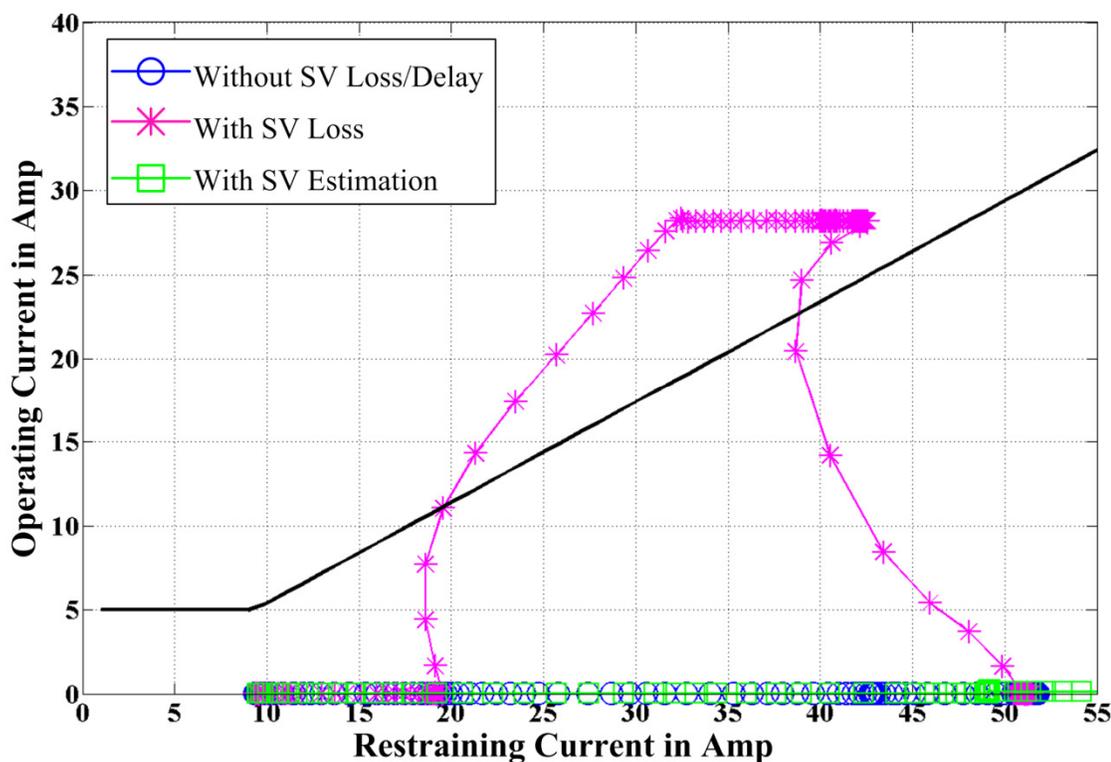


Figure 5-12 Biased differential element performance during external fault with 6 SVs delayed by 12 msec

Table 5-4 illustrates the operating time of the bus differential IED for 3 to 6 SVs delayed by 3 and 12 msec. The tabulated results show that the bus differential protection element does not mis-operate if the lost SVs arrived within 3 msec delay; whereas, for 12 msec delay, the protection element mis-operates within 13-15 msec. Furthermore, the mis-operation of the protection element with SV delays is prevented with SV estimation algorithm.

Table 5-4 Bus differential protection operating times for various SV delays

Total No. of SV Delay -ed	Time of delayed SV arrival (msec)	Bus Differential Relay Operating Time (msec)					
		LG Fault ($R_f=10 \Omega$)				LL Fault ($R_f=0 \Omega$)	
		Internal Fault (on Bus-1)		External Fault (on Line-3)		External Fault (on Line-3)	
		Without SV Esti.	With SV Esti.	Without SV Esti.	With SV Esti.	Without SV Esti.	With SV Esti.
3	3	10.9	9.05	NO	NO	NO	NO
	12	10.3	8.97	13.76	NO	14.72	NO
4	3	10.61	8.83	NO	NO	NO	NO
	12	10.63	9.08	13.99	NO	15.01	NO
5	3	10.12	8.34	NO	NO	NO	NO
	12	10.53	8.56	14.23	NO	15.13	NO
6	3	10.9	8.67	NO	NO	NO	NO
	12	10.98	9.05	14.31	NO	15.25	NO
NO : No Operation of protection element							

Table 5-5 demonstrates the operating time of the bus differential element for various SIRs, fault types, POWs, with 4 SV loss at a 1 sampling interval. It can be observed from the table that the busbar differential relay can lose security even during the external fault with SV loss. On the other hand, with the SV estimation algorithm, the protection remains secure.

Table 5-5 Bus differential protection operating times for various scenarios

System scenarios for the External faults on Line-3		POW	Operating time (msec)	
			Without SV Esti.	With SV Esti.
SIR=0.2	LG fault ($R_f=10 \Omega$)	Zero	14.60	NO
		Mid	13.47	NO
		Peak	12.25	NO
		Avg.	13.44	NO
	LL fault ($R_f=0 \Omega$)	Zero	15.10	NO
		Mid	13.03	NO
		Peak	12.11	NO
		Avg.	13.41	NO
SIR=1	LG fault ($R_f=10 \Omega$)	Zero	13.74	NO
		Mid	16.72	NO
		Peak	12.01	NO
		Avg.	14.16	NO
	LL fault ($R_f=0 \Omega$)	Zero	15.72	NO
		Mid	13.39	NO
		Peak	15.25	NO
		Avg.	14.79	NO
SIR=5	LG fault ($R_f=10 \Omega$)	Zero	19.19	NO
		Mid	14.73	NO
		Peak	11.81	NO
		Avg.	15.24	NO
	LL fault ($R_f=0 \Omega$)	Zero	15.06	NO
		Mid	19.77	NO
		Peak	11.98	NO
		Avg.	15.60	NO
NO : No Operation of protection element				

5.5.2 Distance protection

Mho characteristic with the phase comparator using the memory polarization is developed as a protection element using references [94], [96]. If the angle difference between the polarizing quantity (V_{pol}) and operating quantity ($IZ-V$) is less than 90° , a corresponding distance protection element will pick-up. The transmission line distance protection IED is set to protect 80% of 100km long Line-3 in zone-1. Line-to-ground (L-G) and line-to-line (L-L) faults are applied at 70km of the Line-3 from the relay location, as shown in Figure 5-6. The angle difference between phase comparator quantities with total of 3 SVs loss (at five sampling intervals between each SV loss) and total of 5 SVs loss (at one sampling interval between each SV loss) respectively, from the merging unit corresponding to COMTRADE recoder-5, is shown in Figure 5-13 and Figure 5-14 respectively.

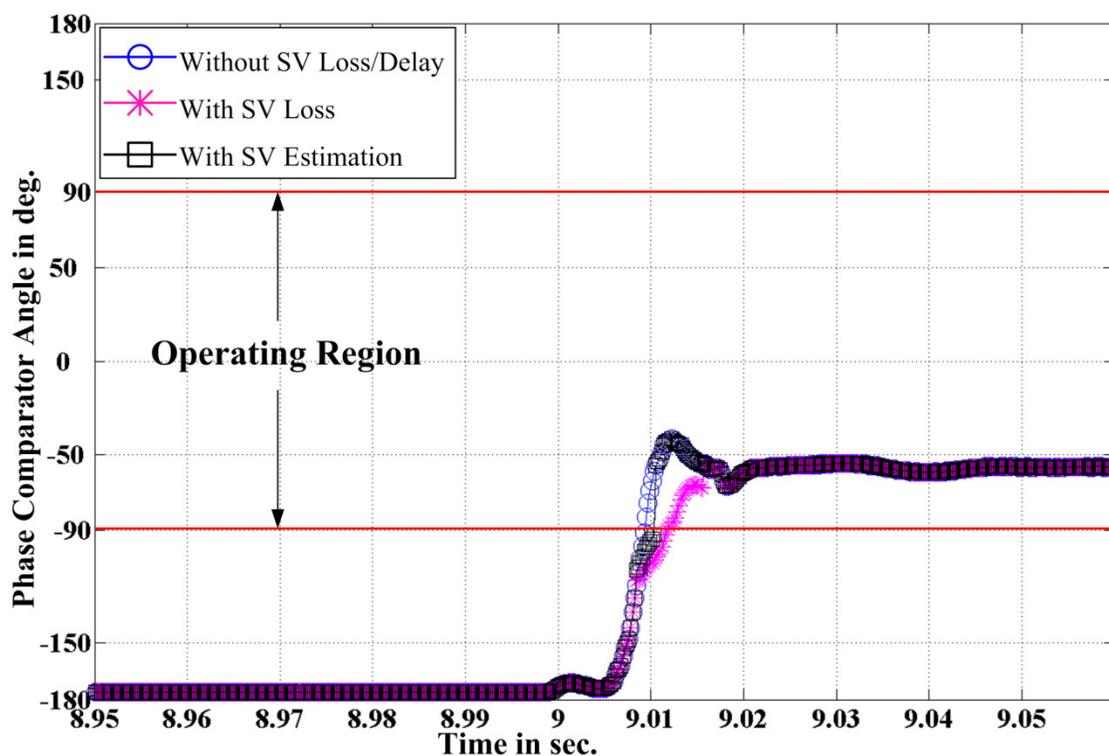


Figure 5-13 Phase comparator angle of Zone-1 distance protection element with total of 3 SVs loss at five sampling intervals between each SV loss

It can be observed from the figures that the locus of angle difference with a total 3 SVs loss at five sampling intervals enters into the operating region with very small delay;

whereas, with total 5 SV loss at one sampling interval, the locus of phase comparator angle remains outside of the operating region for almost one cycle, and this causes a delay in operation of zone-1 protection.

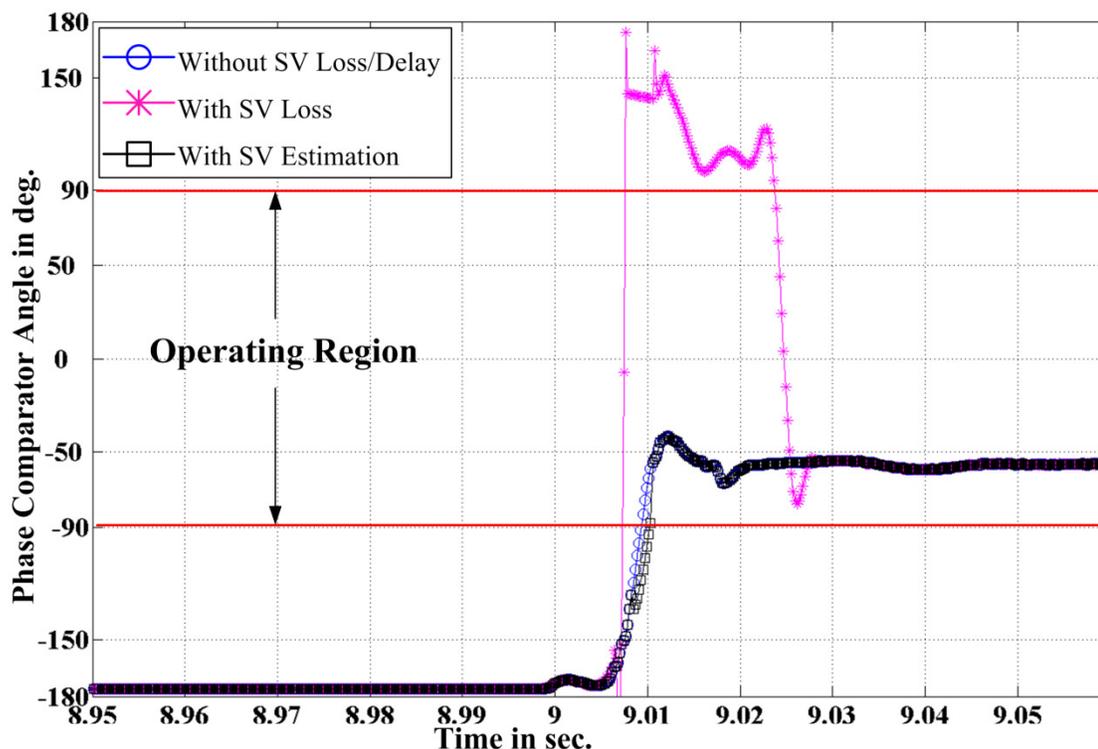


Figure 5-14 Phase comparator angle of Zone-1 distance protection element with total of 5 SVs loss at one sampling interval between each SV loss

Figure 5-15 shows the operating time of the distance protection IED, considering end-to-end communication delays over IEC 61850-9-2 process bus. Without any SV loss or delay, the average operating time of the distance protection element is around 23 msec for the scenarios considered here. It can be observed from the figure that the SV loss can cause an operating time of zone-1 as high as 41 msec; whereas using the SV estimation, the relay can operate normally (in 23-25 msec).

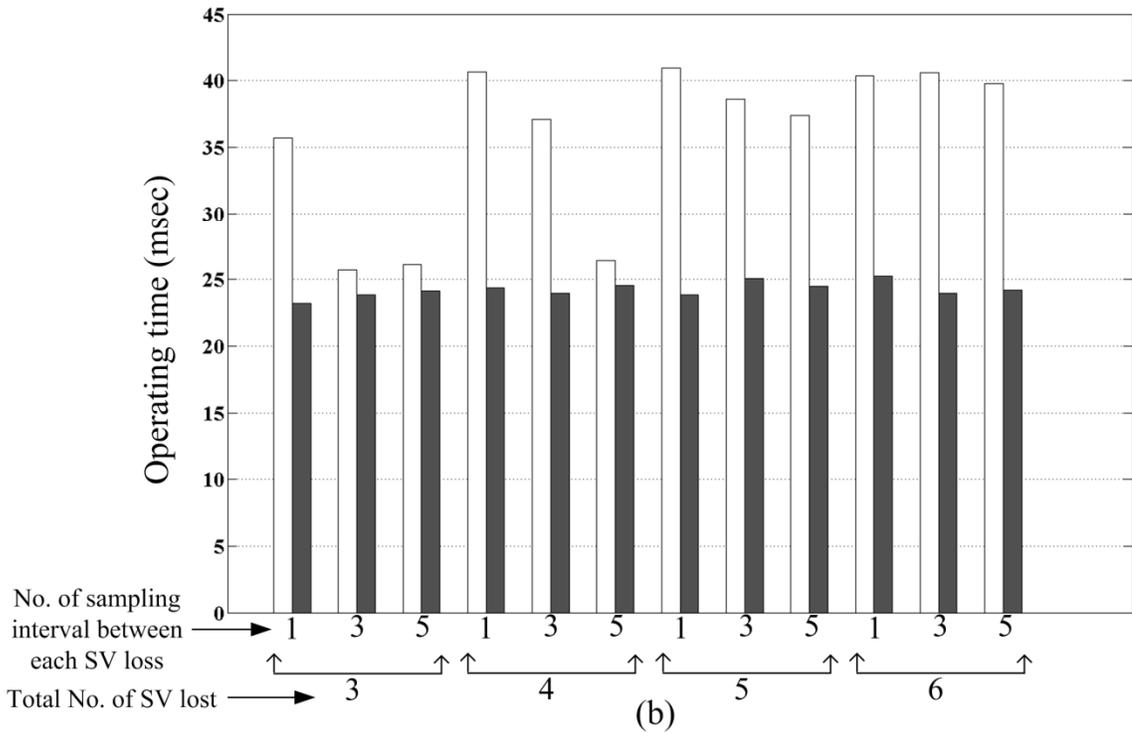
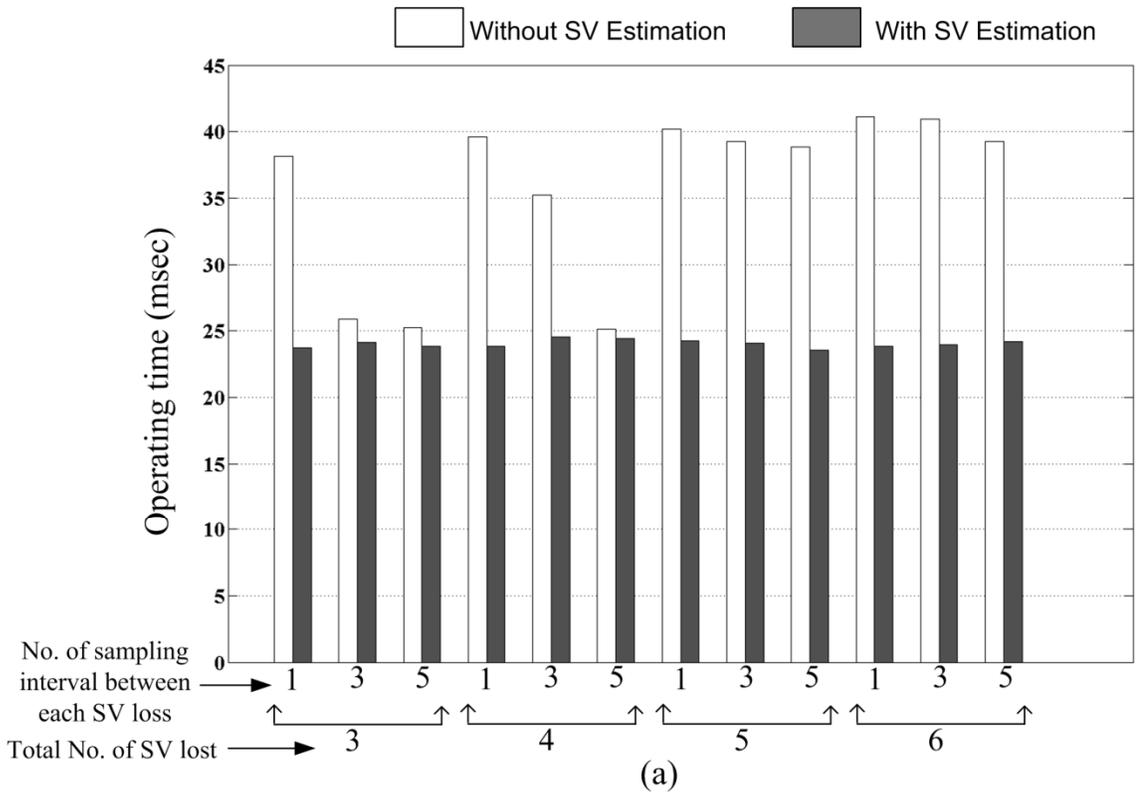


Figure 5-15 Transmission line distance protection IED operating times for various SV loss scenarios: (a) for L-G fault, (b) for L-L fault

Figure 5-16 illustrates the operating times of Line-3 distance protection for 3 to 6 SVs delayed by 3 and 12 msec. Results in the figure show that the SVs causes delay in zone-1 pick-up. And, this delay can be eliminated using the SV estimation algorithm implemented within the line distance IED.

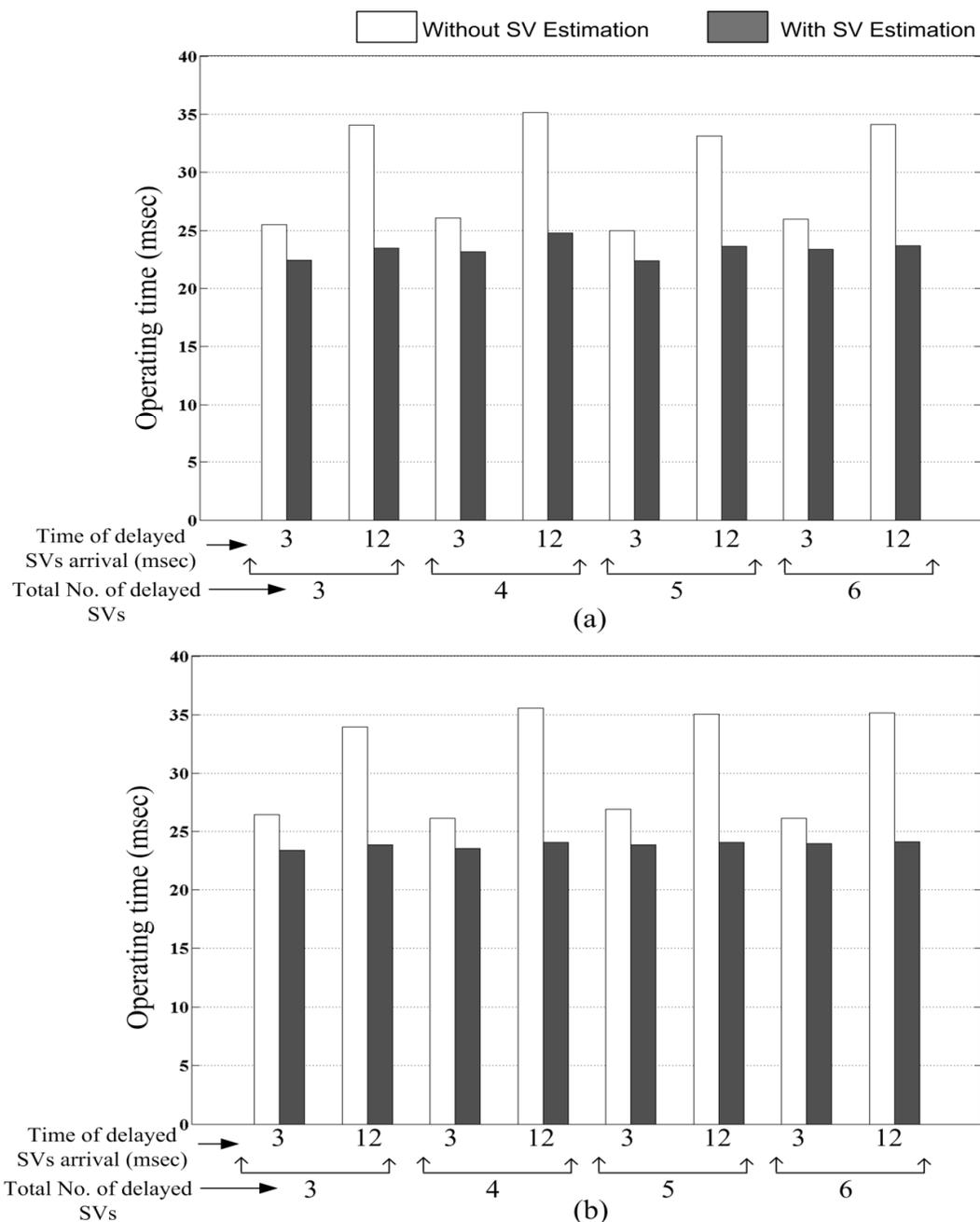


Figure 5-16 Transmission line distance protection IED operating times for various SV delay scenarios: (a) for L-G fault, (b) for L-L fault

Figure 5-17 shows the testing results of the distance protection for various SIRs, fault types, and POWs. For this investigation, 4 SVs loss at one sampling interval between each SV loss is considered. It can be observed from the figure that zone-1 element pick-up is delayed up to 43 msec due to SV loss without SV estimation algorithm.

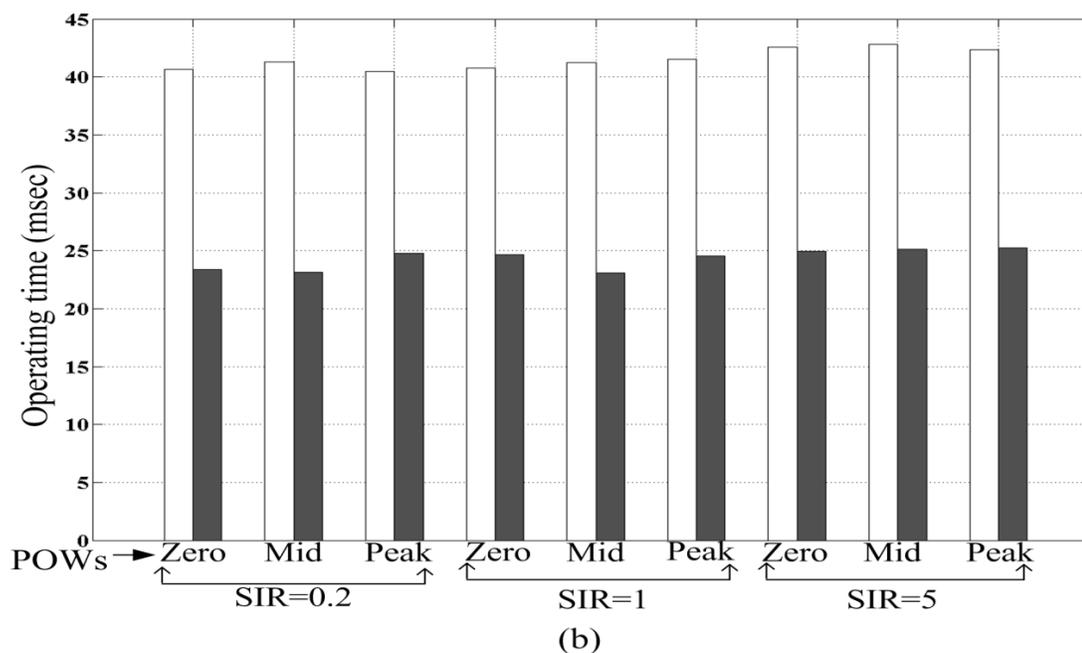
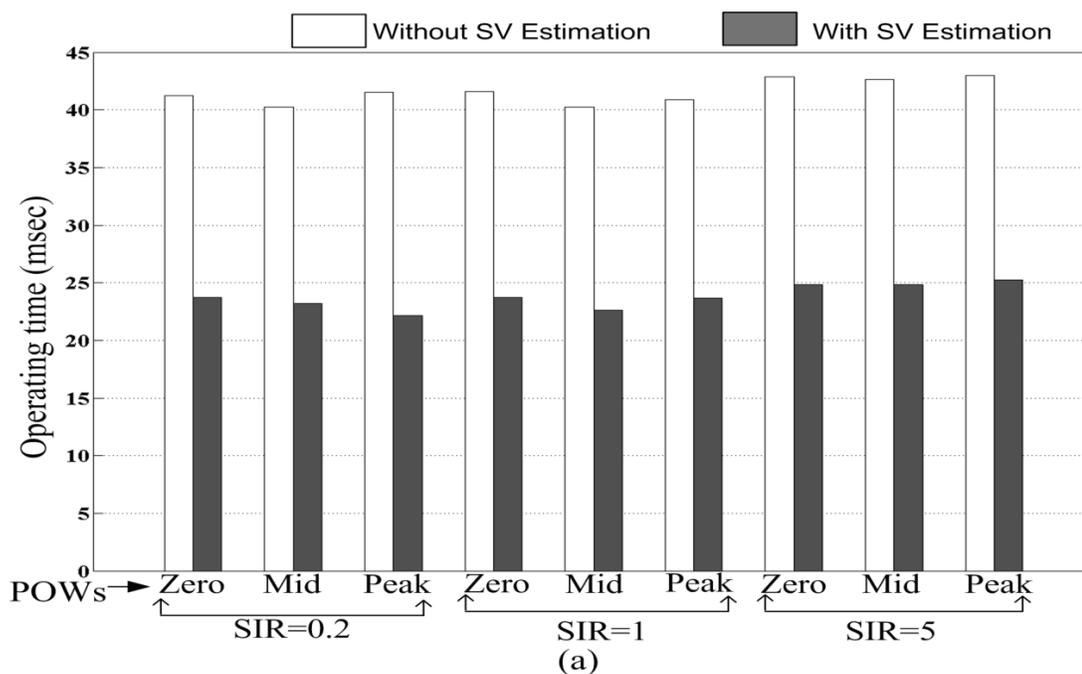


Figure 5-17 Distance protection operating times for various SIR and POW: (a) for L-G fault, (b) for L-L fault

Table 5-6 illustrates the results of testing distance protection for various fault locations over Line-3. The comparison of the results for SV loss and delay shows that zone-1 element operation is not affected by the SV loss/delay, if the SV estimation algorithm is implemented as a part of the protection IED. Moreover, the zone-1 distance protection element remains secure in all cases during the fault in zone-2. The SV estimation algorithm for distance protection with 10 consecutive SVs is presented in [97].

Table 5-6 Distance protection operating times for various fault locations on line-3

Fault Locations on Line-3 (%)	Distance Zone-1 Element Operating Time (msec)				
	Without SV Loss/ Delay	3 SV delayed for 5 msec		4 SV loss with an interval of 1 SV	
		Without SV Esti.	With SV Esti.	Without SV Esti.	With SV Esti.
0	19.26	25.14	20.05	37.05	20.86
10	20.35	25.63	20.17	37.78	21.24
25	20.87	26.03	20.91	38.24	21.07
40	21.49	26.42	21.56	38.72	21.88
65	22.57	27.09	23.34	39.84	23.08
75	23.05	28.54	23.12	40.15	23.25
90	NO	NO	NO	NO	NO
100	NO	NO	NO	NO	NO
NO : No Operation of protection element					

5.6 Summary

To investigate the performance of the proposed SV estimation algorithm, IEC 61850-9-2 enabled protection IEDs and merging unit simulator are developed in a laboratory environment using industrial embedded systems over hard-real time platform. Moreover, a typical process bus communication network is set-up using a network analyzer, traffic generator, and commercial Ethernet switches. Implementation of the SV estimation algorithm is proposed as a part of sampled value buffer in a protection IED, in such a way that it does not interfere with any existing protection functions. And therefore, it is

compatible with any well established traditional digital relaying elements in a protection IED. The impact of sampled value loss/delay on full-cycle DFT based protections is analyzed using MATLAB. From this behavior analysis, it is inferred that in some worst conditions, the phasor used for the protective relaying is affected due to multiple SVs loss. To counteract this adverse effect, the SV estimation algorithm is investigated as a part of busbar differential protection and transmission line distance protection IEDs for various SV loss/delay scenarios in a laboratory environment. With the help of the hardware setup, it is demonstrated that the busbar differential element in the protection IED may lose security, and mal-operates during external fault due to SV loss/delay in certain conditions. Moreover, distance relay zone-1 protection is delayed by 15-20 msec, due to SV loss/delay. It is demonstrated with extensive testing that with implementation of the SV estimation algorithm, the bus differential protection element remains secure during external fault, as well as, the line distance protection element operates correctly in time. It is important to note that the performance of the protection elements may not be affected for various other SV loss/delay scenarios. However, the presented investigation shows that the corrective measure for SV loss/delay can certainly help in improving performance of digital protection functions in IEC 61850-9-2 based environment. The next chapter will analyze the system reliability of the process bus communication networks using a reliability block diagram (RBD) method.

Chapter 6

6. Combinatorial Reliability Analysis of Process Bus Architectures for Protection Systems

This chapter presents the reliability and availability calculations of various process bus communication architectures, considering the practical Ethernet switched networks, e.g. cascaded, ring, star-ring, redundant-ring, as well as, the time synchronization techniques: 1) external TS using IRIG-B, and 2) TS over network using IEEE 1588. The results of reliability and availability are compared for a typical substation layout.

6.1 Reliability and Availability Analysis for Process Bus Architectures

The reliability and availability evaluation of the future process bus architectures with the different possible time synchronization configurations is important to evaluate before studying their impacts on various protection reliability indices. Ethernet communication devices can be connected in various combinations using Ethernet switched LANs [6]. In addition to this, the time synchronization can be employed using different techniques, such as external time synchronization source (using IRIG-B protocol [75]), time synchronization on LAN (using IEEE 1588 [76]). The comparison of all these different process bus architectures is carried out using a sample electric power substation layout. The quantitative values of reliability and availability for these different process bus architectures are obtained using the reliability block diagram technique [98].

The reliability and availability analysis using the Reliability Block Diagram (RBD) method are explained in reference [98]-[100]. Although, the reliability analysis using other methods, such as fault tree, cut set, path set, etc. have different formal presentations, they all may give similar results as RBD [98]. For qualitative and

quantitative analyses, RBD is more preferable, as it is easy to understand, and hence it is used for this work. Basic reliability and availability calculations using RBD method are discussed in Appendix E in detail.

Although, the method to calculate reliability of Ethernet architectures is presented considering a typical transmission substation, these developed models are general and can be applied to any power substation. The practical Ethernet switched architectures suggested by the IEEE PSRC report (as discussed in Chapter 2), such as cascaded, ring, star-ring, redundant-ring are studied here considering two time synchronization techniques: 1) external time synchronization using IRIG-B [75]; 2) time synchronization over the same Ethernet switched network using IEEE 1588-2008 [76].

The reliability block diagrams representation is divided in three subsections: 1) reliability of an Ethernet switched communication network; 2) reliability of the entire substation process bus architecture with the IRIG-B based time synchronization; 3) reliability of the entire substation process bus architecture with the IEEE 1588 based time synchronization. Reliability of the Ethernet switched communication networks is analyzed to obtain failure rate of communication network (λ_{comN}) between two extreme ends of the network. Moreover, the sender ESW is considered separately in series with MUs, to obtain failure rate of communication devices (λ_{comD}) pertaining to a specific protection. This calculated failure will be used in the following chapter.

6.2 Parameters for the Analysis

Reliability can be represented as a Mean Time To Failure (MTTF), which is the average time between system breakdowns or loss of service. The MTTF values for reliability calculations are considered from references [7], [35], and are tabulated in Table 6-1. The basic assumption is applied here that the failure modes are independent from each other [98]. Further, using Mean Time To Repair (MTTR) of 24 hours from the reference [35], availability of individual components is calculated (according to Appendix E), as shown in Table 6-1.

Table 6-1 MTTF considered for each SAS components

SAS component	MTTF (in years)	Availability
Prot. IED with communication interface	150	0.999981735
MU with communication interface	150	0.999981735
TS with communication interface	150	0.999981735
Ethernet Switch	50	0.999945208
Fiber cables	500	0.999994521

Using these tabulated individual component values, the MTTF and availability are calculated for various process bus architectures of a typical power substation described in Appendix B. It can be observed from the Appendix B that this sample substation has total 8 protections which include 4 transmission lines; 2 transformers; and 2 bus protections. All 8 protection system has two protection IEDs: main protection IED-A, and redundant protection IED-B. Moreover, each line protection IED is connected to 3 MUs; each transformer protection IED is connected to 4 MUs; and each bus protection IED is configured with 2 MUs.

6.3 Analysis of Cascaded Process Bus Architecture

In cascaded architectures, all four Ethernet switches are connected in a daisy chain (with open loop) configuration as shown in Figure 6-1. This architecture has only one path for the data communication. The figure only shows the time synchronization over the communication network using IEEE 1588. In external time synchronization architecture, all MUs located in close vicinity are synchronized with the common time synchronization source through external IRIG-B signals. Time synchronization over the network is provided using GPS antenna connected to one of the Ethernet switch (acting as grand master) according to IEEE 1588-2008 standard.

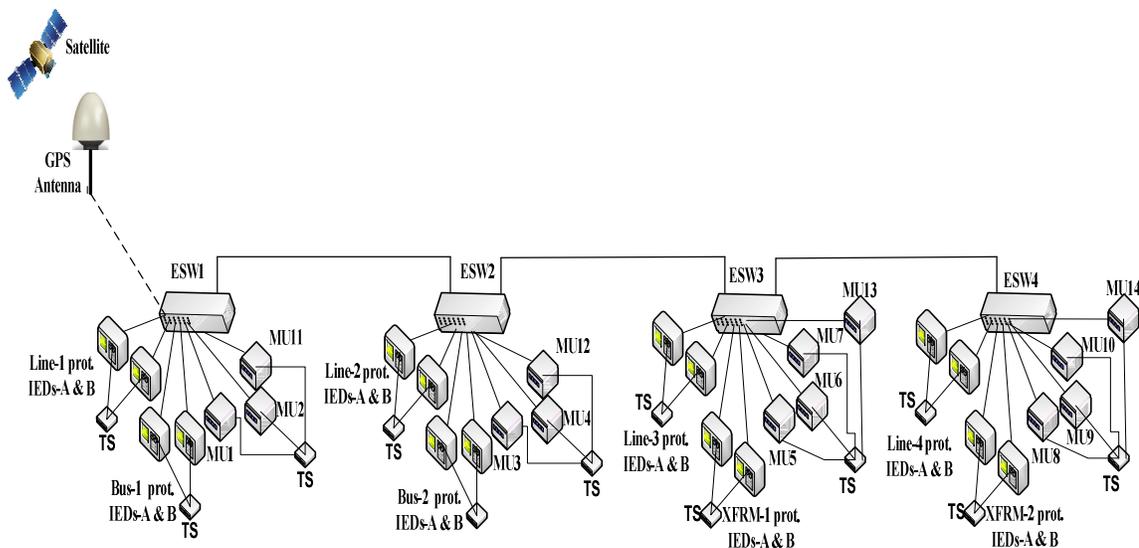


Figure 6-1 Cascaded process bus architecture of 345/230kV substation

6.3.1 Reliability and availability of a cascaded Ethernet switched network

The reliability block diagram of the above four cascaded Ethernet switched architecture is shown in Figure 6-2. To communicate from an Ethernet switch to another Ethernet switch over the process bus, receiving side Ethernet switch, as well as, two Ethernet network switches are required. Moreover, all three fiber cables connecting all four Ethernet switches are important for the communication. Therefore, three Ethernet switches and fiber cables would be in series for the reliability analysis. It can be observed from the RBD that this architecture is not fault tolerant, and any failure can cause loss of communication.



Figure 6-2 Reliability block diagram of a cascaded Ethernet architecture

6.3.2 Cascaded process bus architecture with IRIG-B

A general reliability block diagram for cascaded process bus architecture with external IRIG-B based time synchronization is shown in Figure 6-3. Time synchronization source are considered in series with protection IEDs as well as MUs. Moreover, Ethernet switch of a specific protection should be working to facilitate communication between IEDs and MUs, and therefore, it is connected in series. Protection IEDs-A and B are redundant, and therefore connected in parallel.

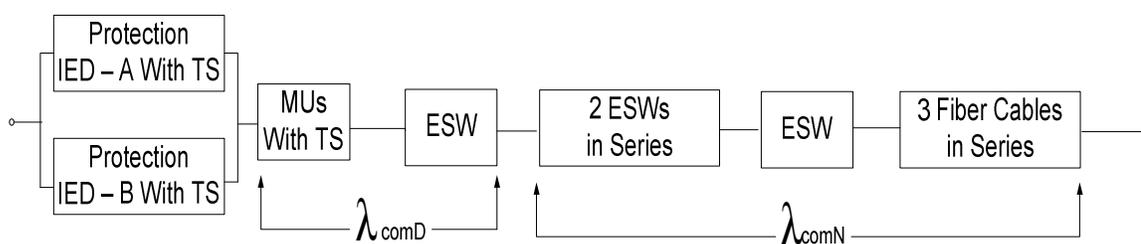


Figure 6-3 RBD for cascaded process bus architecture with TS using IRIG-B

6.3.3 Cascaded process bus architecture with IEEE 1588

Figure 6-4 shows the RBD of the cascaded process bus architecture with the IEEE 1588 based time synchronization over the network. Unlike IRIG-B (of Figure 6-3), the time synchronization source based on IEEE 1588 is connected to one of the Ethernet switch as a part of communication network to synchronize all IEDs and MUs of the process bus. And therefore, IEDs and MUs do not require any external time synchronization source.

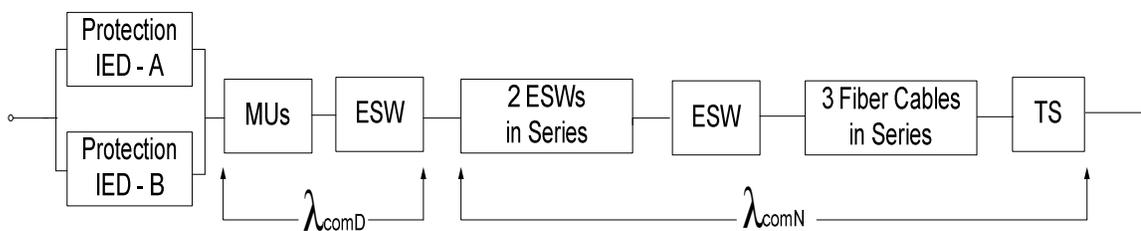


Figure 6-4 RBD for cascaded process bus architecture with TS using IEEE 1588

6.3.4 Reliability and availability results for cascaded process bus architecture

Sample calculations to calculate reliability (MTTF) and availability from reliability block diagram is explained in Appendix E. The reliability and availability of various zones of protections with the cascaded process bus architecture (as shown in Figure 6-1) is tabulated in Table 6-2 considering both IRIG-B and IEEE 1588 based time synchronization techniques. Figure 6-3 and Figure 6-4 are general RBDs for all various protections of the substation, such as line, transformer, and bus. The only difference in RBD of these protections is the number of MUs, e.g. line protections need 3 MUs, transformer protections require 4 MUs, and bus protections demand 2 MUs. Therefore, it can be observed from the table that bus protection has the higher reliability and availability, followed by line protection, and finally the transformer protection (as it has higher requirement for MUs). In addition to that, the reliability and availability of the IEEE 1588 based TS over network has higher reliability and availability as compared to the IRIG-B based external TS technique, as the number of TS devices required for IEEE 1588 technique is less.

Table 6-2 Reliability and availability results for a cascaded process bus architecture

Zones of Protection	Cascaded Architecture			
	External TS (using IRIG-B)		TS over network (using IEEE 1588)	
	MTTF (years)	Availability	MTTF (years)	Availability
Line-1, 2, 3, 4	8.08	0.999671294	8.54	0.999689553
XFMR-1,2	7.67	0.999653035	8.08	0.999671294
Bus-1, 2	8.54	0.999689553	9.05	0.999707812

6.4 Analysis of Ring Process Bus Architecture

In ring architecture, all four managed Ethernet switches are connected in a single loop, as shown in Figure 6-5. In order to prevent messages from circulating in the network loop, the Ethernet switches should support IEEE 802.1w RSTP.

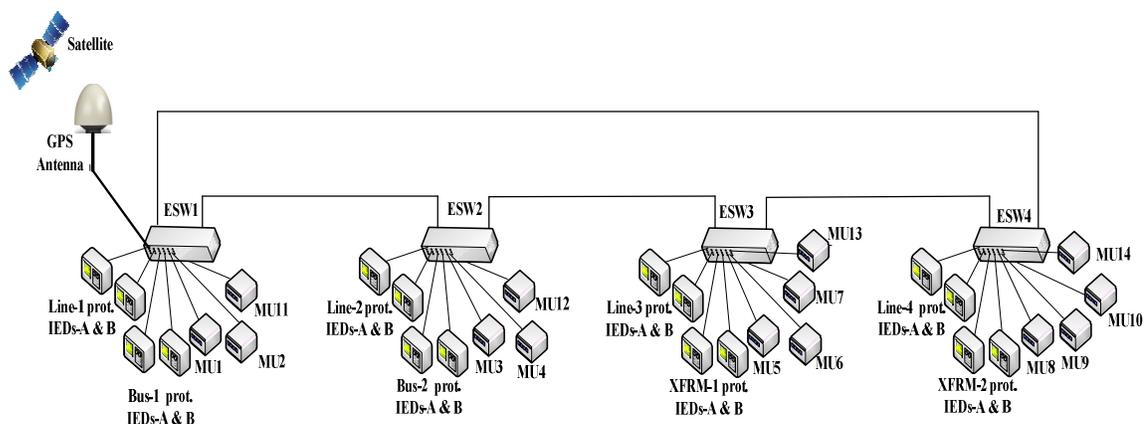


Figure 6-5 Ring process bus architecture of 345/230kV substation

6.4.1 Reliability and availability of a ring Ethernet switched network

Figure 6-6 represents the reliability block diagram of the ring Ethernet switch architecture. For the successful message transfer from a sender Ethernet switch to other (receiving) end Ethernet switch, any 1-out-of-2 remaining network Ethernet switches, plus any 3-out-of-4 fiber cable connections should be working properly, as shown in Figure 6-6. This n-1 redundancy is achieved with the implementation of RSTP into the managed Ethernet switches, which can reconfigure the ring network in case of any one switch and/or a communication cable connection failure.



Figure 6-6 Reliability block diagram of a ring Ethernet architecture

6.4.2 Ring process bus architecture with IRIG-B

The RBD of the ring process bus architecture synchronized using IRIG-B is illustrated in Figure 6-7. As mentioned in the previous section of this chapter, external time synchronization source would be connected to IEDs and MUs. Moreover, the sender end Ethernet switch will be connected in series as a part of communication devices for a specific protection.

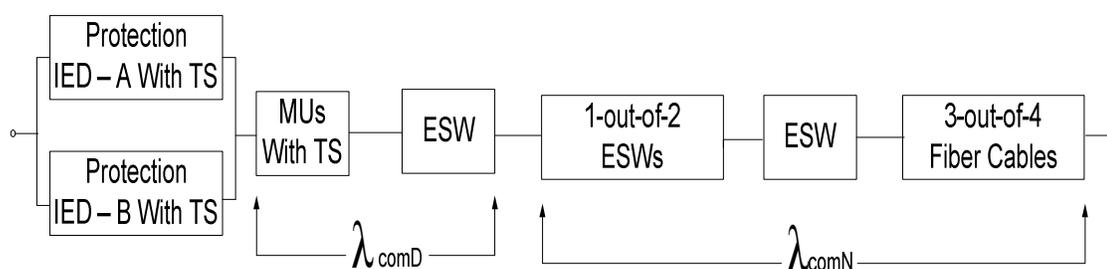


Figure 6-7 RBD for ring process bus architecture with IRIG-B

6.4.3 Ring process bus architecture with IEEE 1588

Figure 6-8 presents the RBD of ring process bus architecture with time synchronization over the network using IEEE 1588 protocol. In this configuration, time synchronization source, TS, should be connected in series with communication network instead of IEDs and MUs, as shown in the figure.

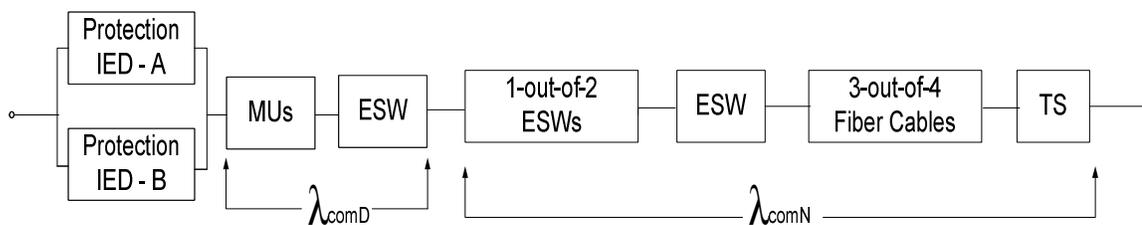


Figure 6-8 RBD for ring process bus architecture with IEEE 1588

6.4.4 Reliability and availability results for ring process bus architecture

Table 6-3 compares the reliability and availability results for the ring process bus architecture of various zones of protection considering external TS, and TS over the network. Comparison of Table 6-3 with the results of cascaded process bus architecture (from Table 6-2) shows that the overall reliability and availability of ring architecture is improved, as ring architecture provides n-1 redundancy for Ethernet switches and fiber cables. As explained earlier, the difference in reliability of various zones of protection is mainly due to the number of MUs required for a particular protection. Moreover, the IRIG-B based TS has lower reliability and availability than the IEEE 1588 based TS over a network.

Table 6-3 Reliability and availability results for ring process bus architecture

Zones of Protection	Ring Architecture			
	External TS (using IRIG-B)		TS over network (using IEEE 1588)	
	MTTF (years)	Availability	MTTF (years)	Availability
Line-1, 2, 3, 4	10.64	0.999780847	11.45	0.999799108
XFMR-1,2	9.93	0.999762586	10.64	0.999780847
Bus-1, 2	11.45	0.999799108	12.40	0.999817369

6.5 Analysis of Star-ring Process Bus Architecture

As shown in Figure 6-9, the star-ring architecture requires two additional redundant Ethernet switches connected in a ring. Both these Ethernet switches will be connected to the rest of the four Ethernet switches in a star configuration with redundant connections. This configuration requires two additional ESWs as compared to the previous process bus

architectures. On the other hand, only the main and redundant station ESWs (from Figure 6-9) should be management type Ethernet switches (i.e. supporting IEEE 802.1w RSTP).

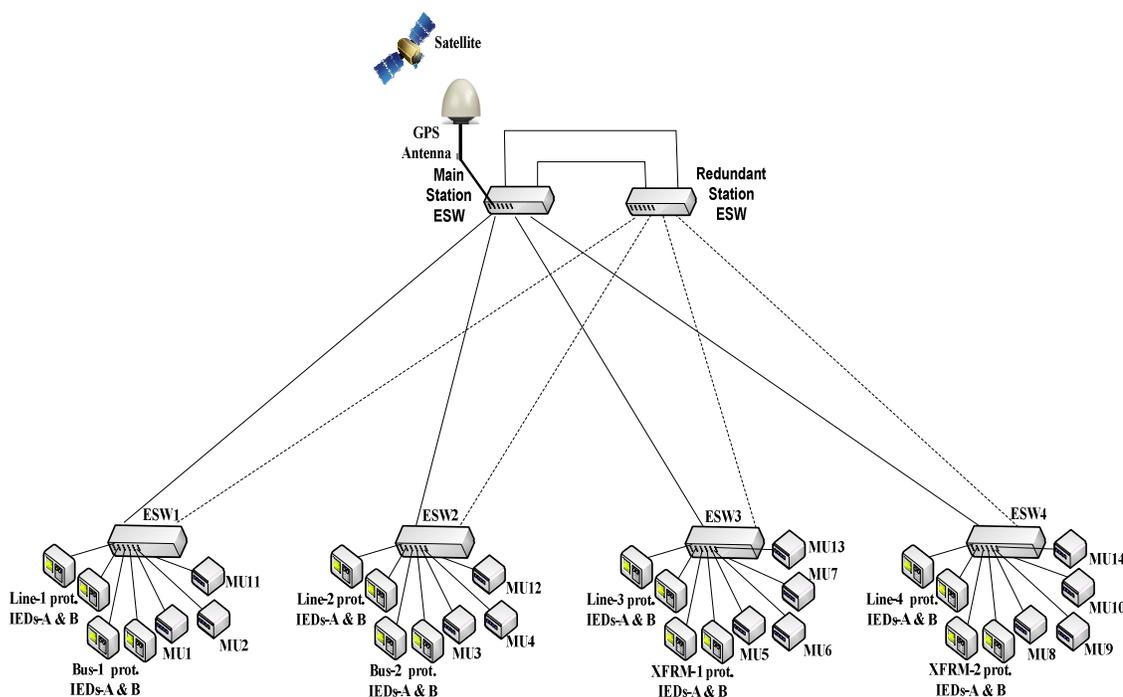


Figure 6-9 Star-ring process bus architecture of 345/230kV substation

6.5.1 Reliability and availability of a star-ring Ethernet switched network

The reliability block diagram of the star-ring Ethernet architecture is illustrated in Figure 6-10. Main and redundant ESWs are in parallel (as any one of these two ESWs should be working), plus the receiving end ESW should be in series. 1-out-of-2 fiber cables between main and redundant ESWs; and 2-out-of-4 fiber cables between protection ESWs should be working to facilitate the message transfer over the network.

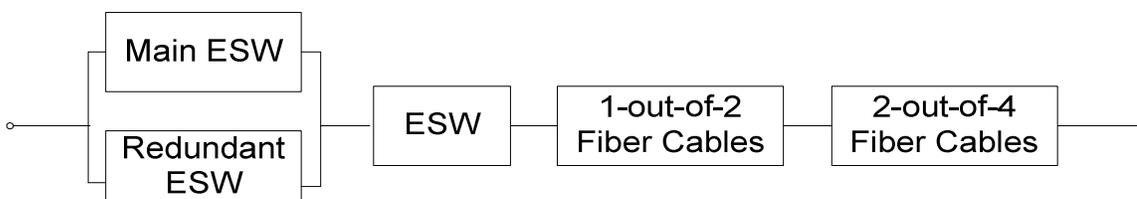


Figure 6-10 Reliability block diagram of a star-ring Ethernet architecture

6.5.2 Star-ring process bus architecture with IRIG-B

Figure 6-11 shows the reliability diagram for the star-ring architecture with the external time synchronization to IEDs and MUs using the IRIG-B. Devices pertaining to a specific protection, e.g. protection IED with TS, MUs with TS and Ethernet switch will be in series with blocks of communication network, as shown in the figure.

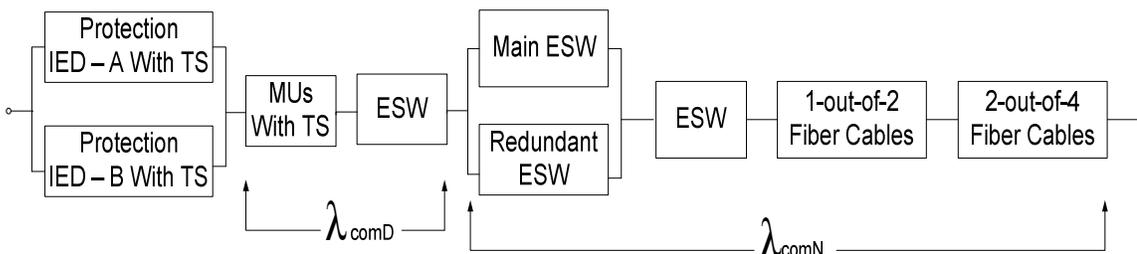


Figure 6-11 RBD for star-ring process bus architecture with IRIG-B

6.5.3 Star-ring process bus architecture with IEEE 1588

With IEEE 1588 based time synchronization technique, time synchronization source will be part of communication, instead of external connection to IEDs and MUs, as shown in Figure 6-12.

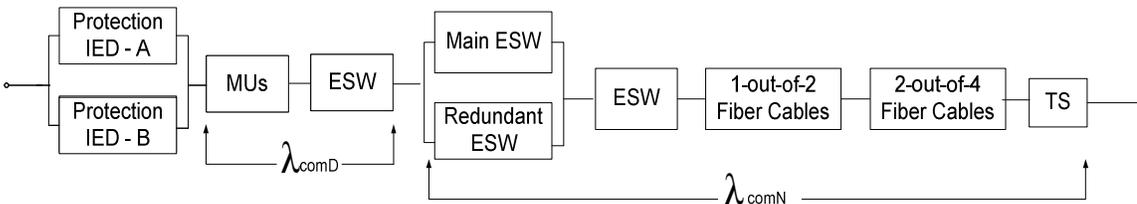


Figure 6-12 RBD for star-ring process bus architecture with IEEE 1588

6.5.4 Reliability and availability results for star-ring process bus architecture

Using the calculations of the series-parallel combinations from the Appendix-E, MTTF and availability of star-ring architecture are tabulated in Table 6-4. It can be observed from the results that star-ring architecture has not improved reliability and availability with respect to the previous ring architecture. This is due to the fact that the process bus has only four Ethernet switches. As the number of Ethernet switches increases the star-ring architecture reliability and availability will improve as compared to ring architecture.

Table 6-4 Reliability and availability results for star-ring process bus architecture

Zones of Protection	Star-Ring Architecture			
	External TS (using IRIG-B)		TS over network (using IEEE 1588)	
	MTTF (years)	Availability	MTTF (years)	Availability
Line-1, 2, 3, 4	10.63	0.999780847	11.44	0.999853891
XFMR-1,2	9.93	0.999762586	10.63	0.999835629
Bus-1, 2	11.44	0.999799108	12.38	0.999872153

6.6 Analysis of Redundant-Ring Process Bus Architecture

As shown in Figure 6-13, all the SAS IEDs are connected to both redundant ring configurations. Both the networks are independent with each other, and support IEEE 802.1w RSTP protocol.

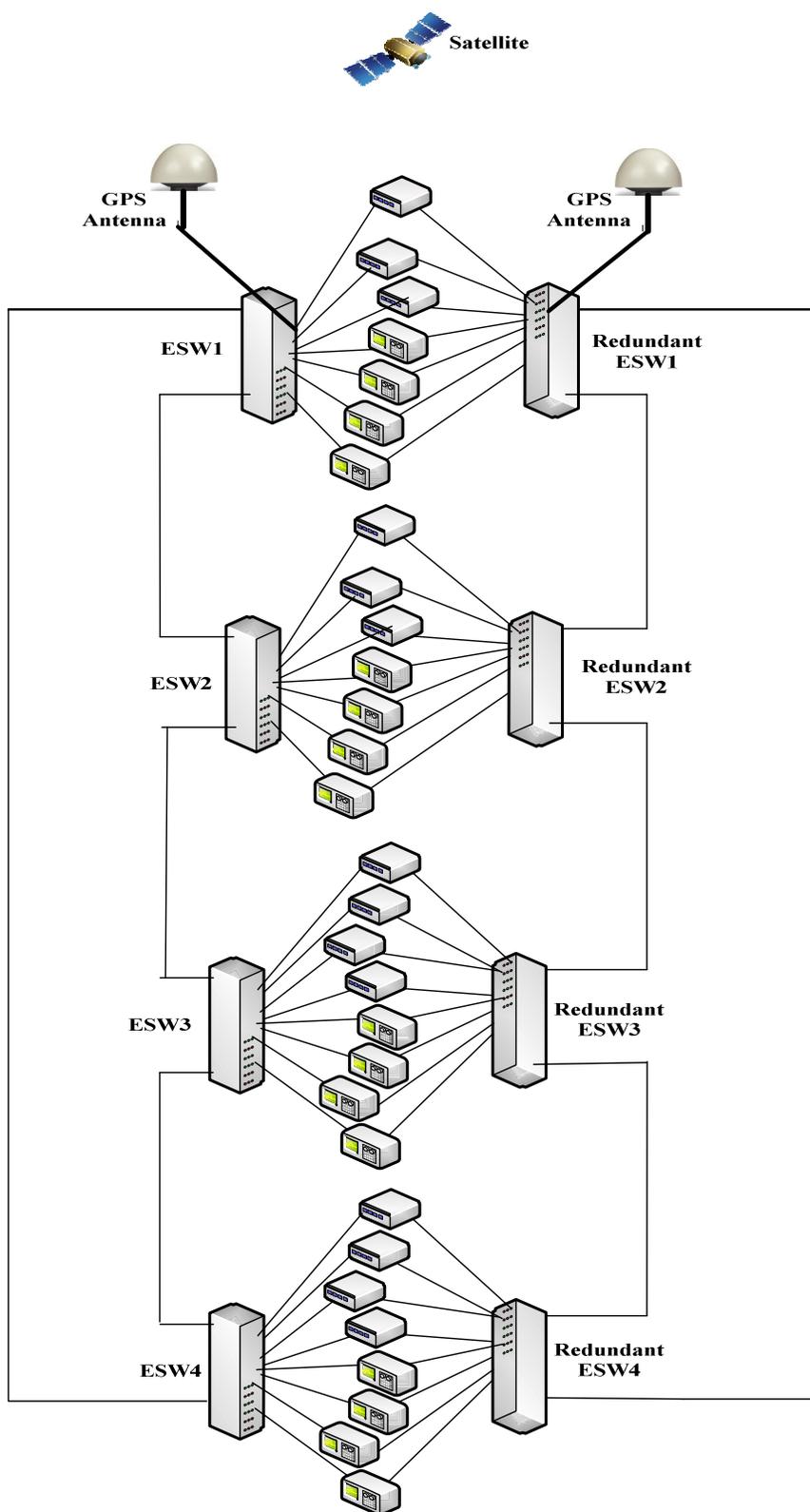


Figure 6-13 Redundant-ring process bus architecture of 345/230kV substation

6.6.1 Reliability and availability of a ring Ethernet switched network

Reliability block diagram for the redundant-ring architecture is shown in Figure 6-14. It can be observed from the figure that unlike the previous process bus architectures (i.e. cascaded, ring, star-ring), redundant ring provides redundancy at communication network level. As the figure shows, there are redundant ESWs at any receiving end, as well as over the network where 1-out-of-2 ESWs are required. Moreover, fiber cables with 3-out-of-4 combination would be in parallel too.

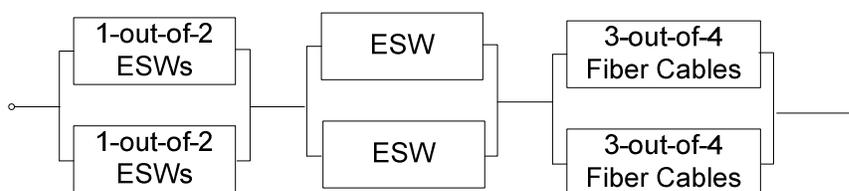


Figure 6-14 RBD of a redundant-ring Ethernet architecture

6.6.2 Redundant-ring process bus architecture with IRIG-B

There are redundant ESWs connected to each specific protection devices, as shown in RBD of redundant-ring process bus architecture with IRIG-B in Figure 6-15. Therefore, there will be a parallel Ethernet switches connected to IEDs and MUs, unlike the previous process bus architectures.

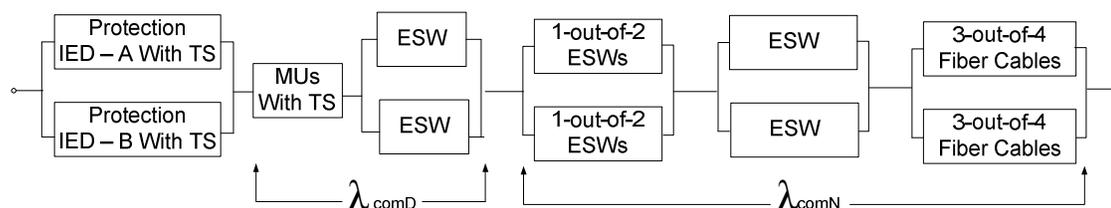


Figure 6-15 RBD for redundant-ring process bus architecture with IRIG-B

6.6.3 Redundant-ring process bus architecture with IEEE 1588

Figure 6-16 shows the RBD for the redundant ring process bus architecture in series with the redundant IEEE 1588 based time synchronization sources. It is important to note that since both rings are independent, each has its own time synchronization from the network. IEDs and MUs can switch to redundant network if it detects any failure in the main network.

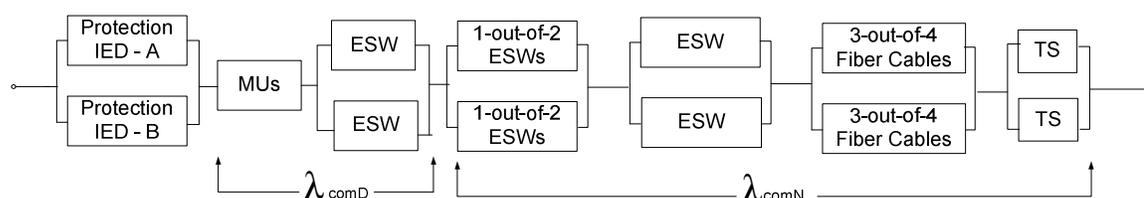


Figure 6-16 RBD for redundant-ring process bus architecture with IEEE 1588

6.6.4 Reliability and availability results for redundant-ring process bus architecture

Reliability (MTTF) and availability of redundant ring architecture are depicted in Table 6-5. Comparing the tabulated results of redundant-ring architecture with the previous architecture, certainly there are improvements in reliability and availability of zones of protection. This is due to the fact that redundant architecture offers complete redundancy in Ethernet switched network at a higher cost & complexity.

Table 6-5 Reliability and availability results for redundant-ring process bus architecture

Zones of Protection	Redundant-Ring Architecture			
	External TS (using IRIG-B)		TS over network (using IEEE 1588)	
	MTTF (years)	Availability	MTTF (years)	Availability
Line-1, 2, 3, 4	13.29	0.999835632	15.07	0.999853894
XFMR-1,2	12.21	0.999817371	13.69	0.999835632
Bus-1, 2	14.58	0.999853894	16.75	0.999872156

6.7 Summary

Four practical Ethernet architectures with different time synchronization techniques are discussed for the substation protection systems from the reliability point of view. With the help of reliability block diagram techniques, MTTFs and availability is calculated for a typical 345/230 kV transmission substation. Further, the reliability block diagrams are demonstrated for practical Ethernet switch architectures, such as cascading, ring, star-ring, and redundant ring. The comparison among these architectures is presented using MTTF, availability and additional component requirements. It is found that the separate network of external time synchronization based on the IRIG-B affects the MTTF and availability of the bay, as compared to the IEEE 1588 based time synchronization over the same communication network. Moreover, the reliability and availability of star-ring and redundant-ring are high as compared to cascaded and ring architecture. However, these architectures are costly and complex due to the fact that it requires additional Ethernet switches.

The comparison of MTTF for the external TS, and the TS over network is tabulated in Table 6-6. These failure rates from the table can be obtained for the further detailed analysis in Markov model, which is presented in the next chapter.

Table 6-6 MTTF comparison of process bus components

Components		ExtTS	TS over NW
MTTFied (a single protective IED)		75	150
MTTFcomD		30	37.5
MTTFcomN	Cascaded	15.15	13.76
	Ring	27.61	23.32
	Star-Ring	27.55	23.27
	Redun-Ring	41.42	34.98

Chapter 7

7. Extended Markov Model for Digital Protection Functions with Process Bus

Most of the literatures available on reliability analysis of the IEC 61850-9-2 process bus communication network are based on combinatorial reliability models, which include Reliability Block Diagram (RBD), fault tree, event tree, etc. This is because the combinatorial reliability models are simple and easy to understand. However, these combinatorial reliability models (i.e. RBD, fault tree, event tree) cannot be used to model system repairs or dynamic reconfiguration of the system. That means, in these modeling schemes, we are assuming that the system components are limited to operational or failed states, and the system configuration does not change during the system operation.

On the other hand, a Markov model can consider various system states (e.g. degraded, under test, temporary failure, reconfiguration, etc.), and the possible transitions among these states. A Markov model using a state transition diagram is more accurate than combinatorial reliability techniques, because it can represent more system states and components failure dependency. Therefore, the proposed reliability models in the literature for traditional protective relaying system are based on the Markov modeling [67]-[73]. Also various reliability indices of a protection system, e.g. abnormal unavailability, un-readiness, protection system unavailability, etc. are derived using the Markov model. However, there is no literature available to look at the impact of IEC 61850-9-2 based communication network on the protection function reliability.

Therefore, this chapter presents an extended Markov model of a protection system, considering the IEC 61850-9-2 based process bus communication architectures. The proposed Markov model includes the impact of communication devices (λ_{comD}) and time synchronization architectures for a protection. Also, the model recognizes the effect of

the proposed SV estimation algorithm by estimating lost/delayed SVs, and a network interface monitoring mechanism, the feature offered by digital process bus. Sensitivity analysis of the protection reliability indices are presented considering various parameters such as, failure and repair rates of a protection IED (λ_{ied} , μ_{ied}), failure rate and recovery time of communication networks (λ_{comN} , μ_{comN}), and SV lost/delayed (λ_{svl}).

7.1 Reliability of Protection Functions

The reliability of protective relaying is usually separated into two different aspects: 1) dependability; 2) Security [99]. Dependability is defined as the probability that a protection IED will operate correctly. In other words, dependability is a measure of the protection IED's ability to operate correctly when required. Whereas, security is defined as the probability that a protection IED will not operate in those situations when tripping is not desired. Therefore, if a protection IED mis-operates in any undesired conditions (e.g. external fault) it is referred to as lack of security of a protection function.

Considerable amount of work is available in the literature to analyze the reliability of protection functions using Markov model. Reference [62] introduced a method to calculate the failure probability of power system protection relays. C. Singh and A. D. Patton have introduced unreadiness probability for protection functions in [70]. This work is further extended in [67] to obtain unavailability of protection function by considering effect of back-up protection, inspection rate of protective relays, etc. Reference [69] modified the previously available models to accommodate self-testing capability of modern protective relays. This work is extended by R. Billinton et. al. in reference [71] in order to obtain optimum routine test and self-checking intervals considering monitoring and self-checking effectiveness, mal-operation of protection, etc. More complex Markov models proposed in [73] recognizes software failure, human errors, and ancillary equipment failures.

7.2 Considerations and Assumptions of Proposed Markov Model

Proposed model considerations and assumptions are listed below:

7.2.1 Considerations

Following items are considered in the extended Markov model:

- I. Failure rate of IEC 61850-9-2 based process bus communication network including Ethernet switches, fiber cables, merging units, and time synchronization source
- II. Recovery/ reconfiguration rate of Ethernet switched process bus network
- III. Time synchronization architectures
- IV. Sampled value loss due to degradation of communication network and/or devices
- V. Self-checking and monitoring features of digital protection IEDs
- VI. Enhancement in monitoring of protection IED due to network port monitoring feature.

7.2.2 Assumptions

The assumptions for simplifying the model are listed below:

- i. Failure rates and repair rates are constant, and all failures are mutually independent. This is a valid assumption, since all switching rates are exponentially distributed for the electronic devices [98].
- ii. Only a portion of the relay failure will be detected by routine test inspection which has not been detected by self-checking or monitoring facilities. And, during inspection, self checking or repair, the entire protective system will be taken out of service.
- iii. Potential mal-trip due to human or software errors, as well as failure of switchyard components CT, VTs, and Breakers, are not considered for the simplicity.

- iv. Only a portion of the relay failure can be detected by routine test that had not been revealed by monitoring or self-checking.
- v. Reconfiguration communication protocols, such as STP, RSTP, etc. are considered to be fully reliable.
- vi. Communication network delays are within the allowable range during normal operating condition. However, SV loss/delay over the process bus network is modeled in this work.
- vii. Common mode of (simultaneous) failure of protective IEDs and communication network/device is neglected for simplification.

7.3 Proposed Markov Model

A detailed Markov model to determine the reliability of protection functions based on IEC 61850-9-2 process bus is shown in Figure 7-1. The component in the figure represents any of the power system elements which need to be protected, such as transmission line, transformer, busbar, generator, etc. The letters C and P in the each state of the figure refer to the component to be protected and corresponding IEC61850-9-2 based protection system of the protected component, respectively. Protection system in this work includes protection IED, MUs and IEC 61850 based process bus communication network. All the states are numbered in the state transition diagram of Figure 7-1. Description of all transition rates used for the model is listed in the following subsection-7.3.1.

State-1 represents the normal operating condition where component is energized (C UP), and the corresponding protecting system is also operating properly (P UP). When a fault occurs in a component, the model transits to state-2 and component goes to down state (C DN). In this state, protection system is healthy, and hence, it detects the fault and operates normally to switch the circuit breaker. This normal switching isolates the faulty component and model transits to state-3. During the routine test of the protection system, the model transits to state-4, and the protection system is unready to respond if component goes down. Moreover, the protection IED has self-checking feature, in which the protection is inhibited. This phenomenon is represented by the transition from state-1

to state-5. If a failure is detected during the self-check, the system will transit to state-6; and if a failure is detected by the monitoring of the IED, model transfers from state-6 to state-8. If failure of IED is not detected by self-check or monitoring, then it will be detected by routine test for which system transit to state-7. If during unavailability of protection system, component fails, back-up protection will clear the fault by isolating additional portion X, i.e. total isolation of C+X components. This phenomenon is represented by transitions from all the states in protection down (component up) to state-9, and then, to state-10. After identifying isolation of an additional portion, a manual switching will restore portion X, and this way model will transit from state-10 to state-11. From the state-11, model can transit to either state-3 if the protection system is repaired or state-8 if the component is repaired before the protection system. The protection IED may mis-operate during external faults. This is represented by direct transition from state-1 to state-12. The protected component is isolated, and model is moved to state-13. Re-energizing the protected component may cause model to transit to state-8 from state-13, if protection system is not healthy, model return back to state-1. Also, the protection system moves to state-12 from state-4, due to mal-operation of protection system caused by human error occurring during the routine test inspection.

With implementation of IEC 61850-9-2, it is important to consider the process bus communication network, as well as communication devices, such as merging unit and time synchronization source as a part of the protection system. The failure of any communication device, i.e. one of the MUs or time synchronization source of the protection system, transits the model from state-1 to state-14. Whereas, the failure of the communication network (process bus Ethernet network switches connected with fiber cables), causes model to move from state-1 to state-15. The failure of a communication device (followed by communication network) transits model from state-15 to state-14. Earlier in this work, two important studies are presented: 1) the loss/delay of multiple sampled values due to degradation of communication network and/or components is studied with the help of detailed dynamic simulations in OPNET tool; 2) the impact on protection functions during sampled value loss/delay is demonstrated using hardware set-up. In case of sampled value loss/delay (due the degradation of communication network and/or devices), the model transit to state-16 from the normal operating state-1. The

model may enter to state-12, if the sampled value loss causes any mis-operation during an external fault, else model return back to state-1.

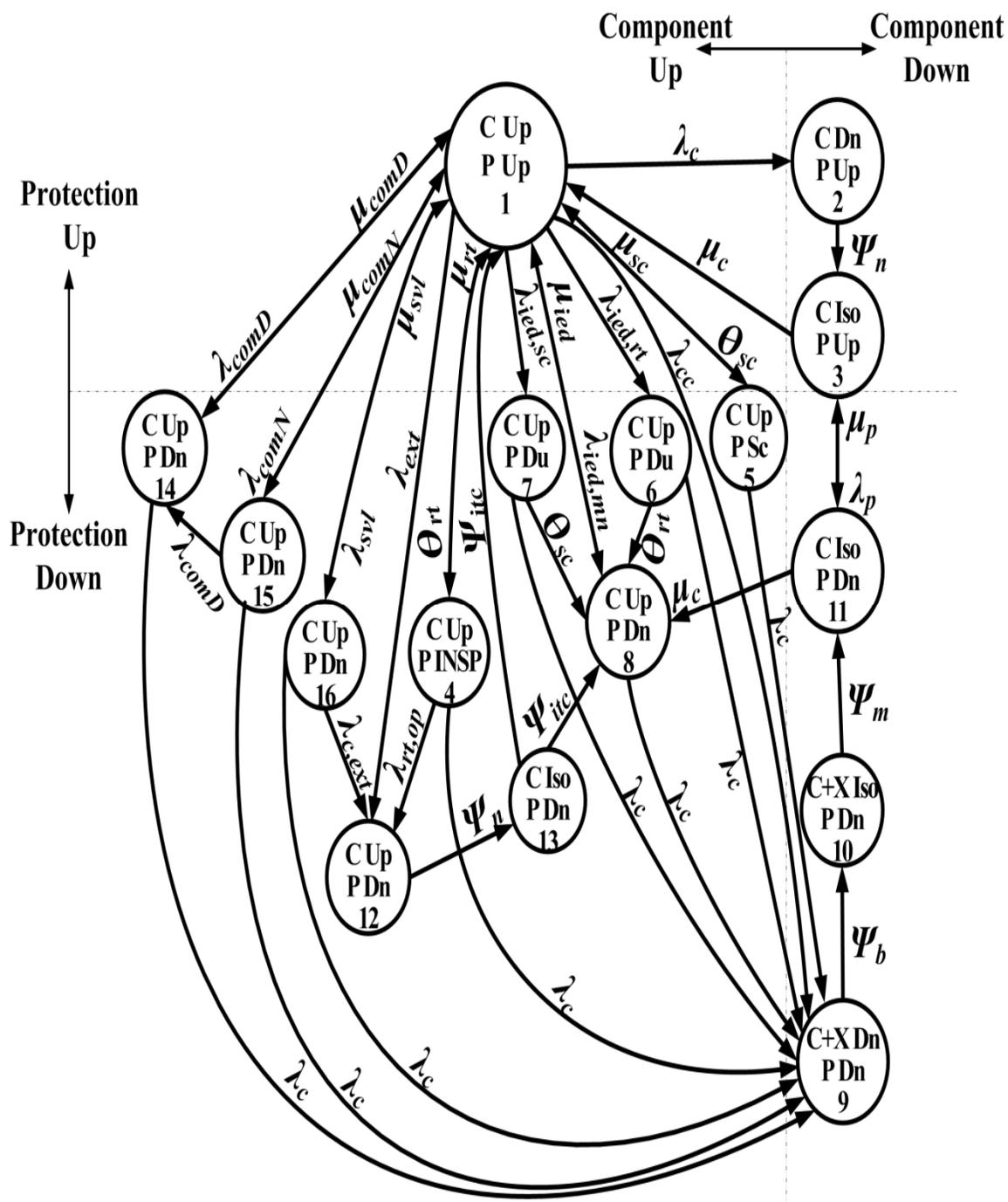


Figure 7-1 Markov model for protective relaying based on process bus

7.3.1 Description of proposed Markov model transition rates

λ_c	failure rate of the protected component (C)
μ_c	repair rate of the protected component
λ_p	failure rate of the protective system (P)
μ_p	repair rate of the protective system
λ_{cc}	common cause of failure rate of C and P
Ψ_n	normal switching rate of the protective system
Ψ_b	back-up protective system switching
Ψ_m	manual switching rate to isolate only faulty component
Ψ_{ic}	manual switching rate to restore component C
Θ_{rt}	routine inspection rate of the protective system
μ_{rt}	number of IEDs inspected per time period
λ_{ied}	failure rate of the protective system (P)
μ_{ied}	repair rate of the protective system
$\Theta_{ied,sc}$	self-checking rate of protection IED
$\mu_{ied,sc}$	number of IEDs self-checked per time period
$\lambda_{ied,sc}$	portion of IED failure rate detected by self-checking
$\lambda_{ied,mn}$	portion of IED failure rate detected by monitoring
$\lambda_{ied,rt}$	portion of IED failure rate detected only by routine inspection
λ_{comN}	failure rate of communication required for P
μ_{comN}	repair or reconfiguration rate of communication required for P
λ_{comD}	failure rate of communication device required for P
μ_{comD}	repair rate of communication device required for P
λ_{svl}	rate of SV loss/delay over the process bus
μ_{svl}	recovery rate of protection IED from the effect of SV loss/delay
$\lambda_{rt,op}$	rate of relay mal-operation revealed during routine test
$\lambda_{c,ext}$	rate of external (other adjacent components in a substation) faults

7.3.2 Reliability indices for substation protection systems

Based on the proposed Markov model of Figure 7-1, the individual state probabilities (P_i) can be obtained, as explained in Appendix E. An improved Markov model in [67], [68] defined the reliability indices for the protection systems, such as, unavailability of a protection system ($ProtUn$), and abnormal unavailability ($AbUn$). This work is extended by R. Billinton, et. al. in [71] and introduced a reliability indice for the loss of security ($Lsecu$) in protective relaying. This work considers all these three reliability indices: 1) Protection system ($ProtUn$), 2) Abnormal unavailability ($AbUn$), and 3) Loss of security ($LSecu$). These three parameters can be obtained from individual state probabilities obtain from the proposed model as follows:

Protection system (ProtUn): Probability that the component to be protected (C) is up, but protection system (P) is down. Therefore,

$$ProtUn = P_4 + P_5 + P_6 + P_7 + P_8 + P_{14} + P_{15} + P_{16}$$

Abnormal unavailability (AbUn): Probability that the component to be protected (C) as well as protection system (P) both are down.

$$AbUn = P_9 + P_{10} + P_{11}$$

Loss of security (LSecu): Probability that the component to be protected is up, but protection function has operated incorrectly.

$$LSecu = P_{12} + P_{13}$$

These reliability indices are studied in the following subsection.

7.4 Results and Discussion

The values of Markov state model transition rates, and the analysis based on these values are discussed in this subsection.

7.4.1 Values of transition rate

The common transition rates obtained from [67], [71] are listed below:

$$\lambda_c = 1 \text{ fault/year}$$

$$\lambda_{cc} = 1 \text{ failure/million hour}$$

$$\mu_c = 0.5 \text{ repair/hour}$$

$$\Psi_n = 43200 \text{ operations/hour (5 cycle)}$$

$$\Psi_b = 21600 \text{ operations/hour (10 cycle)}$$

$$\Psi_m = 0.5 \text{ operations/hour}$$

$$\Theta_{ied,sc} = 1 \text{ test/ 48 hour}$$

$$\mu_{ied,sc} = 720 \text{ test/hour (5sec/test)}$$

$$\mu_{rt} = 1 \text{ test/hour}$$

$$\mu_p = 1 \text{ repair/hour}$$

$$\lambda_p = 1 \text{ failure/100 years (only for traditional protection systems)}$$

Transition rates for protection system, repair rate of 61850-9-2 process bus based IED, MU, and ESW are obtained from [7]. Their values are as follows:

$\mu_{ied} = 1 \text{ repair/1 hour}$

$\mu_{comD} = 1 \text{ repair/24 hour}$

Failure rates of protection IED, communication devices (TS, MU, and ESW), and communication network are obtained from reliability block diagram method (as explained in Chapter 6), and are listed in Table 7-1.

Table 7-1 Transition rates of various process bus architectures

Failure rates		ExtTS (using IRIG-B)	TS over NW (using IEEE 1588)
λ_{ied}		0.01333 failure/year	0.006667 failure/year
λ_{comD}		0.0333 failure/year	0.026667 failure/year
λ_{comN}	Cascaded	0.066 failure/year	0.07267 failure/year
	Ring	0.0362 failure/year	0.04288 failure/year
	Star-Ring	0.0363 failure/year	0.043 failure/year
	Redundant- Ring	0.02414 failure/year	0.02859 failure/year

The impact of various parameters (belongs to process bus communication network) on substation protection (reliability indices) is presented below. Ring architecture with TS over process bus network is considered for the following analysis, until it is specified.

7.4.2 Impact of process bus communication on protection reliability

Figure 7-2 to Figure 7-4 show the impact of process bus communication network on the reliability indices of protection systems, such as, protection unavailability, abnormal unavailability, and loss of security, respectively. It can be observed from Figure 7-2 that the protection unavailability increases from 0.00118 to 0.001378, due to the addition of communication devices and process bus communication network. On the other hand, the optimum routine test interval increases from 2101 hours to 6501 hours with the help of process bus communication. This is due to the fact that a process bus base protection system has higher monitoring effectiveness as compared to traditional protection system. The abnormal unavailability (Figure 7-3) and loss of protection security (Figure 7-4) increase by a small value due to the communication devices and network.

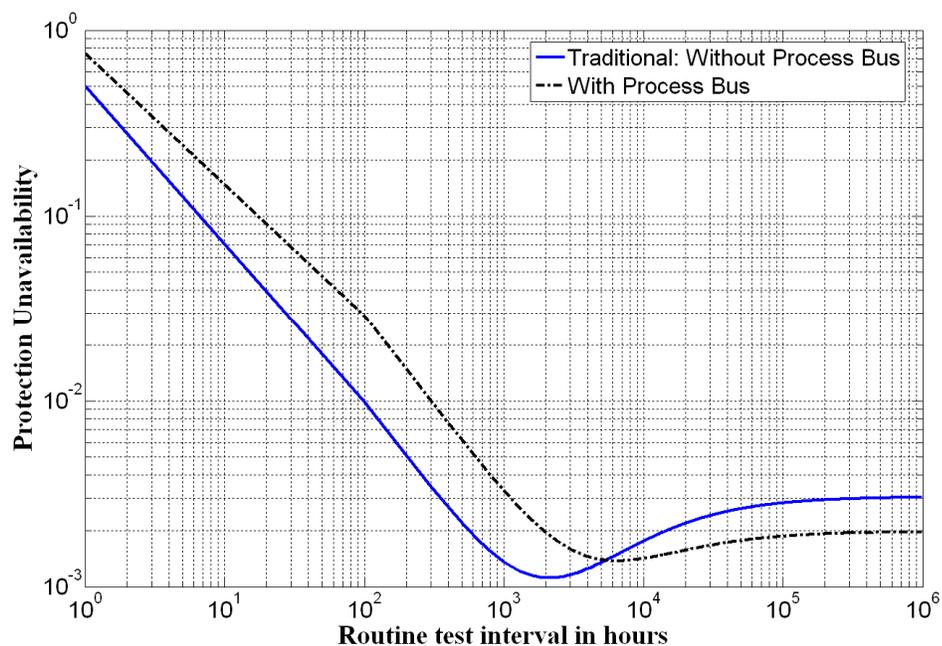


Figure 7-2 Impact of process bus communication on protection unavailability (ProtUn)

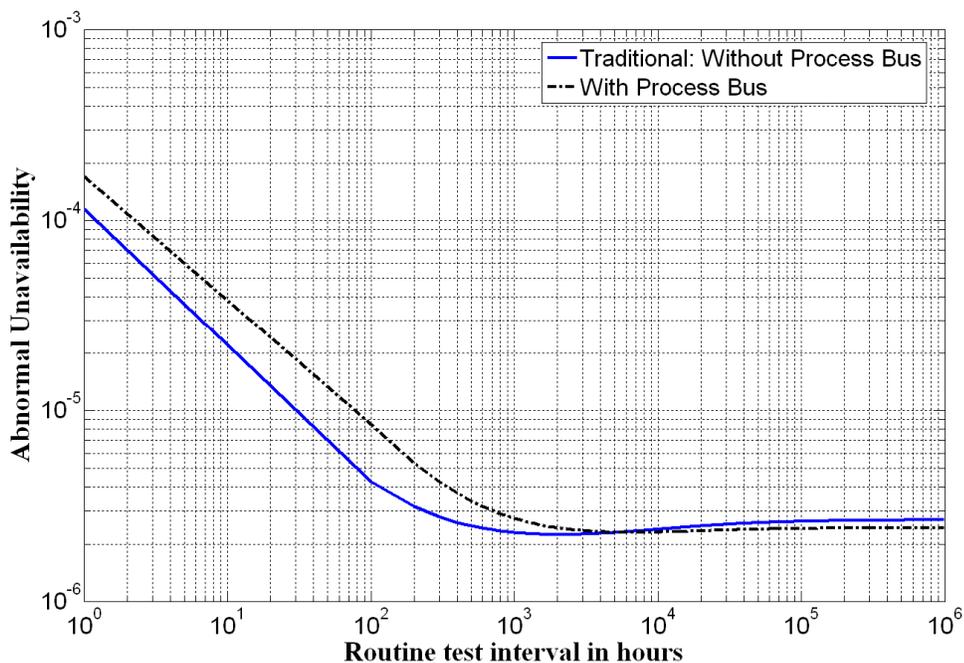


Figure 7-3 Impact of process bus communication on abnormal unavailability (AbUn)

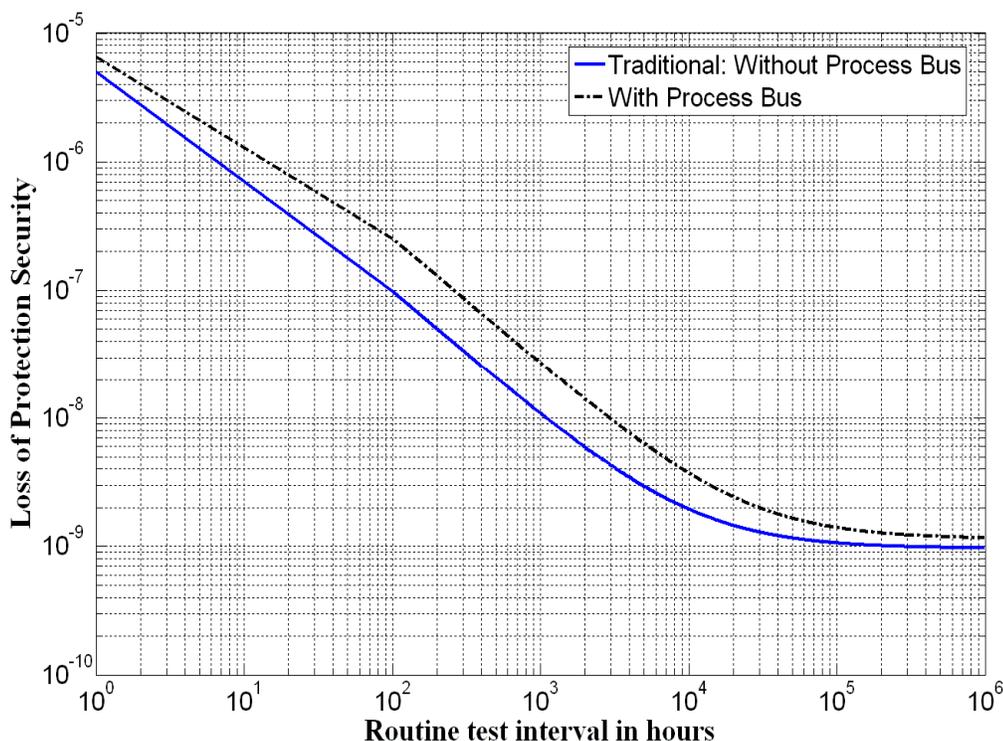


Figure 7-4 Impact of process bus communication on loss of protection security (LSecu)

7.4.3 Impact of process bus time synchronization techniques on protection reliability

As described in the previous chapter, there are mainly two time synchronization techniques appropriate for protection applications: 1) External TS based on IRIG-B; 2) TS over the network using IEEE 1588 capabilities. For both of these time synchronization techniques, the failure rates of protection system components including process bus devices considered for the analysis are tabulated in Table 7-1. Figure 7-5 presents protection unavailability with the IRIG-B and the IEEE 1588 architectures. With the IRIG-B based TS technique, $ProtUn$ is 2.079×10^{-3} with routine test interval of 3900 hours; whereas, for IEEE 1588 base TS technique, $ProtUn$ is 1.378×10^{-3} with routine test interval of 6501 hours. The protection unavailability increases with lower routine test interval for IRIG-B based TS due to the fact that the external TS based on the IRIG-B has higher number of TS components, as compare to the IEEE 1588 based TS technique.

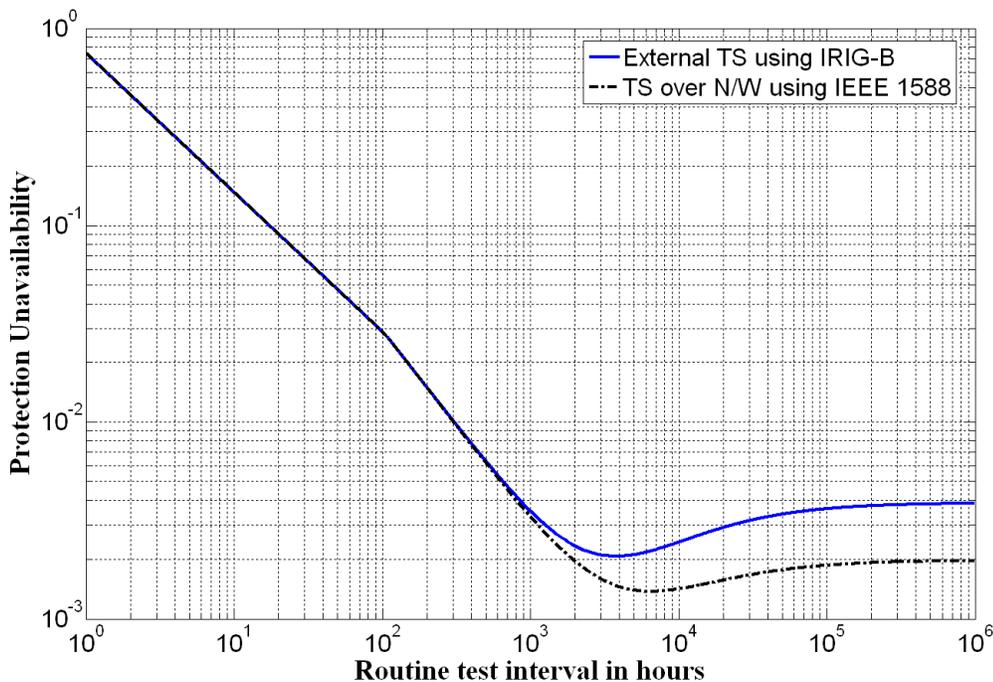


Figure 7-5 Impact of process bus time synchronization techniques on protection unavailability (ProtUn)

Comparison of abnormal unavailability of different TS techniques is shown in Figure 7-6. Abnormal unavailability of external TS using IRIG-B increases from 2.31×10^{-6} to 2.468×10^{-6} . Figure 7-7 shows that TS techniques do not have significant impact on protection security. This is because TS technique does not cause any mis-operation to the protection system.

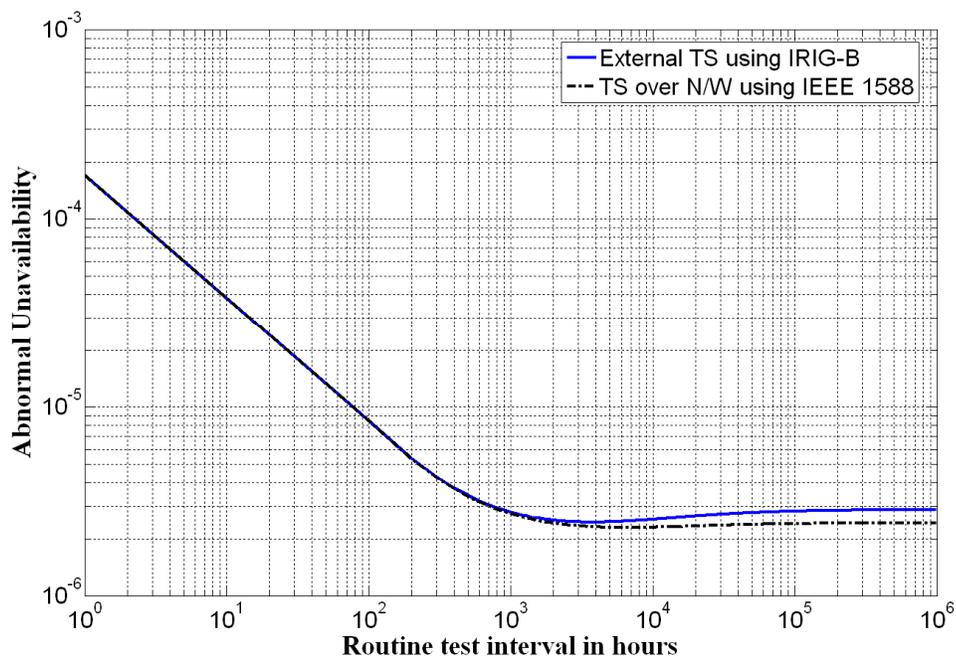


Figure 7-6 Impact of process bus time synchronization techniques on abnormal unavailability (AbUn)

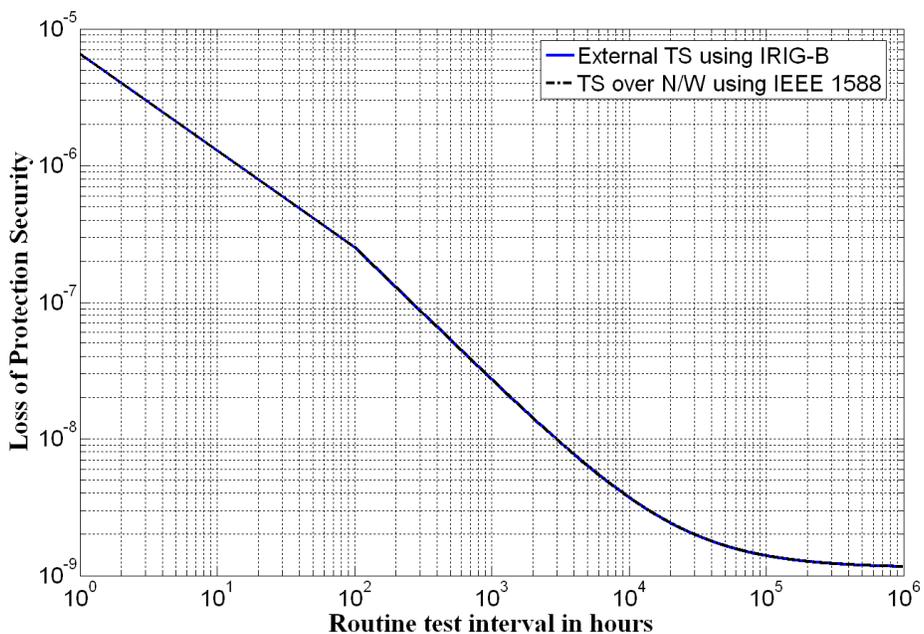


Figure 7-7 Impact of process bus time synchronization techniques on loss of protection security (LSecu)

7.4.4 Impact of sampled value loss/delay over the process bus on protection reliability

As it is explained in the proposed Markov model, loss or delay of multiple sampled values may cause the protection system to mis-operate during an external fault condition. During normal operation, multiple SVs are lost or delayed only during worst case scenario of the traffic, which is assumed to be occurring once in a day. However, in degraded network, i.e. either an Ethernet switch or a fiber link has failed, the event of multiple SVs loss or delay may assumed to be occurred every second. In all cases, the protection functions recover from the impact of multiple SV loss or delay in 16.667 msec (one power cycle for 60Hz system). During this one cycle, protection may mis-operate during external faults.

It can be inferred from Figure 7-8 and Figure 7-9 that the phenomena of sampled value loss and delay has less impact on ProtUn and AbUn, as SV loss or delay fast recovery rate (within one power system cycle). On the other hand, loss or delay of multiple sampled values has significant impact on protection system security. It can be observed from the

Figure 7-10 that loss of security (*LSecu*) probability increases to 2.62×10^{-8} from 5.1×10^{-9} .

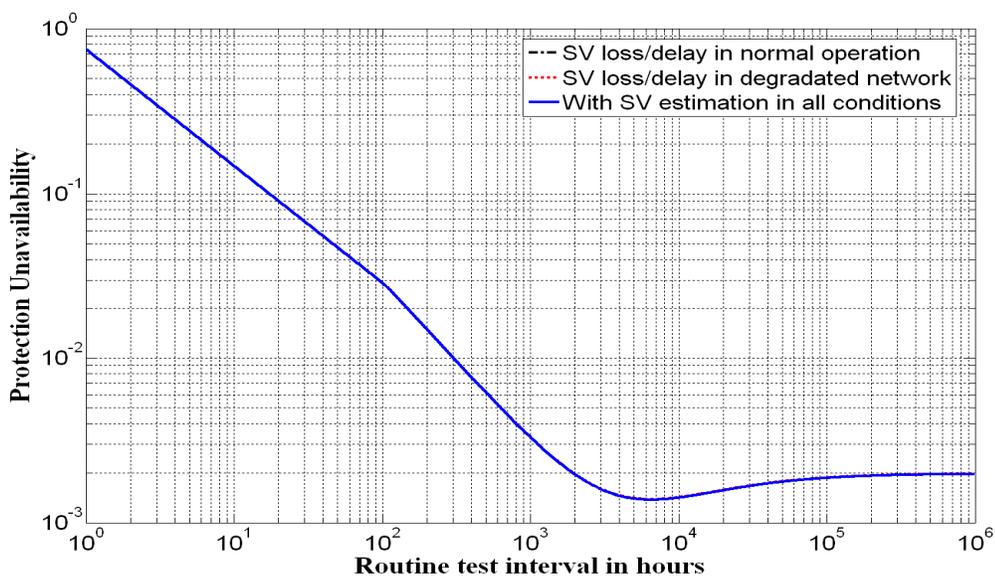


Figure 7-8 Impact of sampled value loss/delay on protection unavailability (ProtUn)

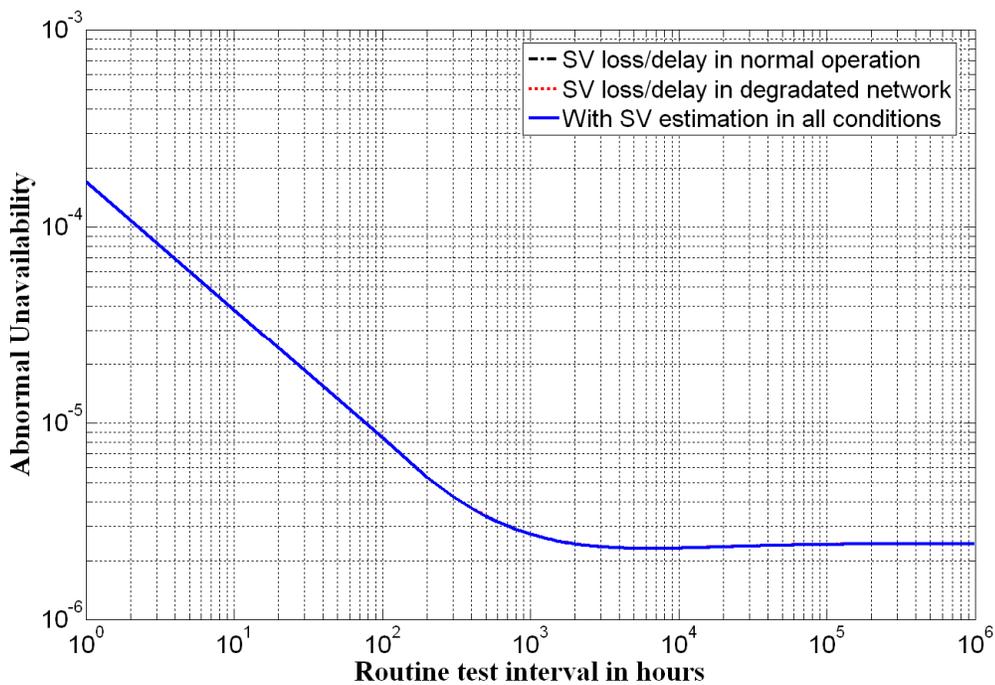


Figure 7-9 Impact of sampled value loss/delay on abnormal unavailability (AbUn)

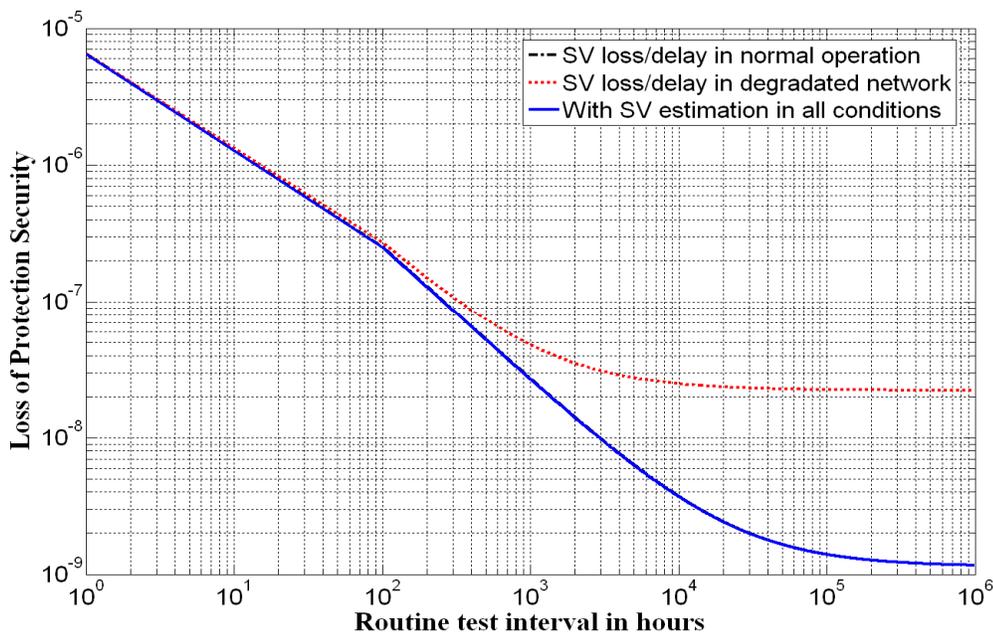


Figure 7-10 Impact of sampled value loss/delay on loss of protection security (LSecu)

7.4.5 Sensitivity to process bus architecture reconfiguration

This subsection presents the sensitivity analysis of the protection system based on process bus architecture reconfiguration rate (μ_{comN}). With cascade Ethernet switched architecture, reconfiguration of the network is not automatic. Therefore, process bus network need to be repaired manually. Therefore, the value of μ_{comN} is considered to be same as repair or replacement rate of an Ethernet switch, which is 24 hours. On the other hand, ring based architectures, e.g. ring, star-ring, etc. has reconfiguration time of 100 msec. It can be inferred from the Figure 7-11 that protection unavailability increases from 0.001385 to 0.001576 while taking more time to reconfigure the process bus. It can also be observed from the figure that process bus architecture reconfiguration does not have any impact on optimum routine test interval, as it is same (6501 hours) in both the scenarios.

Figure 7-12 shows that process bus architecture reconfiguration has modest impact on abnormal unavailability, as the value increases from 2.36×10^{-6} (for cascaded architecture) to 2.31×10^{-6} (for ring based architecture).

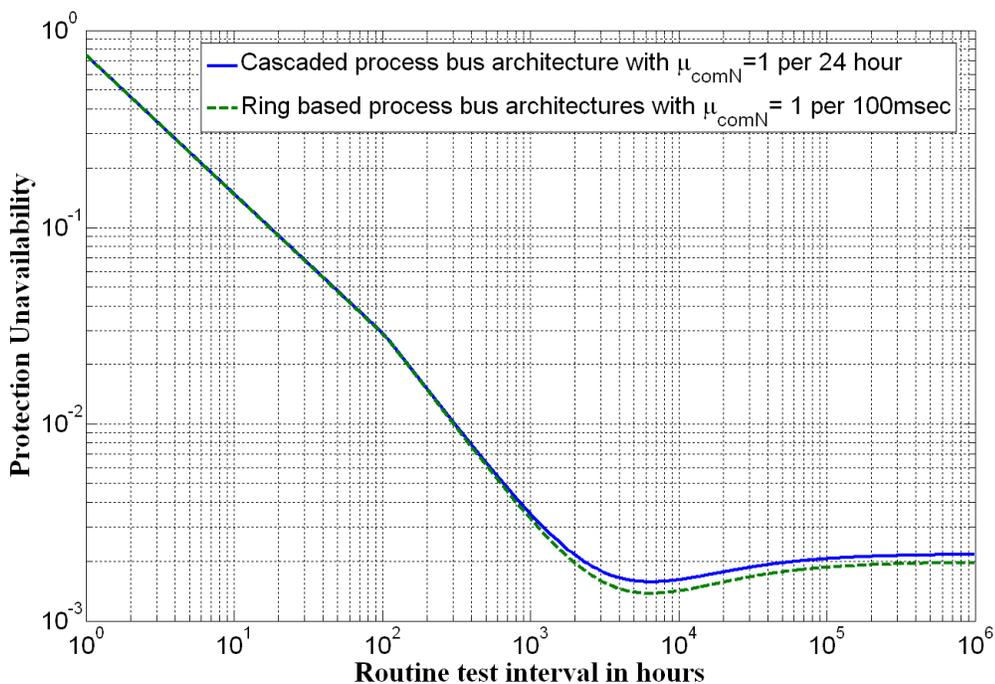


Figure 7-11 Sensitivity of protection unavailability (ProtUn) to process bus architecture reconfiguration

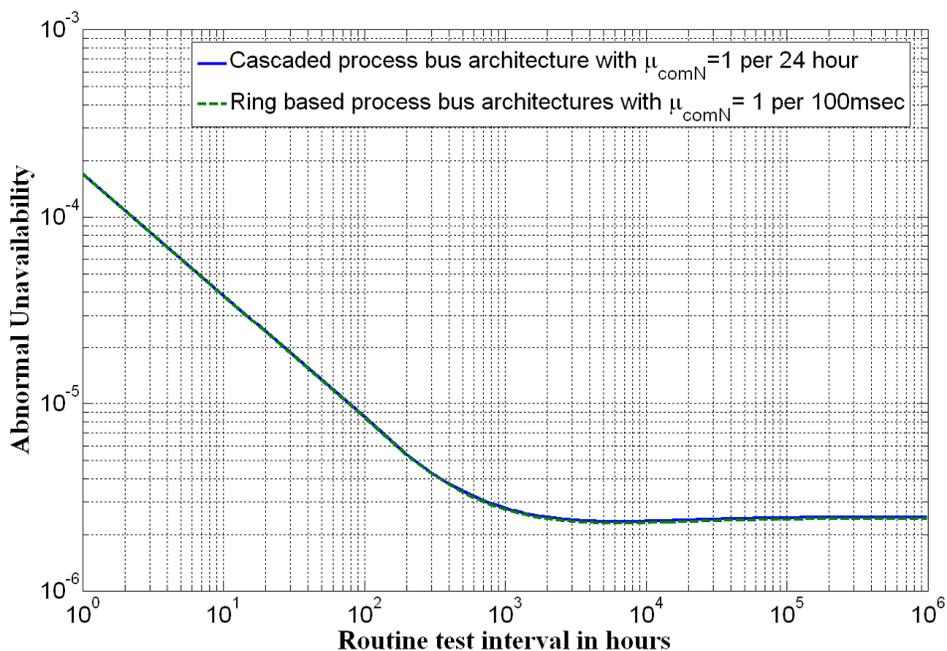


Figure 7-12 Sensitivity of abnormal unavailability (AbUn) to process bus architecture reconfiguration

Figure 7-13 shows that there is negligible impact of process bus architecture reconfiguration on protection system security, as the reconfiguration doesn't cause mis-

operation.

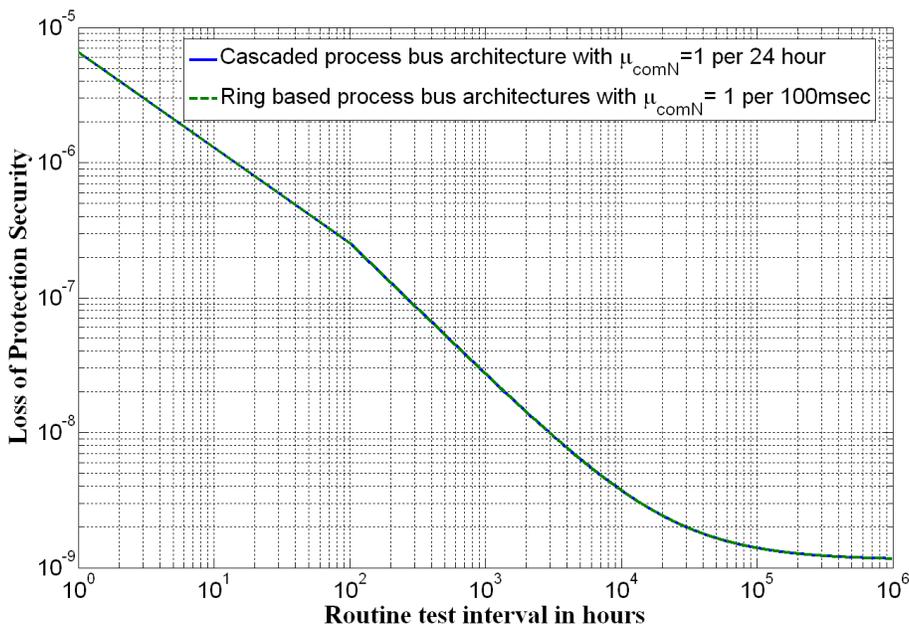


Figure 7-13 Sensitivity of loss of protection security (LSecu) to process bus architecture reconfiguration

7.4.6 Sensitivity to process bus monitoring effectiveness (MNE)

The protection devices with fiber connections over the process bus communication network may have higher MoNitoring Effectiveness, (MNE) as compare to the traditional copper connections. This is because a communication port can continuously monitor the process bus network connection, as well as, it can alarm any failure in the communication link. Normally, the effectiveness of protective relay self-monitoring is 10%; however, it may increase with the process bus communication network based protection. Therefore, sensitivity of the protection system reliability indices are studied for various MNE values. It can be observed from Figure 7-14 that the values of protection unavailability are 0.001434, 0.001132, and 0.0007327 for the MNE of 10%, 20%, and 30%, respectively. At the same time, abnormal unavailability improves from 2.323×10^{-6} to 2.25×10^{-6} and 2.16×10^{-6} , as shown in Figure 7-15. Moreover, Figure 7-16 shows that the enhancement in monitoring does not have any effect on the security of the protection system.

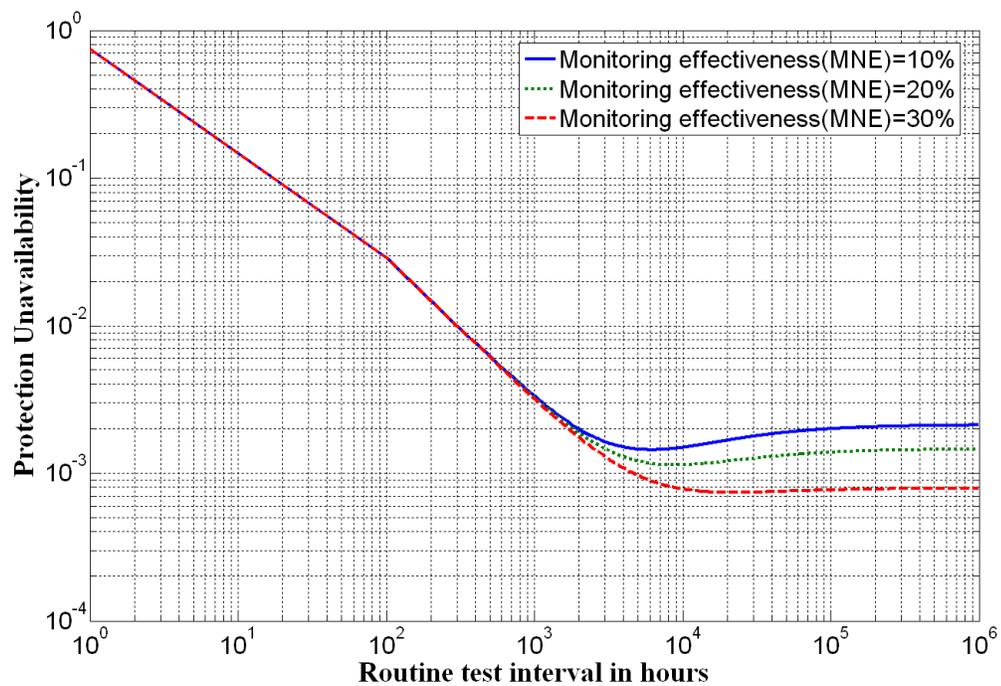


Figure 7-14 Sensitivity of protection unavailability (ProtUn) to process bus monitoring effectiveness

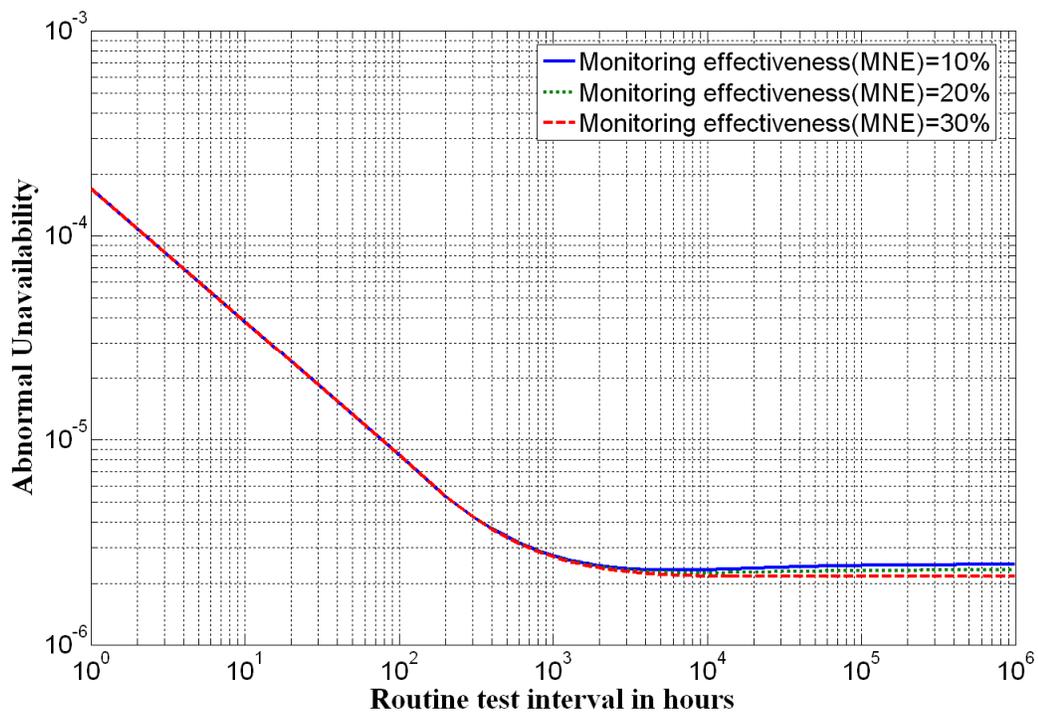


Figure 7-15 Sensitivity of abnormal unavailability (AbUn) to process bus monitoring effectiveness

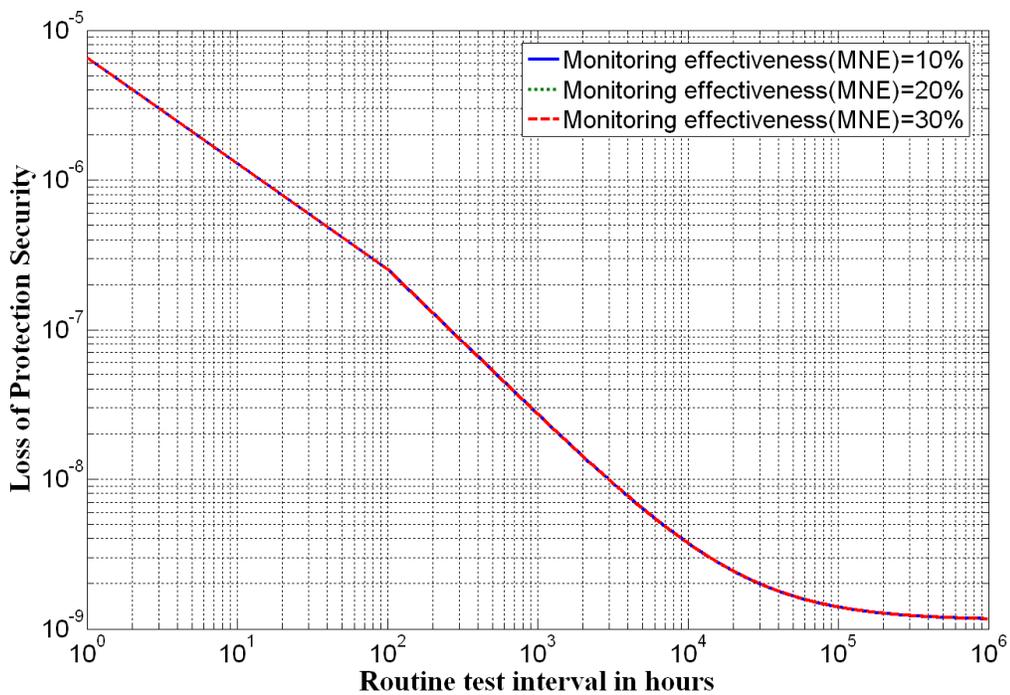


Figure 7-16 Sensitivity of loss of protection security (LSecu) to process bus monitoring effectiveness

7.4.7 Sensitivity to failure rate of protection IED

In order to study the sensitivity of the reliability indices of the protection system, three different failure rates of protection IED are considered, 1/100 year, 1/150 year, and 1/200 year. Figure 7-17 shows the protection system unavailability are 0.001748 at 4700 hour of routine test interval, 0.001378 at 6501 hour of routine test interval, and 0.0016 at 8000 hour of routine interval for the λ_{ied} of 1/100 year, 1/150 year, and 1/200 year respectively. This shows that *ProtUn* increases with decreasing λ_{ied} at the same time routine test interval decreases, which is consistent with the traditional protection system Markov models available in the literature [67], [69]. In addition to that, *AbUn* decreases with the rise in the failure rate of protection IED, as illustrated in Figure 7-18. The values of *AbUn* are 2.394×10^{-6} , 2.31×10^{-6} , 2.261×10^{-6} , for the λ_{ied} of 1/100 year, 1/150 year, and 1/200 year, respectively. Figure 7-19 shows that the failure rate of protection IED has negligible impact on the protection system security.

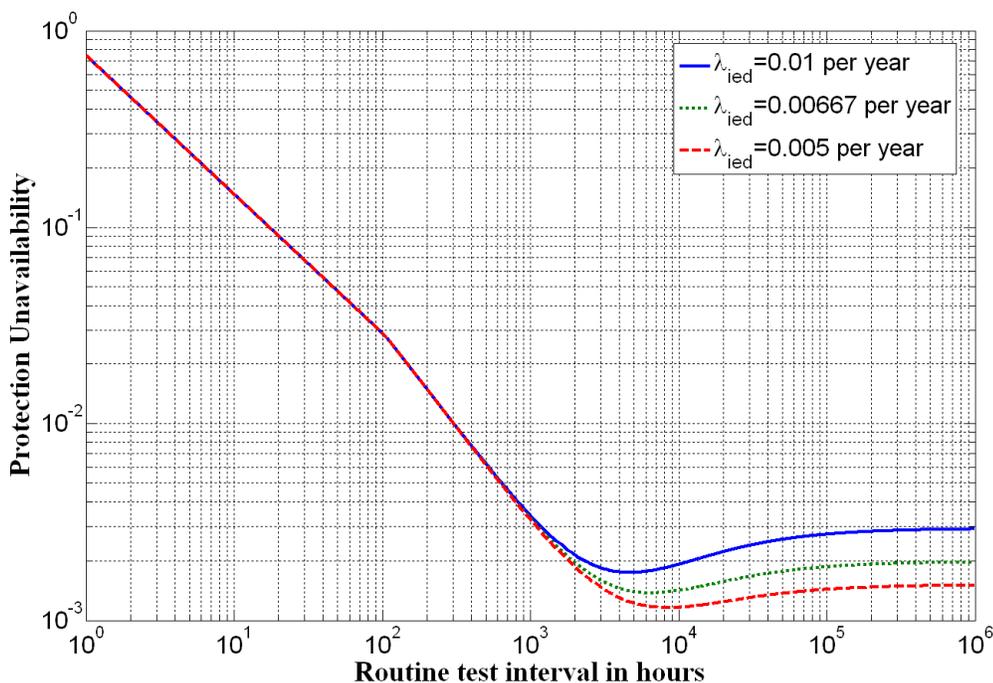


Figure 7-17 Sensitivity of protection unavailability (*ProtUn*) to failure rate of protection IED

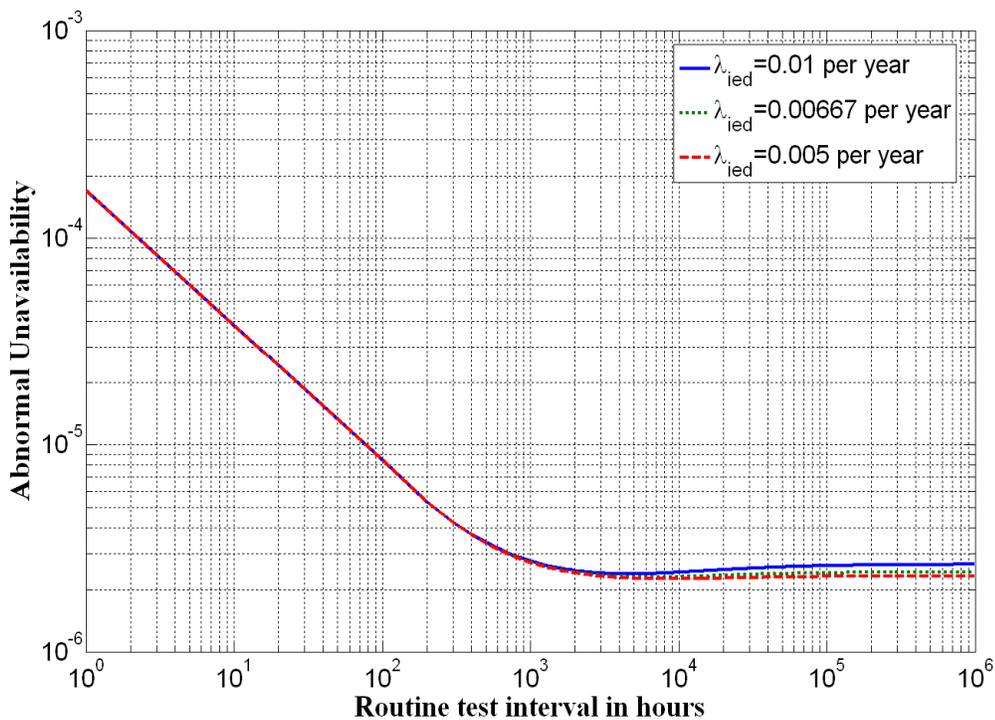


Figure 7-18 Sensitivity of abnormal unavailability (AbUn) to failure rate of protection IED

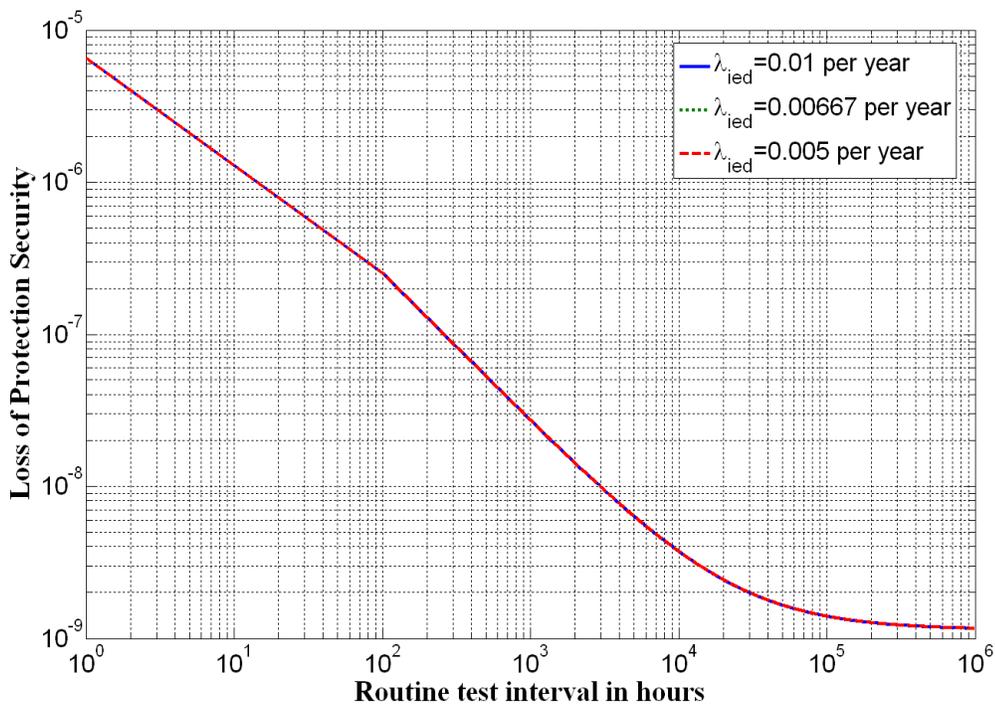


Figure 7-19 Sensitivity of loss of protection security (LSecu) to failure rate of protection IED

7.5 Summary

The extended Markov model is proposed in this chapter by considering the IEC 61850-9-2 based process bus communication networks, as a part of digital substation protection systems. The proposed Markov model recognizes the impact of communication devices (λ_{comD}) and the time synchronization techniques on protection. Also, it includes the effect of network interface monitoring mechanism, recovery time of communication networks (λ_{comN} , μ_{comN}), and the estimation lost/delayed SVs (λ_{svl}) over the network.

Reliability indices of protection systems from literature, such as protection unavailability (ProtUn), abnormal unavailability (AbUn), and loss of protection security (LSecu), are analyzed in this work. It is presented that these reliability indices are slightly affected due to the addition of process bus communication components, as a part of protection systems. However, routine test interval is improved from 2101 hours to 6501 hours, due to higher monitoring effectiveness of communication devices. Moreover, it is studied from the analysis that ProtUn and AbUn are affected more with external time synchronization technique (IRIG-B), as compared to time synchronization over the network (IEEE 1588). On the other hand, SV loss/delay has significant detrimental effect on protection security (LSecu), and has minor impact on ProtUn and AbUn. This is because the SV loss/delay may cause mis-operation of a protection function, (as demonstrated in Chapter 5 using hardware set-up). With the proposed SV estimation algorithm, the effect of SV loss/delay on protection function reliability indices can be alleviated. Furthermore, the sensitivity analysis shows that the ProtUn and AbUn indices are more sensitive to process bus architecture reconfiguration rate, process bus monitoring effectiveness, and failure rate of protection IED, however, LSecu is comparatively very less sensitive to these process bus transition rates.

Chapter 8

8. Research Outcomes and Conclusions

This research work focuses on addressing the major technical challenges related to IEC 61850-9-2 process bus for substation protection systems. The detailed performance and reliability analysis of substation protection functions, in presence of next generation process bus communication network are presented. The specific research outcomes, as well as summary and conclusion of the research work are discussed in this chapter.

8.1 Research Outcomes

Unique contributions of this research to the area of power system protection are as follows:

1. **A platform for the detailed dynamic analysis of IEC 61850-9-2 process bus network** applying to substation protection systems is provided using OPNET. The developed work can recognize various constraints of the practical Ethernet networks, e.g. bit error rate on the communication channel; bit error correction mechanism at communication ports, Ethernet switch packet buffer and service rate, different priority queuing mechanism for time critical messages; IEC 61850 based message traffic flows; and VLAN configuration. This work will provide the perfect platform/tool to analyze the dynamic performance of any typical substation process bus network considering effect of various communication parameters, and also help to design process bus networks during the planning stages of substation automation projects.
2. **Sampled value estimation algorithm** is proposed in this work, which can be implemented with any traditional well-established digital protection algorithm. This estimation technique is generic and can increase order of estimation for

achieving higher levels of accuracies. This algorithm is also tested as a part of protection IEDs over the hardware setup.

3. **IEC 61850-9-2 compliant process bus laboratory**, including: 1) substation protection IEDs; 2) merging unit real time playback simulator; 3) IEEE 1588 based time synchronization; 4) Ethernet switched network with implemented VLAN, RSTP, priority queuing, etc. mechanisms according to IEC 61850-9-2; 5) IEC 61850 based network traffic generator; 6) open source network analyzer suitable for IEC 61850 standard message types, etc. is developed. Using these developed laboratory facilities, the implementation of the proposed SV estimation algorithm is demonstrated as a part of busbar biased differential and line distance protection IEDs. This way, the testing of any developed algorithm can be carried out for various power system fault scenarios, as well as communication network discrepancies using the developed merging unit simulator. The developed laboratory at University of Western Ontario is a unique state-of-the-art facility, which can facilitate implementation of any indigenously developed protection and control algorithms, and also testing in various (power system and communication network) scenarios.
4. **Reliability models of process bus networks using reliability block diagrams** are developed to analyze various practical process bus communication networks, including different Ethernet switched architectures and time synchronization techniques. These developed reliability models are suitable to analyze combinatorial reliability of protection systems of any electric power substation with the process bus communication infrastructures. Moreover, the failure rates of various process bus architectures can be obtained from the developed models, in order to carry out furthermore detailed reliability analysis of protection functions using Markov modeling.
5. **Extended Markov model to analyze impact of process networks on protection reliability indices** is proposed in this work. The traditional protection reliability indices, such as protection unavailability, abnormal unavailability, and loss of protection security are obtained from the proposed Markov model. The developed

model can recognize various parameters of process bus networks, e.g. addition of communication devices and networks, reconfiguration of Ethernet switched networks, time synchronization techniques, and effect of sampled value loss/delay, as well as improvements in presence of SV estimation algorithm.

8.2 Summary and Conclusions

To achieve the labor cost reduction in wiring and engineering of long and complex copper wires between switchyard and substation control room, IEC 61850 standard part-9-2 proposes the Ethernet communication network, which is referred to as process bus. In addition to the cost savings, process bus also offers simple and flexible architecture, enhancement in protection functions, interoperability, etc. Tremendous work is going on from various relaying manufacturers to develop process bus products by addressing technical challenges related to this technology. The issues for process bus implementation studied from extensive literature survey, including relaying manufacturer's technical and white papers, discussion papers based on pilot project experiences, international journals, publications by standard developer committee, international conferences and magazines, etc., are listed in Chapter 1. The identified major technical challenges in this chapter include the dynamic performance (loss/delay) of SV messages over process bus communication network, and the impact of SV loss/delay in IEC 61850-9-2 enabled protection IEDs installed for substation protection; and impact of process bus communication network on the reliability of protection systems. The work is carried out in this thesis to address these major issues.

Chapter 2 discusses the salient features of the IEC 61850-9-2 process bus, such as time critical protection messages and their multicasting, retransmission of GOOSE, time synchronization over the process bus, and fast Ethernet switched networks. Moreover, this chapter also provides brief overview of practical Ethernet switched architectures suggested by the IEEE PSRC report, including cascaded, ring, star-ring and redundant-ring, as well as potential time synchronization techniques, such as the IRIG-B for external time synchronization to each process bus device, and the IEEE 1588 based time synchronization over the Ethernet network.

The performance of the IEC 61850-9-2 process bus is evaluated for the Ethernet switched ring architecture of a typical 345kV/230kV substation in Chapter 3. Using the OPNET simulation tool, the dynamic models of IEC 61850 based process bus devices and communication protocols are developed to analyze the delay and packet loss for the sampled value packets by considering various communication parameters, such as speed of the communication data link, sampling frequency of the merging units, network background traffic, Ethernet switch buffer size, packet services rate, and the communication channel bit error rate. It is demonstrated that these process bus parameters have influence on the number of sampled value packet loss and end-to-end maximum delays.

In order to alleviate the impact of lost and delayed sampled values on digital protection functions, the corrective measure, i.e. sampled value estimation technique is also presented in Chapter 4. Using this SV estimation technique, the SV estimation algorithm with the sets of coefficients is proposed in this chapter. To examine the accuracy of the proposed SV estimation algorithm, the same 345kV/230kV substation is simulated in PSCAD/EMTDC and the sampled value estimation algorithm is programmed in MATLAB, for the various scenarios, such as system SIRS, fault POW, noise levels in the received signal, and instances on the wave. Moreover, the rare worst case scenarios are presented by considering up to 10 consecutive sampled values loss, coinciding with the fault inception. Results shows that up to 5 consecutive sampled values loss at 4800 Hz sampling frequency, the proposed sampled value estimation algorithm not only offers the reasonable accuracy, but also less computational requirements, and compatibility with any traditional digital relaying algorithm.

To investigate the performance of the proposed sampled value estimation algorithm, Chapter 5 presented laboratory development of IEC 61850-9-2 process bus, including protection IEDs and merging unit simulator using industrial embedded systems over hard-real time platform, implementation of IEEE 1588 based time synchronization over the network, IEC 61850 based network traffic generator, etc. Moreover, a typical IEC 61850-9-2 based process bus communication network is set-up using a network analyzer, traffic generator, and commercial Ethernet switches. The implementation of the SV

estimation algorithm is proposed as a part of sampled value buffer in a protection IED, such a way that it does not interfere with any existing protection functions. And therefore, it is compatible with any well established traditional digital protection functions in a protection IED. The impact of sampled value loss/delay on full-cycle DFT based phasor estimation is analyzed using MATLAB. From this behavior analysis, it is inferred that in some worst conditions, the operation of traditional protection elements may have adverse effects due to multiple SVs loss. Therefore, the SV estimation algorithm is investigated as a part of busbar differential protection and transmission line distance protection IEDs for various SV loss/delay scenarios in a laboratory environment. With the help of the hardware setup for IEC 61850-9-2, it is demonstrated that the busbar differential element in a protection IED may lose security, and it mis-operates during external fault due to SV loss/delay in certain conditions. Moreover, the distance relay zone-1 protection is delayed by 15-20 msec, due to the SV loss/delay. It is demonstrated with extensive testing that with the implementation of the SV estimation algorithm, the bus differential protection element remains secure during external fault, as well as, the line distance protection element operates correctly in time. It is important to note that the performance of the protection elements may not be affected for various other SV loss/delay scenarios. However, the presented investigation shows that the corrective measure for the SV loss/delay can certainly enhance the security and reliability of digital protection functions in IEC 61850-9-2 based environment.

In addition to that, Chapter 6 starts with the reliability analysis of the practical Ethernet switched architectures and time synchronization techniques of the process bus. With the help of the reliability block diagram method, MTTFs and availability is calculated for process bus communications networks of a typical transmission substation layout. Further, the reliability block diagrams are developed for the practical Ethernet switch architectures, such as cascading, ring, star-ring, and redundant ring. The comparison among these architectures is presented in terms of MTTF and availability indices. It is found that the time synchronization over the network based on IEEE 1588 improves the reliability of the process bus, as compared to IRIG-B based external time synchronization architecture. The addition of merging unit with time synchronization source, the MTTF and availability of the bay are affected. Also, Ethernet architectures, star-ring and

redundant-ring provide high reliability and availability as compared to cascaded and ring architecture. However, these architectures are costly and complex due to the fact that it requires additional managed Ethernet switches. The failure rates obtained from this analysis can be used for the detailed Markov model analysis.

The extended Markov model is proposed in Chapter 7, which includes the failure rates of process bus communication devices (λ_{comD}) and time synchronization techniques for substation protection functions. Also, it includes the model of network interface monitoring mechanism and the estimation of lost/delayed SVs over the network. Sensitivity of reliability indices (protection unavailability, abnormal unavailability, loss of protection security) are presented considering various parameters such as, reconfiguration time of communication networks (μ_{comN}), failure rate of a protection IED (λ_{ied}), monitoring effectiveness of the protection function. From this detailed analysis, it can be inferred that protection reliability is affected due to addition of process bus communication network components, but at the same time, reliability indices can be improved by implementing the proposed sampled value estimation algorithm in a protection IED; deploying fast reconfiguration of process bus network (using RSTP); enhancing monitoring of communication ports to detect any failure in the communication link; using IEEE 1588 based time synchronization over the network.

8.3 Recommendations for Future Research

Some of the potential areas for further research are recommended below:

- Development of new or enhancement of existing digital protection functions can be carried out using the developed IEC 61850-9-2 laboratory facilities. The implementation of state-of-the-art process bus lab can open up vast range of opportunities for new developments in this area.
- Fault-tolerant time synchronization techniques can be studied for IEC 61850 based substation communication networks, and developed process bus laboratory can also be used for this evaluation. The ongoing work in the area of IEEE 1588

based time synchronization is to create synchronization with at least N-1 redundancy.

- Optimum protection and automation functions allocation considering Logical Nodes (LNs) proposed by IEC 61850 can be obtained using optimization techniques. This work can utilize the flexibility of function allocation proposed in IEC 61850 standard to devise different optimum process bus architectures.

Publications

Journal:

1. M. Kanabar, and T. S. Sidhu, "An Extended Markov Model for a Substation Protection with Process Bus Communication Networks," [under submission process].
2. M. Kanabar, and T. S. Sidhu, "Laboratory Investigation of IEC 61850-9-2 Based Busbar and Distance Relaying with Corrective Measure for Sampled Value Loss/Delay," [accepted for publication], *IEEE Transaction on Power Delivery*, 2011.
3. M. Kanabar, and T. S. Sidhu, "Performance of IEC 61850-9-2 Process Bus and Corrective Measure for Digital Relaying," *IEEE Transaction on Power Delivery*, vol. 26, no. 2, pp. 725-735, Apr. 2011.

Technical magazine article:

1. T.S. Sidhu, M.G. Kanabar and M. Dadashzadeh, "IEC 61850-9-2 based Process Bus", Protection, Automation and Control World (PAC World), Dec. 2010 Issue. (http://www.pacw.org/issue/december_2010_issue/process_bus/iec_6185092_based_process_bus/complete_article/1.html)

Conference:

1. T. S. Sidhu, M. Kanabar, and P. Parikh, Configuration and Performance Testing of IEC 61850 GOOSE, [accepted for publication], Advanced Power system Automation and Protection, Beijing, China, Oct. 2011.
2. T. S. Sidhu, and M. Kanabar, "Comparison of Reliability and Availability of IEC 61850-9-2 based Substation Process Bus Communication Architectures," in Proc. International conference on Quality, Reliability, and Infocom Technology, New Delhi, India, Dec. 2009.
3. M. G. Kanabar, and T. S. Sidhu, "Reliability and availability analysis of IEC 61850 based substation communication architectures," in Proc. IEEE PES General Meeting, Canada, Jul. 2009.
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Appendix A Development of IEC 61850 Enabled Devices Using OPNET Tool

There are some major modifications required in the standard OPNET workstation model to design IEDs with IEC 61850 features, i.e. priority tagging, GOOSE message etc. These modifications are incorporate in to the workstation model by changing source code of standard process modules. This appendix list out the major modification incorporated into *mac* module to achieve the desired features.

A.1 Implementation of IEC 61850-8-1 GOOSE Message Stack in Protection IED

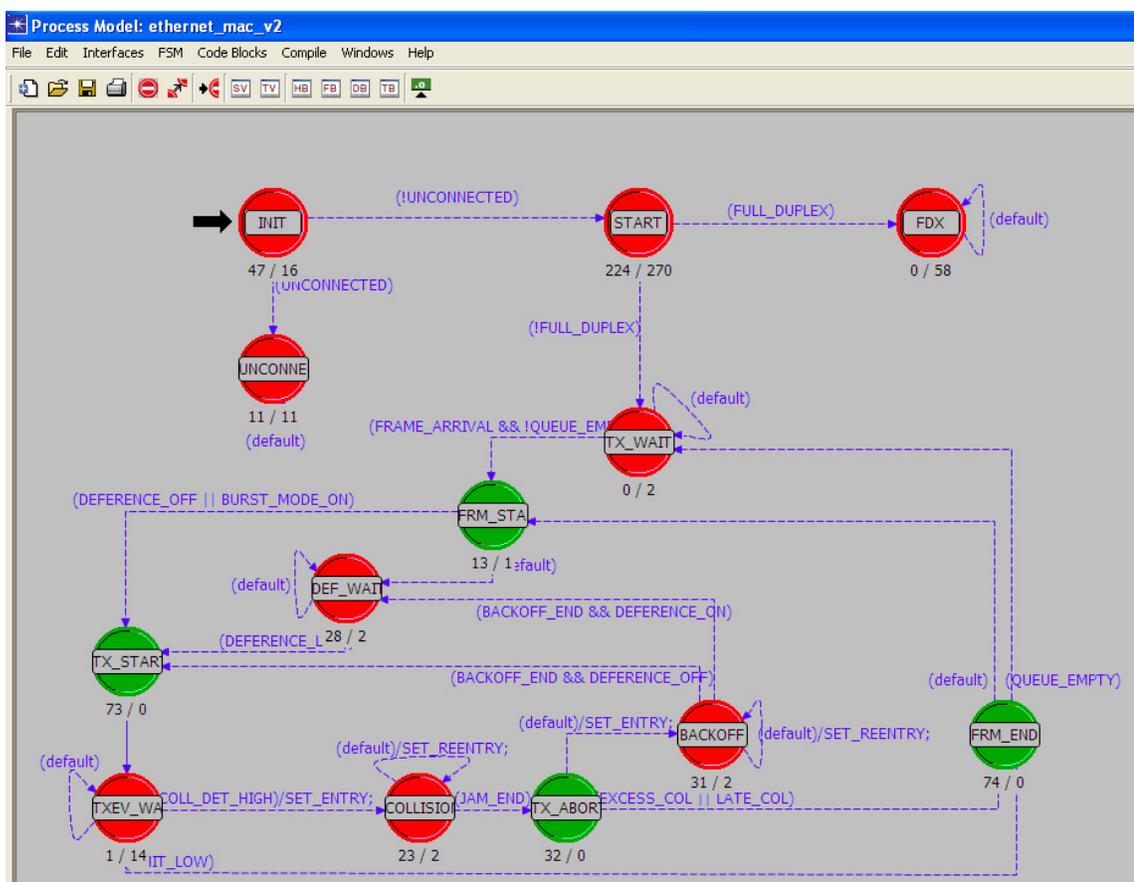


Figure A-1 Ethernet_mac process model

The OPNET workstation mac module only receives packets from arp module. The following modification is incorporated into *mac_ethernet_V2* module of the protection and control IED shown in Figure A-1, which facilitates GOOSE message reception directly at Ethernet layer.

```

static void
eth_mac_fdx_pkt_send (Packet* pkptr)
{
    double          current_time = 0;
    double          tx_delay = 0;
    double          pksize = 0;
    int             out_strm;
    int             num_assoc_out;
    int             tx_index;
    Objid          out_strm_objid;
    Packet*        tmp_pkptr;

    /* Computes delay equal to the transmission and          */
    /* interframe gap delay and send the packet.           */
    FIN (eth_mac_fdx_pkt_send (pkptr));

    /* Set current time.                                    */
    current_time = op_sim_time ();

    /* Compute transmission delay.                          */
    pksize = (double) op_pk_total_size_get (pkptr);
    tx_delay = pksize / ethernet_state_info_ptr->bit_rate;

    /* Compute the total time the next packet has to wait  */
    /* in the queue before it is sent.                      */
    ethernet_state_info_ptr->next_transmission = current_time + tx_delay + INTERFRAME_GAP;

    /* obtain the number of outgoing streams connected to the mac module. */
    num_assoc_out = op_topo_assoc_count (my_objid, OPC_TOPO_ASSOC_OUT,
    OPC_OBJTYPE_STRM);

    /* Loop through all the outgoing streams.                */
    for (tx_index = 0; tx_index < num_assoc_out; ++tx_index)
    {
        /* Obtain ObjectID of the outgoing stream connected to ethernet mac*/
        out_strm_objid = op_topo_assoc (my_objid, OPC_TOPO_ASSOC_OUT, OPC_OBJTYPE_STRM,
        tx_index);

        /* Fetch the outgoing stream number from the stream Objid          */
        op_ima_obj_attr_get (out_strm_objid, "src stream", &out_strm);

        /* Make sure that the stream is not going to higher layer.          */
        if ((out_strm != ethernet_state_info_ptr->strm_to_higher_layer) && (out_strm != ethernet_state_info_ptr->
        >strm_to_ipx)&&(out_strm != ethernet_state_info_ptr->strm_to_eth_layer))
        {

            /* Store the outstream to the transmitter.                */
            ethernet_state_info_ptr->strm_to_lower_layer = out_strm; tmp_pkptr = op_pk_copy (pkptr);
        }
    }
}

```

```

op_pk_send (tmp_pkptr, out_strm);
}
}

op_pk_destroy (pkptr);

FOUT
}

```

A.2 Implementation of Priority Tagging

The following code is added in to the *FDX_Exit_exec* and *mac_function_block* module to support priority tagging features.

FDX Exit exec:

```

switch (intrpt_type)
{
    case OPC_INTRPT_STRM:
    {
        intrpt_strm = op_intrpt_strm ();

        /* If the event is an arrival from the higher */
        /* layer, accept the packet and enqueue it. */

        if ((intrpt_strm == ethernet_state_info_ptr->strm_from_ipx) || (intrpt_strm == ethernet_state_info_ptr->strm_from_higher_layer) || (intrpt_strm == ethernet_state_info_ptr->strm_from_eth_layer))
        {
            if (intrpt_strm == ethernet_state_info_ptr->strm_from_eth_layer)
            {
                goose=1;
            }
            ethernet_mac_llc_pk_accept ();
        }
        else
        {
            /* If the event was an arrival from the physical */
            /* layer, accept the packet and decapsulate it. */

            ethernet_mac_phys_pk_accept ();

        }
        break;
    }
}

```

mac function block:

```

/* Create an Ethernet frame in which to encapsulate the */
/* LLC data. */
*/

```

```
eth_pkptr = op_pk_create_fmt ("ethernet_v2");

    if (eth_pkptr == OPC_NIL)
    {
ethernet_mac_error ("Unable to create Ethernet frame for encapsulation.", OPC_NIL,OPC_NIL);
    }

tag_ptr = oms_vlan_mac_pk_tagstruct_create ();

    if(goose==1)
    {
        tag_ptr->priority=user_priority_1;
        tag_ptr->VID = vid_1;
        goose=0;
    }
else
    {
        tag_ptr->priority=user_priority_2;
    }
```

Appendix B A Typical Substation Configurations

In this appendix, a typical substation configuration used for the analysis purpose in this thesis is explained.

B.1 Test System

Figure B-1 shows a typical 345/230kV transmission substation considered for the analysis. This ring-bus with $1\frac{1}{2}$ circuit-breaker configuration is selected, because this is one of the most common substation layouts in the North-America [35]. Moreover, process bus case study of this particular substation is also discussed in literature [27]. This way, this substation layout is more suitable for process bus analysis. However, the performance and reliability analysis presented in this work is independent of substation layout, and can be applicable to any typical substation.

This substation has total 20 CTs and 8 VTs for the protection and control of total eight substation bays. Furthermore, it is considered that one merging unit can be configured with 8 analog signals from 2 three-phase instrument transformers (CTs/CCVTs), and also with one circuit breaker. Therefore, there will be need of total 14 MUs into the switchyard for this substation. The assignment of primary equipment signals to the particular MU is illustrated in Figure B-1. This sample substation is simulated in PSCAD/EMTDC software, and communication network of this substation is modeled using OPNET.

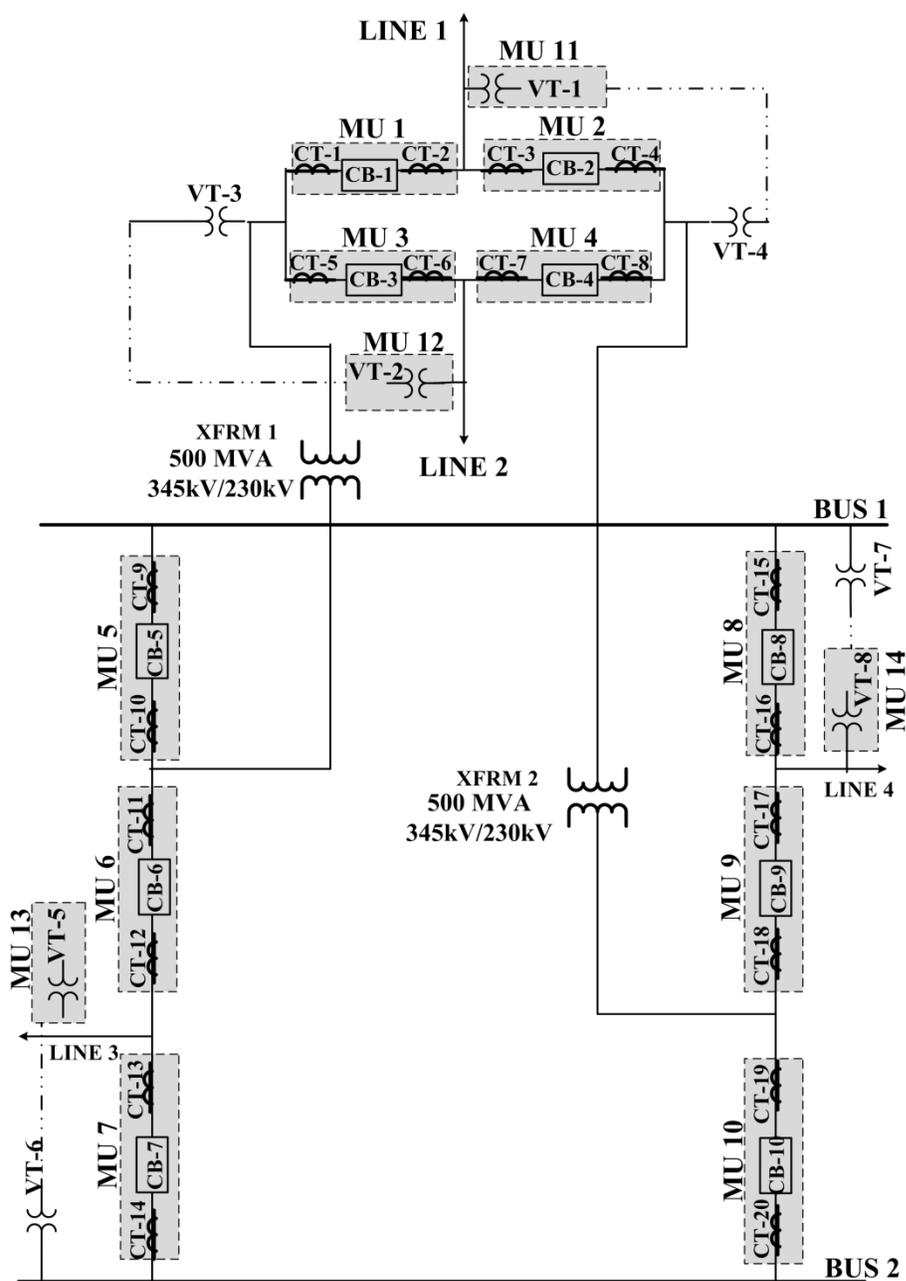


Figure B-1 A typical 345kV/230kV transmission substation layout used for testing

B.1.1 Transmission line

Line Model: Frequency Dependent (Phase) Model

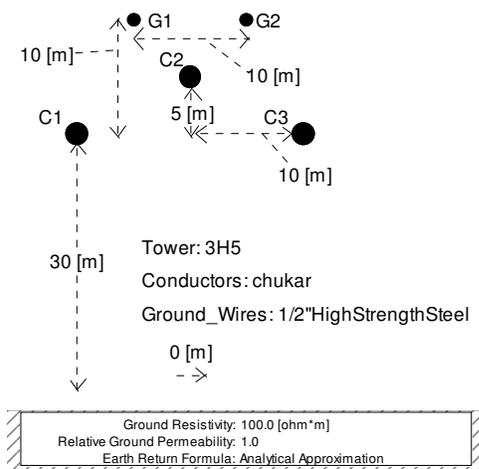


Figure B-2 Tower configuration

Table B-1 Transmission line characteristics

	SEQUENCE RESISTANCE R_{sq} [ohm]/ 100km	SEQUENCE REACTANCE X_{sq} [ohm]/100km	SEQUENCE SUSCEPTANCE B_{sq} [mho]/100km
+ Seq.	3.63	50.86	3.2712e-04
0 Seq.	36.36	132.73	2.3227e-04

Appendix C IEC 61850 Message Formats Used in Hardware Setup

IEC 61850 provides standardized packet formats for Ethernet, GOOSE and Sample value packets. Packet formats of all three types are explained in this appendix. Sample packets of GOOSE and Sample value capture with the help of ethereal are also included along with standardized packet formats.

C.1 Ethernet Message of IEEE 802.3/IEC8802-3

IEC 61850 provides packet format for the IEEE 802.3/IEC8802-3 protocol. Standardized Ethernet packet frame format is shown in Figure 3-6.

Preamble: It is 56-bits field that contains alternating pattern of ones and zeroes, used for synchronization of the receiving physical layers with the incoming but stream.

State-of-Frame: It is the 8 bits value indicating the end of preamble of the Ethernet frame.

Destination MAC Address: It is a 48-bits address that specifies the station(s), to which packet should be sent.

Source MAC Address: It is a 48-bits field which contains address of the transmitting station.

Length Type: Indicates either the number of MAC-client data bytes that are contained in the data field of the frame, or the frame type ID if the frame is assembled using an optional format.

MAC Client Data: A sequence of n bytes ($46 \leq n < 1500$) of nay value. (The total frame minimum is 64 bytes). The pad contains (if necessary) extra data bytes in order to bring the frame length up to its minimum size. A minimum Ethernet frame size is 64 bytes from the Destination MAC address field through the Frame Check Sequence.

C.1.1 Multicast address selection

Multicast address used within IEC 61850 standard shall have the following structure:

The first three octets are assigned by IEEE with 01-0C-CD. The fourth octet shall be 01 for GOOSE, 02 for GSSE, and 04 for multicast sampled values. The last two octets shall be used as individual addresses assigned by the range defined in Table C-1.

Table C-1 Recommended multicast addressing example

Service	Recommended address range assignments	
	Starting address (hexadecimal)	Ending address (hexadecimal)
GOOSE	01-0C-CD-01-00-00	01-0C-CD-01-01-FF
GSSE	01-0C-CD-02-00-00	01-0C-CD-02-01-FF
Multicast sampled values	01-0C-CD-04-00-00	01-0C-CD-04-01-FF

C.1.2 Priority tagging/virtual LAN

According to IEEE 802.1Q priority tagging is used to separate time critical and high priority traffic from low priority bus load. Table C-2 shows packet fields for priority tagging and VLAN. Below is the explanation of those fields, and values defined by IEC 61850.

TPID (Tag Protocol Identifier) Field: It indicates the Ethertype assigned for 802.1Q Ethernet encoded frames. This value shall be 0x8100.

TCI (Tag Control Information) Fields:

- **User Priority:** It should be set by configuration to separate sampled values and time critical GOOSE messages from low priority load. If it is not configured then the default values mentioned in the Table C-2 should be used.
- **CFI (Canonical Format Indicator):** BS1[0]; a single bit flag value. For this standard the CGI bit value shall be reset (value = 0)

- VID (VLAN Identifier): If virtual LAN mechanism is used , then the VID shall be set by configuration. Otherwise it shall be set to zero.

Table C-2 Default VLAN IDs and priorities

Service	Default VID	Default priority
GOOSE	0	4
GSE	0	1
Sampled Values	0	4

C.1.3 Ethertype, and other header information:

GSE, GOOSE, and sampled values shall be directly mapped to the reserved Ethertypes and the Ethertype PDU. The assigned values shall be as defined in Table C-3. APPID (application identifier): It is used to select ISO/IEC 8802-3 frames containing GSE Management and GOOSE messages and to distinguish the application association.

Table C-3 Assigned Ethertype values for IEC 61850 standard Messages

Use	Ethertype value (hexadecimal)	APPID type
IEC 61850-8-1 GOOSE	88-B8	00
IEC 61850-8-1 GSE Management	88-B9	00
IEC 61850-9-2 Sampled Values	88-BA	01

Length: Number of octets including the Ethertype PDU header starting at APPID, and the length of the APDU (Application Protocol Data Unit). Therefore, the value of Length shall be $8 + m$, where m is the length of the APDU and m is less than 1492.

C.1.4 Frame check sequence

The Frame Check Sequence is error checking field contains 32-bits Cyclic Redundancy Check (CRC) field. The CRC is generated based on the destination address, type and data fields. Receiving MAC recalculates the CRC to check for any damage frame.

C.2 SV Message Application Protocol Data Unit (APDU)

The sampled value APDU defined by IEC61850-9-2 is shown in Figure C-1 . This APDU includes various fields with a specific tag. For example, start of SV is with tag 60; number of ASDUs (Application Specific Data Unit) within an APDU has tag 80, and so on. One APDU can include multiple ASDUs. ASDU includes: sampled value ID, sample control, revision, synchronization number, which is followed by sequence of voltage and current signal data. More details on SV data field can be obtained from [13], [14].

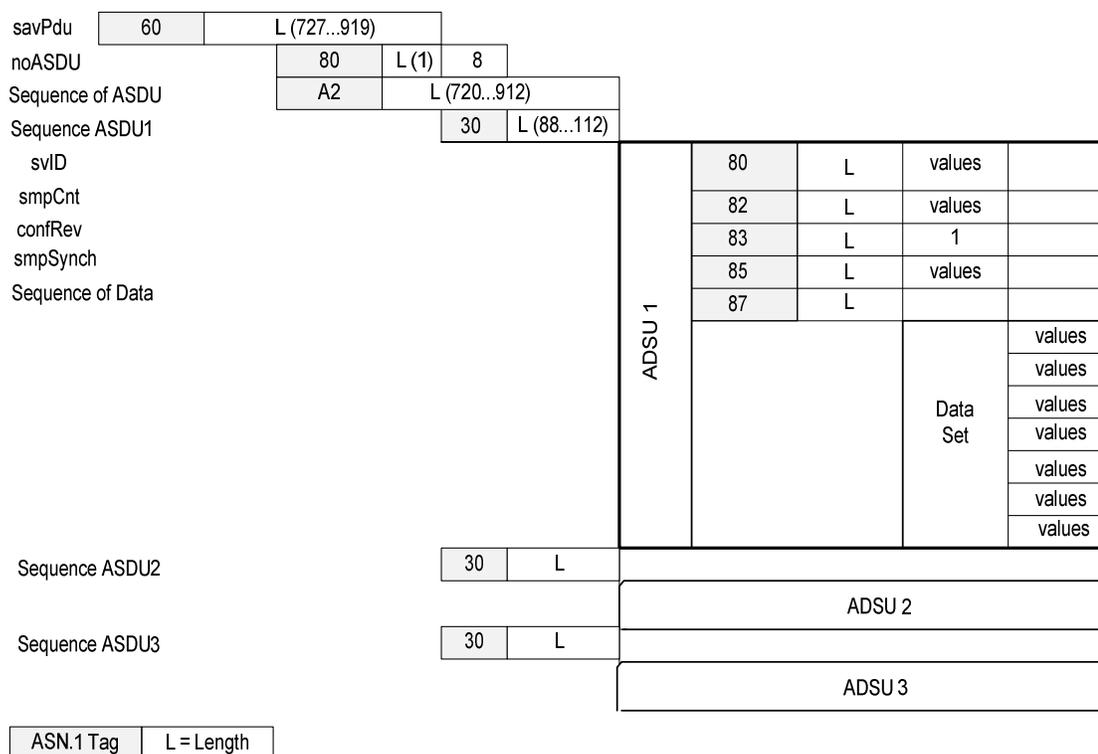


Figure C-1 Application protocol data unit of IEC 61850-9-2 sampled value message

C.2.1 A typical sampled value message used for hardware set-up

Following is the description of SV message used for the laboratory set-up in this work. This message is captured using network analyzer as discussed in Chapter 5.

No.	Time	Source	Destination	Protocol Info
1	0.000000	00:50:c2:4f:90:b2	01:0c:cd:04:00:00	IECSMV SMV 9-2

Publish

Frame 1 (121 bytes on wire, 121 bytes captured)
 Arrival Time: Dec 14, 2009 12:58:20.019265000
 Time delta from previous packet: 0.000000000 seconds
 Time since reference or first frame: 0.000000000 seconds
 Frame Number: 1
 Packet Length: 121 bytes
 Capture Length: 121 bytes
 Protocols in frame: eth:iecsmv

Ethernet II, Src: 00:50:c2:4f:90:b2 (00:50:c2:4f:90:b2), Dst: 01:0c:cd:04:00:00 (01:0c:cd:04:00:00)
 Destination: 01:0c:cd:04:00:00 (01:0c:cd:04:00:00)
 Address: 01:0c:cd:04:00:00 (01:0c:cd:04:00:00)
1 = Multicast: This is a MULTICAST frame
0. = Locally Administrated Address: This is a
 FACTORY DEFAULT address
 Source: 00:50:c2:4f:90:b2 (00:50:c2:4f:90:b2)
 Address: 00:50:c2:4f:90:b2 (00:50:c2:4f:90:b2)
0 = Multicast: This is a UNICAST frame
0. = Locally Administrated Address: This is a
 FACTORY DEFAULT address
 Type: IEC 61850/SV (Sampled Value Transmission (0x88ba))

IEC 61850 SMV
 AppID*: 0x4000
 PDU Length*: 107
 Reserved1*: 0x0000
 Reserved2*: 0x0000

PDU
 SMV 9-2
 {
 Number of ASDUs: 1
 Start of ASDUs
 {
 ASDU
 {
 ID*: 000MU0001
 Sample Count: 461
 Config Rev*: 1
 Sample Synched*: TRUE
 Samples {
 Voltages and Current Data sets.
 }
 }
 }
 }

C.3 GOOSE Message APDU

Figure C-2 shows the APDU of GOOSE message. The fields of the message is explained below:

80	L	gocbRef	
81	L	timeAllowedtoLive	
82	L	dataset	
83	L	goID	
84	L	t	
85	L	stNum	
86	L	sqNum	
87	L	test	
88	L	confRev	
89	L	ndsCom	
8a	L	numDatSetEntries	
		Data	values
			values

ASN.1 Tag	L = Length
-----------	------------

Figure C-2 Application protocol data unit of IEC 61850-8-1 GOOSE message

gocbRef: It specifies control block reference.

timeAllowedtoLive: It provides information about the time allowed to live the.....

dataset: This parameter contains the ObjectReference of the DATA_SET taken from the GOOSE Control reference block.

goID: This is the identifier of the LOGICAL-DEVICE (taken from the GoCB) in which the GoCB is located.

T: The timestamp contains the time at which the attribute StNum was incremented.

StNum: The state number parameter contains the counter that increments each time a value change had been detected within the DATA-SET specified by DataSet and a GOOSE message is sent.

SqNum: The sequence number parameter SqNum contains the counter that increments each time a GOOSE message is sent.

Test: The test parameter indicates with the value of TRUE that the values of the message shall not be used for operational purpose, but only for testing.

ConfRev: The configuration revision parameter ConfRev (taken from the GoCB) contains the count of the number of times that the configuration of the DATA-SET referenced by DataSet is changed.

NdsCom: The parameter needs commissioning contains the attribute NdsCom (taken from the GoCB) of the GoCB and is used to indicate that the GoCB requires further configuration.

numDataSetEntries:

Data: Data contains the user defined information (of the members of DATA-SET) to be included in a GOOSE message. The parameter Value contains the value of a member of the DATA-SET referenced in the GoCB

C.3.1 A typical sampled value message used for hardware set-up

Following is the description of GOOSE message used for the laboratory set-up in this work. This message is captured using network analyzer as discussed in Chapter 5.

No.	Time	Source	Destination	Protocol Info
5	0.325599	00:30:a7:00:12:8b	01:0c:cd:01:00:00	IECGOOSE GOOSE

Request

Frame 5 (134 bytes on wire, 134 bytes captured)

Arrival Time: Dec 15, 2009 10:51:48.643353000

Time delta from previous packet: 0.325308000 seconds

Time since reference or first frame: 0.325599000 seconds

Frame Number: 5

Packet Length: 134 bytes

Capture Length: 134 bytes

Protocols in frame: eth:iecgoose

Ethernet II, Src: 00:30:a7:00:12:8b (00:30:a7:00:12:8b), Dst: 01:0c:cd:01:00:00 (01:0c:cd:01:00:00)

Destination: 01:0c:cd:01:00:00 (01:0c:cd:01:00:00)

Address: 01:0c:cd:01:00:00 (01:0c:cd:01:00:00)

```

....1 ..... = Multicast: This is a MULTICAST frame
....0 ..... = Locally Administrated Address: This is a
FACTORY DEFAULT address
Source: 00:30:a7:00:12:8b (00:30:a7:00:12:8b)
Address: 00:30:a7:00:12:8b (00:30:a7:00:12:8b)
....0 ..... = Multicast: This is a UNICAST frame
....0 ..... = Locally Administrated Address: This is a
FACTORY DEFAULT address
Type: IEC 61850/GOOSE (0x88b8)
IEC 61850 GOOSE
AppID*: 0
PDU Length*: 120
Reserved1*: 0x0000
Reserved2*: 0x0000
PDU
    IEC GOOSE
    {
        Control Block Reference*: SEL_421_1CFG/LLN0$GO$DSet14
        Time Allowed to Live (msec): 2000
        DataSetReference*: SEL_421_1CFG/LLN0$DSet14
        GOOSEID*: SEL_421_1
        Event Timestamp: 2009-12-15 17:29.57.956707 Timequality: bf
        StateNumber*: 2
        SequenceNumber*:      Sequence Number: 64560
        Test*: FALSE
        Config Revision*: 1
        Needs Commissioning*: FALSE
        Number Dataset Entries: 2
        Data
        {
            BOOLEAN: FALSE
            BITSTRING:
                BITS 0000 - 0015: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
        }
    }

```

Appendix D IEEE 1588 based Time Synchronization for IEC 61850-9-2

With the Precision Time Protocol (PTP) described in IEEE 1588, it is possible to synchronize distributed clocks with an accuracy of less than 1 microsecond via Ethernet networks [101], [102]. Working principle of PTP is explained in detail in this appendix. This appendix also includes the message formats of the main PTP messages and sample capture packets for these messages.

D.1 IEEE 1588 PTP Message-Based Time Synchronization

Precision time protocol acts based on Master to Slave mechanism. PTP defined three types of clock, i.e. grand master, transparent clock, and ordinary clock. At the beginning of synchronization process, each clock participating in synchronization process exchange the identity and properties with other clocks using special message called “ANNOUNCE”. Once all clocks know each other’s information, master/slave hierarchy is created using Best Master Clock (BMC) algorithm. BMC algorithm runs continuously to quickly adjust for changes in network configuration [103], [104]. Every slave clock synchronizes with the master clock, so that events and timestamps in all nodes uses the same timer values. A time difference between the master clock and a slave clock is due to a combination of the clock offset and message transmission delay, so process of synchronization is divided in to two phases; offset correction and delay correction.

Figure D-1 shows the message exchange sequence between the master and slave clock during synchronization process. There are four types of message - Sync, Follow Up, Delay Request, Delay Response. The sequence of message exchanges is repeated at a certain fix rate, typically between 8 per second to 64 per second.

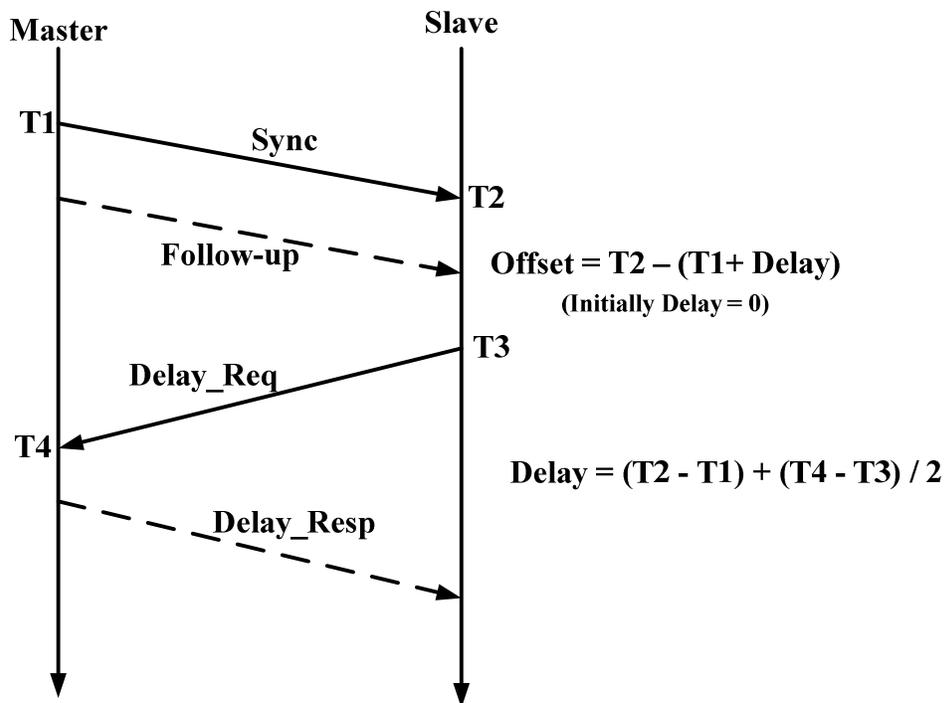


Figure D-1 PTP working principle

The master node initiates offset correction using a sync and follow up message. Follow up message is optional. In the two step mode offset correction method, master node sends Sync message – with essential time information to slave node. And parallel to this accurate time stamp information at which message leaves the master node is send to the slave node in Follow-up message. While, in case of one step mode, accurate time stamp is inserted on-the-fly in to sync message itself by hardware. When the master node sends a sync message, a slave uses its local clock to timestamp (T2) the arrival of the sync message. The slave compares it to the actual sync transmission timestamp (T1) in the master clock's follow up message/ or time stamp inserted into sync message. The slave clock then calculated the offset with reference to master clock using T1 and T2. In the initial phase, when delay is unknown factor, slave clock is corrected by the $(T2 - T1)$ correction factor.

The second phase of the synchronization process, the delay correction, calculates the delay between slave and master. Slave clock time stamp (T3) the Delay_req packet and

sends to master clock. Then, master clock timestamps (T4) the arrival of the Delay_req message. It then sends a Delay_resp message with the Delay_req arrival timestamp. From the local timestamp of T3 and time stamp reception provided by master clock T4, the slave calculates the delay between slave and master. Because the master and slave clocks drift independently, periodic offset and delay correction are performed to maintain clock synchronization [103].

Using this synchronization process, timing fluctuations in the PTP elements especially the protocol stack and the latency time between the master and slave are eliminated [76].

D.2 IEEE 1588 PTP Clocks

The function of IEEE 1588 clocks are described below:

Grand Master Clock/ Master Clock: This is the primary reference source within a PTP sub domain, the “ultimate source of time for clock synchronization using the PTP protocol” [76]. It is very high precision time source. Master clock is controlled by high precision time source such as GPS receiver or Atomic clock, and used to synchronize the slaves connected to it.

Transparent Clock: The path delay measurement process of PTP involves the precision timing of two messages — a sync message and a delay request. The average path delay of the two messages gives the one-way delay. This however, assumes that the communication path is completely symmetric. This assumption does not hold in a switched network however, largely due to the buffering process within Ethernet switches. To overcome this, transparent clocks are added into the revised version of 1588 standard as an improved method of forming cascaded topologies. There are two types of transparent clocks, 1) End to End 2) Peer to Peer. Peer-to-peer transparent clocks can allow for faster reconfiguration after network topology changes. The end-to-end transparent clock forwards all messages just as a normal switch [103].

Ordinary Clock: An ordinary clock is formally defined as a PTP clock with a single PTP port. It is generally used as the end nodes with the synchronization network. It can come in various forms and with different interfaces [103].

D.3 IEEE 1588 PTP Message Formats

D.3.1 IEEE 1588 PTP EtherType and multicast addresses

EtherType:

The specification in this annex shall apply to all PTP implementations directly using Ethernet format packets with the 88F716 Ethertype as a communication service.

Multicast MAC addresses:

By default PTP messages shall use MAC addresses as specified in Table D-1 .

Table D-1 Multicast MAC addresses

Message types	Address (hex)
All except peer delay mechanism messages	01-1B-19-00-00-00
Peer delay mechanism messages	01-80-C2-00-00-0E

D.3.2 IEEE 1588 PTP general header specifications

The common header for all PTP messages is specified in Table D-2.

Table D-2 Common message header

Bits								Octets	Offset
7	6	5	4	3	2	1	0		
transportSpecific				messageType				1	0
reserved				versionPTP				1	1
messageLength								2	2
domainNumber								1	4
reserved								1	5
flagField								2	6
correctionField								8	8
Reserved								4	16
sourcePortIdentity								10	20
sequenceId								2	30
controlField								1	32
logMessageInterval								1	33

transportSpecific: This field may be used by a lower layer transport protocol.

messageType: The value of messageType shall indicate the type of the message as defined in Table D-3

Table D-3 Values of message type field

Message Type	Message class	Value (hex)
Sync	Event	0
Delay_Req	Event	1
Follow_Up	General	8
Delay_Resp	General	9
Announce	General	B

versionPTP: The value of the versionPTP field shall be the value of the portDS.versionNumber member of the data set of the originating node.

messageLength: The value of the messageLength shall be the total number of octets that form the PTP message.

domainNumber: For ordinary clocks, the value of domain Number shall be the value of the defaultDS.domainNumber member of the data set of the originating ordinary clock. For peer-to-peer transparent clock, the value shall be the value defined in standard.

flagField: It is used to determine the circumstance in which the bad block was detected.

correctionField: The correctionField is the value of the correction measured in nanoseconds and multiplied by 2^{16} .

sourcePortIdentity: The value of the sourcePortIdentity field shall be the value of the portDS.portIdentity member of the data set of the port that originated this message.

sequenceId: The value of the sequenceId field shall be assigned by the originator of the message in conformance with 7.3.7 except in case of Follow_Up, Delay_Resp, Pdelay_resp, and Pdelay_Resp_Follow_Up and management messages.

controlField: The value of the controlField depends on the message type defined in the messageType field (Table D-3) and shall have the value specified in Table D-4.

Table D-4 controlField enumeration

Message Type	controlField value (hex)
Sync	00
Delay_Req	01
Follow_Up	02
Delay_Resp	03
Management	04
All others	05
Reserved	06-FF

logMessageInterval: The value of the logMessageInterval field is determined by the type of the messages.

D.3.3 IEEE 1588 PTP Sync and Delay_Req messages format

Sync and Delay_Req message fields are shown in Table D-5. Header field of the messages follow the format of the PTP common message header format explained in Section D.2.2.

Table D-5 Sync and Delay_Req message fields

Bits							Octets	Offset
7	6	5	4	3	2	1		
header (see Table- D-2)							34	0
originTimestamp							10	34

The originTimestamp field of the Sync message shall be 0 or an estimate no worse than ± 1 s of the <syncEventEgressTimestamp>. The correctionField of the Sync message shall be set to 0.

D.3.4 A typical Sync message used for hardware set-up

A typical synchronizing message (Sync_msg) used in the laboratory for the implementation of IEEE 1588 is shown below:

```
No. Time      Source      Destination  Protocol Info
41 10.010524 00:0a:dc:44:39:e4 01:1b:19:00:00:00 0x88f7
Ethernet II
```

```
Frame 41 (60 bytes on wire, 60 bytes captured)
  Arrival Time: Aug 9, 2010 14:57:46.212070000
  Time delta from previous packet: 0.264402000 seconds
  Time since reference or first frame: 10.010524000 seconds
  Frame Number: 41
```

```

Packet Length: 60 bytes
Capture Length: 60 bytes
Protocols in frame: eth:data
Ethernet II, Src: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4), Dst:
01:1b:19:00:00:00 (01:1b:19:00:00:00)
  Destination: 01:1b:19:00:00:00 (01:1b:19:00:00:00)
    Address: 01:1b:19:00:00:00 (01:1b:19:00:00:00)
      .... 01 .... = Multicast: MULTICAST frame
      .... 0. .... = Locally Administrated Address: This is a FACTORY DEFAULT address
    Source: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4)
      Address: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4)
        .... 0 .... = Multicast: UNICAST frame
        .... 0. .... = Locally Administrated Address: This is a FACTORY DEFAULT address
    Type: Unknown (0x88f7)
Data (46 bytes)

```

D.3.5 IEEE 1588 PTP Follow_Up message format

Table D-6 shows the PTP Follow-up message format. Header field of the Follow_up message is explained in the PTP common message header format of section D.2.2.

Table D-6 Follow_Up message fields

Bits								Octets	Offset
7	6	5	4	3	2	1	0		
header (see Table- D-2)								34	0
preciseOriginTimestamp								10	34

The preciseOriginTimestamp field of the Follow_Up message shall be an estimate no worse than ± 1 s of the <syncEventEgressTimestamp> of the associated Sync message excluding any fractional nanoseconds.

D.3.6 A typical Follow_Up message used for hardware set-up

A typical follow-up message (Follow_UP) used in the laboratory for the implementation of IEEE 1588 is shown below:

```

No. Time      Source      Destination  Protocol Info
38 9.011116 00:0a:dc:44:39:e4 01:1b:19:00:00:00 0x88f7
Ethernet II
Frame 38 (60 bytes on wire, 60 bytes captured)
  Arrival Time: Aug 9, 2010 14:57:45.212662000
  Time delta from previous packet: 0.001574000 seconds
  Time since reference or first frame: 9.011116000 seconds

```

Frame Number: 38
Packet Length: 60 bytes
Capture Length: 60 bytes
Protocols in frame: eth:data
Ethernet II, Src: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4), Dst:
01:1b:19:00:00:00 (01:1b:19:00:00:00)
Destination: 01:1b:19:00:00:00 (01:1b:19:00:00:00)
Address: 01:1b:19:00:00:00 (01:1b:19:00:00:00)
.... ..1 = Multicast: MULTICAST frame
.... ..0. = Locally Administrated Address: This is a FACTORY DEFAULT address
Source: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4)
Address: 00:0a:dc:44:39:e4 (00:0a:dc:44:39:e4)
.... ..0 = Multicast: UNICAST frame
.... ..0. = Locally Administrated Address: This is a FACTORY DEFAULT address
Type: Unknown (0x88f7)
Data (46 bytes)

Appendix E Basics of Reliability Analysis

Basic formulas of the reliability and availability used for reliability block diagram methods are explained in this appendix.

E.1 Reliability Functions

One of the most extensively used reliability functions is failure rate function $\lambda(t)$. Failure rate is the measure of the rate at which failure occurs. shows the typical failure rate function of electronic components, which is also referred to as bathtub curve [98].

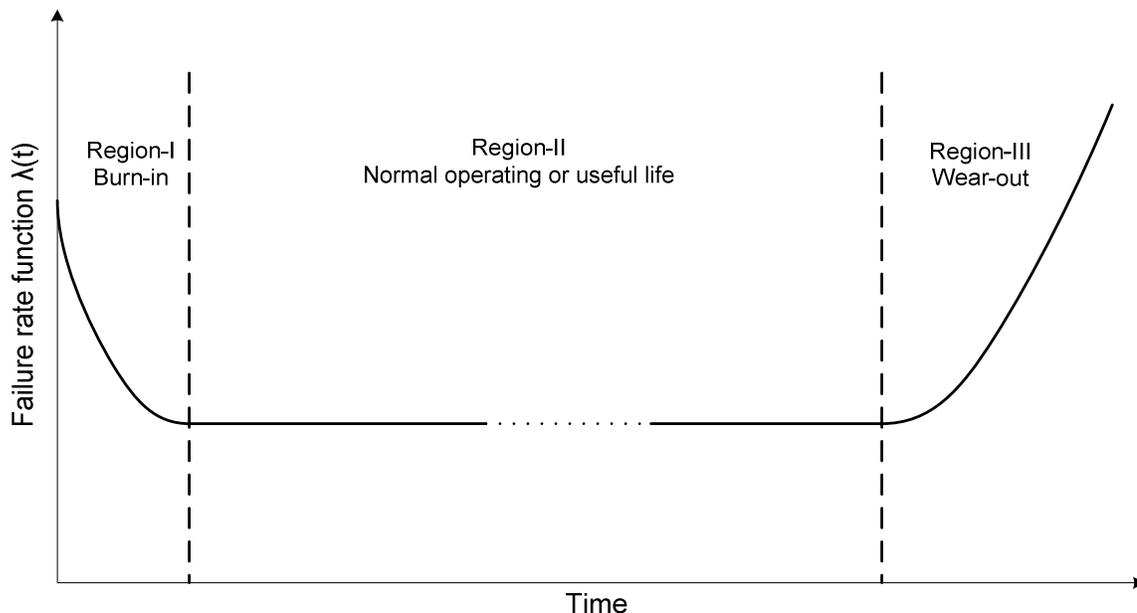


Figure E-1 Typical failure rate function of SAS components

It can be observed from the that during normal operation or useful life (region-II), the failure rate function remains constant. During region-I and III, failure rate is higher comparatively due to manufacturing errors and fatigue because of ageing respectively. This is true for most of the advanced power system protection devices which are based on electronic components. Hence, Poisson or exponential distribution is valid for the reliability and availability analysis of SAS components, as the failure rate remains constant during normal operating period (region-II) [98].

For exponential distribution, reliability function $R(t)$ will be,

$$R_i(t) = e^{-\lambda_i t} \quad (\text{E-1})$$

Mean value for exponential distribution is designated as MTTF,

$$MTTF_i = \int_0^{\infty} R_i(t) dt = \frac{1}{\lambda_i} \quad (\text{E-2})$$

Availability of a component for a given $MTTR_i$,

$$A_i = \frac{MTTF_i}{MTTF_i + MTTR_i} \quad (\text{E-3})$$

E.2 MTTF and Availability using Reliability Block Diagram

Reliability block diagram (RBD) shows the logical connections of functioning components needed to fulfill a specific system function. As shown in Figure E-2 Reliability block diagram for simple systems RBD is consists of components with series-parallel combinations.

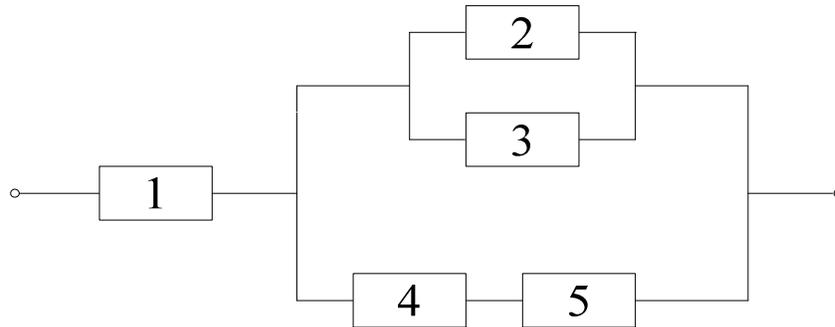


Figure E-2 Reliability block diagram

E.2.1 MTTF and availability calculations for series components

From the reliability point of view, the components are connected in series if they all must work for the successful functioning of the system or only one need to fail for the system failure as shown in Figure E-3 Simple series system with two components.

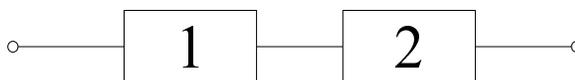


Figure E-3 Simple series system with two components

Reliability function of the series system,

$$R_s(t) = R_1(t)R_2(t) = e^{-\lambda_1 t} e^{-\lambda_2 t} = e^{-(\lambda_1 + \lambda_2)t} \quad (\text{E-4})$$

Hence, MTTF of the series system,

$$MTTF_s = \int_0^{\infty} R_s(t) dt = \frac{1}{\lambda_1 + \lambda_2} = \frac{MTTF_1 \cdot MTTF_2}{MTTF_1 + MTTF_2} \quad (\text{E-5})$$

Availability of the series system,

$$A_s = A_1 \cdot A_2 \quad (\text{E-6})$$

E.2.2 MTTF and availability calculations for parallel components

In contrast, the components are connected in parallel from the reliability point of view (as shown in Figure E-4 Simple parallel system with two components

), if only once needs to be working for successful functioning of the system or all must fail for the system failure,

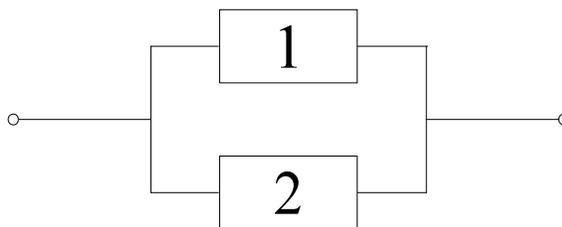


Figure E-4 Simple parallel system with two components

For parallel systems with two components,

$$\begin{aligned}
R_p(t) &= R_1(t) + R_2(t) - R_1(t)R_2(t) \\
&= e^{-\lambda_1 t} + e^{-\lambda_2 t} - e^{-(\lambda_1 + \lambda_2)t}
\end{aligned}
\tag{E-7}$$

MTTF of the parallel system,

$$\begin{aligned}
MTTF_p &= \int_0^{\infty} R_p(t) dt = \frac{1}{\lambda_1} + \frac{1}{\lambda_2} - \frac{1}{\lambda_1 + \lambda_2} \\
&= MTTF_1 + MTTF_2 - \frac{MTTF_1 \cdot MTTF_2}{MTTF_1 + MTTF_2}
\end{aligned}
\tag{E-8}$$

Availability of the parallel system,

$$A_p = A_1 + A_2 - A_1 A_2 \tag{E-9}$$

E.3 Solution Method for Markov Model

This subsection of the appendix describes how to solve Markov model (state-transition diagram). First step is to obtain transition rates of the entire Markov model. Transition rates are mainly due to one of these conditions: failure, repair, reconfiguration, switching, etc. Second step is to construct a stochastic transitional probability matrix ‘T’ as explained in [98]. Using vector of the state probabilities ‘v’, the probabilities associated with individual state can be obtained as follows:

$$v T = v \tag{E-10}$$

where,

$$v = [P_1 \ P_2 \ \dots \ P_n];$$

P_i = individual state probabilities, and $i=1$ to n ;

n = total number of states in Markov model;

$$\text{Stochastic transitional probability matrix, } T = \begin{bmatrix} p_{1,1} & p_{1,2} & \dots & p_{1,n} \\ p_{2,1} & p_{2,2} & \dots & p_{2,n} \\ \dots & \dots & \dots & \dots \\ p_{n,1} & p_{n,2} & \dots & p_{n,n} \end{bmatrix}$$

$p_{i,j}$ = transitional probabilities.

Curriculum Vitae

Name: Mital Kanabar

EDUCATION:

- ❖ **Doctor of Philosophy (Ph.D), [Sept. 2007-Present]**
University of Western Ontario, Canada.
- ❖ **Master of Technology (M.Tech.) in Power Systems Engineering, [July 2007]**
Indian Institute of Technology (IIT) Bombay, India.
- ❖ **Bachelor of Engineering in Electrical Engineering, [July 2003]**
Sardar Patel University, India.

WORK EXPERIENCE:

- ❖ **Instructor at University of Western Ontario** [Jan 2011 – Apr. 2011]: Taught Power System Protection (ECE4456b), University of Western Ontario, Winter 2010.
- ❖ **Research Assistant at University of Western Ontario** [Sept. 2007 - May 2011]: Working on industrial project funded by GE Digital Energy.
- ❖ **Teaching Assistant at University of Western Ontario** [Sept. 2007 – Dec. 2010]: Assisting instructor in various Power Systems courses, and conducting experiments for Electrical Engineering Laboratories.
- ❖ **Research Assistant (Project Engineer) at IIT Bombay** [July 2005 to June 2007]: Worked on industrial project entitled “Study of Infrastructure and Issues involved in Implementation of Distributed Generation in Rural India”, funded by Central Power Research Institute (CPRI) of India.
- ❖ **Engineer at Larsen & Toubro Ltd.** [July, 2003 to May, 2004]: Experience with Engineering, Procurement, Marketing divisions associated with Turnkey Power Plant Project, India.

INTERNATIONAL PUBLICATIONS:

- [1]. **M. Kanabar**, and T. S. Sidhu, “Extended Markov Model for Digital Protection Functions with IEC 61850-9-2 Process Bus,” [submitted for internal review], *IET Journal Generation, Transmission, and Distribution*, 2011.
- [2]. **M. Kanabar**, T. S. Sidhu, and M. Dadash Zadeh “Laboratory Investigation of IEC 61850-9-2 Based Busbar and Distance Relaying with Corrective Measure for Sampled Value Loss/Delay,” [accepted for publication], *IEEE Transaction on Power Deliver*, 2010.
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- [13]. **M. Kanabar**, C. Dobariya, and S. A. Khaparde, "Rotor Speed Stability Analysis of Constant Speed Wind Turbine Generators," in Proc. IEEE conference on PEDES, at Delhi, Dec. 2006.
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- [15]. **M. Kanabar**, S. A. Khaparde, and B. G. Fernandes, "Generalized optimal control strategy for Fuel Cell operation," International conference on Computer Application in Electrical Engineering Research Advances, at IIT Roorkey, Sept. 2005.

BOOK CHAPTER AND TECHNICAL ARTICLE:

- ❖ "Rotor Speed Stability Analysis of a Constant Speed Wind Turbine Generator", [accepted for publication], in Wind Turbine Book by InTech Publisher, Austria, 1st edition expected in 2011.

- ❖ “IEC 61850-9-2 Based Process Bus: Implementation and Testing of an Algorithm for Estimation of Lost/Delayed Sampled Values”, in Protection, Automation, and Control (PAC) World Magazine, Texas, USA, expected in Winter 2011 issue.

PROFESSIONAL COURSES:

- ❖ “Synchronized Phasor Measurements: Fundamentals and Applications” by Dr. J. Chow, Dr. A. Phadke, Dr. J. S. Thorp, etc. at IEEE PES General Meeting, Minneapolis, USA [July 2010].
- ❖ GE Digital Energy Interactive CD course on Power System Protection at University of Western Ontario [Dec. 2009].
- ❖ “Grid Disturbances, Remedial Measures & Restoration” by the PES Distinguished Lecturer Dr. Prabha S. Kundur (Fellow IEEE) of Powertech Labs, Vancouver, BC, Canada, [Dec. 2006].

COMPUTER SKILLS:

- ❖ **Languages:** FORTRAN, C, Microprocessor 8085, Assembly language for DSP (TMS320F240), QNX hard-real time operating system functions.
- ❖ **Simulation Packages:** MATLAB/SIMULINK, DIgSILENT, PSPICE, PSCAD, OPNET, RSCAD.

SCHOLASTIC ACHIEVEMENTS:

- ❖ Achieved **10 out of 10 CPI** (Cumulative Performance Index) in final year Master’s Research Project at IIT Bombay [July 2007].
- ❖ Recipient of **Award of Excellence** in DSP Application Presentation-2005, jointly organized by Texas Instrumentation, IETE and ISTE [October, 2005].
- ❖ Ranked **1st** in Electrical Engineering department of Sardar Patel University in final year of graduation with **10 out of 10 CPI** [July, 2003].
- ❖ Ranked **1st** in Technical paper presentation contest held by Indian Society for Technical Education (ISTE) [March, 2003].

POSITIONS OF RESPONSIBILITY AND AWARDS:

- ❖ Appointed to represent research team at Electrical and Computer Engineering Dept., University of Western Ontario, London, Canada.
- ❖ Independently conducted five laboratory sessions for the 40 delegates from different industries for the Summer School at IIT Bombay [July, 2005].
- ❖ Awarded for the excellence in performance for organizing “Larsen & Toubro sports festival” [Dec., 2004].
- ❖ Honorary Award of Appreciation for volunteer work in developments of Power System Protection Laboratory at Sardar Patel University, India.