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Novel ZCS PWM Methods for Industrial Applications

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Abstract

Pulse width modulation (PWM) converters that consist of two or more interleaved boost/buck converter modules are used widely in industry. Soft-switching approaches for these converters can either be zero-voltage switching (ZVS) if implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. The main idea of this thesis is to implement ZCS for IGBT turn-on and turn-off. Most converters use an auxiliary circuit that is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS.

ZCS-PWM converters that use an auxiliary circuit to help the main converter switch turn-off with ZCS are generally less efficient than hard-switching converters at light loads. The main reason for this is that the auxiliary circuit losses dominate when the converter is operating under these conditions. Auxiliary circuit losses include the turning on and off of the auxiliary switch and additional conduction losses. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads when the switching losses of the main switch are eliminated. These switching losses - especially the IGBT current tail losses - are greater than the auxiliary circuit losses.

Ideally, the auxiliary circuit used to achieve ZCS operation in a ZCS-PWM converter should be activated only when the converter is operating with heavier loads and not used when the converter is operating with lighter loads. The proposed converters operate in such a manner and would ensure the optimal efficiency profile over the entire load range. Also, they operate for a short period of time which leads to reduction of the conduction losses and the ability to operate with higher power.

The operation of novel interleaved ZCS-PWM boost, buck, and multiport converters that can be used in industrial applications is discussed. Afterwards, based on a mathematical analysis of the proposed converters under steady-stage conditions, a procedure for the proper design of each converter is presented and is then used to design a proof-of-concept prototype. The feasibility of the converters proposed in this thesis is confirmed by computer simulation and by experimental results obtained from a proof-of-concept prototype. Finally, after a summary of the contents of this thesis, the conclusions and the contributions of this thesis are stated and suggestions for future work are made.

Keywords

Switch mode power supplies, ZCS PWM converters, Interleaved boost, buck, and multiport converters, soft switching,

Summary for Lay Audience

Power electronics is the field of electrical engineering related to the conversion of power from an input source to that required by an output load, using semiconductor devices and passive energy storage elements such as capacitors and inductors, and controllers. The input source can be renewable energy sources such as solar panels, wind turbines, fuel cell, batteries, or conventional technologies such as natural/diesel generators. The load can be a small cell phone, laptop, or large industrial loads such as motors, pumps, and batteries. The source voltage can be AC or DC with different voltage levels and the loads can be AC or DC as well so that power converters can be AC-AC, AC-DC, DC-AC, and DC-DC converters.

In order to shrink the size of the converters, they need to operate at high switching frequency to reduce the size of the passive energy storage elements. The semiconductor devices of a converter need to be turned on and off tens of thousand times per second, which results in high switching losses due to non-idealities. The main focus of this thesis is implementing zero-current-switching (ZCS) in multi-module converters with IGBT devices in a way that reduces cost and improves efficiency.

In this thesis, ZCS converters for various industrial applications such as for AC-DC power converters and power conversion in solar and wind energy based systems are proposed. Their steady-stage operation is analyzed mathematically and based on the analytical results, a design procedure is established for each converter. This procedure is then used to design a proof-of-concept experimental prototype for each proposed converter by selecting values for key components. Experimental results obtained from the proof-of-concept prototype confirm the feasibility of the proposed converters.

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I am happy to dedicate my thesis to my gorgeous nieces and nephew, Negin, Parsa, and Roya.

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Acronyms

AC	Alternative Current
BJT	Bipolar Junction Transistor
ССМ	Continuous Current Mode
DC	Direct Current
DCM	Discontinuous Current Mode
EMI	Electromagnetic Interference
ESS	Energy Storage System
FC	Fuel Cell
HDER	Hybrid Optimization of Multiple Energy Resources
HOMER	Hybrid Distributed Energy Resources
IGBT	Insulated Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NZEB	Net Zero Energy Buildings
PCS	Power Conversion System
PEMFC	Proton Exchange Membrane Fuel Cell
PFC	Power Factor Correction
PV	Photovoltaic

PWM	Pulse Width Modulation
RMS	Root Mean Square
SOC	State of Charge
THD	Total Harmonic Distortion
WE	Wind Energy
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Abbreviations

Co	Output Capacitor
Cr	Resonant Capacitor
D	Duty Cycle
D ₁	Main Diode 1
D ₂	Main Diode 2
D ₃	Main Diode 2
D _{a1}	Auxiliary Diode 1
D _{a2}	Auxiliary Diode 2
D _{a3}	Auxiliary Diode 3
D _{a4}	Auxiliary Diode 4
D _{a5}	Auxiliary Diode 5
D _{T1}	Auxiliary Transformer Diode 1
D _{T2}	Auxiliary Transformer Diode 2
f_{sw}	Switching Frequency
I _{in}	Input Current
Io	Output Current
L_1	Main Inductor 1

L ₂	Main Inductor 2
L ₃	Main Inductor 3
L _{r1}	Resonant Inductor 1
L _{r2}	Resonant Inductor 2
Ro	Output Resistive Load
R ₁	Relay 1
R ₂	Relay 2
S ₁	Main Switch 1
S_2	Main Switch 2
S ₃	Main Switch 3
Sa	Auxiliary Switch
Ta	Auxiliary Transformer
t	Time
V _{ac}	AC Voltage
V _{dc}	DC Voltage
Vin	Input Voltage
Vo	Output DC Voltage
V_{rec}	Rectified AC Voltage

1 Introduction

1.1 General Introduction

The field of power electronics is concerned with the conversion of power from an input source to meet the requirements of an output load. This is done using semiconductor devices, passive energy storage elements such as capacitors and inductors, and controllers that generate gating signals to turn any active semiconductors on and off appropriately. Active semiconductors are operated as on/off switches as opposed to being partially on, as is the case with many conventional electronic circuits. The power source can be a DC source, such as solar cells, batteries, and fuel cells, or an AC source, such as a utility outlet, electric generator, or wind turbine. The power source will be either single-phase or three-phase depending on the application and frequency (frequency depends on the geographical region). For example, in North America the frequency is 60 Hz whereas Europe and many Asian countries use 50 Hz. The load can be AC or DC, with or without isolation, and single-phase or three-phase. In general, power electronics converters can be classified as being DC to DC, DC to AC, AC to DC, or AC to AC.

The following sections of this chapter will discuss the technical background of this thesis and present a literature review of its main topic.

1.2 Semiconductor Devices

Semiconductor devices, such as transistors and diodes, are an important part of any power electronic converter. They can be classified into uncontrollable and controllable devices, as shown in Fig. 1.1. A diode is an uncontrollable semiconductor device that is turned on and conducts current when it is forward biased and is turned off when it is reverse biased. Bipolar Junction Transistors (BJTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs) are the most common controllable semiconductors.



Fig. 1.1. Different types of semiconductor devices

IGBTs and MOSFETs are the devices of choice for high switching frequency power converters. Diodes, MOSFETs, and IGBTs are explained in more detail in the following subsections.

1.2.1 Diodes

Figure 1.2 shows a diode and its current and voltage characteristics. A diode consists of an anode and a cathode, and current i_d flows through the device in a positive direction when the diode is forward biased, as shown in Fig. 1.2.a. When the voltage across the diode, V_d , is negative, however, it is reverse-biased, and does not conduct current. A diode is, therefore, a unidirectional current device as current can flow only in one direction, from the anode to the cathode. Fig. 1.2.b and Fig. 1.2c show representations of the actual and ideal characteristics of a diode, respectively.

As can be seen from Fig. 1.2.c, an ideal diode does not conduct any negative current; however, as shown in Fig. 1.3, when the current through the diode falls to zero, it becomes negative for a short amount of time then reaches zero eventually. This negative current is called reverse recovery current, and its duration is defined as t_{rr} , which is equal to the time that the current takes to reach negative and return to zero.



Fig. 1.2. (a) Symbol of a diode; (b) actual i-v characteristic; (c) idealized i-v characteristic

From Fig. 1.3, it is clear that voltage and current overlap, and therefore the reverse recovery current causes power losses in the diode during t_{rr} . The other drawback of reverse recovery in a power electronic circuit is electromagnetic interference (EMI), which is caused by very high frequency harmonic reverse-recovery frequency components that are propagated and that can affect the operation of the converter itself and of sensitive electrical equipment close-by. Increasing switching frequency decreases the size of passive energy storage elements and increases reverse-recovery losses, thus, power electronic engineers use fast recovery diodes that have a short t_{rr} .



Fig. 1.3. Reverse recovery current of a diode

1.2.2 MOSFETs

The metal oxide field effect transistor (MOSFET) is one of the most common types of power semiconductor devices that are used as switches in power converters. MOSFETs have three terminals: gate (G), source (S) and drain (D), as shown in Fig. 1.4. MOSFETs are the best choice for lower power, high switching frequency applications (> 100 kHz) for several reasons. First, their switching speed is fast; second, their on-state losses are low when operating with low drain-source voltage; third, just a small voltage is needed to initiate the on/off transition of the forward current (i_{DS}) in MOSFETs because of its high impedance gate. Although MOSFETs are controllable semiconductor devices with the ability to block positive drain-source voltage (V_{DS}), they cannot block negative V_{DS} because they have an intrinsic anti-parallel diode. The voltage between the gate and source (V_{GS}) should be approximately greater than 4 V to conduct current. This voltage is called the threshold voltage, and MOSFETs are considered open circuits for voltages less than this value. By maintaining the gate voltage at a higher value (close to 10 V), MOSFETs can conduct drain current (i_D) and are considered to be on. During an on-state, a real MOSFET has a small resistance between the drain and source ($R_{DS(on)}$) that leads to conduction losses in the device. This conduction loss is one of the main reasons why MOSFETs are not the best choice for high power applications.



Fig. 1.4. Circuit symbol of an N-Channel power MOSFET

1.2.3 IGBTs

The insulated gate bipolar transistor (IGBT) is a combination of a MOSFET and a BJT. Its on-state is similar to that of a BJT, whereas its gate is like that of a MOSFET. This device consists of three terminals: a gate (G), an emitter (E) and a collector (C). In Fig. 1.5, a

circuit symbol of an IGBT is shown. Unlike a MOSFET, an IGBT may or may not have an anti-parallel body diode.

Conduction losses in MOSFETs increase as the amount of current i_D increases, whereas those in BJTs are fixed; thus, for higher power applications, BJTs have lower conduction losses than MOSFETs. BJTs are slower than MOSFETs, however, because they require continuous base current to operate, and since IGBTs share some characteristics with BJTs, they are also slower than MOSFETs. IGBTs turn off more slowly than MOSFETs because they have a current tail due to being minority carrier devices. This means that electrons must be removed from these devices before they are turned off, causing a significant overlap of voltage and current during this switching transition. Switching losses of IGBTs are higher than those of MOSFETs, but IGBTs are preferred over MOSFETs for higher power, lower switching frequency applications (< 100 kHz).



Fig. 1.5. Circuit symbol of an IGBT with an anti- parallel diode

1.3 Reasons for High Switching Frequency Operation

The main energy storage components in converters include capacitors, inductors, and transformers. Usually, the size and weight of a converter depends on its energy storage components, which are necessary for storing and transferring energy. The size of the energy storage elements can be decreased by increasing the switching frequency of the converter. Smaller capacitors and inductors can store enough voltage and current, respectively, for a short amount of time, which leads to a lighter and smaller converter. As a result, one of the

advantages of increasing the switching frequency is reducing the overall size and weight of the converter.

In ideal switches, there is no overlap between current and voltage during turn-on and turnoff switching transitions, thus there is no power loss. In real switches, current and voltage overlap, as shown in Fig. 1.6, which leads to power losses. In Fig. 1.6, I_{sw} and V_{sw} are defined as being the current through and the voltage across the switch respectively. It can be seen from Fig. 1.6 that in an actual switch, current and voltage overlap during the switching transition from on to off and vice versa. As power losses due to switching transitions are related to the multiplication of current and voltage, increasing the switching frequency increases switching losses as well.



Fig. 1.6. Typical actual switch voltage and current waveforms

The dominant switching losses for a MOSFET occur while turning the switch on because its internal drain-source capacitance stores energy, which is dissipated in the device when it is turned on; therefore, there is an overlap between current and voltage until the capacitor is discharged completely. The main switching losses for an IGBT, however, occur while turning the switch off because it has a current tail, as shown in Fig. 1.7; thus, when the device is turned off, the current tail and the voltage overlap until the current tail goes to zero.



Fig. 1.7. Current tail in an IGBT

1.4 Soft Switching Techniques

Methods must be found to reduce losses when operating a converter with high switching frequency so that the size of power converters can be reduced without a significant drop in power conversion efficiency. This can be done by using soft-switching techniques that make switching transitions more gradual, or "soft". This is opposed to turning switches on and off suddenly, which is referred to as hard-switching in the power electronics literature. With these soft-switching techniques, either the voltage across or the current through a switch is zero during a switching transition. Since there is no overlap between the voltage across and the current through the switch, switching losses can be almost eliminated and EMI can be reduced significantly.

Soft switching techniques can be categorized into two main types: zero current switching (ZVS) and zero current switching (ZCS) methods. The ZVS principle of operation is based on forcing the voltage to zero just before turning the switch on or off and keeping it zero during the switching transition time. In industry, all MOSFETs and many kinds of IGBTs have an anti-parallel diode in their body that allows them to conduct current in the reverse direction. By having anti-parallel diodes, MOSFETs conduct current from the source to the drain and IGBTs from the emitter to the collector. MOSFETs and IGBTs with anti-parallel diodes can be turned on with ZVS by forcing current through the body diode just before the switch is turned on, maintaining the voltage across the switch at nearly zero during the switching transition. Also, when turning the switch off with ZVS, the rate of voltage rising across the switch should be decreased to restrict the overlap between voltage and current

during the switching transition time. This can be done by adding a capacitor in parallel with the switch, or by simply taking advantage of the internal drain-source capacitance of the device if it is a MOSFET and the switch current is low, as shown in Fig. 1.8.

On the other hand, ZCS can be achieved by forcing the current through the switch to zero just before the switch is turned on or off and maintaining it at zero during the switching transition. When turning a switch off with ZCS, current should be diverted from the switch just before the switching transition. The most common way to do this is to impose a negative voltage across the switch or in the current path of the switch. Also, when turning the switch on with ZCS, the rate of current rise through the switch should be reduced to limit the overlap between voltage and the current of the switch during the switching transition.



Fig. 1.8. Applying ZVS for MOSFET

On the other hand, because IGBTs have a tail current, they are used in high current and lower switching frequency applications as opposed to MOSFETs. Usually, the soft-switching technique that is used for IGBTs is ZCS (Fig. 1.9). It is worth noting that the most important switching losses for MOSFETs and IGBTs that should be eliminated are turn-on and turn-off losses, respectively. In this thesis, soft switching methods for IGBTs that use ZCS will be presented.



Fig. 1.9. Applying ZCS for IGBT

1.5 The Interleaved Converter Topology in DCM Mode

AC-DC converters are typically implemented with some sort of power factor correction (PFC) that shapes their input current so that it is sinusoidal and in phase with the input AC voltage. The most popular topology used in AC-DC converters with PFC is the AC-DC boost converter shown in Fig. 1.10.a, which can be operated in continuous current mode (CCM) with a continuous input current or in discontinuous current mode (DCM) with a discontinuous input current drops to zero before the end of a switching cycle). CCM operation results in less input current ripple than DCM operation, but is more difficult to implement. The output voltage is dependent on the ratio of the time that the switch is conducting over the time of the switching cycle, which is the inverse of the switching frequency, $T_S = \frac{1}{f_s}$. This ratio is called the duty cycle (D) and is defined as follows:

$$D = -\frac{T_{on}}{T_S} \tag{1-1}$$

Converters that can be controlled by varying their duty cycle are called pulse-width modulated (PWM) converters.

Interleaving techniques are often used in AC-DC converters to reduce the input current ripple of AC-DC boost converters operating with DCM. These techniques involve paralleling at least two DCM operated converters so that current is shared evenly among the converters. Fig. 1.10.b shows an interleaved boost converter that is formed by paralleling two AC-DC boost converter modules.



(a)



Fig. 1.10. Topology of a basic AC-DC converter (a) boost (b) interleaved boost

As shown in Fig. 1.10.b, a boost interleaved converter consists of two switches (S_1 and S_2), which are IGBTs in this thesis. These switches need a periodic pulse or gating signal that should be applied between their gate and emitter terminals to turn them on and off periodically. Additional converter components include two inductors (L_1 , L_2) and two diodes (D_1 , D_2) that are connected to a common filter capacitor (C_0). Each inductor carries half the current of an inductor in a conventional boost converter. If the switches are made to operate 180° out of phase, the ripple currents of the inductors overlap in a way that decreases the ripple of the overall input current, which results in less input filtering being

needed. Although there are multiple input inductors, their overall size can be less than the size of a single input inductor in a standard single-module AC-DC boost converter. The effective switching frequency is doubled as well, so that the peak-to-peak variation in the output capacitor current is also reduced, which allows a smaller filter capacitor to be used in comparison with that in a single boost converter with the same output voltage ripple. With smaller inductors and capacitor, the price and size of the inductors and capacitor can be decreased significantly. There is also less current stress on the converter components as they handle a fraction of the overall current.

Operating an interleaved boost converter in DCM also allows switches to be turned on with ZCS since there is no current flowing in the circuit at the start of a switching cycle. Reverse-recovery losses of the diodes are eliminated as their current falls to zero before the end of a switching cycle, and smaller inductances can also be used. Switches still have turn-off losses, however, and these should be reduced by using a soft-switching method. Inductor current waveforms are shown in Fig. 1.11.a for a DCM switching pattern for $D \ge 0.5$, and Fig. 1.11.b for D < 0.5.

As can be seen from Fig. 1.11, inductor current ripple is reduced by using interleaving. Since an AC input source is comparable to a DC input source during a very short switching cycle, different equations such as voltage gain can be derived by assuming the input source is DC. In the following equations, DT and D_1T are defined as the switching on-time and the time period in which the phase current becomes zero after DT, respectively:

$$\frac{di_{L1,2}}{d_t} = -\frac{V_{in}}{L_{1,2}} \qquad \text{(rising slope)} \tag{1-2}$$

$$\frac{di_{L1,2}}{d_t} = -\frac{V_{in} - V_{out}}{L_{1,2}} = -\frac{D V_{in}}{L_{1,2} D_1} \quad \text{(falling slope)}$$
(1-3)

The voltage gain of the interleaved boost converter is obtained as follows:

$$\frac{V_{out}}{V_{in}} = \frac{D+D_1}{D_1} \tag{1-4}$$

As discussed before, half of the input current flows from each boost converter. Thus, the average diode current can be expressed as:

$$I_{D1,2} = \frac{1}{2} \left(\frac{V_{in} DT}{L_{1,2}} \right) D_1 = \frac{1}{2} \frac{V_{out}}{R}$$
(1-5)

Rearranging this equation results in:

$$D_1 = \left(\frac{V_{out}}{V_{in}}\right) \frac{L}{RDT} \tag{1-6}$$

Substituting equ. (1-6) into equ. (1-4) results in:

$$\left(\frac{V_{out}}{V_{in}}\right)^2 - \left(\frac{V_{out}}{V_{in}}\right) - \frac{D^2 RT}{L_{1,2}} = 0$$
(1-7)

ZCS can be performed in interleaved converters by using additional circuitry that is not a part of the main power circuit. For such converters, which are often referred to as resonant-transition converters in the literature, the auxiliary switch operates only for a small portion of the switching cycle. Before turning each main switch off, the auxiliary switch is turned on which makes a capacitor in the auxiliary circuit undergo resonance with the auxiliary inductors. By resonating this capacitor, a negative voltage is imposed across the auxiliary inductor-switch, so the currents of the main switches are forced to be reduced to zero before the pulses at the gates of the main switches are removed; therefore, the main switches can be turned off with ZCS. In the next section, several ZCS methods that have been presented in the literature are reviewed.



(a)



Fig. 1.11. Inductor current waveforms according to the switching pattern in the DCM

1.6 Literature Review

PWM converters that consist of two or more interleaved boost/buck converter modules are used widely in industry [1-13]. As discussed previously, soft-switching approaches for these converters can either be zero-voltage switching (ZVS) if implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. The main idea of this thesis is to implement ZCS for IGBT turn-on and turn-off transitions. Most converters use an auxiliary circuit that is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can be turned off with ZCS.

ZCS methods in boost or buck converters have at least one of the following drawbacks [14-51]:

- a) Each module of a boost/buck converter must have its own auxiliary circuit to help its main switch turn off with ZCS, instead of using just one active auxiliary circuit for both main switches. This adds cost to the overall converter.
- b) Auxiliary circuit components must be placed in the main part of the converter. With more components in the main path of the current, conduction losses are increased, and the auxiliary circuit components need to have higher current ratings.
- c) The auxiliary circuit injects current into the main switches, which increases peak and RMS current stresses, as is typical of resonant-type auxiliary circuits. This creates a need for a higher rated device for the main switch and increases conduction losses that can offset any gain in efficiency caused by the reduction of switching losses.
- d) The auxiliary switch does not operate with ZCS but operates with hard switching instead.
- e) Generally, in any ZCS-PWM converter, the auxiliary circuit causes the light-load efficiency of the converter to decrease, as it produces more losses than it saves for light loads. Any active auxiliary circuits that are used to reduce switching losses

are effective when the converter is operating with heavy-loads so there is current in the converter to create losses. They are less effective when the converter is operating with light-loads, as there is little current in the converter, thus few current-related losses. These active auxiliary circuits cannot be disengaged from the converter.

- f) Energy pumped into the auxiliary circuit when it is activated, from the main converter circuit, is trapped in the auxiliary circuit where it is dissipated. There is no path for some of this energy to be transferred to the output.
- g) The auxiliary circuit increases the voltage stress of the boost diode by a significant amount. This is especially true of resonant-type auxiliary circuits that present a negative voltage at the anode of the boost diode while active, which forces the peak voltage stress of the diode to be greater than the output voltage.
- h) For a two-module interleaved ZCS-PWM converter that has just a single active auxiliary circuit to help the main switches turn off with ZCS, the auxiliary switch in the circuit must be turned on and off twice during a switching cycle. This means that the switch operates with double the converter switching frequency as a result. If the switch needs to be on for a significant amount of time, then turning it on twice during a switching cycle increases both the RMS current stress of the auxiliary switch and the auxiliary circuit losses. If an auxiliary switch is to be implemented with a device that is cheaper and that has better switching characteristics than that used for the main switches, the power rating of the converter must be limited so that the auxiliary switch can handle the power in the auxiliary circuit.

These drawbacks will now be explained in more detail with reference to several sample papers.

ZCS-PWM converters that use an auxiliary circuit to help the main converter switch turn on with ZCS are generally less efficient than hard switching converters at light loads. The main reason for this is that the auxiliary circuit losses dominate when the converter is operating under these conditions. Auxiliary circuit losses include the turning on and off of the auxiliary switch and additional conduction losses, as there can be an increased amount of circulating current flowing in the converter. ZCS-PWM converters achieve their improved efficiency over hard switching converters at heavier loads when the switching losses of the main switch are eliminated. These switching losses, especially the IGBT current tail losses, are greater than the auxiliary circuit losses.

Ideally, the auxiliary circuit used to achieve ZCS operation in a ZCS-PWM converter should be activated only when the converter is operating with heavier loads and deactivated when the converter is operating with lighter loads. Operating the converter in such a manner would ensure the optimal efficiency profile over the entire load range. This, however, generally cannot be done with ZCS-PWM converters because of the presence of an inductor placed in series with the main switch. As can be seen in the example converters shown in Fig. 1.12 and Fig. 1.13, an inductor is typically placed in series with the main switch so that it can turn on with ZCS.



Fig. 1.12. ZCS boost converter proposed in [48]


Fig. 1.13. ZCS boost converter proposed in [49]

The series inductor slows down the rate of current rising after the switch has been turned on so that the overlap between the voltage and the current in the switch is reduced.

Although the presence of this series inductor in a ZCS-PWM converter is beneficial, it prevents the auxiliary circuit from being disengaged from the main circuitry when the converter is operating under light load conditions. As long as the series inductor is in the converter, the auxiliary circuit must be used at all times, across the full load range, even when it is not necessary under light load conditions because failure to do so would result in damage of the main switch. Given the size of the series inductance, which may be relatively small compared to that of the input boost inductor, but not insignificant, the energy stored in this inductor would result in the appearance of high voltage spikes across the switch when it is turned off, as there would be no path for current to flow.

There are several possible solutions to the problem of having an inductor in series with the main switch, but none of them are truly satisfactory. It may be possible to place a bypass switch of some sort across the series inductor so that when the auxiliary circuit is not needed, the bypass switch could be turned on and current would bypass the main switch. This, however, would add cost and make the converter more complex.

Another possible solution is to implement the converter with an active auxiliary circuit and a passive snubber. With such a scheme, the active auxiliary circuit would be activated only when the converter is operating with heavier loads. The passive snubber would be used to deal with the series inductor's energy when the main converter switch is turned off while the auxiliary circuit is disengaged from the main circuit. This approach would again increase the cost and the complexity of the converter.

If the main switch could be made to turn on with ZCS without having an inductor in series with it, then it would be possible to avoid using the auxiliary circuit when the converter is operating under light load conditions. This is, in fact, possible when the converter is operating with a discontinuous input inductor current. In such a case, the main converter switch would turn on with ZCS, as initially there would be no current flowing through the switch. Current through the switch would rise gradually, due to the size of the input boost inductor.

As shown above, an interleaved boost converter can be implemented with two converter modules in parallel operating with DCM and the modules are interleaved with a phase difference of 180° from each other. In the ZCS scheme being described, if the individual converter modules are ZCS-PWM converters, then it would be possible to disengage the auxiliary circuit from the main circuit, as there would be no need for a series inductance to help the main switch turn on with ZCS.

Papers discussing this method include [17] and [40] and the topologies are shown in Fig. 1.14 and Fig. 1.15, respectively. The main drawback is that each module of the proposed interleaved boost/buck converter must have its own ZCS auxiliary circuit to help its main switch turn off with ZCS. Since two switches would be used, the price and complexity of the converter is increased. Another disadvantage of the topology in [17] is that the converter, in the absence of a high-voltage conversion ratio, does not have an appropriate ZCS. The next problem is that each auxiliary switch should not be turned off immediately after turning its corresponding main switch off. This means both auxiliary switches need some time after turning their main switches off to be turned off with ZCS, increasing conduction losses.



Fig. 1.14. Interleaved ZCS boost converter proposed in [17]



Fig. 1.15. Interleaved ZCS buck converter proposed in [40]

In the auxiliary circuit proposed in [50] and shown in Fig. 1.16, the main switches are turned on and off with soft switching, but the resonant switch operates with hard-switching. Although the auxiliary switch in the circuit shown in Fig. 1.17 [41] operates with soft switching, the auxiliary circuit causes the auxiliary switch to operate with a considerably higher peak voltage stress than the main switches, which creates a need for a higher rated device for the auxiliary switch.



Fig. 1.16. Interleaved ZCS boost converter proposed in [50]



Fig. 1.17. Interleaved ZCS buck converter proposed in [41]

The authors in [18] used two inductors in series with the input inductors, shown in Fig. 1.18. Since the auxiliary inductors are in the path of the main power circuit, the voltages across the main switches and diodes are higher than the output voltage. The voltage across the auxiliary switch is almost two times that of the output voltage.

In the converter proposed in [36], shown in Fig. 1.19, an inductor is in series with the main switch. This doubles the voltage across the main diode so that a more expensive device with a higher rating is needed, thus increasing the cost of the converter.



Fig. 1.18. Interleaved ZCS boost converter proposed in [18]



Fig. 1.19. Interleaved ZCS buck converter proposed in [36]

In ZCS-PWM converters such as those shown in Fig. 1.20 and Fig. 1.21 [21], current must be gradually diverted away from the main switch in order for it to turn off with ZCS. If the transfer is performed too quickly, the main IGBT switch device will not have a soft turnoff due to residual charge in the device. The auxiliary switch must conduct at least the full inductor current for a minimum of 2-3 μ s. If the auxiliary switch is used twice during a switching cycle, as is the case when only one auxiliary circuit is used in an interleaved buck converter, then the RMS current stress of this switch will be high, thereby increasing conduction losses. The operation of the auxiliary circuit increases the voltage stress of the main diodes as well.



Fig. 1.20. Interleaved ZCS boost converter proposed in [21]



Fig. 1.21. Interleaved ZCS buck converter proposed in [21]

Ideally, the auxiliary circuit used to achieve ZCS operation in a ZCS-PWM converter should be activated only when the converter is operating with heavier loads and not used when the converter is operating with light loads to improve the efficiency. This, however, generally cannot be done with ZCS-PWM converters because of the presence of auxiliary circuitry in the path of the main switch. Such a topology can be seen in Fig. 1.22 and Fig. 1.23.



Fig. 1.22. Interleaved ZCS boost converter proposed in [23]



Fig. 1.23. ZCS buck converter proposed in [42]

1.7 Thesis Objectives

The main objectives of this thesis are as follows:

- To propose a novel interleaved ZCS-PWM converter that does not have any of the drawbacks mentioned in the previous section, without adding any new components in the main power path.
- To implement this converter and its topological variations in various industrial applications, including for AC-DC applications and renewable energy applications.
- To analyze the steady-state characteristics of the proposed converter by mathematical analysis so that its properties can be understood.
- To derive a design procedure for the new interleaved converter that can be used for selecting the proper components based on the results of the mathematical analysis.
- To confirm the feasibility of the converter proposed in this thesis using computer simulation and experimental results obtained from a proof-of-concept prototype.

1.8 Thesis Outline

The thesis is organized as follows:

- In Chapter 2, a new interleaved PWM boost converter that has a single auxiliary switch that allows all the converter switches to operate with ZCS will be introduced, its modes of operation will be explained, and its features will be described. In this chapter, the operation of the proposed converter will be explained in detail and a mathematical analysis of its steady-state operation will be performed. Based on the mathematical analysis, a set of steady-state characteristic curves that can be used in the design of the converter will be generated and will be used to derive design curves. The operation of the converter will be confirmed with simulation and experimental results.
- In Chapter 3, a novel AC-DC interleaved ZCS-PWM boost converter with reduced auxiliary switch RMS current stress that has an auxiliary transformer and a single auxiliary switch to perform ZCS for all switches will be presented. In this chapter,

the operation of the proposed converter is explained in detail and mathematical equations are derived for steady-state operation. Based on the equations, design curves will be generated using MATLAB and used to design the converter. The feasibility of the converter will be confirmed by experimental results obtained from a proof-of-concept prototype.

- In Chapter 4, a novel ZCS PWM buck converter with improved light-power efficiency in a wind power system is presented. The operation of the proposed converter is explained in detail, then experimental results will be shown to confirm the feasibility of the converter. To demonstrate how the proposed converter's ability to disengage its auxiliary circuit at light loads can save energy, a small wind turbine is modelled using HOMER software. Based on the simulation results, the energy that can be saved by using the proposed converter for the entire load range in a case study in Canada will be shown.
- In Chapter 5, the implementation of a DC nano grid with a new ZCS PWM multiport converter is presented. A variety of configurations of the proposed converter will be shown. The modes of operation for the worst-case scenario of operating conditions will be presented and general equations related to soft switching will be derived. Experimental results will be shown to confirm the feasibility of the converter when all the ports supply the load.
- In Chapter 6, the content of this thesis will be summarized and the conclusions of the thesis will be stated, along with the main contributions of this thesis and suggestions for future work.

2 A novel AC-DC interleaved ZCS-PWM boost converter

2.1 Introduction

As stated in the previous chapter, AC-DC converters that operate with input power factor correction (PFC) and consist of two or more interleaved boost converter modules are popular in industry [1-13]. PFC is required in modern AC-DC converters as their input current must meet harmonic standards set by regulatory agencies. With interleaving, the input current of each module can be made to be discontinuous, and the size of their input inductors reduced. Interleaving can reduce the high ripple in each module and produce a net input current with a ripple that is comparable to that achieved by a single boost converter module with a large input inductor. Moreover, there is less current stress on the converter components because they each handle a fraction of the overall current and the control is easier as the more sophisticated control methods required for continuous current mode (CCM) operation are avoided.

In the first chapter it was shown that the soft-switching methods for these converters should be zero-current switching (ZCS) if they are implemented with IGBTs. Previously proposed methods for interleaved boost converters have at least one of the drawbacks (a-h) that were discussed in the beginning of the literature review, in Section 1-6.

The interleaved AC-DC boost converter that is proposed in this chapter uses a single active auxiliary circuit that assists all of the main converter switches to operate with ZCS and operates with ZCS itself. This circuit does not increase the peak voltage or current stresses of the main switches and can be deactivated from the main power circuit if necessary to improve the efficiency for the entire load range. In this chapter, the operation of the converter is fully explained, its features are discussed, and guidelines for the design of key auxiliary circuit components are given. Results obtained from an experimental prototype are presented to confirm the feasibility of the proposed converter.

2.2 General Converter Principles and Modes of Operations

The proposed AC-DC converter, shown in Fig. 2.1, consists of two boost converter modules: one with L_1 , S_1 and D_1 , the other with L_2 , S_2 and D_2 . The gating signals of the two main switches, S_1 and S_2 are identical, but shifted 180° out of phase with each other.

The currents in L₁ and L₂ are discontinuous and identical, but also shifted 180° with respect



Fig. 2.1. Proposed interleaved AC-DC ZCS-PWM boost converter [19]

to each other. The two boost modules are connected to the same auxiliary circuit which consists of connection diodes D_{a1} and D_{a2} , reverse blocking diode D_{a3} , switch voltage clamping diode D_{a4} , inductors L_{r1} and L_{r2} and capacitor C_{r1} . The auxiliary circuit is activated whenever one of the two main switches is about to be turned off and is active for only a fraction of the switching cycle.

The modes of operation are studied for the case when the converter is operating in steadystate, which can be defined as the converter components having the same voltage and current at the end of a switching cycle (and the start of a new one) as they have at the start of the cycle. In other words, the voltage and current waveforms of all components of the proposed interleaved converter should be identical for every switching cycle when the converter is operating in steady-state.

The proposed converter has the following modes of operation for a half switching cycle when the duty cycle is $D \ge 0.5$ and when S_2 is turned on and S_1 is turned off. Typical converter waveforms are shown in Figs. 2.3 to 2.9 and circuit diagrams for these modes are shown in Fig. 2.4. The modes of operation for the other half-cycle when S_1 is turned on and S_2 is turned off are identical.



Fig. 2.2. Typical waveforms of the proposed converter

<u>Mode 1 ($T_0 < t < T_1$)</u>: This mode begins when switch S₂ is turned on. The rectified voltage is applied to L₂ and the current through L₂ linearly increases, as does the input current in the input inductor (I_{in}). The slope of the current is $\frac{V_{in}}{L_2}$. Since I_{in} is the summation of I_{L1} and I_{L2}, it will increase with greater slope.

<u>Mode 2 ($T_1 < t < T_2$)</u>: This mode begins when the auxiliary switch (S_a) is turned on in preparation to turn off main switch S_1 with ZCS. S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases.

<u>Mode 3 ($T_2 < t < T_3$)</u>: This mode begins when the voltage across C_r (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. The voltage across D₁ and D₂ is limited to the output voltage. The current through L_{r1} increases, thus I_{L1} and I_{L2} flow through L_{r1}. The current in L₂ is less than L₁, thus the current through S₁ becomes zero and S₁ can be turned off with ZCS. The current through S₂ becomes negative and flows through its body diode.

<u>Mode 4 ($T_3 < t < T_4$)</u>: This mode begins when the current in L_{r2} reaches zero because of its resonance with C_r . S_a can then be turned off with ZCS conditions. During this mode, energy in L_{r1} is transferred to C_r , thus increasing its voltage so that V_{Cr} becomes less negative and is in the process of eventually becoming positive.

<u>Mode 5 ($T_4 < t < T_5$)</u>: This mode begins when the net voltage across the C_r and L_{r1} becomes positive thus, auxiliary diode D_{a2} stops conducting and I_{L2} flows through S₂. D_{a1} continues to conduct during this mode.

<u>Mode 6 ($T_5 < t < T_6$)</u>: This mode begins when V_{Cr} reaches the output voltage (V_o). D₄ clamps the voltage across the auxiliary switch to V_o and the stored energy in L_{r1} is transferred to the output so that the current in L_{r1} decreases. When the current through L_{r1} becomes less than I_{L1}, diode D₁ starts to carry the current difference. The voltage across L₁ becomes V_o-V_{rec} and the current through L₁ starts to decrease linearly.

<u>*Mode* 7 ($T_6 < t < T_7$)</u>: This mode begins when the current in L₁ reaches zero. This is the last mode of the half-cycle. The next half-cycle begins when S₁ is turned on under ZCS.



Fig. 2.3. Current flow in Mode 1







Fig. 2.5. Current flow in Mode 3







Fig. 2.7. Current flow in Mode 5









2.3 Circuit Analysis

Mathematical equations of each mode in steady-state must be derived to determine the effect of the proposed auxiliary circuit on each component. These equations can be used to determine the parameters that should be met to satisfy the ZCS conditions. Thus, characteristic behaviors of different components are specified to use in design analysis. It should be noted that, during most time intervals, the proposed interleaved converter operates like that of a conventional interleaved converter, so only the equations for the time in which the auxiliary circuit operates will be derived.

The analysis in this chapter is done with $D \ge 0.5$, S_2 turned on, and S_1 turned off; the analysis and formulas for the other half-cycle when S_1 is turned on and S_2 is turned off is identical. In Mode 1, shown in Fig. 2.3, when switch S_2 is turned on, the rectified voltage is applied to L_2 , leading to a gradual increase of the current through L_2 and the input current in the input inductor (I_{in}). The slope of L_2 , which is equal to the slope of S_2 , rises according to

$$V_{in} = L_2 \frac{dIL_2(t)}{dt}$$
(2-1)

By integrating from time T_0 to T_1 , the main switch current can be expressed as

$$I_{S2}(t) = \frac{V_{in}}{L_2} (T_1 - T_0)$$
(2-2)

All the input current goes through S_1 and S_2 so that

$$I_{in} = I_{S1} + I_{S2} \tag{2-3}$$

The next mode begins when the auxiliary switch (S_a) is turned on in preparation for the ZCS turn-off of main switch S_1 . The equivalent circuit diagram at time T_2 is shown in Fig. 2.4.

By applying KVL, the following equation can be obtained:

$$V_{Cr}(t) = L_{r2} \frac{d}{dt} i_2(t)$$
 (2-4)

By applying KCL, the following equation can be obtained:

$$i_{Lr2}(t) = i_{Cr}(t) = -\frac{d}{dt} q_{Cr}(t) = -C_r \frac{d}{dt} V_{Cr}(t)$$
(2-5)

By substituting equ. (2-5) into equ. (2-4), the following result can be obtained:

$$V_{Cr}(t) = -L_{r2} C_r \frac{d^2}{dt^2} V_{Cr}(t)$$
(2-6)

In order to solve the above-mentioned equations, the initial capacitor voltage ($V_{cr}(0)$) and the initial auxiliary inductor current ($i_{Lr2}(0)$) should be defined. $V_{cr}(0)$ is assumed to be equal to V_o and $i_{Lr2}(0)$ is equal to zero in this mode. As a result, the derivative of the capacitor voltage ($dV_{cr}(0)/dt$) can be determined to be

$$\begin{bmatrix} \frac{d}{dt} V_{Cr}(t) \end{bmatrix}_{t=0} = -\left(\frac{1}{C_r}\right) \begin{bmatrix} \frac{d}{dt} q_{Cr}(t) \end{bmatrix}_{t=0} = \left(\frac{1}{C_r}\right) \begin{bmatrix} i_{Lr2}(t) \end{bmatrix}_{t=0}$$

$$= 0$$
(2-7)

By substituting equ. (2-7) into equ. (2-6), the following can be obtained:

$$V_{Cr}(t) = V_0 \cos \omega_2 t \text{ for } T_1 < t < T_2$$
 (2-8)

Based on the initial conditions of this mode, the following equation can be written:

$$i_{Lr2}(t) = i_{Cr}(t) = -C_r \frac{d}{dt} V_{Cr}(t) = C_r V_o \omega_2 \sin \omega_2 t$$
 (2-9)

$$= \frac{v_o}{z_2} \sin \omega_2 t \qquad \qquad \text{for} \quad T_1 < t < T_2$$

In the above equation, $\omega_2 = \frac{1}{\sqrt{L_{r2}C_r}}$ and the characteristic impedance of the auxiliary circuit is defined as $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$. Mode 2 is finished when the voltage of the auxiliary capacitor V_{cr} reaches zero; therefore, the duration of this mode can be calculated by making equ. (2-8), equal to zero as follows:

$$V_{Cr}(t) = V_0 \cos \omega_2 t = 0$$
 for $t = T_2$ (2-10)

where

$$\omega_2 t = \frac{\pi}{2}$$

Thus, the current at $t=T_2$, which is the time in which the maximum current flows through the auxiliary circuit, can be determined to be

$$i_{Lr2}(t) = i_{Lr2}(T_2) = \frac{V_o}{Z_2} \sin \omega_2 t$$
 (2-11)

$$i_{Lr2}(T_2) = \frac{V_0}{Z_2} \qquad \qquad \text{for } t = T_2$$

The next mode begins when the voltage across the resonant capacitor is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} begin to conduct. In Mode 3, shown in Fig. 2.5, current through the main switch S_1 and auxiliary switch S_a should go to zero or negative before turning them off so that ZCS conditions are met.

It can be seen from Fig. 2.5 that

$$i_{Lr1}(t) = i_{Lr2}(t) + i_{Cr}(t)$$
(2-12)

Initial conditions for Mode 3, which should be derived from the previous mode, show that the initial value of the voltage across the auxiliary capacitor (V_{Cr} (t_2)) and the current through the auxiliary inductor (i_{Lr1} (t_2)) are zero. Meanwhile, the initial current through the second auxiliary inductor (i_{Lr2} (t_2)) in this mode is equal to

$$i_{Lr2}(T_2) = \frac{V_o}{Z_2}$$
(2-13)

Since D_{a3} is conducting, the voltage across auxiliary circuit inductor L_{r2} is

$$V_{Lr2} = V_{Cr} \tag{2-14}$$

Since D_{a2} is conducting, the voltage across auxiliary circuit inductor L_{r1} is

$$V_{Lr1} = -V_{Lr2} = -V_{Cr} (2-15)$$

By differentiating equ. (2-12) with respect to time, the following equation is obtained:

$$\frac{d}{dt}i_{Lr1}(t) = \frac{d}{dt}i_{Lr2}(t) + \frac{d}{dt}i_{Cr}(t)$$
(2-16a)

This can be rewritten as

$$\frac{V_{Lr1}}{L_{r1}}(t) = \frac{V_{Lr2}}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t)$$
(2-16b)

By substituting equ. (2-15) into equ. (2-16b), the following result is obtained:

$$\frac{V_{Cr}}{L_{r1}}(t) + \frac{V_{Cr}}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$
(2-16c)

This can be rewritten as

$$\frac{V_{Cr}}{L_{r1}}(t)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r2}}(t)\frac{L_{r1}}{L_{r1}} + C_r\frac{d^2}{dt^2}V_{Cr}(t) = 0$$

$$\frac{V_{Cr}(L_{r1}+L_{r2})}{L_{r1}L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$

By defining $L_{eq} = \frac{L_{r_1}L_{r_2}}{L_{r_1}+L_{r_2}}$, equ. (2-16c) can be simplified to be

$$\frac{V_{Cr}}{L_{eq}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$
(2-16d)

This is equal to

$$\frac{V_{Cr}}{L_{eq}}(t) = -C_r \frac{d^2}{dt^2} V_{Cr}(t)$$
(2-16e)

which can be rearranged to be

$$\frac{V_{Cr}}{L_{eq}C_r}(t) = -\frac{d^2}{dt^2} V_{Cr}(t)$$
(2-16f)

By defining $\omega_e = \frac{1}{\sqrt{L_{eq}C_r}}$ and substituting it into equ. (2-16f), the following equation can be obtained:

$$V_{Cr}(t)\omega_e^2 = -\frac{d^2}{dt^2}V_{Cr}(t)$$
(2-16g)

As mentioned previously, the initial voltage of the auxiliary capacitor is zero. The derivative of the initial magnitude of the auxiliary capacitor can be determined to be

$$\left[\frac{d}{dt}V_{Cr}(t)\right]_{t=0} = -\left(\frac{1}{C_r}\right)\left[\frac{d}{dt}q_{Cr}(t)\right]_{t=0} = -\left(\frac{1}{C_r}\right)\left[i_{Lr2}(t)\right]_{t=0}$$
(2-17)

Substituting equ. (2-13) into equ. (2-17) results in

$$\left[\frac{d}{dt}V_{Cr}(t)\right]_{t=0} = -\left(\frac{V_o}{Z_2C_r}\right)$$
(2-18)

Using equ. (2-16g), the voltage across capacitor Cr can be determined to be

$$V_{cr}(t) = -\left(\frac{V_o}{\sqrt{\left(1 + \frac{L_{r2}}{L_{r1}}\right)}}\right) \sin \omega_e t$$
(2-19)

$$V_{Lr1}(t) = -V_{Cr}(t) = -V_{Lr2}(t)$$
(2-20a)

Since the voltage across an inductor is related to the derivative of the current through it, this can be rewritten as

$$L_{r1}\frac{d}{dt}i_{Lr1}(t) = -L_{r2}\frac{d}{dt}i_{Lr2}(t)$$
(2-20b)

Substituting equ. (2-20a) into equ. (2-20b) results in

$$\frac{d}{dt}i_{Lr1}(t) = -\frac{V_{Cr}}{L_{r1}}(t)$$
(2-20c)

which can then be rewritten as

$$di_{Lr1}(t) = -\left(\frac{V_{Cr}}{L_{r1}}(t)\right)dt$$
(2-20d)

The above equation can be solved by integrating it during the interval of this mode of operation. The initial magnitude of the auxiliary inductor I_{Lr1} , which is equal to zero, can be derived from the previous mode as

$$i_{Lr1}(t) = \left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right) (1 - \cos \omega_e t)$$
(2-20e)

During this mode of operation, I_{S1} should go to zero or negative in order to meet the ZCS condition; thus, the direction of current through S_1 is changed and flows through its body diode. Based on Fig. 2.5, the following condition should be satisfied to ensure the soft switching of S_1

$$i_{in}(t) - i_{Lr1}(t) \le 0$$
 (2-21a)

This means that i_{Lr1} should be greater than $i_{in}(t)$. Substituting equ. (2-20e) into equ. (2-21a) results in

$$i_{in}(t) - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r1}} \right) (1 - \cos \omega_e t) \right] \le 0$$
(2-21b)

By applying KVL, the following expression can be written

$$V_{Cr}(t) = L_{r2} \frac{d}{dt} i_{Lr2}(t)$$
(2-22a)

which can be rewritten as

$$di_{Lr2}(t) = \left(\frac{V_{Cr}}{L_{r2}}(t)\right)dt$$
(2-22b)

Based on equ. (2-13), the initial current through the second auxiliary inductor in this mode is equal to $i_{Lr2}(T_2) = \frac{V_0}{Z_2}$. By substituting equ. (2-19) into equ. (2-22b), the current through L_{r2} can be determined to be

$$i_{Lr2}(t) = \frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}} \right) (1 - \cos \omega_e t) \right]$$
(2-22c)

The auxiliary switch (S_a) is turned on to help the main switches turn off with ZCS and should be turned off soon afterwards. At the end of this mode of operation, I_{Sa} should go to zero or become negative so that it turns off with ZCS as well. It can be seen from Fig. 2.5 that

$$I_{Sa}(t) = i_{Lr2}(t)$$
 (2-23)

In order to turn off the auxiliary switch (S_a) with ZCS, $i_{Lr2}(t)$ should be zero or negative; this can be expressed as

prerequisit of ZCS of
$$I_{Sa}$$
: $I_{Sa}(t) = i_{Lr2}(t) \le 0$ (2-24a)

Substituting equ. (2-22c) into equ. (2-24a) results in

$$\frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}} \right) (1 - \cos \omega_e t) \right] \le 0$$
(2-24b)

The voltage across the main diodes (V_{D1} and V_{D2}) can be derived based on the KVL in Fig. 2.5 to be

$$V_{D2} + V_o = 0 \tag{2-25}$$

$$V_{D1} - V_{Cr} - V_{Lr1} + V_o = 0 (2-26a)$$

Based on equ. (2-15) during this mode, $V_{Lr1} = -V_{Cr}$, so equ. (2-26a) can be rewritten as

$$V_{D1} + V_o = 0 (2-26b)$$

The above-mentioned equations show that, in this mode of operation, the voltage across each main boost diodes are equal to the output voltage. This is one of the advantages of this topology - that the maximum voltage across the main diodes is equal to the output voltage.

Based on equ. (2-24a), at the end of this mode i_{Lr2} should be zero or negative to turn off the auxiliary switch with ZCS. However, by using a blocking diode (D_{a3}) the negative current cannot flow through L_{r2} . The equations for the rest of the modes are not required to characterize the converter and are thus not presented.

It is worth noting that the maximum voltage across the auxiliary capacitor, which is achieved in Mode 6 (Fig.2.8) by the resonance among C_r , L_{r1} and L_{r2} when the capacitor voltage reaches to the output voltage should be determined.

The following equations can be written

$$i_{Lr1}(t) = i_{Lr2}(t) + i_{C}(t)$$
(2-27)

$$V_{Cr}(t) = V_o + L_{r2} \frac{d}{dt} i_{Lr2}(t)$$
(2-28)

$$V_{Cr}(t) = V_o - L_{r1} \frac{d}{dt} i_{Lr1}(t)$$
(2-29)

Differentiating equ. (2-27) with respect to time results in

$$\frac{d}{dt}i_{Lr1}(t) = \frac{d}{dt}i_{Lr2}(t) + \frac{d}{dt}i_{Cr}(t)$$
(2-30a)

which can be rewritten as

$$\frac{V_{Lr1}}{L_{r1}}(t) = \frac{V_{Lr2}}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t)$$
(2-30b)

Substituting equ. (2-28) and equ. (2-29) into equ. (2-30b) results in

$$\frac{V_{Cr} - V_o}{L_{r1}}(t) + \frac{V_{Cr} - V_o}{L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$
(2-30c)

which can be rewritten as

$$\frac{V_{Cr} - V_o}{L_{r1}}(t)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr} - V_o}{L_{r2}}(t)\frac{L_{r1}}{L_{r1}} + C_r \frac{d^2}{dt^2}V_{Cr}(t) = 0$$

$$\frac{(V_{Cr} - V_o)(L_{r1} + L_{r2})}{L_{r1}L_{r2}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$

By defining $L_{eq} = \frac{L_{r_1}L_{r_2}}{L_{r_1}+L_{r_2}}$, this can be simplified to:

$$\frac{V_{Cr} - V_o}{L_{eq}}(t) + C_r \frac{d^2}{dt^2} V_{Cr}(t) = 0$$
(2-30d)

This is equal to

$$\frac{V_{Cr} - V_o}{L_{eq}}(t) = -C_r \frac{d^2}{dt^2} V_{Cr}(t)$$
(2-30e)

Which can be rearranged as

$$\frac{V_{Cr} - V_o}{L_{eq}C_r}(t) = -\frac{d^2}{dt^2} V_{Cr}(t)$$
(2-30f)

By defining $\omega_e = \frac{1}{\sqrt{L_{eq}C_r}}$ and substituting it into equ. (2-30f), the following equation can be derived

$$(V_{Cr} - V_o)(t)\omega_e^2 = -\frac{d^2}{dt^2}V_{Cr}(t)$$
(2-30g)

Mode 6 begins when the voltage across the auxiliary reaches the output voltage, therefore the initial voltage of the auxiliary capacitor is equal to V_0 . The derivative of the initial magnitude of the auxiliary capacitor is determined to be

$$\left[\frac{d}{dt}V_{Cr}(t)\right]_{t=0} = \left(\frac{1}{C_r}\right)\left[i_{Lr1}(t)\right]_{t=0} = \left(\frac{1}{C_r}\right)\left[i_{L1}(t)\right]_{t=0}$$
(2-31)

Therefore, equal. (2-30g) can have the following solution:

$$V_{cr}(t) = i_{L1} Z_e \sin \omega_e t + V_o$$
(2-32)

where characteristic impedance is defined as $Z_e = \sqrt{\frac{L_{eq}}{c_r}}$. The following equation shows the time in which the voltage of the resonant capacitor reaches its maximum value at the start of this mode of operation:

$$\omega_e t = \frac{\pi}{2}$$

$$t = \frac{\pi}{2} \sqrt{L_{eq}C_r}$$
(2-33)

Thus, at the above time in Mode 6, V_{Cr} reaches its maximum value which is equal to

$$V_{cr}\left(\frac{\pi}{2}\sqrt{L_{eq}C_r}\right) = i_{L1}Z_e + V_o \tag{2-34}$$

During this mode of operation, current through the input inductor L_{r1} decreases based on the following equation:

$$\frac{d}{dt}i_{L1} = \frac{V_{in} - V_o}{L_1}$$
(2-37)

Since the input inductor current of each converter is discontinuous, this mode ends when i_{L1} at T_5 reaches zero:

$$V_{cr}(\mathbf{T}_5) = V_o \tag{2-38}$$

The last mode of the half cycle is like that of the conventional boost converter so equations for this mode are not required to characterize the converter and are not presented. It should be noted that the equations for the other half-cycle, when S_1 is turned on and S_2 is turned off, are identical.

2.4 Design Procedure and Example

All the analysis and equations that have been presented in the previous section have been derived from a DC input voltage, because an AC input voltage of the proposed AC-DC interleaved ZCS boost converter can be considered to be a DC source during a very short switching cycle. Therefore, the characteristic curves for the key components of the proposed converter will be presented by using MATLAB simulations. The value of each component can then be determined to satisfy the key design objectives. Finally, an example will be given to demonstrate the design procedure.

There are some parameters that should be satisfied so that all the switches of the proposed PWM AC-DC interleaved converter, which is shown in the following figure, can be turned off with ZCS.

Based on the modes of operation, ZCS conditions for the main switches should be met when the proposed converter operates in Mode 3 (Fig. 2.5). Since the auxiliary switch should be turned off right after turning off the main switch, the ZCS conditions for the auxiliary switch must be met in this mode of operation as well. The equation that determines the ZCS conditions for the main switches can be expressed as follows:

$$i_{Lr1}(t) = \left(\frac{V_o L_{eq}}{Z_2 L_{r1}}\right) (1 - \cos \omega_e t)$$
(2-39a)

I_{S1} should go to zero or a negative value to meet ZCS conditions; thus, current through S₁ should be diverted through its body diode. According to Fig. 2.5 and equ. (2-21a), the current through i_{Lr1} should be more than the $i_{in}(t)$ in order to provide the ZCS conditions for I_{S1}, as expressed as follows:

$$i_{in}(t) - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r1}} \right) (1 - \cos \omega_e t) \right] \le 0$$
(2-39b)

When the result of the following formula is zero or negative, it means that the switching losses related to the turn-off the auxiliary switch have been eliminated:

$$I_{Sa}(t) = i_{Lr2}(t) = \frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}} \right) (1 - \cos \omega_e t) \right]$$
(2-40a)

Therefore, to turn off the auxiliary switch S_a with ZCS, $i_{Lr2}(t)$ should be zero or negative:

$$I_{Sa}(t) = \frac{V_o}{Z_2} - \left[\left(\frac{V_o L_{eq}}{Z_2 L_{r2}} \right) (1 - \cos \omega_e t) \right] \le 0$$
(2-40b)

It is worth noting that negative values of I_{S1} and I_{Sa} in equ.(2-39b) and equ. (2-40b) represent that current is flowing through the body diodes of the main and auxiliary switches, respectively.

As can be seen from the above equations, the prerequisite for meeting ZCS conditions for the auxiliary switch depends mainly on the output voltage. On the other hand, current through the main switch depends on both output voltage and input current (i_n) , according

$$i_{in} = \frac{\sqrt{2}P_o}{\eta \, V_{in}} \tag{2-41}$$

where the parameters of the above equation are defined as:

Iin= Rectified input current,

V_o= Output power,

V_{in}= Rectified input voltage,

 η = Efficiency of the proposed interleaved converter.

2.4.1 Design Curves

It should be noted, when designing the components of the converter, that the maximum magnitude of I_{in} should be considered as the worst-case scenario. It can be seen from the equ. (2-39b) that if ZCS conditions can be met when the input current is at its maximum value ($I_{in} = I_{in,max}$), then soft switching is ensured for other values of the rectified input current. Based on equ. (2-41), the maximum input current can be obtained by considering the minimum input voltage. It should also be mentioned that the total harmonic distortion should meet the IEEE 519 standard on harmonics.

Another design objective that should be considered for turning off the main switch with ZCS, is that the current through L_{r2} should be more than the current through L_{r1} to divert the current from the main switch to the auxiliary switch. Thus, the magnitude of L_{r1} should be more than L_{r2} to ensure ZCS under all operating loads. During this time $I_{Sa} = I_{Lr2}$ and the maximum value of the auxiliary circuit can be determined to be

$$I_{Sa,max} = \frac{V_o}{Z_2} \tag{2-42}$$

As explained in the previous section, $Z_2 = \sqrt{\frac{L_{r2}}{c_r}}$ is defined as the characteristic impedance of the auxiliary circuit and V_o is defined as the output voltage. Minimizing the peak current through the auxiliary switch at the end of Mode 2 can be considered as another design objective.

Since the peak voltage across all the diodes, from the main boost diodes D_1 and D_2 to the auxiliary clamp diode D_4 , are each equal to the output voltage, there is no need to consider them as design objectives. On the other hand, based on the following equation, the maximum voltage across the auxiliary capacitor can be expressed as

$$V_{cr,max} = i_{L1}Z_e + V_o \tag{2-43}$$

where L_{eq} and Z_e are defined as $\frac{L_{r_1}L_{r_2}}{L_{r_1}+L_{r_2}}$ and $\sqrt{\frac{L_{eq}}{C_r}}$ respectively. Minimizing the maximum voltage across the auxiliary capacitor in Mode 6 of operation can thus be chosen as another design objective.

Overall, design objectives that should be considered are as follows:

- The ZCS turn-off conditions expressed in equ. (2-39b) and equ. (2-40b) should be satisfied for ZCS turn-off of all main and auxiliary switches, respectively. Since the proposed interleaved converter operates in discontinuous current mode, all switches are inherently turned on with ZCS.
- The peak current through the auxiliary switch presented in equ. (2-42) should be minimized.
- The peak voltage across the auxiliary capacitor presented in equ. (2-43) should be minimized.

Graphs of steady-state characteristic curves that can be used in the design of the converter were generated by MATLAB software. The MATLAB programs that were used to generate these graphs presented in Appendixes A-F. The design graphs were generated for the following operating conditions:

Output Voltage V₀= 400 Volts DC

Output Power $P_0 = 1 \text{ kW}$

Input Voltage V_{in}= 85- 265 Volts RMS

Expected Efficiency $\eta = 95 \%$

Switching Frequency
$$= f_S = \frac{1}{T_S} = 50$$
 kHz.

It should be noted that the maximum value of i_{in} should be considered in designing the converter as the worst-case scenario. According to the equ. (2-39b), if ZCS conditions can be met by the maximum value of i_{in} , then soft switching can be ensured by lower values of the rectified input current as well. Thus, although the input voltage varies from 85 to 265 volts RMS, the design should be done when the input voltage is at its minimum value which is 85 volts RMS.

Substituting V_{in} = 85 V in equ. (2-41) results in

$$i_{in,max} = rac{\sqrt{2} P_o}{\eta V_{in}} \xrightarrow{\text{yields}} rac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 A$$



Fig. 2.10. Characteristic graph of variation of maximum voltage across auxiliary capacitor with the variation of Cr when other parameters are constant

Fig. 2.10 was generated by the MATLAB program in Appendix 1 and illustrates the variation of the maximum voltage across the auxiliary capacitor ($V_{Cr,max}$) with different values of C_r, when other parameters are held constant.

The main function of the resonant capacitor is to impose a counter voltage across L_{r2} that allows current to be diverted away from the main switches so that they can turn off with ZCS. The value of this capacitor should not be too low, as there will not be sufficient time for current to be diverted away from the main switches as the capacitor would quickly charge up and its voltage polarity would become positive. If the voltage across V_{Cr} becomes positive as current is being diverted away from a main switch, then current will stop flowing in C_r and the switch will turn on with ZCS. Moreover, a very low value of C_r will increase the voltage stress of the converter components.



Fig. 2.11. Characteristic graph of variation of peak current through auxiliary switch with the variation of characteristic impedance of the auxiliary circuit

If C_r is too large, then the transfer of current away from the main switch becomes very gradual. This will result in increased current stress and conduction losses of the auxiliary circuit components because they will be forced to conduct current for a longer amount of time. This may also interfere with the operation of the main circuit, as a longer turn-off switching duration will result in a reduction of the effective duty cycle of the converter.

Fig. 2.11 was generated by the MATLAB program in Appendix B and illustrates the characteristic graph of variation of peak current through the auxiliary switch with respect to the variation of characteristic impedance of the auxiliary circuit (Z_2).

Characteristic impedance of the auxiliary circuit is defined as $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$, thus it is inversely proportional to the resonant capacitor; therefore, the peak current through the auxiliary circuit is one of the key design objectives. It can be concluded that the value of the resonant capacitor should not be selected to be very low because in this situation $V_{cr,max}$ increases considerably whereas high values of the resonant capacitor create additional stress in S_a by increasing I_{Sa,max}.

In order to ensure that ZCS is achieved, the current through the main and auxiliary switches should be zero or negative for an appropriate amount of time. The characteristic graphs illustrated in Figs. 2.12-2.15, are used to indicate the amount of time in which the current through the main and auxiliary switches are negative.

It should be noted that the value of the characteristic impedance of the auxiliary circuit (Z₂) should be designed in a way that $I_{S2,max} = \frac{V_0}{Z_2} > I_{in,max}$. According to the operating condition selected in the beginning of this section:

$$i_{in,max} = \frac{\sqrt{2} P_o}{\eta V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 A$$

$$\frac{V_o}{Z_2} = \frac{400}{Z_2} > i_{in,max} = 17.5 \ A \quad \xrightarrow{\text{yields}} \quad Z_2 < 22.8 \ \Omega$$

 Z_2 should therefore be less than 22.8 Ω . To provide margin, $Z_2=18 \Omega$ is assumed in all of the following figures. The characteristic graphs in Fig. 2.12 and Fig. 2.13, which are generated by the MATLAB program given in Appendix C and Appendix D respectively, show the current through the main and auxiliary switches versus time for various values of L_{r2} when other parameters are held constant. It can be seen that by increasing L_{r2} when other parameters are constant, the time in which current through the main and auxiliary switches reduce to zero increases as well. As a result, the conduction losses are increased.

On the other hand, by increasing L_{r2} , the window for ZCS increases as the current through the main switch can be in negative for a longer time. Therefore, a trade off should be made



Fig. 2.12. Characteristic graph of time in which main switch current get reduced to zero with the variation of L_{r2} while other parameters are constant



Fig. 2.13. Characteristic graph of time in which auxiliary switch current get reduced to zero with the variation of L_{r2} while other parameters are constant

between the length of time that current through the main switch goes to zero and the length of time in which the current stays negative.

As discussed previously, one of the prerequisites for diverting the current from the auxiliary circuit to provide ZCS is that the current through L_{r1} should be less than current through L_{r2} in Mode 3 of operation; thus the value of L_{r1} should be more than the value of L_{r2} . As can be seen from Fig. 2.13, when the value of L_{r1} is equal or less than L_{r2} , the current through the auxiliary switch does not go to zero so S_a cannot be turned off with ZCS.

The characteristic graphs in Fig. 2.14 and Fig. 2.15, which are generated by the MATLAB programs given in Appendix E and Appendix F respectively, demonstrate the current through the main and auxiliary switches vs time for various values of L_{r1} when other parameters are constant.

It can be seen from Fig. 2.14 that by increasing L_{r1} when other parameters are held constant, the time in which current through the main switch is reduced to zero increases as well; thus conduction losses are increased. It is shown in Fig. 2.15 that by increasing L_{r1} when other parameters are constant, the time in which the current through the auxiliary switch is reduced to zero decreases. In addition, it can be concluded from Fig. 2.14 that by increasing L_{r1} , the window for ZCS decreases as the current through the main switch is negative for a shorter amount of time.

It can be seen that as the value of L_{r1} becomes greater than L_{r2} , the possibility of reducing the current through the auxiliary switch to zero increases considerably. This action, however, reduces the chance of ZCS for the main switches and thus $\frac{L_{r2}}{L_{r1}}$ should be designed in a way that ensures that all the switches can be turned off with ZCS.


Fig. 2.14. Characteristic graph of time in which main switch current get reduced to zero with the variation of L_{r1} while other parameters are constant



Fig. 2.15. Characteristic graph of time in which auxiliary switch current get reduced to zero with the variation of L_{r1} while other parameters are constant

The design procedure is divided into two parts including a main power circuit design, which is the same as that for the conventional boost interleaved converter in operating in DCM, and an auxiliary circuit design. Each part is considered below.

2.4.2 Design Procedure for the Main Power Circuit

The main power circuit components that must be designed are comprised of two input inductors (L_1 and L_2), two main boost diodes (D_1 and D_2), two main switches (S_1 and S_2), and an output capacitor (C_0).

2.4.2.1 Design Procedure for Input Inductors L₁ and L₂

While designing the input inductors in this chapter, it should be considered that with interleaving, the input current of each module can be made to be discontinuous. The maximum input inductor value that allows the converter to operate in DCM can be expressed as

$$L_{in,max} < \frac{D(1-D)^2 R}{2f}$$
 (2-44)

where the parameters of the above equation are defined as

L_{in,max}= Maximum value for input inductors in order to work in DCM,

D= Duty cycle of the main switches,

R=Load,

f = main switch frequency.

f can be set to 50 kHz in this example. R can be determined from

$$P_o = \frac{V_o^2}{R} \tag{2-45}$$

By substituting the given design specifications for this example into equ. (2-45), a value for *R* can be determined as follows:

$$R = \frac{V_o^2}{P_o} \xrightarrow{\text{yields}} \frac{400^2}{1000} = 160 \,\Omega$$

An expression for the maximum duty cycle when the converter is in DCM, D_{max} , can be expressed as

$$\frac{V_o}{V_{in,peak}} > \frac{1}{1 - D_{max}}$$

By rewriting this expression, D_{max} can be expressed as

$$D_{max} < 1 - \frac{V_{in,peak}}{V_o} \tag{2-46}$$

Substituting the given design specifications into equ. (2-46) results in

$$D_{max} < 1 - \frac{\sqrt{2} * 85}{400} \xrightarrow{\text{yields}} D_{max} < 0.7$$

 D_{max} should be chosen for the case when the input voltage is at its lowest, 85 volts RMS in this example. D_{max} should be less than 0.65 to provide some margin. With D_{max} , R, and f known, these values can be substituted into equ. (2-44) to give

$$L_{in,max} < \frac{D(1-D)^2 R}{2f} \xrightarrow{\text{yields}} \frac{0.65 * (1-0.65)^2 * 160}{2 * 50000} < 127 \ \mu H$$

For a more conservative design, a value of $L_{in} = L_1 = L_2 = 125 \ \mu H$ is selected.

2.4.2.2 Design Procedure for Output Capacitor Co

The capacitor should be selected so that it can store enough energy to maintain the output voltage above a specified minimum voltage (V_{min}) that the load can temporarily operate with when the input voltage is not available for a specified amount of time called the hold-up time (T_h). For this example, V_{min} is chosen to be 350 volts and the holdup time (T_h) is chosen to be 20 ms. During this time, the following amount of energy is transferred to the output:

$$\mathbf{E} = P_o T_h \tag{2-47}$$

This energy, which is the same as the energy discharged by the capacitor, can be expressed as

$$E = \frac{C_o \left(V_o^2 - V_{o,min}^2 \right)}{2}$$
(2-48)

so that the output capacitor can be determined to be

$$C_o \ge \frac{2P_o T_h}{\left(V_o^2 - V_{o,min}^2\right)} \xrightarrow{\text{yields}} \frac{2 * 1000 * 0.02}{(400^2 - 350^2)} = 1.06 \, mF$$

2.4.2.3 Design Procedure for Main Switches S₁ and S₂

In designing the main boost switches, the maximum current through them and the maximum voltage across them should be considered. The maximum current through the switches is less than maximum current through the input inductors and can be determined as follows:

$$i_{S1,max} = i_{S2,max} < i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2} P_o}{\eta V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 \text{ A}$$

A current of 17.5 A through the main switches can be assumed for the worse-case design. The second parameter that should be considered is the maximum voltage across the switches. As can be seen from Mode 6, the maximum voltage across the main switches is clamped to the output voltage:

$$V_{S1,max} = V_{S2,max} = V_o = 400 \text{ V}$$

Two STGP 10NC60KD IGBT devices with 400 peak voltage stress and 20 A peak current stress are chosen for the design.

2.4.3 Design Procedure for the Auxiliary Circuit

Auxiliary circuit components that should be designed include: one auxiliary switch (S_a), two auxiliary inductors (L_{r1} and L_{r2}), four auxiliary diodes (D_{a1} , D_{a2} , D_{a3} , and D_{a4}), and a resonant capacitor (C_r). The auxiliary diodes D_{a1} and D_{a2} connect L_1 and L_2 to the auxiliary

circuit. The maximum current through D_{a1} and D_{a2} is equal to the maximum current through the input inductors:

$$i_{Da1,max} = i_{Da2,max} = i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2}P_o}{\eta V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 \text{ A}$$

The maximum voltage across D_{a1} and D_{a2} is clamped to the output voltage:

$$V_{Da1,max} = V_{Da2,max} = V_o = 400 \text{ V}$$

These auxiliary diodes are attached in series with L_{r1} to make a path between the input inductors and L_{r1} . This path diverts the current from the main switches to provide ZCS conditions for turning them off by resonating with L_{r2} and C_r . Since the proposed converter is operating in DCM, it does not have the main power diodes do not have any reverse recovery current. Values for L_{r1} , L_{r2} , and C_r can be determined from graphs of steady-state characteristic curves such as those shown in Fig 2.10-2.15.

As discussed previously, the value of the characteristic impedance of the auxiliary circuit (Z₂) should be designed in such a way that $I_{Sa,max} = \frac{V_o}{Z_2} > I_{in,max}$. According to the design specifications:

$$\frac{V_o}{Z_2} = \frac{400}{Z_2} > i_{in,max} = 17.5 \ A \quad \xrightarrow{\text{yields}} \quad Z_2 < 22.8 \ \Omega$$

In order to provide some margin, a value of $Z_2=18$ ohms is selected based on Fig. 2.11 so that:

$$I_{Sa,max} = \frac{V_o}{Z_2} = \frac{400}{18} = 22.22 \ A$$

It should be considered that the time it takes for the current through the main and auxiliary switches to be reduced to zero should be minimized to shrink the operating time of the auxiliary switch. The conduction losses can then be reduced by shrinking the duty cycle of the auxiliary circuit. At the end of Mode 2, it was shown that when the voltage of the auxiliary capacitor (V_{cr}) reaches zero, the currents through the main and auxiliary switches start to fall to zero. By shrinking the duration of the time of Mode 2, the auxiliary switch needs to be operated for a shorter period of time, thus resulting in a decrease in conduction losses. This time can be calculated by equ. (2-10) and, based on the trade-off, it can be assumed to be less than 0.5 μs to minimize the conduction losses; therefore, the two following equations should be satisfied:

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} = 18 \ \Omega$$
$$T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2}C_r} < 0.5 \ \mu s$$

As it was shown in Fig. 2.10, a very low value for the resonant capacitor should not be selected, because doing so increases $V_{cr,max}$ significantly. Choosing high values for the resonant capacitor, however, creates additional stress in S_a by increasing both $I_{Sa,max}$ and the operating time of the auxiliary switch. On the other hand, by increasing L_{r2} when C_r is held constant, the peak current through the auxiliary circuit decreases while the time during which the current through the main and auxiliary switches are reduced to zero increases. An appropriate trade-off should be made in designing these components and thus values of $L_{r2} = 4 \ \mu H$ and $C_r = 12$ nf are selected so that

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} = \sqrt{\frac{4 * 10^{-6}}{12 * 10^{-9}}} = 18.25 \,\Omega$$

$$T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2}C_r} = \frac{\pi}{2} \sqrt{4 * 10^{-6} * 12 * 10^{-9}} = 0.34 \ \mu s$$

It was shown in Fig. 2.13 and Fig. 2.15 that the value of L_{r1} should be greater than the value of L_{r2} in order to divert the current from auxiliary circuit so the auxiliary switch can be turned off with ZCS. Based on Fig 2.14, however, designing the ratio of $\frac{L_{r2}}{L_{r1}}$ close to one increases the chance of ZCS occurring for the main switches. Using the characteristic

graphs show in Figs 2.12-2.15, $\frac{L_{r_2}}{L_{r_1}} = 0.8$ is selected as an appropriate trade off, which means that $L_{r_1} = 5 \ \mu H$ should be selected.

The maximum current through blocking diode D_{a3} , which is attached in series with the auxiliary switch, is equal to $i_{sa,max}$:

$$I_{Da3,max} = I_{S2,max} = \frac{V_o}{Z_2} = \frac{400}{18} = 22.22 \ A$$

The maximum voltage across the blocking diode is obtained from Mode 4, when the current is diverted from auxiliary switch to turn it off with ZCS. $V_{Da3, max} = Vc_r = -V_{Lr1}$ during Mode 4 when V_{cr} is reduced to zero; therefore the maximum voltage across the clamping diode is low and well under 100 V.

The maximum current through clamping diode D_{a4} , which clamps the voltage of auxiliary switch to the output voltage, is almost equal to the input current $I_{in,max}$ during Mode 6.

$$I_{Da4,max} < I_{in,max} = 17.5 \ A$$

Since the voltage across the diode is clamped to the output voltage, this means $V_{Da4,max} = V_o = 400$ V.

2.5 Converter Features

The proposed converter has the following features:

- (i) All the converter switches turn on and off with ZCS.
- (ii) There is only one active auxiliary circuit for both main switches instead of each main switch needing its own active auxiliary circuit to help it turn off with ZCS.
- (iii) The main switch does not have increased peak and RMS current stresses, as is the case with resonant type ZCS auxiliary circuits, because no current from the auxiliary circuit flows into the main circuit.

- (iv) None of the auxiliary circuit components are in the main power path, so they only handle a fraction of the current that the main circuit components endure.
- (v) The voltage stress of the auxiliary switch is clamped to the output voltage and does not exceed this voltage.
- (vi) The main boost diodes do not have reverse recovery current as the input inductor currents are discontinuous.
- (vii) The auxiliary circuit does not interfere with the interleaving operation of the converter; therefore all the advantages of interleaving are maintained.
- (viii) The auxiliary circuit can be deactivated when the converter is operating under light-load conditions. This is unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load. Thus, light-load efficiency is improved because there is no auxiliary circuit component in the main power circuit.

2.6 Experimental Results

In this section, the feasibility of the proposed AC-DC interleaved ZCS-PWM boost converter will be validated with an experimental prototype that uses the values designed in the previous section, along with the following specifications:

- Output Voltage: V₀= 400 Volts DC
- Output Power: $P_0 = 1 \text{ kW}$
- Input Voltage: V_{in}= 85- 265 Volts RMS
- Switching Frequency: $f_S = \frac{1}{T_S} = 50 \text{ kHz}$

As discussed in the previous section, the following components should be used for the laboratory prototype:

- Input Inductors $L_{1,2}$: 125 μH
- Main Boost Diodes D_{1,2}: BYC10DX
- Main Switches S_{1,2}: STGP 10NC60KD

- Output Capacitor: 2X560µF 3316(M)
- Auxiliary Switch S_a: FGP3440G2
- Auxiliary Diodes D_{a 1,2,4} and D_{T 1,2} : STTH20RD4
- Auxiliary Diode D_{a 3}: SF3003PT
- Resonant Inductor L_{r1} : 5 μH
- Resonant Inductor L_{r2} : 4 μH
- Resonant Capacitor C_r: 0.012 µf

Fig. 2.16 shows typical input voltage and input current waveforms. It can be seen that the input current is sinusoidal, in phase with the input voltage, and continuous. Fig. 2.17 shows current waveforms for the input boost inductors (L_1 and L_2). It can be seen that these currents are discontinuous and identical. Fig. 2.18 shows the interleaved current that is a sum of the currents in L_1 and L_2 .

Fig. 2.19 shows typical current and gating signal waveforms for one of the main switches. It is seen that the switch can be turned on and off with ZCS, without a current tail, because the current through the switch goes to zero before switching. The same waveforms are shown in Fig. 2.20 for the auxiliary switch, and it can be seen that the auxiliary switch turns on and off with ZCS as well.



Fig. 2.16. Input voltage and current waveforms V_{in}, I_{in}



Fig. 2.17. Main input inductors L_1 and L_2 current waveforms I_{L1} , I_{L2}



Fig. 2.18. Rectified input current waveform IL1+ IL2



Fig. 2.19. Main switch S_1 voltage and current waveforms V_{S1} , I_{S1}



Fig. 2.20. Auxiliary switch S_a voltage and current waveforms V_{Sa}, I_{Sa}

Fig. 2.21 shows the efficiency of the AC-DC interleaved ZCS-PWM boost converter compared to the conventional converter which operates with hard-switching. As can be seen, the efficiency of the conventional converter is decreased by increasing the load while the efficiency of the proposed converter is increased. When the power is less than 600W (light load), the hard-switching method is more efficient while for higher power (more than 600 W) the proposed soft-switching method is more efficient.

The main reason for this is that the auxiliary circuit losses dominate when the converter is operating under light loads. Auxiliary circuit losses include the turning on and off of the auxiliary switch and additional conduction losses as there can be an increased amount of circulating current flowing in the converter. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads, when the eliminated switching

losses of the main switches - especially the IGBT's current tail losses - are greater than the auxiliary circuit losses.

The optimum efficiency can be obtained when the auxiliary circuit is used to achieve ZCS operation in a ZCS-PWM converter when the converter is operating with heavier loads, and not used when the converter is operating with light loads. Operating the converter in such a manner would ensure the optimum efficiency profile over the entire load range. It can be achieved in this thesis, as the auxiliary circuit of the proposed converter can be disengaged during light loads.



Fig. 2.21. Comparative of efficiency graphs between soft-switching and hardswitching for different output loads at input voltage of 110 V and output voltage 400V.

2.7 Conclusion

A new AC-DC interleaved ZCS-PWM converter is proposed in this chapter. Advantages of this converter include full ZCS operation of all converter switches, just one active auxiliary circuit for the two main switches, no additional voltage or current stresses on the main switches, no increased peak voltage stress on the auxiliary switch, and the auxiliary circuit can be deactivated from the main power circuit at any time. The feasibility of the converter was confirmed with results obtained from an experimental prototype.

3 An AC-DC Interleaved ZCS-PWM Boost Converter with Reduced Auxiliary Switch RMS Current Stress

3.1 Introduction

AC-DC interleaved boost converters are widely used in industry. To eliminate their switching losses, soft switching methods are implemented. These techniques were discussed in Chapter 1. It was shown that the zero-current switching (ZCS) is more efficient for IGBTs because of their current tail.

In Chapter 2, An interleaved ZCS-PWM AC-DC boost converter that consisted of two boost converter modules and just one auxiliary switch was proposed. Although it addressed a number of the drawbacks (a-h) named in Section 1-6, it did not address the issue of the energy which is trapped in the auxiliary circuit when it is activated. The reason for this is that there is no path for this energy to be transferred to the output.

In this chapter, an improved version of the proposed converter in Chapter 2 is presented. The new proposed converter has an auxiliary transformer that transfers a portion of the trapped energy in the auxiliary circuit to the output of the converter whenever the auxiliary switch needs to be activated; therefore, it does not have any of the drawbacks (a-h) mentioned in Section 1-6.

The interleaved AC-DC ZCS-PWM boost converter proposed in this chapter requires the use of just a single active auxiliary switch to assist in turning off the main power circuit switches with ZCS. The auxiliary switch can be turned on and off with ZCS itself and its auxiliary circuit allows the converter to operate without an increase in the main switches' peak current or voltage stresses. The auxiliary switch in the converter is active for a much shorter time than in most other ZCS-PWM converters. This allows the converter to operate at higher power levels than other previously proposed interleaved ZCS-PWM converters with a single auxiliary switch. The proposed converter's operation is explained in this chapter and its key features and design considerations are discussed. Experimental results that confirm the operation of the proposed converter are presented as well.

3.2 General Converter Principles and Modes of Operations

The proposed AC-DC converter, shown in Fig. 3.1 [52][53], consists of two boost converter modules: one with L_1 , S_1 and D_1 , the other with L_2 , S_2 and D_2 . The gating signals of the two main switches, S_1 and S_2 are identical, but shifted 180° with respect to each other. The currents in L_1 and L_2 are discontinuous and identical, but also shifted 180° with respect to each other.



Fig 3.1 Proposed interleaved AC-DC ZCS-PWM boost converter [52], [53]

The two boost modules are connected to the same auxiliary circuit, which consists of: connection diodes D_{a1} and D_{a2} , reverse blocking diode D_{a3} , inductors L_{r1} and L_{r2} , capacitor Cr, and center tap feed forward transformer T_a which has two diodes D_{T1} and D_{T2} . The auxiliary circuit is activated whenever a main switch is about to be turned off and is active for only a fraction of the switching cycle. The proposed converter has the following modes of operation for a half switching cycle when duty cycle is $D \ge 0.5$ and when S_2 is turned on and S_1 is turned off. Typical waveforms and circuit diagrams for these modes are shown in Fig. 3.2 and Figs. 3.3 - 3.9 respectively.



Fig 3.2 Typical waveforms of the proposed converter

The modes of operation for the other half-cycle when S_1 is turned on and S_2 is turned off are identical.

The modes of operation are derived based on the following assumptions:

- Since the AC input voltage can be considered to be a DC input source in a very short amount of time, the steady-state analysis is done with DC input voltage.
- The proposed circuit has two boost modules that are designed to be operated in DCM, so the input inductor current of each one will become discontinuous. However, the input current of the converter, which is the sum of the inductor currents, should be continuous.
- The output filter capacitor (C_o) is large enough to be considered as a voltage source (V_o).
- All semiconductor switches are ideal with no parallel capacitor across them.
- All inductors and capacitors are ideal; therefore, they have negligible resistances.
- All diodes are ideal and reverse recovery time of each one of them is zero.

<u>Mode 1 ($T_0 < t < T_I$)</u>: This mode begins when switch S₂ is turned on. The rectified voltage is applied to L₂ and the current through L₂ linearly increases, as does the input current in the input inductor (I_{in}). The slope of the current is $\frac{V_{in}}{L_2}$. Since I_{in} is the summation of I_{L1} and I_{L2}, it will increase with greater slope.

<u>Mode 2 ($T_1 < t < T_2$)</u>: This mode begins when the auxiliary switch (S_a) is turned on in preparation to turn off main switch S_1 with ZCS. S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases.

<u>Mode 3 ($T_2 < t < T_3$)</u>: This mode begins when the voltage across C_r (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. D_{T1} starts to conduct so that the circulating energy from the auxiliary circuit is transferred to the output during this time. The current through L_{r1} and L_{r2} decreases and goes to zero. The currents through S_1 and S_2 then become negative and flow through their body diodes. When this happens, S_1 can be turned off with ZCS. During this mode, the current in L_{r2} reaches

zero because of its resonance with C_r . Afterwards, the energy in L_{r1} is transferred to C_r , thus increasing its voltage so that V_{Cr} becomes less negative and eventually becomes positive.

<u>Mode 4 ($T_3 < t < T_4$)</u>: This mode begins when S_a is turned off with ZCS. V_{cr} keeps increasing, so the current through S_2 starts to become less negative. The negative current through body diode of S_2 rises to zero, thus the auxiliary diode D_{a2} stops conducting at the end of this mode.

<u>Mode 5 ($T_4 < t < T_5$)</u>: This mode begins when the net voltage across the C_r and L_{r1} becomes positive, causing D₁ to start conducting. This mode ends when the current through L_{r1} reaches zero. At the end of this mode, the maximum voltage across the auxiliary capacitor (V_{cm}) can be derived.

<u>Mode 6 ($T_5 < t < T_6$)</u>: This mode begins when I_{Lr1} reaches zero, thus D_{a1} and D_{T1} stop conducting. During this mode, the current in the magnetizing inductance of the feed forward transformer is discharged to the output by D_{T2} . The voltage across L_1 becomes $V_{in,rec}$ - V_o and the current through L_1 starts to decrease linearly.

<u>Mode 7 ($T_6 < t < T_7$)</u>: This mode begins when the current in L₁ reaches zero. This is the last mode of the half-cycle. The next half-cycle begins when S₁ is turned on under ZCS.







Fig. 3.4. Current flow in Mode 2















Fig. 3.8. Current flow in Mode 6



Fig. 3.9. Current flow in Mode 7

The proposed converter has the following features:

- (i) All the converter switches turn on and off with ZCS.
- (ii) There is only one active auxiliary circuit for both main switches instead of each main switch needing its own active auxiliary circuit to help it turn off with ZCS.
- (iii) The main switch does not have increased peak and RMS current stresses, as is the case with resonant type ZCS auxiliary circuits, because no current from the auxiliary circuit flows into the main circuit.
- (iv) None of the auxiliary circuit components are in the main power path, therefore they only handle a fraction of the current that the main circuit components handle.

- (v) The maximum voltage stress of the auxiliary switch is close to the output voltage because of the transformer. Also, the current in the auxiliary circuit can be transferred to the output to increase the efficiency.
- (vi) The main boost diodes do not have reverse recovery current because the input inductor currents are discontinuous.
- (vii) The auxiliary circuit does not interfere with the interleaving operation of the converter; thus all the advantages of interleaving are maintained.
- (viii) The auxiliary circuit can be deactivated when the converter is operating under light-load conditions, unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load. This leads to an improvement in the light-load efficiency because it removes the auxiliary circuit losses under operating conditions where the current in the converter is low and ZCS is unnecessary. This can be done because there are no auxiliary circuit components in the main power circuit.
- (ix) The auxiliary circuit needs to be operational for a very short amount of time, typically around 0.7 μ s. Since the auxiliary transformer is not in series with the auxiliary switch, the maximum voltage of the resonant capacitor increases which leads to faster soft switching for S₁. Also, because L_{r1} is in series with the resonant circuit, the auxiliary switch can go to zero current faster. In addition, since the converter operates in DCM, there is no reverse recovery current for the main diodes, therefor L_{r1} does not need to be chosen high enough to eliminate it. As a result, small L_{r2} can be chosen which decreases the operating time of the auxiliary switch.

3.3 Circuit Analysis

Like the previous chapter, mathematical equations of each mode in steady-state must be derived to determine the effects of the proposed AC-DC PWM boost converter on each component. Then, the equations are used to determine the parameters that should be met to satisfy the ZCS conditions. The analysis in this chapter is done with $D \ge 0.5$, S_2 turned

on, and S_1 turned off; the analysis and formulas for the other half-cycle when S_1 is turned on and S_2 is turned off is identical.

In Mode 1, shown in Fig. 3.3, when switch S_2 is turned on, the rectified voltage is applied to L_2 and leads to a gradual increase of the current through L_2 and the input current in the input inductor (I_{in}). The slope of L_2 , which is equal to the slope of S_2 , is increased as follows:

$$V_{in} = L_2 \frac{dL_2(t_1)}{dt}$$
(3-1)

By integrating from time T_0 to T_1 , the main switch current can be expressed as

$$I_{S2}(t_1) = \frac{V_{in}}{L_2} (T_1 - T_0)$$
(3-2)

All the input current goes through S₁ and S₂ so that

$$I_{in} = I_{S1} + I_{S2} \tag{3-3}$$

The next mode begins when the auxiliary switch (S_a) is turned on in preparation for the ZCS turn-off of main switch S_1 . S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases. The equivalent circuit diagram at time T_2 was shown in Fig. 3.4.

By applying KVL, the following equation can be obtained:

$$V_{Cr}(t_2) = L_{r2} \frac{d}{dt} i_2(t_2)$$
(3-4)

By applying KCL, the following equation can be obtained:

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -\frac{d}{dt} q_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2)$$
(3-5)

By substituting equ. (3-5) into equ. (3-4), the following result can be obtained:

$$V_{Cr}(t_2) = -L_{r2} C_r \frac{d^2}{dt^2} V_{Cr}(t_2)$$
(3-6)

In order to solve the above-mentioned equations, the initial capacitor voltage $V_{cr}(0)$ and the initial auxiliary inductor current $i_{Lr2}(0)$ should be defined. $V_{cr}(0)$ is assumed to be equal to the maximum voltage across the capacitor(V_{cm}), and $i_{Lr2}(0)$ is equal to zero in this mode. As a result, the derivative of the capacitor voltage $dV_{cr}(0)/dt$ can be determined to be

$$\begin{bmatrix} \frac{d}{dt} V_{Cr}(t_2) \end{bmatrix}_{t=0} = -\left(\frac{1}{C_r}\right) \begin{bmatrix} \frac{d}{dt} q_{Cr}(t_2) \end{bmatrix}_{t=0} = \left(\frac{1}{C_r}\right) [i_{Lr2}(t_2)]_{t=0}$$

$$= 0$$
(3-7)

By substituting equ. (3-7) into equ. (3-6), the following can be obtained:

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 \quad \text{for} \quad T_1 < t < T_2$$
 (3-8)

Based on the initial conditions of this mode, the following equation can be written:

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2) = C_r V_{cm} \omega_2 \sin \omega_2 t_2$$
(3-9)

$$= \frac{V_{cm}}{Z_2} \sin \omega_2 t_2 \qquad \qquad \text{for} \quad T_1 < t < T_2$$

In the above equation, $\omega_2 = \frac{1}{\sqrt{L_{r2}C_r}}$ and the characteristic impedance of the auxiliary circuit is defined as $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$. Mode 2 is finished when the voltage of the auxiliary capacitor V_{cr} reaches zero. As a result, the duration of this mode can be calculated by making equ. (3-8), equal to zero as follows:

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 = 0$$
 for $t = T_2$ (3-10a)

$$\omega_2 t_2 = \frac{\pi}{2} t_2 = T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2} C_r}$$
(3-10b)

The maximum current through the auxiliary circuit at the end of this mode can be determined to be

$$i_{Lr2}(t_2) = \frac{V_{cm}}{Z_2} \sin \omega_2 \frac{\pi}{2} \frac{1}{\omega_2}$$
(3-11)

$$i_{Lr2}(t_2) = i_{samax} = \frac{V_{cm}}{Z_2} \qquad \text{for } t = T_2$$

Mode 3, shown in Fig. 3.5, begins when the voltage across C_r (V_{Cr}) reaches zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. D_{T1} also starts to conduct so that the circulating energy from the auxiliary circuit is transferred to the output during this time. The current through L_{r1} and L_{r2} decreases and goes to zero. The currents through S_1 and S_2 then become negative and flow through their body diodes. When this happens, S_1 can be turned off with ZCS.

In deriving the equation of this mode, it should be noted that since S_a has to be turned off right after turning off the main switches, the ZCS conditions for main and auxiliary switches must both be met in this mode of operation. It can be seen from Fig. 3.5 that

$$i_{Lr1}(t_3) = i_{Lr2}(t_3) + i_{Cr}(t_3)$$
 (3-12)

Initial conditions for Mode 3, which should be derived from the previous mode, show that the initial value of both the voltage across the auxiliary capacitor $V_{Cr}(t_2)$ and the current through the auxiliary inductor $i_{Lr1}(t_2)$ are zero. As well, the initial current through the second auxiliary inductor $i_{Lr2}(t_2)$ in this mode is equal to

$$i_{Lr2}(T_3) = \frac{V_{cm}}{Z_2}$$
(3-13)

Since D_{a3} is conducting, the voltage across auxiliary circuit inductor L_{r2} is

$$V_{Lr2} = V_{Cr} \tag{3-14}$$

Since D_{a2} is conducting the voltage across auxiliary circuit inductor L_{r1} is

$$V_{Lr1} = -(V_{Cr} + V_X) \tag{3-15}$$

The auxiliary transformer's primary side voltage is clamped to $V_X = V_0/N$, where $N=N_2/N_1$ is the turns ratio.

By differentiating equ. (3-12) with respect to time, the following equation can be obtained:

$$\frac{d}{dt}i_{Lr1}(t_3) = \frac{d}{dt}i_{Lr2}(t_3) + \frac{d}{dt}i_{Cr}(t_3)$$
(3-16a)

This can be rewritten as

$$\frac{V_{Lr1}}{L_{r1}}(t_3) = \frac{V_{Lr2}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3)$$
(3-16b)

By substituting equ. (3-15) into equ. (3-16b), the following result can be obtained:

$$\frac{V_{Cr} + V_X}{L_{r1}}(t_3) + \frac{V_{Cr}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(3-16c)

This can then be rewritten as

$$\frac{V_X}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r2}}(t_3)\frac{L_{r1}}{L_{r1}} + C_r\frac{d^2}{dt^2}V_{Cr}(t_3) = 0$$

$$\frac{V_{Cr}(L_{r1}+L_{r2})+V_{X}L_{r2}}{L_{r1}L_{r2}}(t_{3})+C_{r}\frac{d^{2}}{dt^{2}}V_{Cr}(t_{3})=0$$

By defining $L_e = \frac{L_{r1}L_{r2}}{L_{r1}+L_{r2}}$, equ. (3-16c) can be simplified to

$$\frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3) + \frac{V_{Cr}}{L_e}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(3-16d)

This is also equal to:

$$\frac{V_{Cr}}{L_{eq}}(t_3) = -C_r \frac{d^2}{dt^2} V_{Cr}(t_3) - \frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3)$$
(3-16e)

Solving these equations gives equ. (3-17), where:

$$\omega_{1} = \frac{1}{\sqrt{L_{r1}C_{r}}}$$
$$\omega_{e} = \frac{1}{\sqrt{L_{e}C_{r}}}$$
$$Z_{1} = \sqrt{\frac{L_{r1}}{C_{r}}}$$
$$Z_{e} = \sqrt{\frac{L_{re}}{C_{r}}}$$
$$L_{e} = \frac{L_{r1} * L_{r2}}{L_{r1} + L_{r2}}$$

$$V_{Cr}(t_3) = \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - \frac{(V_{Cm} Z_e)(\sin(w_e t_3))}{Z_2}$$
(3-17)

Applying KVL to Fig. 3.5 results in:

$$V_{Lr1}(t_3) = -V_{Cr}(t_3) - V_X = -V_{Lr2}(t_3) - V_X$$
(3-18)

The above equation can be solved by integrating it over the interval of time for this mode of operation. The initial magnitude of the auxiliary inductor current I_{Lr1} , which is equal to zero, can be derived from the previous mode:

$$i_{Lr1}(t_3) = \frac{(V_{Cm}L_e)(1-\cos(w_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r1}^2} - \frac{V_X t_3}{L_{r1}}$$
(3-19)

During this mode of operation, I_{S1} should go to zero or a negative value in order to meet the ZCS conditions; therefore, the direction of current through S_1 is changed and it flows through its body diode. Based on Fig. 3.5, the following condition should be satisfied to ensure the soft switching of S_1 :

$$i_{in}(t_3) - i_{Lr1}(t_3) \le 0 \tag{3-20}$$

This means that current i_{Lr1} should be greater than $i_{in}(t)$. Substituting equ. (3-20) into equ. (3-19) results in

$$i_{in} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r_1}} + \frac{(V_X L_e)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{{L_{r_1}}^2} - \frac{V_X t_3}{L_{r_1}}\right) \le 0$$
(3-21)

By applying KVL in Fig. 3.5, the following expression can be written:

$$V_{Cr}(t_3) = L_{r2} \frac{d}{dt} i_{Lr2}(t_3)$$
(3-22)

This can be rewritten as

$$di_{Lr2}(t_3) = \left(\frac{V_{Cr}}{L_{r2}}(t_3)\right)dt$$
(3-23)

The initial current through the second auxiliary inductor $(i_{Lr2}(t_2))$ in this mode is $i_{Lr2}(T_2) = \frac{V_{cm}}{Z_2}$. By substituting equ. (3-22) into equ. (3-23), the current through the L_{r2} can be determined to be

$$i_{Lr2}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2) \left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r2} w_e^2}\right)$$
(3-24)

Auxiliary switch S_a is turned on to help the main switches turn off with ZCS. It should then be turned off soon afterwards. At the end of this mode of operation, I_{Sa} should go to zero or become negative so that S_a turns off with ZCS as well. It can be seen from Fig. 3.5 that:

$$I_{Sa}(t_3) = i_{Lr2}(t_3) \tag{3-25}$$

In order to turn off the auxiliary switch (S_a) with ZCS, $i_{Lr2}(t_3)$ should be zero or negative. This can be expressed as

$$I_{Sa}(t) = i_{Lr2}(t) \le 0 \tag{3-26}$$

The time in which the currents of the main switches go to zero is equal to the time in which V_{Lr1} is at its maximum since all the currents go to L_{r1} at that time

$$V_{Lr1}(t_3) = \frac{(V_{Cm}Z_e)(\sin(w_e t_3))}{Z_2} - \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - V_X$$
(3-27)

As a result, the following expression for t₃ can be derived:

$$t_{3} = -\frac{\log\left(\frac{\sqrt{\left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)j + \left((\frac{V_{cm}L_{e}}{Z_{2}L_{r1}})^{2}w_{e}^{2} + \left(\frac{V_{X}L_{e}}{L_{r1}^{2}}\right)^{2} - \left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)^{2})}{\frac{V_{X}L_{e}}{L_{r1}^{2}}j - \frac{V_{cm}L_{e}}{Z_{2}L_{r1}}w_{e}}}{w_{e}}\right)j}$$
(3-27)

Adding the time of Mode 2 to Mode 3 sets the entire time that the auxiliary switch needs to be turned on:

$$t_{isa-on\,time} = t_2 + t_3 \tag{3-28}$$

This results in

$$t_{isa-on\,time} = 2(\frac{\pi - tan^{-1}\left(\frac{V_{cm}w_e^{\ 2}Z_e}{V_Xw_1^{\ 2}Z_2}\right)}{w_e})$$
(3-29)

The voltage across the main diodes, V_{D1} and V_{D2} , can be derived based on KVL in Fig. 3.5 to be:

$$V_{D2} + V_o = 0 (2-30)$$

$$V_{D1} - V_{Cr} - V_{Lr1} - V_X + V_o = 0 (3-31)$$

During this mode, $V_{Lr1} = -V_{Cr} - V_X$, so equ (3-31) can be rewritten as

$$V_{D1} + V_o = 0 \tag{3-32}$$

The above-mentioned equations show that in this mode of operation, the voltage across each of the main boost diodes is equal to the output voltage. This is one of the advantages of this topology, that the maximum voltage across each of the main diodes is equal to the output voltage.

The maximum voltage of the resonant capacitor, which is the maximum voltage across the auxiliary switch, should be derived by considering Modes 4-6. At t_3 , V_{cr} is equal to equ. (3-33), which can be the initial value for Vcr(t_4):

$$V_{Cr_4}(0) = \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - \frac{(V_{Cm} Z_e)(\sin(w_e t_3))}{Z_2}$$
(3-33)

The initial value of the current through L_{r1} at Mode 4 can be expressed as

$$i_{lr1_4}(0) = \frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r1}^2} - \frac{V_X t_3}{L_{r1}}$$
(3-34)

The maximum voltage of the resonant capacitor at the end of this mode is:

$$V_{Cr}(t_4) = \left(V_{Cr_4}(0) + V_X\right)(\cos(w_1 t_4)) + \frac{i_{lr_{1_4}}(0)(\sin(w_1 t_4))}{c_r w_1} - V_X$$
(3-35)

The time duration of Mode 4 can be expressed as

$$t_{4} = -\frac{\log\left(\frac{\left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)i + \sqrt{\left(\left(\frac{V_{Cm}L_{e}}{Z_{2}L_{r1}}\right)^{2}w_{e}^{2} + \left(\frac{V_{X}L_{e}}{L_{r1}^{2}}\right)^{2} - \left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)^{2}\right)}{\frac{V_{X}L_{e}}{L_{r1}^{2}}i - \frac{V_{Cm}L_{e}}{Z_{2}L_{r1}}w_{e}} - \frac{W_{e}}{W_{e}} - \frac{W_$$



During Mode 5, V_{cr} keeps increasing so that the current through S_2 starts to become less negative. The negative current through body diode of S_2 rises to zero, thus the auxiliary diode D_{a2} stops conducting at the end of this mode.

The initial conditions for equ. (3-37) and equ. (3-38) are $V_{cr_5}(0)$ and $i_{Lr1_5}(0)$, which are the voltage of the auxiliary capacitor and the current of through L_{r1} at the end of Mode 4.

$$i_{Cr}(t_5) = i_{Lr1}(t_5) = C_r \frac{dV_{Cr}}{dt} (t_5)$$
(3-37)

$$-\frac{d^2 V_{Cr}(t_5)}{dt^2} - \frac{V_{Cr}}{L_{r1} C_r}(t_5) - \frac{V_X}{L_{r1} C_r} = 0$$
(3-38)

Solving these equations gives the following expression for the voltage of the auxiliary capacitor at the end of this mode:

$$V_{Cr}(t_5) = \left(V_{Cr_5}(0) + V_X\right)(\cos(w_1 t_5)) + \frac{i_{lr_1}(0)(\sin(w_1 t_5))}{c_r w_1} - V_X$$
(3-39)

The current through L_{r1} can be expressed as

$$i_{Lr1}(t_5) = -((c_r w_1) (V_{Cr_5}(0) + V_X) (\sin(w_1 t_5)))$$

$$+ (i_{lr1_5}(0) (\cos(w_1 t_5)))$$
(3-40)

The time of Mode 5 can be expressed as

$$t_{5} = -\frac{\log\left(\frac{\left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)i + \sqrt{\left(\left(\frac{V_{cm}L_{e}}{Z_{2}L_{r1}}\right)^{2}w_{e}^{2} + \left(\frac{V_{X}L_{e}}{L_{r1}^{2}}\right)^{2} - \left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}^{2}}\right)^{2}}{\frac{V_{X}L_{e}}{L_{r1}^{2}}i - \frac{V_{cm}L_{e}}{Z_{2}L_{r1}}w_{e}}}\right)i}{w_{e}} - \frac{\tan^{-1}\left(\frac{\left(\frac{V_{X}w_{1}^{2}}{w_{e}}\right) - \sqrt{\left(\frac{V_{X}w_{1}^{2}}{w_{e}}\right)^{2} + \left(\frac{V_{cm}w_{e}Z_{e}}{Z_{2}}\right)^{2}}{\frac{V_{cm}}{Z_{2}}}\right) + \pi}{-\left(2 * \frac{w_{e}}{W_{e}}\right)} + \frac{w_{e}}{W_{e}}\right)}$$

$$(3-41)$$

It is worth noting that the maximum voltage across the auxiliary capacitor is achieved in Mode 5 (Fig. 3.7), due to the resonance among C_r , L_{r1} , and L_{r2} . This mode ends when the current through the L_{r1} reaches zero.

The initial conditions for (3-33) and (3-34) are $V_{cr_6}(0)$ and $i_{Lr_1_6}(0)$, which can be calculated by substituting (3-31) into (3-29) and (3-30) respectively. Solving these equations gives (3-35) - (3-37).

The initial conditions for equ. (3-42) and equ. (3-43) are $V_{cr_6}(0)$ and $i_{Lr_16}(0)$ which are the voltage of the auxiliary capacitor and the current through L_{r_1} at the end of Mode 5.

$$i_{Cr}(t_6) = i_{Lr1}(t_6) = C_r \frac{dV_{Cr}}{dt}(t_6)$$
 (3-42)

$$-\frac{d^2 V_{Cr}(t_5)}{dt^2} - \frac{V_{Cr}(t_5)}{L_{r1} C_r} - \frac{V_X - V_O}{L_{r1} C_r} = 0$$
(3-43)

Solving these equations gives the voltage of the auxiliary capacitor at the end of this mode:

$$V_{Cr}(t_6) = \left(V_{Cr_6}(0) + V_X - V_0\right)(\cos(w_1 t_6)) + \frac{i_{lr1_6}(0)(\sin(w_1 t_6))}{c_r w_1} - V_X + V_0$$
(3-44)

The current through L_{r1} can be expressed as:
$$i_{Lr1}(t_6) = -((c_r w_1) (V_{Cr_6}(0) + V_X - V_0) (\sin(w_1 t_6)))$$

$$+ (i_{lr1_6}(0) (\cos(w_1 t_6)))$$
(3-45)

The duration of Mode 6 can be expressed as

$$t_{6} = \frac{tan^{-1} \left(\frac{i_{lr1_{6}}(0)}{(c_{r}w_{1}) \left(V_{Cr_{6}}(0) + V_{X} - V_{0} \right)} \right) + \pi}{w_{1}}$$
(3-46)

As an example of how the equations derived in this section can be used, Fig. 3.10 shows a simple flowchart of a computer program that determines whether the auxiliary circuit is functioning under steady-state conditions. This is done by determining whether the voltage across capacitor C_r (V_{cr}) after the auxiliary circuit has gone through a cycle is equal to its initial value before the auxiliary circuit was activated. Once it has been determined that the auxiliary circuit is in steady-state, the desired value of a certain voltage or current (i.e., auxiliary switch peak current) can be determined for a specific operating point. When this is done, the whole process can be repeated for several operating points until a curve is generated.



Fig 3.10 Flow chart of the program to determine if the converter is operating under steady-state conditions and obtaining the maximum value of the V_{cr}

3.4 Design Procedure and Example

All the analysis and equations that have been presented in the previous section have been derived from a DC input voltage. This is because the AC input voltage of the proposed AC-DC interleaved ZCS boost converter can be considered to be a DC source during a very short switching cycle. Therefore, the characteristic curves for the key components of the proposed converter will be presented by using MATLAB simulations. Then, the value of each component can be determined to satisfy the key design objectives. Finally, an example will be given to illustrate the design procedure. It should be noted that the total harmonic distortion should meet the IEEE 519 standard on harmonics.

There are some parameters that should be satisfied so that all the switches of the proposed PWM AC-DC interleaved converter, which is shown in the following figure, can be turned off with ZCS.

Based on the modes of operation, ZCS conditions for the main switches should be met when the proposed converter operates in Mode 3 (Fig. 3.5). Since the auxiliary switch should be turned off right after turning off the main switch, the ZCS for the auxiliary switch must be met in this mode of operation as well. The equation that determines the ZCS condition for the main switches was derived as follows:

$$\left(\frac{(V_{Cm}L_e)(1-\cos(w_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{{L_{r1}}^2} - \frac{V_X t_3}{L_{r1}}\right)$$
(3-47a)

Is1 should go to zero or negative in order to meet ZCS conditions; thus, the current through S1 should be diverted through its body diode. According to Fig. 3.5, i_{Lr1} should be greater than $i_{in}(t)$ in order to provide the ZCS conditions for Is1:

$$i_{S1,2}(t_3) = i_{in} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r_1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{{L_{r_1}}^2} - \frac{V_X t_3}{L_{r_1}}\right) \le 0$$
(3-47b)

When the result of the following formula is zero or negative, it means that the switching losses related to turning off the auxiliary switch have been eliminated:

$$i_{Sa}(t_3) = i_{Lr2}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2) \left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r2} w_e^2}\right)$$
(3-48a)

Therefore, to turn off the auxiliary switch (S_a) with ZCS, $i_{Lr2}(t)$ should be zero or negative:

$$i_{Sa}(t_3) = i_{Lr2}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r_2}} + \frac{(V_X w_1^2)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r_2} w_e^2}\right) \le 0$$
(3-48b)

It is worth noting that negative values of I_{S1} and I_{Sa} in equ. (2-39b) and equ. (2-40b) represent a flow of current through the body diodes of the main and auxiliary switches, respectively.

As can be seen from the above-mentioned equations, the prerequisite for meeting ZCS conditions for the auxiliary switch depends mainly on the output voltage. Also, it can be seen that the current through the main switch depends on both output voltage and input current (i_{in}), which can be calculated as follows:

$$i_{in} = \frac{\sqrt{2}P_o}{\eta \, V_{in}} \tag{3-49}$$

where the parameters of the above equation are defined as:

Iin= Rectified input current,

V_o= Output power,

V_{in}= Rectified input voltage,

 η = Efficiency of the proposed interleaved converter.

3.4.1 Design Curves

It worth noting that in designing the components of the converter, the maximum magnitude of I_{in} should be considered as the worst-case scenario. It can be seen from equ. (3-40b) that if ZCS conditions can be met when the input current is at its maximum value ($I_{in} = I_{in,max}$), then soft switching is ensured for all other values of the rectified input current. Based on equ. (3-49), the maximum input current is obtained by considering the minimum input voltage.

Another design objective that should be considered for turning off the main switches with ZCS is that the current through L_{r2} should be greater than the current through L_{r1} . This ensures the current is diverted from the main switch to the auxiliary switch; thus the magnitude of L_{r1} should be greater than L_{r2} to ensure ZCS across all operating loads. During this time, $I_{Sa} = I_{Lr2}$ so that the maximum value of the auxiliary switch current can be expressed as

$$I_{Sa,max} = \frac{V_{cm}}{Z_2} \tag{3-50}$$

As explained in the previous section (circuit analysis), $Z_2 = \sqrt{\frac{L_{r2}}{c_r}}$ is defined as the characteristic impedance of the auxiliary circuit and V_o is defined as the output voltage. Minimizing the peak current through the auxiliary switch at the end of Mode 2 can be considered as another design objective. The peak voltage across the auxiliary switch is equal to the peak voltage across the auxiliary capacitor and should be minimized. This voltage can be determined from

$$V_{Sa-max} = V_{Cm} = \left(V_{Cr_6}(0) + V_X - V_0\right)\left(\cos(w_1 t_6)\right) + \frac{i_{tr_16}(0)(\sin(w_1 t_6))}{c_r w_1} - V_X + V_0$$
(3-51)

In general, the following design objectives should be considered:

- The conditions expressed in equ. (3-47b) and equ. (3-48b) should be satisfied for the ZCS turn-offs of all main and auxiliary switches respectively. Since the proposed interleaved converter operates in DCM, all switches are turned on with ZCS inherently.
- The peak current through the auxiliary switch presented in equ. (3-50) should be minimized.
- The peak voltage across the auxiliary capacitor and auxiliary switch presented in equ. (3-51) should be minimized.

Design graphs can be generated by MATLAB software; the relevant MATLAB programs are presented in Appendix G. The most important feature of these graphs is the ability to check that the current through and voltage across any component of the proposed interleaved converter at the start of a switching cycle is the same as that at the end of the switching cycle. Doing so ensures that steady-state operation has been achieved. Graphs that have been generated by MATLAB and that can be used to confirm steady-state operation are shown in Fig. 3.10. The simulated voltage and current waveforms of each component of the proposed interleaved converter should be identical for every switching cycle. When this prerequisite is satisfied, the voltage across and current through each component, then their characteristic curves and graphs can be obtained by MATLAB. These graphs indicate how changing a particular component value such as an inductor or a capacitor affects the current and voltage waveforms of the proposed converter. The curves are generated for the following operating conditions:

• Output Voltage: V₀= 400 Volts DC

- Output Power: $P_0 = 1 \text{ kW}$
- Input Voltage: V_{in}= 85- 265 Volts RMS
- Expected Efficiency: $\eta = 95 \%$
- Switching Frequency: $f_S = \frac{1}{T_S} = 50 \text{ kHz}.$

The design procedure that is presented here is iterative and requires several iterations before the final design can be completed. Only the final iteration will be shown in the example that follows. The key auxiliary circuit components that should be designed are the resonant capacitor (C_r), the two auxiliary circuit inductors (L_{r1} and L_{r2}), and the transformer turns ratio.

The key circuit voltages that need to be considered are the output voltage (V_0 = 400 V) and the worst-case input voltage. This input voltage is the voltage that causes the maximum current to flow through the converter, which is the minimum input voltage (V_{in} =8 5 V). Based on equ. (3-47b), if the auxiliary circuit can be designed to maintain ZCS under worstcase conditions with minimum the input voltage and the maximum load, then it can operate under all other conditions.

The maximum input current, assuming a targeted efficiency of 95% is determined by substituting V_{in} = 85 V into equ. (3-49), resulting in:

$$i_{in,max} = \frac{\sqrt{2} P_o}{\eta V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 A$$

It should be noted that to maintain ZCS for the main switches, the value of the maximum current through the auxiliary switch should be greater than the input current. In order to ensure ZCS operation of the main switches, a potential maximum current of 17.5 A needs to be diverted away from these switches. This means that a current of at least 17.5 A must be allowed to flow in the auxiliary switch. To fully ensure ZCS operation, the current that can flow in the auxiliary switch should be more than this. Assuming a conservative 20% - 30% margin, the converter can be designed to ensure that the auxiliary switch conducts 22 A of current so that

$$i_{sa,max} = \frac{V_{cm}}{Z_2} > i_{in,max}$$

$$i_{samax} = \frac{V_{cm}}{Z_2} = 22 A$$
(3-52)

3.4.2 Design Procedure for the Main Power Circuit

First, the main power circuit components need to be chosen which are two input inductors $(L_1 \text{ and } L_2)$, two main boost diodes $(D_1 \text{ and } D_2)$, two main switches $(S_1 \text{ and } S_2)$, and the output capacitor (C_0) .

3.4.2.1 Design Procedure for Input Inductors L₁ and L₂

In designing the input inductors, interleaving needs to be considered. As discussed earlier, the input current of each module can be made to be discontinuous. The following equation can be used to determine the maximum input inductor value that allows the converter to operate in DCM:

$$L_{in,max} < \frac{D(1-D)^2 R}{2f}$$
 (3-52)

where:

L_{in,max}= Maximum value for input inductors in order to work in DCM,

D= Duty cycle of the main switches,

R=Load,

f = Main switch frequency.

f is set to be 50 kHz for this example. R can be determined from the following equation:

$$P_o = \frac{V_o^2}{R} \tag{3-53}$$

Substituting the design specifications for this example into equ. (3-53) yields

$$R = \frac{V_o^2}{P_o} \xrightarrow{\text{yields}} \frac{400^2}{1000} = 160 \,\Omega$$

The maximum duty cycle when the converter is in DCM, D_{max} , can be expressed as

$$\frac{V_o}{V_{in,peak}} > \frac{1}{1 - D_{max}}$$

Through substitution, the maximum value of duty cycle is found to be

$$D_{max} < 1 - \frac{V_{in,peak}}{V_o} \tag{3-54}$$

Substituting into equ. (3-54) results in

$$D_{max} < 1 - rac{\sqrt{2} * 85}{400} \xrightarrow{\text{yields}} D_{max} < 0.7$$

For a sufficient margin, D_{max} is chosen to less than 0.65 and equ. (3-52) can then be solved as follows:

$$L_{in,max} < \frac{D(1-D)^2 R}{2f} \xrightarrow{\text{yields}} \frac{0.65 * (1-0.65)^2 * 160}{2 * 50000} < 127 \ \mu H$$

 L_{in} is chosen to be $L_1=L_2=125 \ \mu H$.

3.4.2.2 Design Procedure for Output Capacitor Co

The capacitor should be selected so that it can store enough energy to maintain the output voltage above a specified minimum voltage (V_{min}) that the load can temporarily operate with when the input voltage is not available for a specified amount of time called the hold-up time (T_h). For this example, V_{min} is chosen to be 350 volts and the holdup time (T_h) is chosen to be 20 ms. During this time, the following amount of energy is transferred to the output:

$$\mathbf{E} = P_o T_h \tag{3-55}$$

This energy can be expressed as

$$E = \frac{C_o (V_o^2 - V_{o,min}^2)}{2}$$
(3-56)

A value for the output capacitor can be determined as follows:

$$C_o \ge \frac{2P_o T_h}{\left(V_o^2 - V_{o,min}^2\right)} \xrightarrow{\text{yields}} \frac{2 * 1000 * 0.02}{(400^2 - 350^2)} = 1.06 \, mF$$

3.4.2.3 Design Procedure for Main Switches S₁ and S₂

The two main factors that should be considered in designing the main boost switches are the maximum current flowing through them and the maximum voltage across them. As was shown in the equations, the maximum current through the main boost switches is less than the maximum current through the input inductors:

$$i_{S1,max} = i_{S2,max} < i_{L1,max} = i_{L2,max} < i_{in,max} = \frac{\sqrt{2} P_o}{\eta V_{in}} \xrightarrow{\text{yields}} \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 \text{ A}$$

The second parameter is the maximum voltage across the main boost switches. It was shown in Mode 6 that the maximum voltage across the main switch is clamped to the output voltage so that

$$V_{S1,max} = V_{S2,max} = V_o = 400 \text{ V}$$

STGP 10NC60KD IGBT devices with 400 peak voltage stress and 20 A peak current stress are selected as the main boost switches.

3.4.3 Design Procedure for the Auxiliary Power Circuit

The key auxiliary components that need to be designed are one auxiliary switch (S_a), two auxiliary inductors (L_{r1} and L_{r2}), the resonant capacitor (C_r), and the auxiliary transformer.

Figs. 3.11-3.18 show graphs of main switch current vs time and auxiliary switch current vs time for various parameters. Fig. 3.11 and Fig.3.12 show graphs for the main switch current versus time and the auxiliary switch current versus time with fixed values of L_{r1} , L_{r2} , and N with varying values of C_r . Fig. 3.13 and Fig.3.14 are graphs with fixed values of C_r , L_{r1} , and N, with varying values of L_{r2} . Fig. 3.15 and Fig. 3.16 are graphs with fixed values of C_r , L_{r2} , and N, with varying values of L_{r1} . Fig. 3.17 and Fig. 3.18 are graphs with fixed values of C_r , L_{r2} , and L_{r1} , with varying values of N. Each of the graphs in Figs. 3.11-3.18 are drawn with the start of Mode 3 as t = 0 as this is when current begins to be diverted from the main switch after the auxiliary switch has been turned on, which happens during Mode 2. For all of the curves in the graphs, current falls after t = 0. If a current curve in these graphs reaches zero or becomes negative, this is an indication of ZCS because this means that the current in the switch can be removed and/or current can flow in the body-diode of the switch device. If a current curve cannot reach zero, this is an indication that current cannot be fully removed from a switch so that that switch cannot turn off with ZCS.

A. Resonant Capacitor (C_r)

In order to have less voltage stress on the auxiliary switch, the peak auxiliary switch voltage (V_{cr}) is designed to be approximately 450 V, as determined from equ. (3-51). This value was chosen by considering the fact that the auxiliary switch is not directly connected across the anode of a boost diode and ground. It should be noted that this voltage would be much higher if there was no transformer (T_a) to help transfer energy to the output.

In Fig. 3.11 and Fig. 3.12, it can be seen that by decreasing the value of the resonant capacitor (C_r), the maximum current through the auxiliary switch is decreased, but the ZCS condition of the main switches is lost as the current cannot fall to zero.



Fig. 3.11. Effect of increasing the Cr on the ZCS conditions for S1,2

 C_r should impose a negative voltage across resonant inductor L_{r2} after S_a is turned on to allow current to be transferred away from either S_1 or S_2 before a turn-off occurs to ensure that it is done with ZCS. A negative voltage across C_r allows current to be diverted away from a main switch to C_r . C_r should be large enough to ensure that its voltage does not become positive as this transfer of current is taking place, but not too large as this will force the auxiliary switch to be on for a longer amount of time, thus increasing its losses.

According to Fig. 3.11 and fig. 3.12, C_r should be greater than 8 nF in order to ensure that the main switches and the auxiliary switch can turn on with ZCS – the main switches will not be able to turn on with ZCS if C_r is less than 8 nF. C_r should not be too large, however, as this would increase the peak current stress and slow down the transfer of current away from the auxiliary switch, which would require that the auxiliary switch be on longer, thus increasing the RMS current stress and conduction losses. In order to have an appropriate margin for ZCS and maintain the maximum current through the auxiliary switch between 18-22 Amps, C_r is chosen to be 12 nF.



Fig. 3.12. Effect of increasing the C_r on the ZCS conditions for S_a

B. Resonant inductor (L_{r2})

With a value of C_r chosen and the maximum auxiliary switch current set to be 22 A, as described at the start of this section, a value of L_{r2} can be determined as follows:

$$i_{samax} = \frac{V_{cm}}{Z_2} = \frac{V_{cm}}{\sqrt{\frac{L_{r2}}{C_r}}} = 22 A$$
$$22 = \frac{450}{\sqrt{\frac{L_{r2}}{\int_{12e^{-9}}}}} \rightarrow L_{r2} = 4.9 \,\mu H$$

This value of L_{r2} is a preliminary value that can only be set in conjunction with L_{r1} , which will be described next.

C. Resonant inductor (L_{r1})

The choice of L_{r1} can be made by using the graphs of L_{r2}/L_{r1} in Figs 3.13-3.16. As can be seen from Fig. 3.13 and Fig. 3.14, the ratio of L_{r2}/L_{r1} should be small enough to minimize the time that the auxiliary switch is on, thereby reducing RMS switch current stress and conduction losses. It should, however, also be large enough to reduce the auxiliary peak current.



Fig. 3.13. Effect of increasing the Lr2 on the ZCS conditions for S1,2



Fig. 3.14. Effect of increasing the Lr2 on the ZCS conditions for Sa



Fig. 3.15. Effect of increasing the Lr1 on the ZCS conditions for S1,2



Fig. 3.16. Effect of increasing the L_{r1} on the ZCS conditions for S_a

Based on the characteristic curves in Fig. 3.15 and Fig. 3.16, the value of L_{r1} should be greater than that of L_{r2} . This is because the current through L_{r1} should be less than current through L_{r2} in Mode 3 of operation to divert the current from the auxiliary circuit and turn it off with ZCS. In other words, L_{r2}/L_{r1} should be less than 1 because the auxiliary switch will not be able to turn off with ZCS otherwise. L_{r2}/L_{r1} should not be too small, however, as it would cause the maximum current through the auxiliary switch to increase. As a result, a ratio of $L_{r2}/L_{r1} = 0.95$ is chosen to have lower peak current but maintain ZCS. Knowing the ratio and that $L_{r2} = 4.9 \ \mu\text{H}$, L_{r1} can be set to be 5.15 μH .

$$L_{r1} > L_{r2} \rightarrow L_{r1} = 5.15 \,\mu H$$

D. Transformer (Ta) Turns Ratio (N)

The value of N, defined as the ratio of N_2/N_1 , cannot be too large or too small as the converter switches will not be able to operate with ZCS in either case. As shown in Fig. 3.17 and Fig. 3.18, by increasing the value of N, the ability of the auxiliary switch to turn off with ZCS is reduced as the current in the switch becomes less likely to fall to zero.



Fig. 3.17. Effect of increasing the N on the ZCS conditions for S1,2



Fig. 3.18. Effect of increasing the N on the ZCS conditions for Sa

According to Fig. 3.18, the auxiliary switch cannot be turned off with ZCS if N > 5. If too small of a value for N is chosen (e.g. N < 3), however, the ZCS condition for the main switches will be lost because the counter voltage produced at the transformer's primary will be too high. It will then counteract the voltage across C_r to such an extent that the full amount of the main switches' current will not be diverted. As a result, the value of N should be between 3 and 5.

Fig. 3.19 shows the power that the transformer transfers to the load for different turns ratios. It can be seen from this graph that as N is decreased, the transformer must handle more power and thus must be made larger. As a result, if the range of N that allows the converter switches to operate with ZCS is between 3 and 5, then a value of N = 5 should be chosen to minimize the amount of power that the transformer must handle and thus its size.



Fig. 3.19. Auxiliary transformer power vs turns ratio.

E. Operating Time of the Auxiliary Switch

The time that the auxiliary switch operates, which is the time it needs to perform ZCS for itself and the main switches, was derived in equ. (3-29). By substituting in the values of the parameters that have been chosen in this section: L_{r1} = 5.15 µH, L_{r2} = 4.9 µH, N=5, C_r =12 nF, and the V_{cm}=450 V, the time that the auxiliary switch needs to perform ZCS for main switches and itself is found to be equal to 0.6 µs.

$$t_{isa-on\,time} = 2 * \frac{\pi - tan^{-1} \left(\frac{450w_e^2 Z_e}{V_X w_1^2 Z_2}\right)}{w_e} = 0.6 \,\mu s$$

3.5 Comparison of Power Losses

The key power losses of the converter are discussed in this section (only the key power losses are covered to simplify the discussion). The loss analysis of the proposed converter is made based on three main sources of losses: conduction losses, switching losses and transformer losses. In addition, a comparison is made for the proposed converter when it works with ZCS and without ZCS. There are three main sources of conduction losses in the proposed converter: power losses in IGBT devices, power losses in diodes (e.g. device body diodes, output, and auxiliary diodes), and transformer winding losses. Switching losses will be considered only when the converter is operating without ZCS. The conduction losses of the inductors are not considered here. These losses can be reduced using inductors with high quality factor, but with higher cost as well. More details will be explained as follows:

A. Conduction Losses of the IGBT Transistors

In the proposed converter, there are two main switches and one auxiliary switch and the power dissipated when current is flowing through the IGBT switches can be determined from

$$P_{c} = \frac{1}{T_{s}} \int_{0}^{T_{s}} P_{c}(t) dt = v_{CE0} I_{savg} + r_{c} I_{srms}^{2}$$
(3-57)

 T_s is the switching cycle, V_{ceo} is the collector-emitter saturation voltage, r_c is the collector resistor when the transistor is turned on, I_{savg} is the collector's average current, and I_{srms} is the collector's RMS current. The conduction losses of the main switches (S₁ and S₂) can be determined by

$$P_{c_m} = 2(v_{CE0}I_{sm_avg} + r_c I_{sm_rms}^2)$$
(3-58)

 $I_{sm_{avg}}$ and $I_{sm_{rms}}$ can be determined by integrating the current waveform of each main switch in DCM operation for a conventional boost converter as follows:

$$I_{sm_avg} = \left(\frac{V_{in}D_1}{L_{in}f_s}\right) \left(\frac{D_1}{2}\right)$$
(3-59)

$$I_{sm_rms} = \left(\frac{V_{in}D_1}{L_{in}f_s}\right) \sqrt{\frac{D_1}{3}}$$
(3-60)

 V_{in} is the input voltage, L_{in} is the input inductor for one leg, D_1 is the duty cycle during on time, and f_s is the switching frequency for main switch. The values of v_{co} and r_c can be determined by the transistor specifications. The other conduction loss is the power loss in the auxiliary switch (S_a), and it can be determined by using:

$$P_{c_a} = v_{CE0} I_{sa_a vg} + r_c I_{sa_r ms}^2$$
(3-61)

 I_{sa_avg} and I_{sa_rms} are the average and RMS collector currents for the auxiliary switch and they can be calculated as follows:

$$I_{sa_ang} = \frac{1}{T_s} \left(\int_{t_1}^{t_2} i_{sa}(t) dt + \int_{t_2}^{t_3} i_{sa}(t) dt \right)$$
(3-62)

$$I_{sa_{rms}} = \sqrt{\frac{1}{T_s} \left(\int_{t_1}^{t_2} i_{sa}^2(t) dt + \int_{t_2}^{t_3} i_{sa}^2(t) dt \right)}$$
(3-63)

It should be noted that i_{sa} during the time interval t_1 to t_2 , is determined by equ. (3-11) and i_{sa} during the time interval t_2 to t_3 is determined by equ. (3-48b).

B. Conduction Losses of the Diodes

The power dissipated when current is flowing through the body diodes of the converter switches and through the output and auxiliary diodes can be determined by multiplying the average value of the current (I_{Favg}) by the forward voltage drop (V_F), as follows:

$$P_{CD} = V_F I_{Favg} \tag{3-64}$$

In the proposed converter, the body diodes of the IGBT devices conduct for a very small amount of time, thus, the conduction losses in these diodes will be neglected in this analysis. The total conduction losses of the diodes in the proposed converter is

$$P_{C_D} = 2(V_{F_{D_1}}I_{Favg_{D_1}}) + 2(V_{F_{Da_1}}I_{Fav_{Da_1}}) + V_{F_{Da_3}}I_{Fav_{Da_3}} + V_{F_{DT_1}}I_{Fav_{DT_1}} + V_{F_{DT_2}}I_{Fav_{DT_2}}$$
(3-65)

C. Transformer Losses

Two kinds of transformer losses will be considered in this analysis: core loss and copper (winding) loss. The core loss depends on the size of the transformer, therefore the transformer's size will be selected first. The core size of the transformers in the proposed converter can be selected by using:

$$A_P = \frac{P_t(10^4)}{K_f K_u B_m J f_{sw}}$$
(3-66)

 A_p is the area product, B_m is the density, J is the current density, K_u is the window utilization factor, K_f is the waveform coefficient, f_{sw} is the switching frequency, and P_t is the transformer's apparent power. In this design ETD 29 is selected to be the cores of the auxiliary transformer. The transformer's core losses can be estimated from the manufacturer's datasheet and the transformer's ohmic losses can be estimated as

$$P_{wind-Tr} = \left(R_{pri}l_{prms}^2 + R_{sec}l_{srms}^2\right) \tag{3-67}$$

 R_{pri} and R_{sec} are the primary and secondary winding resistances for the auxiliary transformer, respectively. I_{prms} and I_{srms} are the primary and secondary RMS currents for the auxiliary transformer, respectively.

D. Switching Losses

During a switching transition, there is an overlap between the voltage across the switch and the current flowing through it and it is this overlap of voltage and current that creates losses. Switching losses of IGBT devices in the proposed converter will only be considered in this analysis when the auxiliary circuit is deactivated because there are no switching losses when the auxiliary circuit is engaged. There are two types of switching losses: turn-on losses and turn-off losses. The switching losses for one of the main switches is represented as:

$$P_{sw} = (E_{on} + E_{off})f_{sw} \tag{3-68}$$

where E_{on} is turn-on energy, E_{off} is turn-off energy, and f_{sw} is the switching frequency. Since the proposed converter works under DCM mode of operation, the turn-on losses will not be considered as the switches always turn on with ZCS. In other words, the proposed converter only has turn-off losses when it works without the auxiliary circuit, which are the dominant losses in IGBTs. The turn-off losses can be calculated as follows:

$$P_{sw} = \left[\left(A_{off} I_c + B_{off} \right) Z \right] f_{sw}$$
(3-69)

$$Z = \frac{E_{off(R_{guser})}}{E_{off(R_{gdatasheet})}} \frac{V_{DCoff(user)}}{V_{DCoff(datasheet)}} \frac{E_{off(T_j)}}{E_{off(T_{jmax})}}$$
(3-70)

 A_{off} and B_{off} are parameters that can be calculated by using the datasheet of the IGBT transistor such as in [54]. I_c is the collector current when the switch is turned off. Since the gate resistor of the gate driver used in this paper does not have the same value as the gate resistor in the test circuit specified in the datasheet, the actual values of the gate driver are considered. $E_{off(Rguser)}$ is the turn-off energy of the actual gate resistor, $E_{off(Rgdatasheet)}$ is the turn-off energy from the datasheet. $V_{DCoff(user)}$ is the actual collector voltage when the switch is turned off, $V_{DCoff(datasheet)}$ is the collector voltage in the datasheet. $E_{off(Tjmax)}$ is the turn-off energy at the operating temperature, and $E_{off(Tjmax)}$ is the turn-off energy at maximum temperature.

E. Power Loss Comparison

In this section, a loss comparison between the proposed converter operating with and without the auxiliary circuit (conventional interleaved converter) is presented. The comparison is made at full load and 20% of rated power and is based on different power losses: conduction of the switches (PC_S), switching (Poff), conduction of the diodes



(PC_D), transformer (PTr), and other losses. The power loss breakdown for each converter is shown in Fig. 3.20.

Fig. 3.20. Loss comparison for the proposed converter and the converter without ZCS. (a) rated load, (b) 20% load.

It can be seen that at a light load, the hard-switching converter is more efficient, while at rated power, the proposed soft-switching converter has considerably better efficiency than the standard hard-switching converter (close to 60 W reduction in switching losses). Since the proposed converter has the capability to operate with hard-switching at light loads and operate with soft-switching at heavier loads, high converter efficiency can be maintained throughout the load range.

3.6 Converter Features

The features of the proposed converter are reviewed in this section. The features that are discussed in this section address the eight drawbacks that were stated in the Introduction of this chapter.

a) The proposed converter has only one auxiliary circuit that helps the main switch in both modules turn off with ZCS. Although this circuit may seem complex, the

number of passive elements in the circuit is comparable to that of two previously proposed active circuits, and there is just one active switch instead of two.

- b) There is no auxiliary circuit component in the main current path, so less expensive, lower current and power rated devices can be used as auxiliary circuit components.
- c) The auxiliary circuit does not inject current into the main converter switches, as is the case with resonant-type auxiliary circuits in other ZCS-PWM converters. This is because there is a blocking diode for each module that prevents the auxiliary circuit from doing so. This makes the current stresses of the main switches the same as those of the main switches of a hard-switching PWM boost converter.
- d) The auxiliary switch has a ZCS turn-on because inductor L_{r2} limits the rise of current that starts to flow through it when it is turned on and has a ZCS turn-off as described in Mode 3.
- e) If desired, the auxiliary circuit does not have to be used when the converter is operating under light-load conditions. This is unlike many ZCS-PWM converters that require the auxiliary circuit to be used even under light-load conditions, where it is actually detrimental as it has components in the main path of the circuit. This helps improve light-load efficiency.
- f) Energy that is pumped into the auxiliary circuit is not trapped inside it because the auxiliary circuit transformer provides a mechanism by which some of it can be removed through diodes D_{T1} and D_{T2}. Without the transformer, energy that is pumped into the auxiliary circuit from the main modules would have to be dissipated in the auxiliary circuit, which would create losses.
- g) The boost diode in each module has a lower peak voltage stress that that found in other previously proposed ZCS-PWM converters with resonant auxiliary circuits. This is because, the auxiliary circuit transformer makes the voltage of the anode less negative since it provides a counter-voltage to the voltage across resonant capacitor (C_r).
- h) The RMS current stress of the auxiliary switch is significantly less than that found in other ZCS-PWM converters. This allows the auxiliary circuit to be implemented in a two-module interleaved boost converter and to assist both of the main converter switches to turn off with ZCS. Also, it does so while allowing the converter to

operate at a higher power level than other previously proposed interleaved ZCS-PWM converters.

A more detailed explanation of the final feature is given here. In ZCS-PWM converters, current must be gradually diverted away from the main switch for it to turn-off with ZCS. If the current transfer is performed too quickly, the main switch IGBT will not have a soft turn-off due to residual charge in the device. In converters where a snubber capacitor is connected across the main switch/series inductor, the snubber capacitor voltage can swing to as high as $-V_0$. If this voltage swing from V_0 to $-V_0$ is too fast, then the current diversion away from the main switch will be too fast as well. As a result, this voltage swing needs to occur gradually, which means that the snubber capacitor needs to be discharged gradually. The auxiliary switch, therefore, must conduct current for some time (but not as long as the main switch) in order for the main switch to turn off with ZCS.

In the proposed converter, since the transformer in the auxiliary circuit in placed in series with capacitor C_r , where it acts like a counter voltage source, the current transfer will automatically be more gradual as the net voltage across L_{r1} is reduced. C_r can thus be discharged more quickly so that the polarity of its voltage swings to negative, which allows current to be diverted away from a main switch. As well, the counter voltage produced by T_a prevents this capacitor from then being charged too quickly and causing the time window for ZCS to be lost. As a result, the auxiliary switch in the proposed converter does not have to stay active for as long as the auxiliary switch in other ZCS-PWM converters because it can be used just to quickly discharge C_r . RMS current stress is lower and cheaper so a lower current-rated device can be used as the auxiliary switch. Even more important, given the fact that the auxiliary switch is activated twice during a switching cycle, as stated in the Introduction, it allows the proposed multi-module converter to operate at higher power levels despite having one auxiliary switch. This is in comparison to other previously proposed interleaved multi-module ZCS-PWM converters that that have just one auxiliary switch.

Table 3.1 shows a list of previously proposed ZCS-PWM converters that use auxiliary switch to perform ZCS. The key things to note from this table are as follows:

Reference	BC/IBC ⁽¹⁾	Features								T _{aux-}	P _{kW}
		Α	В	C	D	Е	F	G	Н	μs ⁽²⁾	
[15]	IBC	~	~	~	×	~	×	~	×	3	0.6
[17]	IBC	×	~	~	~	~	×	~	×	3	1.2
[18]	IBC	~	×	×	~	×	×	×	×	1.5	0.5
[20]	IBC	~	×	~	>	×	×	~	×	14	0.25
[21]	IBC	~	×	×	>	×	×	×	×	2.5	0.25
[22]	BC	-	×	×	>	×	>	×	×	2	1
[23]	IBC	~	×	×	>	×	>	×	×	7	1
[25]	BC	-	×	~	~	×	×	~	×	0.6	0.3
[26]	IBC	~	×	×	~	×	×	×	×	0.6	0.2
[27]	IBC	~	×	×	~	×	~	~	×	1.5	0.12
[28]	BC	-	×	×	~	×	>	×	×	16	0.7
[30]	BC	-	×	×	~	×	>	×	×	10	1
[34]	BC	-	×	~	~	×	>	×	×	4	2.5
[55]	BC	-	×	~	~	×	~	~	×	8	0.25
[56]	BC	-	×	~	~	×	~	~	×	4	0.5
Proposed Converter	IBC	~	~	~	~	~	~	~	~	0.6	1

 Table 3.1 Comparison of ZCS-PWM converter features

- Table 3.1 includes references to ZCS-PWM converters that consist of just one module and are non-interleaved. This is to examine whether these converters can be adapted to two-module interleaved converters.
- The proposed converter is the only converter that has all eight of the features that are discussed in this section.
- The conducting-time of the auxiliary switch after it has been activated is much less than that of almost all the other converters, as can be seen in the second last column. With some of the other converters, the conducting-time is so long that the auxiliary circuit must handle a considerable amount of power. If lower power-rated components are used in the auxiliary circuit, this places limitations on the power that the converter can operate with, as can be seen in the last column. It should be noted that non-interleaved ZCS-PWM converters cannot be adapted for use in ZCS-PWM interleaved converters if the auxiliary switch conducting-time is significant.

3.7 Experimental results

A prototype of the proposed converter was built to confirm its feasibility. The prototype was built with the following specifications as indicated at Table 3.2: Input voltage $V_{in} = 85-265 V_{rms}$, output voltage $V_o = 400 V_{dc}$, switching frequency $f_{sw} = 50 \text{ kHz}$, and maximum output power $P_{o,max} = 1 \text{ kW}$. The picture of the prototype, which is a simple proof-of-concept prototype, is shown in Fig. 3.21 and the experimental results are shown in Figs. 3.22- 3.28.



Fig. 3.21. Prototype Picture

Symbol	Item	Value
V _{in}	Input voltage	85- 265 Volts
Vout	Output voltage	400 Volts
P _{o,max}	Maximum output power	1000 W
P _{o,min}	Minimum output power	200 W
f _{sw,main}	Main switches frequency	50 k HZ
f _{sw,aux}	Auxiliary switch frequency	100 k HZ
S ₁ , S ₂	Main switches	K20H603
Sa	Auxiliary switch	K20H603
L_1, L_2	input inductors	120µН
Co	Output capacitor	1000µF
D ₁ , D ₂	Output diodes	40EPF06
$\begin{array}{c} D_{a1}, D_{a2},\\ D_{a3} \end{array}$	Auxiliary diodes	40EPF06
D_{T1}, D_{T2}	Output auxiliary diodes	LXA20T600
Cr	Auxiliary capacitor	12nf
L _{r1}	Auxiliary inductance	5.15 μΗ
L _{r2}	Auxiliary inductance	4.9 μΗ
n	The turns ratio of the auxiliary transformer	1:5:5

 Table 3.2 Specification of the converter components

Fig. 3.22 shows typical input voltage and input current waveforms. It can be seen that the input current is sinusoidal, in phase with the input voltage, and continuous. Fig. 3.23 shows current waveforms for input boost inductors L_1 and L_2 . It can be seen that these currents are discontinuous and identical. Fig. 3.24 shows the interleaved current that is a sum of the currents in L_1 and L_2 .

Typical current and gating signal waveforms for one of the main switches are shown in Fig. 3.25. It can be seen that the switch can be turned on and off with ZCS, without a current tail, because the current through the switch goes to zero before turning off. The same waveforms are shown in Fig. 3.26 for the auxiliary switch, and it can be seen that the auxiliary switch turns on and off with ZCS as well. Fig. 3.27 shows the voltage and the current of one of the main boost diodes where the maximum voltage of the diode is clamped to the output voltage, which is 400 V. Fig. 3.28 shows the voltage across the auxiliary capacitor which is less than 450 V as discussed in the design procedure.

It should be noted that there is some voltage oscillation in the waveforms of Fig. 3.25 and 3.28 when one of the main switches is turned on. This oscillation is caused by the interaction of the input inductor and the output capacitance of the main switch in a module. This phenomenon arises when the input inductor current of a module is discontinuous. It has nothing to do with the proposed auxiliary circuit and can be found in any boost converter operating with a discontinuous input current. A full explanation of this phenomenon can be found in [33].

Efficiency measurements show a maximum converter efficiency above 97% that is caused by a 70 W reduction of switching losses, which is close to the 60 W reduction that was predicted by the loss analysis, and by improvement in light-load efficiency by 4 % when the auxiliary circuit is disengaged. Fig. 3.29 shows an efficiency comparison of the proposed ZCS-PWM. The interleaved boost converter and a conventional hard switching PWM interleaved boost converter were implemented on the same prototype, one with the auxiliary circuit and one without.



Fig. 3.22. Input current and input voltage



Fig. 3.23. Input inductors currents



Fig. 3.24. Interleaved current



Fig. 3.25. S₁ current and voltage



Fig. 3.26. S_a current and voltage



Fig. 3.27. D₁ current and voltage



Fig. 3.28. Cr voltage



Fig. 3.29. Interleaved boost converter efficiency with input voltage V_{in} =85 V and output voltage V_0 =400 V.

As can be seen from Fig. 3.29, the efficiency of the conventional converter is decreased by increasing the load, whereas the efficiency of the proposed converter is increased. The proposed converter has a significantly better efficiency than the conventional PWM boost converter above 40% of the full load, which is 1 kW, and its efficiency is consistently about 95%. The main reason for this, is that the auxiliary circuit losses dominate when the converter is operating under light loads.

Auxiliary circuit losses include turning on and off the auxiliary switch and additional conduction losses as there can be an increased amount of circulating current flowing in the converter. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads, when the eliminated switching losses of the main switches - especially the IGBT current tail losses - are greater than the auxiliary circuit losses. It should be noted that it is possible with the proposed converter to operate the converter with hard-switching when the converter is operating with light loads and with ZCS when it is operating with heavier loads, so that the converter can operate with "maximum" efficiency throughout the entire load range.

The proposed converter needs only one auxiliary circuit with just one active switch to help the two main converter switches turn off with ZCS. This auxiliary circuit does not need to be used when the converter is operating with light loads and its switch can be turned on or off with ZCS. None of its components are in the main path of the current of any of the modules so cheaper, lower current and power rated devices can be used as auxiliary circuit components. Blocking diodes prevent the auxiliary circuit from injecting current into any of the main switches.

- The proposed converter has a transformer in its auxiliary circuit. This transformer allows energy that would otherwise be trapped in the auxiliary circuit to be transferred to the load.
- Since there are no auxiliary components in the path of the main boost diodes, the peak voltage stress across them is clamped to the output voltage. This is significantly less than the voltage stress of two times V_o found in some other ZCS-PWM converters.

 The auxiliary circuit transformer helps reduce the RMS current stress of the auxiliary switch. Due to how the transformer is placed in the auxiliary circuit, the on-time of the auxiliary switch and thus its RMS current stress can be reduced significantly. For the proposed converter, an on-time of 0.6 µs was used, which is much less than the on-time typically found in other ZCS-PWM converters.

To the best knowledge of the authors, no other presently existing ZCS-PWM interleaved boost converter has all these features.

It should also be mentioned that it is the existence of transformer T_a , and its appropriate placement in the auxiliary circuit, that allows the auxiliary switch to be implemented with a lower on-time than the auxiliary switches in other previously proposed interleaved ZCS-PWM boost converters. The transformer puts a counter voltage in the resonant circuit path that slows down the transfer of current away from the main circuit module switches. Due to this, the auxiliary switch needs to be on for only a very short amount of time to quickly change the polarity of C_r. As a result, it is possible to implement an interleaved AC-DC boost converter with just one auxiliary circuit for heavier loads because the auxiliary switch will not have severe RMS stresses. This removes the need for a second auxiliary circuit, so that any increase in cost, size, and weight due to T_a is more than offset by the elimination of a second auxiliary circuit.

3.8 Conclusion

A new AC-DC interleaved ZCS-PWM converter is proposed in this chapter. In the chapter, its operating principles, modes of operation, and features were discussed. An analysis of the converter's steady-state operation was performed, and the results of the analysis were used to generate graphs of characteristic curves for various parameters that were then used to develop a design procedure. The design procedure was demonstrated with an example and the results of the example were used to implement a proof-of-concept experimental prototype that confirmed the feasibility of the converter.
4 A Novel ZCS PWM Buck Converter with Improved Light-Power Efficiency in Wind Power Systems

4.1 Introduction

There is a growing worldwide demand for increasing the penetration of renewable energies and reducing the emissions of greenhouse gases. In places where the transmission infrastructure is weak or there are no centralized utility grids, and in rural areas where building transmission lines is not cost-effective, off-grid stand-alone wind turbine have a vital role to play in generating on-site electricity. Based on the International Renewable Energy Agency (IRENA), an estimated 1.16 billion people (17% of the world's population) currently live without access to electricity. This creates a large market for off-grid distributed renewable systems where wind turbines can be a cost-effective replacement for diesel generators or can be used in tandem with diesel generators. Either option would reduce fuel consumption and as a result decrease the emission of Greenhouse gases, creating an important market for off-grid wind power systems specifically in residential applications.

Small wind turbines used in residential applications typically range in size from 400 W to 20 kW [57]. These small wind turbines can lower the price of energy by 50%–90% by avoiding the high costs of having utility power lines extended to a remote location or operating a diesel generator 24/7. Small wind electric systems can also be used for a variety of other applications, including water pumping on farms and ranches [58]. Thus, there is a significant trend toward using these small wind turbines around the world (1100 MW) and in north America (170 MW) [59].

In order to increase their reliability, energy storage systems (ESSs) such as batteries are often used with wind turbines as a hybrid system [60]. Therefore, power converters such as buck or boost should be implemented to decrease or increase the output voltage of the wind turbine to the batteries' level, which usually is in the range of 24-48 V. The overall cost of batteries is high due to the high capital cost, maintenance, and short lifetime. Thus,

to reduce the project cost in low power applications, only one or two batteries are used so the voltage is low and a buck converter is needed. In higher power applications, it is likely to connect several batteries in series to form higher voltages, therefore boost converters are used. In this section, a small wind turbine for a low power, standalone home is discussed so a buck converter will be covered.

Two module buck converters, such as the ones shown in Fig. 4.1.a, are implemented to decrease the current stress of each switch and to charge the batteries faster with higher current. Fig. 4.1.a shows a standard interleaved buck converter where AC input voltage is stepped down to charge the ESS. The main buck switches, in addition to their traditional duties, can be used for maximum power point tracking (MPPT) and S_b is used to control the charging of the batteries, as discussed in [60]. Fig. 4.1.b shows a stand-alone wind turbine which charges its batteries with a buck converter.

These converters operate with a high frequency, therefore, it is beneficial to implement soft-switching features to reduce the switching losses. Soft-switching methods for these converters can either be zero-voltage switching (ZVS) if they are implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. Although recently developed wide bandgap devices represent the future of semiconductor technology, silicon (Si) IGBTs are still widely used in converters such as the one in Fig. 4. 1.a. This is because they are thought to be cheaper, more readily available, and more reliable; they also have fewer conduction losses than MOSFETs. Si-IGBTs, however, have a turn-off current tail that overlaps with voltage, thus creating considerable turn-off switching losses, unless they are made to operate with zero-current-switching (ZCS) techniques. These techniques typically use an active auxiliary circuit that consists of a relatively low current-rated active switch and passive components to gradually divert current away from an IGBT switch. Doing so allows that device to turn off with no current flowing through the device and thus, no overlapping current tail.

Previously proposed ZCS techniques, however, have at least one of the following fundamental drawbacks that make them unsuitable for use in interleaved buck converters that are used as interfaces in small wind turbine-based energy systems:



Fig. 4.1. Buck converters (a) typical interleaved buck converter [60]. (b) Standalone wind turbine for battery charging.

- Each module of an interleaved buck converter must have its own auxiliary circuit to help its main switch turn off with soft switching. This adds cost to the overall interleaved converter. [39], [40].
- The auxiliary circuit causes the main converter components, such as diodes, to operate with higher peak voltage stresses that create a need for higher rated devices for the main circuitry [36].
- The auxiliary switch must conduct, at minimum, the full inductor current for at least 2-3 μs. Therefore, if it is used twice during a switching cycle, as is the case when only one auxiliary circuit is used in an interleaved buck converter, then the RMS current stress of this switch will be high [36], [42], [61], [62].
- The auxiliary circuit causes the auxiliary switch to operate with a considerably higher peak voltage stress than that of main switches, creating a need for a higher rated device for the auxiliary switch. [36]-[38].
- The auxiliary circuit injects current into the main switches, which increases peak and RMS current stresses. This is typical of resonant-type auxiliary circuits. This creates a need for a higher rated device for the main switch and also increases conduction losses that may offset any gain in efficiency caused by the reduction of switching losses.
- Energy pumped into the auxiliary circuit when it is activated, from the main converter circuit, is trapped in the auxiliary circuit where it is dissipated. There is no path for at least some of this energy to be transferred to the output [36]-[42].
- Auxiliary circuit components must be placed in the main path of the converter so that the auxiliary and main circuits are not completely separated. This means that conduction losses are increased, so higher current rated components need to be used. This also means that the auxiliary circuit can never be disengaged from the main power circuit during light-load operation [36]-[42].

ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads, when the main switch switching losses that are eliminated (especially the IGBT current tail losses) are greater than the auxiliary circuit losses. ZCS-PWM IGBT converters that use an auxiliary circuit to help the main converter switches turn off with

ZCS, however, are generally less efficient than hard-switching converters at low power, such as when the wind speed is low. This is because the auxiliary circuit losses dominate the switching losses when the converter is operating under these conditions. A converter used in a wind turbine must be operated under light power for a considerable amount of time (when the wind speed is low). Ideally, the auxiliary circuit should be activated only when the switching losses are higher than the auxiliary circuit losses, when the wind turbine produces higher power.

In this chapter, a new interleaved buck converter is proposed to improve the performance of the battery charger of a stand-alone wind turbine. The converter uses just a single active auxiliary circuit to assist all the main converter switches with ZCS operation and operates with ZCS itself. This circuit does not increase the peak voltage or current stresses of the main switches and does not have any components in the main path of the current, which results in improved light-power efficiency.

In this chapter, the operation of the converter is explained, equations are derived, its features are discussed, and results obtained from an experimental prototype are presented to confirm the feasibility of the proposed converter. Finally, a case study will be simulated to demonstrate the frequency of times that the converter should be operated at light powers by HOMER-software. It will prove the practicality of the proposed converter in the small wind turbine.

4.2 General Converter Principles and Modes of operations

The proposed AC-DC converter, shown in Fig. 4.2 [63], consists of two buck converter modules: one with L_1 , S_1 and D_1 , the other with L_2 , S_2 and D_2 . it also has one low frequency switch (S_b) used for battery charging as discussed in [60] and the proposed auxiliary circuit. The converter operates with discontinuous current to give enough time for the chemical actions of the battery to stabilize before the next charging period, as recommend in [60], to improve battery charging efficiency; thus both main switches are turned on and off together.



Fig. 4.2. Proposed interleaved AC-DC ZCS-PWM buck converter [63].

The two buck modules are connected to the same auxiliary circuit, which consists of connection diodes (D_{a1} , D_{a2} , D_{a3} , and D_{a4}), a reverse blocking diode (D_{a5}), auxiliary inductors (L_{r1} , L_{r2}), resonant capacitor (C_r), and a center tap feed forward transformer (T_a) which has two diodes (D_{T1} and D_{T2}). The auxiliary circuit is activated whenever main switches are about to be turned off and is active for only a fraction of the switching cycle.

Typical waveforms and circuit diagrams for these modes are shown in Fig. 4.3 and Figs. 4.4 - 4.10, respectively.

The modes of operation are derived based on the following assumptions:

- Since the AC input voltage can be considered to be a DC input source in a very short amount of time, the steady-state analysis is done with DC input voltage.
- The proposed circuit has two boost modules that are designed to be operated in DCM, so the input inductor current of each one will become discontinuous.
- All semiconductor switches are ideal with no parallel capacitor across them.
- All inductors and capacitors are ideal; therefore, they have negligible resistances.
- All diodes are ideal and the reverse recovery time of each of them is zero.



Fig. 4.3. Typical waveforms of the proposed converter

<u>Mode 1 ($T_0 < t < T_1$)</u>: This mode starts with the turning on of S₁ and S₂. The rectified input voltage appears across L₁ and L₂ and their currents rise linearly, as does the currents in the input inductors L₁ and L₂. The slope of the current is $\frac{V_{in}-V_{out}}{L_{1,2}}$. They turn on with ZCS because the current of the inductors is discontinuous.

<u>Mode 2 ($T_1 < t < T_2$)</u>: This mode starts when switch S_a is turned on just before main switches S_1 and S_2 are to be turned off with ZCS. L_{r2} limits the rise of the auxiliary switch current so that this switch turns on with ZCS. C_r begins to resonate with L_{r2} after S_a is turned on, thus the current in inductor L_{r2} rises while the voltage across C_r falls.

<u>Mode 3 ($T_2 < t < T_3$)</u>: This mode starts when the voltage across C_r (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} through D_{a4} begin to conduct, thus the current in inductor L_{r1} rises. D_{T1} starts conducting as well. The current through L_{r2} falls and eventually goes to zero. The currents through the two main switches, S_1 and S_2 , then become negative and flow through the body diodes of the main switches. S_1 and S_2 can be turned off with ZCS during this time. Then the current in L_{r2} reaches zero because of its resonance with C_r ; S_a can then be turned off with ZCS. Energy in L_{r1} is transferred to C_r , which results in the increase of the voltage across this capacitor so that V_{Cr} becomes less negative. V_{Cr} becomes positive sometime during this mode.

<u>Mode 4 ($T_3 < t < T_4$)</u>: This mode begins when S_a is turned off with ZCS. The voltage across V_{cr} keeps increasing. The current through L_{r1} stays constant so the voltage across it is equal to zero. The voltage across the auxiliary capacitor reaches the output voltage at the end of this mode.

<u>Mode 5 ($T_4 < t < T_5$)</u>: This mode starts when the voltage across L_{r1} becomes negative. During this mode, when the net voltage across C_r and L_{r1} becomes equal to the input voltage minus the output voltage, main buck diodes D_1 and D_2 start conducting. When the current through L_{r1} reaches zero, this mode is over.

<u>Mode 6 ($T_5 < t < T_6$)</u>: During this mode, the current in the magnetizing inductance of the feed-forward transformer is discharged to the output through D_{T2} . The voltage across L_1 and L_2 becomes -V₀ and the current through them starts to fall in a linear manner.

<u>*Mode* 7 ($T_6 < t < T_7$)</u>: This mode starts when the current in L₁ and L₂ reach zero. This is the last mode of the operation; the next cycle begins when S₁ and S₂ are turned on under ZCS.

The converter has the following features:



Fig. 4.4. Current flow in Mode 1







Fig. 4.6. Current flow in Mode 3







Fig. 4.8. Current flow in Mode 5









- (i) All the converter's main and auxiliary switches turn on and off with ZCS.
- (ii) There is only one active auxiliary circuit for both of the main buck switches instead of each main switch needing its own active auxiliary circuit to help it turn off with ZCS.
- (iii) The main switches do not have increased peak and rms current stresses, as is the case with resonant type ZCS auxiliary circuits because no current from the auxiliary circuit flows into the main circuit.
- (iv) None of the auxiliary circuit components are in the main power path, so they only handle a fraction of the current that the main circuit components endure.
- (v) The maximum voltage stress of the auxiliary switch is close to the input voltage because of the transformer. Also, the current in the auxiliary circuit can be transferred to the output to increase the efficiency.
- (vi) Since the main inductor currents operate in discontinuous mode, the main buck diodes do not have reverse recovery current.
- (vii) The auxiliary circuit can be deactivated when the converter is operating under light-power conditions, unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load. This leads to an improvement in light-wind power efficiency. This is because no auxiliary circuit, means no auxiliary circuit losses under operating conditions where ZCS is unnecessary. This can be done as there are no auxiliary circuit components in the main power circuit.
- (viii) The auxiliary switch (S_a) does not have to conduct the full current from the power circuit when it is on. It only conducts the smaller amount if current from the discharge of C_r . Moreover, S_a needs to be on for less than 1 µs. Since the auxiliary transformer is not in series with the auxiliary switch, the maximum voltage of the resonant capacitor increases which leads to faster soft switching

for S_1 and S_2 . Also, because L_{r1} is in series with the resonant circuit, the auxiliary switch can go to zero faster.

(ix) Since the converter operates in DCM, there is no reverse recovery current for the main diodes, therefor L_{r1} does not need to be chosen high enough to eliminate it. As a result, small L_{r2} can be chosen which decreases the operating time of the auxiliary switch.

4.3 Circuit Analysis

Mathematical equations of the key modes of operations in steady-state are derived in this section to illustrate the effects of the novel AC-DC PWM buck converter on each component. The method of solving the equations is similar as Chapter 3. The analysis in this chapter is done when S_1 and S_2 are turned on and off simultaneously.

In Mode 1, shown in Fig. 4.3, when switches S_1 and S_2 are turned on, the rectified voltage is applied to $L_{1,2}$ and leads to a gradual increase of the current through the main buck inductors. The slope of $L_{1,2}$ which is equal to the slope of $S_{1,2}$, is increased according to

$$V_{in} = L_{1,2} \frac{dL_{1,2}(t_1)}{dt} + V_{out}$$
(4-1)

By integrating from time T_0 to T_1 , the main switch current can be expressed as

$$I_{S1,2}(t_1) = \frac{V_{in} - V_{out}}{L_{1,2}} (T_1 - T_0)$$
(4-2)

All the input current goes through S_1 and S_2 so that

$$I_{in} = I_{S1} + I_{S2} \tag{4-3}$$

Mode 2 starts when the auxiliary switch (S_a) is turned on in preparation for the ZCS turnoff of main switches S_1 and S_2 . S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases, as shown in Fig. 4.5. By using KVL

$$V_{Cr}(t_2) = L_{r2} \frac{d}{dt} i_2(t_2)$$
(4-4)

By using KCL

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -\frac{d}{dt} q_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2)$$
(4-5)

By substituting equ. (4-5) into equ. (4-4), the following equation can be obtained:

$$V_{Cr}(t_2) = -L_{r2} C_r \frac{d^2}{dt^2} V_{Cr}(t_2)$$
(4-6)

In order to solve the above-mentioned equations, the initial capacitor voltage $V_{cr}(0)$ and the initial auxiliary inductor current $i_{Lr2}(0)$ should be defined. $V_{cr}(0)$ is assumed to be equal to V_{cm} , which is the maximum voltage across the capacitor, and $i_{Lr2}(0)$ is equal to zero in this mode:

$$\begin{bmatrix} \frac{d}{dt} V_{Cr}(t_2) \end{bmatrix}_{t=0} = -\left(\frac{1}{C_r}\right) \begin{bmatrix} \frac{d}{dt} q_{Cr}(t_2) \end{bmatrix}_{t=0} = \left(\frac{1}{C_r}\right) \begin{bmatrix} i_{Lr2}(t_2) \end{bmatrix}_{t=0}$$

$$= 0$$
(4-7)

Substituting equ. (4-7) into equ. (4-6) yields

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 \text{ for } T_1 < t < T_2$$
 (4-8)

By considering the initial conditions:

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2) = C_r V_{cm} \omega_2 \sin \omega_2 t_2$$
(4-9)

$$= \frac{V_{cm}}{Z_2} \sin \omega_2 t_2 \qquad \qquad \text{for} \quad T_1 < t < T_2$$

where, $\omega_2 = \frac{1}{\sqrt{L_{r_2}C_r}}$ and the characteristic impedance of the auxiliary circuit is defined as $Z_2 = \sqrt{\frac{L_{r_2}}{C_r}}$. When the voltage of the resonant capacitor reaches zero, this mode is finished; thus by making equ. (4-8) equal to zero, the duration of this mode can be determined to be

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 = 0$$
 for $t = T_2$ (4-10a)

$$\omega_2 t_2 = \frac{\pi}{2} t_2 = T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2} C_r}$$
(4-10b)

Also, the maximum current through the auxiliary switch can be determined at the end of this mode by the following equation:

$$i_{Lr2}(t_2) = \frac{V_{cm}}{Z_2} \sin \omega_2 \frac{\pi}{2} \frac{1}{\omega_2}$$

$$i_{Lr2}(t_2) = i_{samax} = \frac{V_{cm}}{Z_2} \qquad \text{for } t = T_2$$
(4-11)

Fig. 4.6 shows Mode 3, which begins when the voltage across the resonant capacitor (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} and D_{a2} and then D_{a3} and D_{a4} start to conduct. D_{T1} also starts to conduct, so circulating energy from the auxiliary circuit is transferred to the output in this mode. The current through the auxiliary inductors decreases and goes to zero. The currents through the main buck switches then become negative and flow through their body diodes. As a result, S_1 and S_2 can be turned off with ZCS in Mode 3.

As discussed in Chapter 3, the auxiliary switch (S_a) has to be turned off right after turning off the main switches. The ZCS condition for main and auxiliary switches must be met in this mode of operation.

$$i_{Lr1}(t_3) = i_{Lr2}(t_3) + i_{Cr}(t_3)$$
(4-12)

As was shown at the end of the previous mode, the initial value for this mode for voltage across the resonant capacitor (V_{Cr} (t_2)) and current through the auxiliary inductor (i_{Lr1} (t_2)) are zero. The initial current through the second auxiliary inductor i_{Lr2} (t_2) in this mode is derived as:

$$i_{Lr2}(T_3) = \frac{V_{cm}}{Z_2}$$
(4-13)

Since the blocking diode (D_{a3}) is conducting

$$V_{Lr2} = V_{Cr} \tag{4-14}$$

By applying KVL

$$V_{Lr1} = -(V_{Cr} + V_X) \tag{4-15}$$

The auxiliary transformer primary voltage is clamped to $V_X = V_0/N$, where $N=N_2/N_1$ is the turns ratio.

Differentiating equ. (4-12) results in

$$\frac{d}{dt}i_{Lr1}(t_3) = \frac{d}{dt}i_{Lr2}(t_3) + \frac{d}{dt}i_{Cr}(t_3)$$
(4-16a)

This is equivalent to

$$\frac{V_{Lr1}}{L_{r1}}(t_3) = \frac{V_{Lr2}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3)$$
(4-16b)

By substituting equ. (4-15) into equ. (4-16b), the following equation can be derived

$$\frac{V_{Cr} + V_X}{L_{r1}}(t_3) + \frac{V_{Cr}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(4-16c)

This is equal to

$$\frac{V_X}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r2}}(t_3)\frac{L_{r1}}{L_{r1}} + C_r\frac{d^2}{dt^2}V_{Cr}(t_3) = 0$$

$$\frac{V_{Cr}(L_{r1}+L_{r2})+V_{X}L_{r2}}{L_{r1}L_{r2}}(t_{3})+C_{r}\frac{d^{2}}{dt^{2}}V_{Cr}(t_{3})=0$$

In order to simplify equ. (4-16c), $L_e = \frac{L_{r1}L_{r2}}{L_{r1}+L_{r2}}$ is defined, which results in

$$\frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3) + \frac{V_{Cr}}{L_e}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(4-16d)

This can be rewritten as

$$\frac{V_{Cr}}{L_{eq}}(t_3) = -C_r \frac{d^2}{dt^2} V_{Cr}(t_3) - \frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3)$$
(4-16e)

where $\omega 1,\,\omega e,\,Z_1$, and Z_e are defined as

$$\omega_{1} = \frac{1}{\sqrt{L_{r1}C_{r}}}$$
$$\omega_{e} = \frac{1}{\sqrt{L_{e}C_{r}}}$$
$$Z_{1} = \sqrt{\frac{L_{r1}}{C_{r}}}$$
$$Z_{e} = \sqrt{\frac{L_{re}}{C_{r}}}$$
$$L_{r1} * L_{r2}$$

$$L_e = \frac{L_{r1} * L_{r2}}{L_{r1} + L_{r2}}$$

$$V_{Cr}(t_3) = \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - \frac{(V_{Cm} Z_e)(\sin(w_e t_3))}{Z_2}$$
(4-17)

Using KVL with Fig. 4.6 results in

$$V_{Lr1}(t_3) = -V_{Cr}(t_3) - V_X = -V_{Lr2}(t_3) - V_X$$
(4-18)

Using integration results in

$$i_{Lr1}(t_3) = \frac{(V_{Cm}L_e)(1-\cos(w_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r1}^2} - \frac{V_X t_3}{L_{r1}}$$
(4-19)

Using KVL with Fig. 4.6 results in

$$V_{Cr}(t_3) = L_{r2} \frac{d}{dt} i_{Lr2}(t_3)$$
(4-20)

This is also equal to

$$di_{Lr2}(t_3) = \left(\frac{V_{Cr}}{L_{r2}}(t_3)\right)dt$$
(4-21)

Finally, this results in:

$$i_{Lr2}(t_3) = \frac{V_{Cm}}{Z_2} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r2} w_e^2}\right)$$
(3-22)

In this section, the generalized equations showing the soft switching of the main and auxiliary switches of the N-module buck converter with the proposed ZCS unit are derived.

As can be seen from the Fig. 4.11, the ZCS cell can be implemented to N-module buck converters as follows:



Fig. 4.11. Proposed N-cell ZCS buck converter

During this mode of operation, the current through both main buck switches should go to zero or negative in order to meet the ZCS conditions; thus the direction of current through them are changed and flows through their body diodes.

prerequisite of ZCS of
$$I_{S1,2}$$
: $i_{in}(t_3) - i_{Lr1}(t_3) \le 0$ (4-20)

In other words, the current through the first auxiliary inductor (i_{Lr1}) must be more than the input current $(i_{in}(t))$.

$$\sum_{j=1}^{n} I_{Sj}(t_3) = \left(\sum_{j=1}^{n} I_j(t_3)\right) - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r_1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r_1}^2} - \frac{V_X t_3}{L_{r_1}}\right) \le 0$$
(4-21)

As can be seen from Fig. 4.11

$$I_{Sa}(t_3) = i_{Lr2}(t_3) \tag{4-22}$$

ZCS conditions for the auxiliary switch are met if

prerequisite of ZCS of
$$I_{Sa}$$
: $I_{Sa}(t) = i_{Lr2}(t) \le 0$ (4-23)

This results in

$$i_{Sa}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r2} w_e^2}\right) \le 0$$
(4-24)

In order to find the time of this mode, V_{Lr1} needs to be derived. This can be expressed as

$$V_{Lr1}(t_3) = \frac{(V_{Cm}Z_e)(\sin(w_e t_3))}{Z_2} - \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - V_X$$
(4-25)

As a result, by finding the derivative, which gives the maximum value, t₃ can be derived as:

$$t_{3} = -\frac{\log\left(\frac{\sqrt{\left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)j + \left(\frac{V_{cm}L_{e}}{Z_{2}L_{r1}}\right)^{2}w_{e}^{2} + \left(\frac{V_{X}L_{e}}{L_{r1}^{2}}\right)^{2} - \left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)^{2})}{\frac{V_{X}L_{e}}{L_{r1}^{2}}j - \frac{V_{cm}L_{e}}{Z_{2}L_{r1}}w_{e}}\right)j}{w_{e}}$$
(4-26)

As a result, the entire operation time of the auxiliary switch is

$$t_{isa-on\,time} = t_2 + t_3 \tag{4-27}$$

This results in

$$t_{isa-on\,time} = 2(\frac{\pi - tan^{-1}\left(\frac{V_{cm}w_e^{\ 2}Z_e}{V_Xw_1^{\ 2}Z_2}\right)}{w_e})$$
(4-28)

Since driving the equations and design procedure of this topology can be done in a similar way as the topology that was introduced in Chapter 3, they are not repeated here and only the final key equations related to the soft switching were provided.

By following the design procedure that was introduced in Chapter 3, the following auxiliary components are selected for a 400 Watts buck converter that has $V_{in} = 70V$ and $V_o = 24V$. L_{r1} , L_{r2} , C_r , and T_a , are selected as: 1 µH, 0.95 µH, 20 nF, and 1:3, respectively. Therefore, by substituting in equ. (4-28), t_{aux} is equal to: 0.7 nS.

4.4 Converter Features

The main features of the proposed converters are as follows:

- a) There is only one active auxiliary circuit for both main buck switches instead of each main buck switch needing its own active auxiliary circuit to help it turn off with ZCS. This leads to a less expensive converter.
- b) The main switches do not have increased peak and rms current stresses, as is the case with resonant type ZCS auxiliary circuits, because no current from the auxiliary circuit flows into the main circuit.
- c) The auxiliary switch (S_a) does not have to conduct the full current from the power circuit when it is on. It only conducts the smaller current from the discharge of C_r. Moreover, S_a needs to be on for less than 1 μs. As a result, the proposed dual module converter can operate with heavier loads than previously proposed dual-module converters with just one auxiliary circuit. Previous converters are limited in power due to the stress that these converters induce on the single auxiliary switch in their circuit.
- d) The converter operates with discontinuous current to give enough time for the chemical reactions of the battery to stabilize before the next charging period, as

recommend in [60] to improve battery charging efficiency. As a result, the main switches (S_1 and S_2) turn on with ZCS and the auxiliary circuit is used only to help them turn off with ZCS.

- e) The main buck switches are turned on with ZCS since the converter operates in DCM mode.
- f) The auxiliary circuit can be disengaged when the conduction losses are more than the switching losses. In other words, it can be deactivated when the converter is operating under light-wind power conditions. This is unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the power generation. This leads to an improvement in light-power efficiency.

4.5 Experimental Results

The feasibility of the proposed AC-DC interleaved ZCS-PWM buck converter is validated in this section by the experimental prototype with the following specifications:

Output Voltage: V₀= 24 Volts DC

Output Power: $P_0 = 400$ Watts

Input Voltage: V_{in}= 70 Volts RMS

Switching Frequency for main switches: $f_S = \frac{1}{T_S} = 50$ kHz.

Switching Frequency for auxiliary switch: $f_{Sa} = \frac{1}{T_S} = 50$ kHz.

As discussed in the previous section, the following components should be used for the laboratory prototype:

- Input Inductances $L_{1,2}$: 22 μH
- Main Buck Diodes D_{1,2}: LQA06T300
- Main Switches S_{1,2}: FGAF40N60UFD
- Output Capacitor: 2X560µF 3316(M)
- Auxiliary Switch Sa: FGAF40N60UFD

- Auxiliary Diodes D_{a 1,2,3,4} and D_{T 1,2} : LQA06T300
- Auxiliary Diode D_{a 5}: SF3003PT
- Resonant Inductor L_{r1} : 1 μH
- Resonant Inductor L_{r2} : 0.95 μH
- Resonant Capacitor C_r: 20 nF

A prototype of the proposed converter was built to confirm its feasibility, with the following specifications: $V_{in} = 70$ V to demonstrate the output voltage of the small wind turbine used in [60], $V_o = 24$ V to charge the battery, $f_{sw} = 50$ kHz, $P_{o,max} = 400$ W. Experimental results are shown in Figs. 4.12- 4.14.

Fig. 4.12 shows the gating signal and current of the main switches S_1 and S_2 . As can be seen, both the switches turn on and off together, therefore the auxiliary switch needs to operate only one time in each cycle to maintain the ZCS for both switches. Fig. 4.13 shows typical current and gating signal waveforms for the main switches. As can be seen, they can be turned on and off with ZCS, without a current tail, because the current through the switch is forced to go to zero before turning off. The same waveforms are shown in Fig. 4.14 for the auxiliary switch, and it can be seen that the auxiliary switch turns on and off with ZCS as well. Also, it only needs to operate for a very short amount of time, 0.9 μ s, which reduces both the current stress of the auxiliary switch and losses.

Fig. 4.15 shows an efficiency comparison of the proposed ZCS-PWM buck converter and a conventional hard switching PWM buck converter. Both converters were implemented on the same prototype, one with the auxiliary circuit and one without. As can be seen, efficiency measurements show a maximum efficiency above 96% for the proposed converter, and an improvement in light-power efficiency of 7% when the auxiliary circuit is disengaged.



Fig. 4.12. Main switches S1 and S2 current and gating signals



Fig. 4.13. ZCS for main switches



Fig. 4.14. ZCS for auxiliary switch



Fig. 4.15. Comparative of efficiency graphs between soft-switching and hardswitching for different output loads at input voltage of 70 Volts and output voltage 24 Volts.

4.6 Case Study

In order to demonstrate how the proposed converter's ability to disengage its auxiliary circuit at light loads can save energy for small wind energy systems, a small 400 W wind turbine (scaled down from the 1 kW Future Energy FE1012U model) was modelled using HOMER software. This software can be used to determine how much wind turbine (WT) output power is available during a day or a year and is also used to perform an economic analysis of the hybrid system.

HOMER software acquires solar, temperature, and wind profiles from NASA surface meteorology sources and uses them in its models. For example, Fig. 4.16 shows the annual wind speed profile at the location of the case study used in this work, which is at 7PWJ+43 Raleigh, Chatham-Kent, ON, Canada – a location commonly used to install large and small wind turbines in the southwest area of the Canadian province of Ontario for the year 2020. The horizontal axis of the graph is the date, and the vertical axis shows the corresponding wind speed for each date.

Fig. 4.17 shows the amount of power that can be generated by the 400 W turbine for any particular wind speed. For example, the WT can deliver 400 W rated output power when it is operating with 15 m/s wind speed. By multiplying the data in Fig. 4.16 and 4.17, the graph shown in Fig. 4.18, which is the output power of the wind turbine during each day of the year can be derived. The average value of Fig. 4.18, which is the average output power of the WT, is 107 W. A yearly production can then be obtained by integrating the curve, which is equal to 640 kWh/year (HOMER provides the value).

Fig. 4.19 is a cumulative data graph of the wind turbine at the case study location, obtained by sorting the frequency of time that each power level occurs in Fig. 4.18. The horizontal axis is the maximum output power that the WT produces, and the vertical axis shows the percentage of time during the course of a year that the WT can produce this maximum power.

For example, the WT did not produce any power for 28% of the time under study; this was because the WT speed was less than the cut-in value (4 m/s based on the Future Energy

FE1012U data sheet). Especially important, is the fact that according to the graph in Fig. 4.19, the WT produced an output power of less than 130 W for about 82% of the time under study. Looking at the efficiency graph shown in Fig. 4.15, this means that if the wind energy systems had been implemented with the proposed converter, the converter would have to operate without the auxiliary circuit for 82% of the time under study. This is because 130 W is the amount of output load that is the crossover point between hard-switching and soft-switching operation to maximize converter efficiency. If the converter works with less than 130 W power for 82% of the time, the auxiliary circuit must thus be inactive for 82% of the time and active for only the remaining 18% of the time to maximize converter efficiency.

The difference between the efficiency of the proposed converter when it is operating with hard-switching (η HS) and the efficiency of the converter when it is operating with soft-switching (η SS) versus load is shown in Fig. 4.20. The region where hard-switching results in higher efficiency has been shaded in blue; what is plotted in the blue region is η HS minus η SS. The region where soft-switching results in higher efficiency has been shaded in green; what is plotted in the green region is η SS minus η HS.

If the annual power generated by the wind turbine, which is 640 kWh, is multiplied by the values shown in Fig. 4.19 and the result of this multiplication is adjusted, then a graph such as the one shown in Fig. 4.21 can be plotted.

For example, according to Fig. 4.19, the wind turbine provides no power 28% of the time, which means that it provides some power for 72% of the time (the time mentioned being over the course of 2020 at the WT location). The 640 kWh that the wind turbine generates is generated over a period of time that accounts for 72% of the year. According to the graph in Fig. 4.19, over a period of time that accounts for 55% of the year of 2020 at the WT's location, the WT delivered 50 W of output power or less. Given that the WT did not deliver power for 28% of the time, this means that the WT delivered up to 50 W for 37.5% of the time that it actually produced output power:

$$\frac{This \ period's \ on_time}{72\% \ (Total \ on_time)} x \ 100 = percentage \ of \ this \ period$$
(4-29)

percentage of this period
$$x 640 \ KWh = energy of this period$$
 (4-30)

This results in:

$$\frac{55\% (Total time) - 28\% (Off_time)}{72\% (Total on_time)} x \ 100 = 37.5\%$$

This is equal to:

$$37.5 \% \times 640 \, KWh = 240 \, KWh$$

So 240 kWh of the total 640 kWh that is delivered by the WT was delivered during that time period.

Similarly, according to Fig. 4.19, the WT delivered up to 100 W for 73% of the year. The WT could deliver 640 kWh of output during the time that it delivered power, which was 72% of the time, and it could only provide 50 W output power or less for 55% of the time. This means that the WT could deliver at least 50 W but at most 100 W for 25 % of the time that it could deliver power

$$\frac{73\% - 55\% \text{ (This periode on_time)}}{72\% \text{ (Total on_time)}} x \ 100\% = 25\%$$

This is equal to

$$25 \% \times 640 \, KWh = 160 \, KWh$$

In other words, the WT delivered 160 kWh during 25% of the time that it could produce output power.

If the points of the graph in Fig. 4.20 is multiplied by the points of the graph in Fig. 4.21, then the graph shown in Fig. 4.22 can be obtained. This graph shows the amount of kWh that can be saved by operating the proposed converter with hard-switching for light-load operation and soft-switching for heavy-load operation.

For example, the efficiency improvement of the proposed converter by disengaging at light loads for less than 50 and 100 W are 3.4% and 2.5% respectively. Also, improvement of efficiency at higher power, for example 400 W, due to the activation of the auxiliary circuit to perform the soft switching is 6.9 %. Therefore:

 $221.44 \ KWh \times 3.4\% = 7.53 \ KWh$ $147.2 \ KWh \times 2.5\% = 3.68 \ KWh$ $8.2 \ KWh \times 6.9\% = 0.565 \ KWh$

As can be seen in Fig. 4.21, since the auxiliary circuit has the ability to be engaged and performs ZCS at normal power, where ZCS operation is more efficient, and to be disengaged at light power where the hard switching is more efficient, it is a tailored solution for small wind turbines. This is because they generate low power for a considerable amount of time.



Fig. 4.16. Wind speed profile at the case study location



Fig. 4.17. Wind turbine power curve



Fig. 4.18. Output power of the wind turbine



Fig. 4.19. Cumulative power frequency of the wind turbine



Fig. 4.20. Efficiency comparison at high and light loads



Fig. 4.21. Energy production (kWh) of the wind turbine at light and higher power



Fig. 4.22. Energy (kWh) saving of the wind turbine at light and higher power.
4.7 conclusion

A novel buck ZCS-PWM converter is proposed in this chapter. The advantages of this converter include: full ZCS operation of all converter switches, just one active auxiliary circuit for the two main switches, no additional voltage or current stresses on the main switches, almost no increased peak voltage stress on the auxiliary switch, and the auxiliary switch can be deactivated from the main power circuit at any time to improve low power efficiency. The equations were derived. The feasibility of the converter was confirmed with results obtained from an experimental prototype. The energy that can be saved by using the proposed converter for entire load range was shown using HOMER software.

5 Improvement of DC Nanogrid Energy Performance with a New Multi-Port Converter

5.1 Introduction

Buildings account for approximately 40% of energy consumption in North America and Europe [64]. This consumption, which is continuously expanding, places considerable stress on utility grids. As a result, nanogrids, which are either a cluster of houses or a single house that generate their own power, are becoming more popular as a way of relieving this stress. Nanogrids are mostly powered by hybrid distributed energy resource (HDER) systems that consist of rooftop solar panels, generators, energy storage (batteries), and the grid. Whenever energy from the HDERs is available, it is fed to the buildings and any excess is fed to the grid; when the energy is insufficient to power the buildings, then the missing energy is supplied by the grid. Ideally, the amount of energy absorbed by the grid and the amount supplied by the grid should sum to be zero over time to achieve a net zero energy building (NZEB).

Due to the intermittent nature of solar photovoltaic (PV) generation, HDERs in nanogrids often consist of rooftop solar panels, energy storage (i.e. batteries), and auxiliary generation (i.e., diesel, gas, or fuel cell) that can be on or off the grid to ensure a reliable energy supply. If only solar panels are used, then the levelized cost of energy (LCOE), which is the net present value of the unit-cost of electricity over the lifetime of a generating asset, will be increased and there will be a greater need for energy to be supplied from the grid. It has been demonstrated in literatures that a hybrid system with PV panels, energy storage, and generators is more reliable, cheaper, less stressful to the grid and smaller than a purely solar system [65-66]. But the challenge is that each one of them has different voltages and all need to be converted to specific magnitudes.

Multi-port converters such as the ones shown in Fig. 5.1 should be implemented in the HDER to convert the different input voltages to the different voltage magnitudes. Fig. 5.1.a shows a standard two input converter where a DC source (such as solar panel) and an energy storage (commonly a battery) both supply a DC-bus, while the DC source can charge the ESS as well [67]. Fig. 5.1.b shows a three-input converter where a DC generator, such as proton exchange membrane fuel cell (PEMFC), is used along with solar panels to increase the reliability and reduce the number of solar panels.

These converters operate at high frequencies, therefore, it is beneficial to implement softswitching features to reduce the switching losses. The devices used in the power converters can be traditional silicon (Si) devices or newer wide bandgap devices. Although recent trends indicate that wide bandgap devices will probably replace Si devices in the future, Si devices continue to be used in industrial applications today. They will also continue to be used for some time as they are thought to be cheaper, more readily available, and more reliable for the time being.

For this work, Si-IGBTs are considered as they have fewer conduction losses than MOSFETs in higher current applications. Since the main source of losses in an IGBT device are the turn-off switching losses that result from a current-tail that overlaps with the switch voltage during the turn-off process, it is beneficial to operate IGBTs with zero-current-switching (ZCS) as this can eliminate their turn-off current-tail.

To achieve ZCS for IGBTs, an auxiliary circuit is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS. Previously proposed ZCS methods have at least one of the following drawbacks [43-48], [51]:

- The auxiliary circuit causes the main converter switch to operate with a higher peak current stress, thus requiring a higher rated device for the main switch.
- The auxiliary circuit creates circulating current in the main part of the converter that increases conduction losses, thus offsetting the gain in efficiency caused by the reduction of switching losses.

- Auxiliary circuit components must be placed in the main part of the converter so that the auxiliary circuit is not completely separated from the main converter. This means that conduction losses may be increased so that higher current rated components need to be used.
- Each module of a multi-port converter must have its own ZCS auxiliary circuit to help its main switch turn off with ZCS. This adds cost to the overall multi-port converter. Although some multi-module ZCS-PWM converters with just a single active auxiliary circuit have been proposed, these converters are very limited in power as the auxiliary switch in the circuit is subjected to high stresses.
- Another critical drawback is that ZCS-PWM IGBT converters that use an auxiliary circuit to help the main converter switch turn off with ZCS are generally less efficient than hard-switching converters at light loads. This is because the auxiliary circuit losses dominate when the converter is operating under light-load conditions. ZCS-PWM converters have better efficiency at heavier loads, as the IGBT current tail losses that they eliminate are greater than the auxiliary circuit losses.

The converter used in a multi-port converter will operate under light-power conditions for a considerable amount of time, such as when the solar radiation is low or when the consumer does not need much power. The auxiliary circuit, therefore, should be activated only when the converter is operating with heavier loads and not used when it is operating with light loads.

A new multi-port boost converter is proposed in this chapter to improve the performance of DC nanogrids. The converter uses just a single active auxiliary circuit to assist all the main converter boost switches with ZCS operation and operates with ZCS itself. This circuit does not increase the peak voltage or current stresses of the main switches and does not have any components in the main path of the current, which results in improved lightload efficiency. In this chapter, the operation of the converter is briefly explained, the equations are derived, its features are discussed, and results obtained from an experimental prototype are presented to confirm the feasibility of the proposed converter.



Fig. 5.1. Multiport converters (a) typical multiport converter [67]. (b) three input multiport converter.

5.2 Converter Configurations

The proposed multi-port DC-DC converter, shown in Fig. 5.2, consists of: two DC-DC boost converters for two DC input sources, a bidirectional battery converter for a battery, and a single auxiliary circuit (ZCS cell) that can be used to help all the main boost switches (S_1, S_2, S_3) turn on and off with ZCS.



Fig. 5.2. Proposed ZCS-PWM multiport converter [68].

It should be noted that if a configuration requires the use of more than one switch (S_1 , S_2 , S_3), then the gating signals of these switches should be such that they are all turned off at the same time, as shown in Fig. 5.3. The auxiliary circuit thus needs to be activated just once during a switching cycle.

PV and fuel cell sources are considered as DC Source 1 and 2, respectively, in this chapter. The converter can be operated in various configurations, as shown in Figs. 5.4-5.13, to meet all possible scenarios regarding which DC source (or both) supplies power to the load and whether the battery is being charged, discharged, or is idle.

Relays R_1 and R_2 are used to change to the appropriate configuration of the overall topology when needed and only change their ON/OFF state a few times a day to form the following configurations:

- PVs and batteries supply the load.
- PEMFC and batteries supply the load.
- Battery supplies the load.
- PVs charge the batteries and supply the load.
- PVs supply the load.
- PEMFC supply the load.
- PVs charge the batteries.
- PEMFC charge the batteries.
- PEMFC charge the batteries, PVs supply the load.
- PEMFC, batteries, and PVs supply the load.

For example, in the configuration shown in Fig. 5.4, the PV panels and battery supply energy to the load, the PEM fuel cells do not, and the auxiliary circuit is used if the multiport converter is not operating under light load conditions.

The auxiliary switch is turned on just before turning off the boost switches to divert the current from them and from their body diodes. At this time, the main boost switches can be turned off with ZCS and then the auxiliary switch is turned off exactly after it with ZCS as well. So, the auxiliary ZCS unit needs to operate for a very short amount of time.

Table 5.1 shows the operation of each switch in different configurations of the multi-port converter. It is possible for S_1 , S_2 , S_3 , S_4 , and S_a to operate with ZCS under any one of 26 possible conditions with one exception, where only S_4 can turn on and off with ZCS.

Mode	Topology	S_1	S_2	S_3	S-4	S-a
PV & B to Load	Ι		Yes	Yes		Yes
FC & B to Load	II	Yes		Yes		Yes
B to Load	III			Yes		Yes
PV to B & Load	IV		Yes		No	Yes
PV to Load	V		Yes			Yes
FC to Load	VI	Yes				Yes
PV to B	VII		Yes			Yes
FC to B	VIII	Yes				Yes
PV to B. FC-Load	IX	Yes	Yes			Yes
FC & B & PV to Load	Х	Yes	Yes	Yes		Yes

Table 5.1 ZCS operation of the proposed multiport converter



Fig. 5.3. Gating signals of the proposed converter.







Fig. 5.5. Topology II (FC & Battery to Load)



Fig. 5.6. Topology III (Battery to Load)



Fig. 5.7. Topology IV (PV to Battery & Load)







Fig. 5.9. Topology VI (FC to Load)



Fig. 5.10. Topology VII (PV to Battery)



Fig. 5.11. Topology VIII (FC to Battery)



Fig. 5.12. Topology IX (PV to Battery – FC to Load)



Fig. 5.13. Topology X (PV & Battery & FC to Load)

General Converter Principles and Modes of Operation

5.3

The multiport DC-DC converter shown in Fig. 5.2, consists of: two DC input sources, a bidirectional battery converter, and a single auxiliary circuit to perform soft switching for all the main boost switches (S₁, S2, S₃) and itself. The converter operates with discontinuous current. The two boost modules and the bidirectional boost module are connected to the same auxiliary circuit, which consists of connection diodes D_{a1} , D_{a2} , and D_{a3} , reverse blocking diode D_{a4} , auxiliary inductors L_{r1} , L_{r2} , resonant capacitor C_r , and a center tap feed forward transformer T_a which has two diodes D_{T1} and D_{T2} . The auxiliary circuit is activated whenever the main switches are about to be turned off and is active for only a fraction of the switching cycle. Typical waveforms are shown in Fig. 5.14 and an example of the modes of operation that have the ZCS turn-off operation when all the main switches are on are shown in Figs. 5.15 – 5.21.

The modes of operation are derived based on the following assumptions:

- The proposed circuit has three boost modules that are designed to be operated in DCM, so the input inductor current of each one will become discontinuous.
- All the main switches are turned on and off simultaneously.
- All semiconductor switches are ideal with no parallel capacitor across them.
- All inductors and capacitors are ideal; therefore, they have negligible resistances.
- All diodes are ideal and the reverse recovery time of each one of them is zero.

<u>*Mode 1* ($T_0 < t < T_1$)</u>: This mode starts with the turning on of S₁, S₂, and S₃. Voltage appears across L₁, L₂, and L₃ and their current rises linearly.

<u>Mode 2 ($T_1 < t < T_2$)</u>: This mode starts when switch S_a is turned on just before the main switches are to be turned off with ZCS. L_{r2} limits the rise of the auxiliary switch current so that this switch turns on with ZCS. C_r begins to resonate with L_{r2} , thus the current in inductor L_{r2} rises while the voltage across C_r falls.

<u>Mode 3 ($T_2 < t < T_3$)</u>: This mode starts when the voltage across C_r (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} through D_{a4} begin to conduct, thus the current in inductor L_{r1} rises. D_{T1} starts conducting as well. The current through L_{r2} falls

and eventually goes to zero. The currents through the main switches S_1 , S_2 , and S_3 then become negative and flow through their body diodes. S_1 to S_3 can be turned off with ZCS during this time. Then the current in L_{r2} reaches zero because of its resonance with C_r ; S_a can then be turned off with ZCS. Energy in L_{r1} is transferred to C_r , which results in the increase of the voltage across this capacitor so that V_{Cr} becomes less negative. V_{Cr} becomes positive sometime during this mode.

<u>Mode 4 ($T_3 < t < T_4$)</u>: This mode begins when S_a is turned off with ZCS. The voltage V_{cr} keeps increasing and the current through L_{r1} stays constant so the voltage across it is equal to zero. The voltage across the auxiliary capacitor reaches the output voltage at the end of this mode.

<u>Mode 5 ($T_4 < t < T_5$)</u>: This mode starts when the voltage across L_{r1} becomes negative. During this mode, when the net voltage across C_r and L_{r1} becomes equal to the output voltage, main boost diodes D_1 and D_2 and D_3 of the bidirectional converter start conducting. When the current through L_{r1} reaches zero, this mode is over.

<u>Mode 6 ($T_5 < t < T_6$)</u>: During this mode, the current in the magnetizing inductance of the feed-forward transformer is discharged to the output through D_{T2} . The voltage across L_1 and L_2 becomes V_{in} - V_0 and the current through them starts to fall in a linear manner.

<u>Mode 7 ($T_6 < t < T_7$)</u>: This mode starts when the currents in L₁, L₂, and L₃ reach zero. This is the last mode of operation; the next cycle begins when S₁, S₂, and S₃ are turned on under ZCS.



Fig. 5.14. Typical waveforms of the proposed convert







Fig. 5.16. Current flow in Mode 2







Fig. 5.18. Current flow in Mode 4



Fig. 5.19. Current flow in Mode 5



Fig. 5.20. Current flow in Mode 6



Fig. 5.21. Current flow in Mode 7

The key features of the novel converter are:

- (i) The auxiliary circuit can be deactivated when the converter is operating under lightload conditions, unlike most ZCS methods where the auxiliary circuit must always be in operation, regardless of the load. As a result, in a HDER, when the load of a residential house is low, the proposed converter can operate with hard-switching and with ZCS for heavier loads.
- (ii) There is only one active auxiliary circuit for all three main boost switches instead of each one needing its own active auxiliary circuit to help it turn off with ZCS; this results in a less expensive converter.
- (iii)The main switches and diodes do not have increased peak and RMS current stresses as is the case with resonant type ZCS auxiliary circuits because no current from the auxiliary circuit flows into the main circuit.
- (iv)The auxiliary circuit only needs to be operational for a very short amount of time and the auxiliary switch does not have to conduct the combined current from

multiple sources. Instead, it just needs to conduct the current caused by the discharge of the auxiliary circuit capacitor C_r through L_{r2} . Moreover, since all the main boost switches are turned off together, the auxiliary switch only needs to operate one time in each period, so the auxiliary switch encounters little RMS current stress.

- (v) The presence of transformer T_a in the auxiliary circuit also reduces RMS stress. It is the combination of all the above factors that allows the proposed multi-port converter to operate with just one auxiliary switch, at power levels that are much higher than other interleaved ZCS-PWM boost converters with just one auxiliary switch.
- (vi)None of the auxiliary circuit components are in the main power path so they only handle a fraction of the current that the main circuit components handle.

5.4 Circuit Analysis

As in previous chapters, mathematical equations of the key modes of operation in steadystate need to be derived to illustrate the effects of the novel DC-DC PWM multiport converter on each component. The analysis in this chapter is done for one of the configurations that was shown in the modes of operation in Figs. 5. 15- 5.21, which is when all the main switches S_1 , S_2 , and S_3 are turned on and off simultaneously.

In Mode 1, shown in Fig. 5.15, all the main switches S_1 , S_2 , and S_3 are turned on. When they turn on, the rectified voltage is applied to $L_{1,2,3}$ and leads to a gradual increase of the current through the main boost inductors. The slope of $L_{1,2,3}$ which is equal to the slope of $S_{1,2,3}$ is increased according to

$$V_{in1} = L_1 \frac{dL_1(t_1)}{dt}$$
(5-1a)

$$V_{in2} = L_2 \frac{dL_2(t_1)}{dt}$$
(5-1b)

$$V_{in3} = L_3 \frac{dL_3(t_1)}{dt}$$
(5-1c)

By integrating from time T_0 to T_1 , the main switch current can be expressed as

$$I_{S1}(t_1) = \frac{V_{in1}}{L_1} (T_1 - T_0)$$
(5-2a)

$$I_{S2}(t_1) = \frac{V_{in2}}{L_2} (T_1 - T_0)$$
(5-2b)

$$I_{S2}(t_1) = \frac{V_{in3}}{L_2} (T_1 - T_0)$$
(5-2c)

All the input current goes through each main boost switch, according to

$$I_{in1} = I_{S1} \tag{5-3a}$$

$$I_{in2} = I_{S2}$$
 (5-3b)

$$I_{in3} = I_{S3}$$
 (5-3c)

By turning the auxiliary switch (S_a) on, Mode 2 is started. It is turned on to perform ZCS turn-offs of main switches S_1 , S_2 , and S_3 . S_a turns on with ZCS because L_{r2} limits the rise of the switch's current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} increases while the voltage across C_r reduces, as shown in Fig. 5.16.

By applying KVL

$$V_{Cr}(t_2) = L_{r2} \frac{d}{dt} i_2(t_2)$$
(5-4)

By applying KCL in Fig. 5.16

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -\frac{d}{dt} q_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2)$$
(5-5)

Substituting equ. (5-5) into equ. (5-4) results in

$$V_{Cr}(t_2) = -L_{r2} C_r \frac{d^2}{dt^2} V_{Cr}(t_2)$$
(5-6)

First, the initial capacitor voltage $V_{cr}(0)$ and the initial auxiliary inductor current $i_{Lr2}(0)$ should be defined. $V_{cr}(0)$ is assumed to be equal to V_{cm} , which is the maximum voltage across the capacitor, and $i_{Lr2}(0)$ is equal to zero in this mode, according to

$$\left[\frac{d}{dt}V_{Cr}(t_2)\right]_{t=0} = -\left(\frac{1}{C_r}\right)\left[\frac{d}{dt}q_{Cr}(t_2)\right]_{t=0} = \left(\frac{1}{C_r}\right)\left[i_{Lr2}(t_2)\right]_{t=0}$$
(5-7)
= 0

Substituting equ. (5-7) into equ. (5-6) yields

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 \text{ for } T_1 < t < T_2$$
 (5-8)

This is equal to

$$i_{Lr2}(t_2) = i_{Cr}(t_2) = -C_r \frac{d}{dt} V_{Cr}(t_2) = C_r V_{cm} \omega_2 \sin \omega_2 t_2$$
(5-9)

$$= \frac{V_{cm}}{Z_2} \sin \omega_2 t_2 \qquad \text{for} \quad T_1 < t < T_2$$

The parameters are defined as: $\omega_2 = \frac{1}{\sqrt{L_{r2}C_r}}$, and the characteristic impedance of the auxiliary circuit is $Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$. At the end of this mode, the voltage across the resonant capacitor reaches zero; therefore the duration is

$$V_{Cr}(t_2) = V_{cm} \cos \omega_2 t_2 = 0$$
 for $t = T_2$ (5-10a)

$$\omega_2 t_2 = \frac{\pi}{2} t_2 = T_2 - T_1 = \frac{\pi}{2} \sqrt{L_{r2} C_r}$$
(5-10b)

As can be seen from Fig. 5.16, the maximum current through the auxiliary switch can be determined at the end as follows:

$$i_{Lr2}(t_2) = \frac{V_{cm}}{Z_2} \sin \omega_2 \frac{\pi}{2} \frac{1}{\omega_2}$$

$$i_{Lr2}(t_2) = i_{samax} = \frac{V_{cm}}{Z_2} \qquad \text{for } t = T_2$$
(5-11)

Mode 3 is shown in Fig. 5.17, which begins when the voltage across the resonant capacitor (V_{Cr}) is zero. During this mode, V_{cr} is charged to a negative voltage and D_{a1} , D_{a2} , and D_{a3} start to conduct. D_{T1} also starts to conduct, so circulating energy from the auxiliary circuit is transferred to the output in this mode. The current through the auxiliary inductors decreases and goes to zero. The currents through the main boost switches then become negative and flow through their body diodes. As a result, all the main switches S_1 , S_2 , and S_3 can be turned off with ZCS in Mode 3.

The auxiliary switch (S_a) has to be turned off right after turning off the main switches to reduce the conduction losses; therefore, the ZCS conditions for both main and auxiliary switches must be met in this mode of operation.

Applying KCL in Fig. 5.17 results in

$$i_{Lr1}(t_3) = i_{Lr2}(t_3) + i_{Cr}(t_3)$$
 (5-12)

Also

$$i_{Lr2}(T_3) = \frac{V_{cm}}{Z_2}$$
(5-13)

Considering the blocking diode D_{a4}

$$V_{Lr2} = V_{Cr} \tag{5-14}$$

By applying KVL in Fig. 5.17

$$V_{Lr1} = -(V_{Cr} + V_X) \tag{5-15}$$

The auxiliary transformer primary voltage is clamped to $V_X = V_0/N$, where $N=N_2/N_1$ is the turns ratio.

Differentiating equ. (5-12) results in

$$\frac{d}{dt}i_{Lr1}(t_3) = \frac{d}{dt}i_{Lr2}(t_3) + \frac{d}{dt}i_{Cr}(t_3)$$
(5-16a)

This is equal to

$$\frac{V_{Lr1}}{L_{r1}}(t_3) = \frac{V_{Lr2}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3)$$
(5-16b)

Substituting equ. (4-15) into equ. (4-16b) yields

$$\frac{V_{Cr} + V_X}{L_{r1}}(t_3) + \frac{V_{Cr}}{L_{r2}}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(5-16c)

This leads to

$$\frac{V_X}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r1}}(t_3)\frac{L_{r2}}{L_{r2}} + \frac{V_{Cr}}{L_{r2}}(t_3)\frac{L_{r1}}{L_{r1}} + C_r\frac{d^2}{dt^2}V_{Cr}(t_3) = 0$$

$$\frac{V_{Cr}(L_{r1}+L_{r2})+V_{X}L_{r2}}{L_{r1}L_{r2}}(t_{3})+C_{r}\frac{d^{2}}{dt^{2}}V_{Cr}(t_{3})=0$$

This can then be simplified by defining $L_e = \frac{L_{r_1}L_{r_2}}{L_{r_1}+L_{r_2}}$ so that

$$\frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3) + \frac{V_{Cr}}{L_e}(t_3) + C_r \frac{d^2}{dt^2} V_{Cr}(t_3) = 0$$
(5-16d)

This can then be rewritten as

$$\frac{V_{Cr}}{L_{eq}}(t_3) = -C_r \frac{d^2}{dt^2} V_{Cr}(t_3) - \frac{V_X L_{r2}}{L_{r1} L_{r2}}(t_3)$$
(5-16e)

The above-mentioned parameters are defined as

$$\omega_{1} = \frac{1}{\sqrt{L_{r1}C_{r}}}$$
$$\omega_{e} = \frac{1}{\sqrt{L_{e}C_{r}}}$$
$$Z_{1} = \sqrt{\frac{L_{r1}}{C_{r}}}$$
$$Z_{e} = \sqrt{\frac{L_{re}}{C_{r}}}$$
$$L_{e} = \frac{L_{r1} * L_{r2}}{L_{r1} + L_{r2}}$$

$$V_{Cr}(t_3) = \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - \frac{(V_{Cm} Z_e)(\sin(w_e t_3))}{Z_2}$$
(5-17)

Applying KVL to Fig. 5.17 results in

$$V_{Lr1}(t_3) = -V_{Cr}(t_3) - V_X = -V_{Lr2}(t_3) - V_X$$
(5-18)

Integrating this equation yields

$$i_{Lr1}(t_3) = \frac{(V_{Cm}L_e)(1-\cos(w_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r1}^2} - \frac{V_X t_3}{L_{r1}}$$
(5-19)

Applying KVL in Fig. 5.17 yields

$$V_{Cr}(t_3) = L_{r2} \frac{d}{dt} i_{Lr2}(t_3)$$
(5-20)

This results in

$$di_{Lr2}(t_3) = \left(\frac{V_{Cr}}{L_{r2}}(t_3)\right)dt$$
(5-21)

which then leads to

$$i_{Lr2}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r2} w_e^2}\right)$$
(5-22)

In this section, the generalized equations showing the soft switching of the main and auxiliary switches of the N-port boost converter with the proposed ZCS auxiliary circuit are derived. The N-port configuration is shown in Fig. 5.22. As can be seen, the auxiliary ZCS cell can be implemented in an N-port boost converter.



Fig. 5.22. Proposed N-port ZCS converter

During this mode of operation, the current through the main boost switches should go to zero or negative in order to meet the ZCS conditions. The direction of current through them is changed and current flows through their body diodes.

prerequisite of ZCS of
$$I_{S1}$$
: $i_{in1}(t_3) - i_{Lr1}(t_3) \le 0$ (5-20a)

prerequisite of ZCS of
$$I_{S2}$$
: $i_{in2}(t_3) - i_{Lr1}(t_3) \le 0$ (5-20b)

prerequisite of ZCS of
$$I_{S3}$$
: $i_{in3}(t_3) - i_{Lr1}(t_3) \le 0$ (5-20c)

If all the switches need to be turned off at the same time, then

$$\left(i_{in3}(t_3) + i_{in3}(t_3) + i_{in3}(t_3)\right) - i_{Lr1}(t_3) \le 0$$
(5-21)

$$i_{S1 to Sn} = \left(\sum_{j=1}^{n} I_{j}\left(t_{3}\right)\right) - \left(\frac{\left(V_{Cm}L_{e}\right)\left(1 - \cos\left(w_{e}t_{3}\right)\right)}{Z_{2}L_{r1}} + \frac{\left(V_{X}L_{e}\right)\left(t_{3} - \frac{\sin\left(w_{e}t_{3}\right)}{w_{e}}\right)}{L_{r1}^{2}} - \frac{V_{X}t_{3}}{L_{r1}}\right) \le 0$$
(5-22)

Applying KCL in Fig. 5.17 results in

$$I_{Sa}(t_3) = i_{Lr2}(t_3) \tag{5-23}$$

As a result, ZCS condition is met for the auxiliary switch if

prerequisite of ZCS of
$$I_{Sa}$$
: $I_{Sa}(t) = i_{Lr2}(t) \le 0$ (5-24)

which is equal to

$$i_{Sa}(t_3) = \frac{V_{cm}}{Z_2} - \left(\frac{(V_{Cm}L_e)(1 - \cos(w_e t_3))}{Z_2 L_{r2}} + \frac{(V_X w_1^2)\left(t_3 - \frac{\sin(w_e t_3)}{w_e}\right)}{L_{r2} w_e^2}\right) \le 0$$
(5-25)

V_{Lr1} is derived as:

$$V_{Lr1}(t_3) = \frac{(V_{Cm}Z_e)(\sin(w_e t_3))}{Z_2} - \frac{(V_X w_1^2)(\cos(w_e t_3) - 1)}{w_e^2} - V_X$$
(5-26)

VLr1 reaches its maximum at the end of this mode; therefore the duration can be expressed as

$$t_{3} = -\frac{\log\left(\frac{\sqrt{\left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)j + \left(\left(\frac{V_{cm}L_{e}}{Z_{2}L_{r1}}\right)^{2}w_{e}^{2} + \left(\frac{V_{X}L_{e}}{L_{r1}^{2}}\right)^{2} - \left(\frac{V_{X}L_{e}}{L_{r1}^{2}} - \frac{V_{X}}{L_{r1}}\right)^{2})}{\frac{V_{X}L_{e}}{L_{r1}^{2}}j - \frac{V_{cm}L_{e}}{Z_{2}L_{r1}}w_{e}}}{w_{e}}\right)j}$$
(5-27)

By adding t_2 and t_3 , the entire time that the auxiliary switch needs to operate can be determined to be

$$t_{isa-on\,time} = t_2 + t_3 \tag{5-28}$$

which is equal to

$$t_{isa-on\,time} = 2(\frac{\pi - tan^{-1}\left(\frac{V_{cm}w_e^{\ 2}Z_e}{V_Xw_1^{\ 2}Z_2}\right)}{w_e})$$
(5-29)

Since deriving the equations and design procedure of this topology can be done in a similar way as the topology that was introduced in Chapter 3, they are not repeated here and only the final key equations related to the soft switching were provided.

By following the design procedure that was introduced in Chapter 3, the following auxiliary components are selected for a 1000 Watt multi-port boost converter that has V_{in1} = V_{in2} =90 V, V_{in3} =144 V and V_o =200 V. L_{r1} , L_{r2} , C_r , and T_a , are selected as: 4 μ H, 3.8 μ H, 9 nF, and 1:3 respectively. Substituting these parameters in equ (5-29) results in t_{aux} = 0.9 ns.

5.5 Converter Features

The main features of the proposed multiport converter are as follows:

- a) The auxiliary circuit can be deactivated when the converter is operating under light-load conditions, unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load. This leads to an improvement in light-load efficiency as no auxiliary circuit means no auxiliary circuit losses under operation conditions where ZCS is unnecessary. This can be done as there are no auxiliary circuit components in the main power circuit.
- b) As a result, when this converter is implemented in a HDER to meet the load requirements in a nanogrid, more kWh and money can be saved. The reason is that when the load of a residential house is very low, the proposed converter

can operate with hard-switching, while during normal loads the converter operates with soft-switching.

- c) This converter is suitable for an HDER system as it operates with ZCS in boost modes in all 10 of the different topologies demonstrated in Table. 5.1, whenever soft-switching is needed.
- d) There is only one active auxiliary circuit for all main boost switches instead of each main boost switch needing its own active auxiliary circuit to help it turn off with ZCS. This leads to a less expensive converter, so the initial cost of implementing an HDER in a nanogrid is reduced.
- e) All the main boost switches can be turned off together, so the auxiliary switch only needs to operate one time in each period. Therefore, the conduction losses are reduced.
- f) The main switch does not have increased peak and RMS current stresses, as is the case with resonant type ZCS auxiliary circuits, because no current from the auxiliary circuit flows into the main circuit.
- g) None of the auxiliary circuit components are in the main power path, so they only handle a fraction of the current that the main circuit components handle.
- h) The auxiliary circuit only needs to be operational for a very short amount of time, typically around 0.9 μs.
- i) Since the auxiliary transformer is not in series with the auxiliary switch, the maximum voltage of the resonant capacitor increases which leads to faster soft switching for all main switches S_1 , S_2 , and S_3 . In addition, since the converter operates in DCM, there is no reverse recovery current for the main diodes, therefore L_{r1} does not need to be chosen high enough to eliminate it. As a result, small L_{r2} can be chosen which decreases the operating time of the auxiliary switch.

5.6 Experimental Results

The feasibility of the proposed DC-DC multiport ZCS-PWM boost converter was confirmed with results obtained from an experimental prototype with the following specifications:

Output Voltage: $V_0 = 200$ Volts DC

Output Power: P₀= 1000 Watts

Input Voltage 1: V_{in1}= 90 Volts DC

Input Voltage 2: V_{in2}= 90 Volts DC

Input Voltage 3: V_{in3}= 144 Volts DC

Switching Frequency for main switches: $f_S = \frac{1}{T_S} = 50$ kHz.

Switching Frequency for auxiliary switch: $f_{Sa} = \frac{1}{T_S} = 50 \text{ kHz}.$

The following components were used for the laboratory prototype:

- Input Inductances $L_{1,2,3}$: 130 μH
- Main Boost Diodes D_{1,2,3}: LQA06T300
- Main Switches S_{1,2,3}: FGAF40N60UFD
- Output Capacitor: 2X560µF 3316(M)
- Auxiliary Switch S_a: FGAF40N60UFD
- Auxiliary Diodes D_{a 1,2,3}: STTH20RD4
- Auxiliary Diode D_a 4: SF3003PT
- Resonant Inductor L_{r1} : 4 μH
- Resonant Inductor L_{r2} : 3.8 μH
- Resonant Capacitor Cr: 9 nF

A prototype of the proposed converter was built with the following specifications: 2 DC sources with voltages of 90 V and a third source with 144 V were used to demonstrate the PEMFC, PV, and battery respectively. The DC bus voltage was 200 V, $f_{sw} = 50$ kHz, and $P_{o,max} = 1$ kW. Experimental results are shown in Figs. 5.23- 5.25.

Experimental results when all the three sources supply the load together are shown in this section. Fig. 5.23 shows typical current and gating signal waveforms for main switches S_1 and S_2 , which represent the two DC sources. As can be seen, they can be turned on and off

with ZCS, without a current tail, because the current through the switch goes to zero before turning it off.

The same waveforms are shown in Fig. 5.24 for the main switch S_3 and it can be seen that it turns on and off with ZCS as well. It should be mentioned that the output voltage of DC Source 3 (battery) is higher than that of DC Source 1 (PV) and DC Source 2 (FC), so the duty cycle of S_3 is less than that of S_1 and S_2 to turn all the switches off together.

Fig. 5.25 shows the auxiliary switch waveforms and it can be seen that the auxiliary switch needs to operate for just 1 µs and it does so with ZCS. The 1µs on-time is much less than that of the auxiliary switch on-time in other multiport boost converters with single auxiliary circuits, so it can operate with less current stress than them. As a result, the proposed multi-module converter can operate with just one auxiliary circuit with heavier loads than other converters. As discussed in the converter features, when the input power is low, the proposed converter's auxiliary circuit can be disengaged and operate with hard switching to improve the efficiency for the entire load range.

Fig. 5.26 shows efficiency curves of the proposed ZCS-PWM multi-port converter and a conventional hard switching PWM multi-port converter. Both converters were implemented on the same prototype, one with the auxiliary circuit and one without. As can be seen, preliminary efficiency measurements show a maximum proposed converter efficiency above 96%, and an improvement in light-power efficiency of 5% when the auxiliary circuit is disengaged.



Fig. 5.23. ZCS for main switches S_1 and S_2



Fig. 5.24. ZCS for main switch S₃



Fig. 5.25. ZCS for auxiliary switch $S_{\rm a}$


Fig. 5.26. Comparative of efficiency graphs between soft-switching and hardswitching for different output loads.

5.7 Conclusion

A novel DC-DC multi-port ZCS-PWM converter that improves the energy efficiency of a DC nanogrid is proposed in this chapter. Advantages of this converter include: just one active auxiliary circuit that is used to perform ZCS, no additional voltage or current stresses on the main switches, the auxiliary switch operates for a very short amount of time and once each cycle to perform ZCS for all the switches simultaneously, and the auxiliary switch can be deactivated from the main power circuit at any time to improve the efficiency during light loads. Different configurations were discussed and one of the modes of operations were shown. The equations were derived, and the feasibility of the converter was confirmed with results obtained from an experimental prototype.

6 Conclusion

6.1 Introduction

In this chapter, the contents of the thesis are summarized, the conclusions that have been reached as a result of the work done in the thesis for a variety of novel ZCS PWM topologies are presented, and the main contributions of the thesis to the field of power electronics are stated. At the end, the suggestions for future work are given.

6.2 Summary

Addressing issues related to the soft switching of the AC-DC and DC-DC converters has been the main focus of this thesis. Pulse width modulation (PWM) converters that consist of two or more interleaved boost/buck converter modules are used widely in industry. Softswitching methods for these converters can either be zero-voltage switching (ZVS) if they are implemented with MOSFETs or zero-current switching (ZCS) if implemented with IGBTs. The focus of the thesis has been on ZCS methods for IGBT converters. Most methods use an auxiliary circuit that is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS. ZCS is beneficial for IGBTs as it eliminates the current tail that would otherwise exist when turning it off. This current tail overlaps with the switch voltage and causes significant turn-off losses.

In literatures, most converters use an auxiliary circuit that is activated whenever a main converter switch is about to be turned off, gradually diverting current away from the switch so that it can turn off with ZCS. ZCS-PWM converters that use an auxiliary circuit to help a main converter switch turn-off with ZCS are generally less efficient than hard-switching converters at light loads. The main reason for this is that the auxiliary circuit losses dominate when the converter is operating under these conditions. Auxiliary circuit losses

include the turning on and off of the auxiliary switch and additional conduction losses. ZCS-PWM converters achieve their improved efficiency over hard-switching converters at heavier loads when the switching losses of the main switch are eliminated. These switching losses - especially the IGBT current tail losses - are greater than the auxiliary circuit losses.

Ideally, the auxiliary circuit used to achieve ZCS operation in a ZCS-PWM converter should be engaged only when the converter is operating with heavier loads and not when the converter is operating with lighter loads.

The proposed novel converters in this thesis have the ability to operate in such a manner and would ensure the optimal efficiency profile over the entire load range. Since the auxiliary switch only needs to operate for a short period of time, the conduction losses are low, and the converters can be used for heavier loads.

In this thesis, the operation of the novel interleaved boost, buck, and multiport converters were discussed. The proof-of-concept prototypes have been built based on the given mathematical equations and design criteria to validate the feasibility of the proposed converters.

The content of the thesis can be summarized as follow:

In Chapter 1, the need for applying soft switching methods such as ZVS and ZCS were discussed. Then, a ZCS technique which is widely used for IGBTs was explained in detail. Afterward, what other authors proposed in this area for boost, buck, and multiport converters were reviewed and their drawbacks were stated. Finally, the thesis objectives, which are proposing novel ZCS PWM boost, buck, and multiport converters that do not have the previously stated drawbacks, were stated.

In Chapter 2, a novel AC-DC interleaved ZCS PWM boost converter was proposed. The main advantage of the proposed converter over the other topologies, which is having a single auxiliary switch to perform ZCS for all the switches, was explained. Then modes of operation showing its operation were discussed. The features of the novel converter were stated. Mathematical equations of the proposed converter were derived, and design curves

were drawn which were used to select the components. Experimental results from the proof-of-concept prototype show the feasibility of the converter.

In Chapter 3, an AC-DC interleaved ZCS PWM boost converter with reduced auxiliary switch RMS current stress was proposed. This converter has an auxiliary transformer to reduce the operation time of the auxiliary switch and reduce its maximum voltage. Also, the auxiliary transformer can transfer some part of the circulating current to the output to improve the efficiency. The proposed converter has only one auxiliary switch to perform ZCS for all switches and can be disengaged at light loads to improve the efficiency. In this chapter, the operation of the proposed converter was explained in detail, and mathematical equations were derived in steady-state. Based on the equations, the design curves were achieved by MATLAB simulations. The main features of the novel converter were stated. The loss analysis was performed. The proof of concept was presented by experimental results and was compared with other literatures to demonstrate its superiority.

In Chapter 4, a novel ZCS PWM buck converter with improved efficiency for the entire load range to be used in stand-alone wind power system was proposed. The auxiliary circuit is similar to that of in Chapter 3, meaning it had only one auxiliary circuit which can be disengaged at light loads. The modes of operation were shown. The key equations regarding the soft switching of all switches were derived. The main features of the converter were stated. Then the experimental results, obtained from a prototype, demonstrated the validity of the auxiliary circuit. In order to prove the feasibility of the converter in a power system, a small wind turbine was simulated with HOMER software. Based on the simulation results, the energy that can be saved by using the novel proposed converter for the entire load range in a case study in Ontario, Canada was calculated. The energy saving showed the superiority of the proposed converter for the entire load range in a wind turbine system.

In Chapter 5, improvement of DC nanogrid energy with a new ZCS PWM multi-port converter was presented. All 10 different configurations that this converter can be used for were shown. The auxiliary circuit of this topology is similar to that of in Chapter 3, meaning that it has a single auxiliary circuit to perform ZCS for all the main switches and the

auxiliary switch itself and can be disengaged at light loads. The modes of operation for the worse-case scenario when all the main switches need to be turned off at the same time were explained in detail. The key mathematical equations related to the soft switching of all the main and auxiliary switches were derived. Finally, the experimental results were obtained from a proof-of-concept prototype to show the feasibility and superiority of the proposed multiport converter.

6.3 Conclusion

Based on the work that has been done in this thesis, the following key conclusions can be made:

- It is possible to implement a multi-module, interleaved ZCS-PWM converter for boost, buck, and multiport applications converters with just one auxiliary circuit for the overall converter instead of an auxiliary circuit for each module. This can be done with the converter proposed in this thesis due to the novel way in which the auxiliary circuit components are implemented.
- A significant savings in power losses can be achieved if the auxiliary circuit of a ZCS-PWM converter can be disengaged at light loads. This is due to the fact that the auxiliary circuit creates losses over the entire load range that become dominant under light-load operation. Not activating the auxiliary circuit when the converter is operating with light loads results in the elimination of auxiliary circuit losses and thus improved light-load efficiency.
- It is possible to use an auxiliary inductor in series with the auxiliary switch to turn it on with ZCS because inductor limits the rise of current that starts to flow through it when it is turned on.
- It is possible to connect the auxiliary circuit to the main converter in a way that if desired, not operating the auxiliary switch stopes the resonance between the auxiliary capacitor and inductors results in reverse biased of the auxiliary diodes which means that the entire auxiliary circuit can be disengaged. This is unlike many ZCS-PWM converters that require the auxiliary circuit to be used even under light-

load conditions where it is actually detrimental because there are components in the main part of the circuit. This helps improve light-load efficiency.

- In Chapter 3, an interleaved ZCS-PWM converter with a single auxiliary circuit containing a transformer was proposed. Based on the steady-state analysis that was performed, it was determined that the auxiliary transformer turns ratio N is a critical parameter in the design of the auxiliary circuit if N is too low, then ZCS becomes less likely for the main switches; if N is too high, then the auxiliary switch will not operate with ZCS. As a result, the value of N is constrained to a range of values so that all converter switches can operate with ZCS. Regardless of the value of N, significant reduction in auxiliary component voltage stress can be achieved with the auxiliary transformer.
- A small wind energy conversion system with a buck-type converter interface needs to operate with a wide variety of loads as opposed to operating within a limited load range. This conclusion was reached by analyzing real time date obtained from a small wind turbine in Chatham, Ontario, by using HOMER software, which can translate real data into data that can be used in wind turbine models. This confirms the need of a power electronic converter interface that can operate with improved light-load and heavy-load efficiency as opposed to operate with improved heavy-load efficiency at the cost of reduced light-load efficiency.
- It is possible to implement a ZCS-PWM boost multiport converter with various DC sources if the converter is operated with a proper gating signal sequence. If the module that is connected to the highest DC voltage is turned on later in the switching cycle then any issues related to differences in the input voltage such as circulating current can be avoided.

6.4 Contributions

The most significant contributions of this thesis to the power electronics literatures are as follows:

- A novel AC-DC multi-module interleaved ZCS-PWM boost converter that has a single auxiliary circuit that can be disengaged at light loads to improve the overall efficiency was proposed. This converter is unlike previously proposed converter that do not allow the auxiliary circuit to be disengaged at light loads.
- An AC-DC interleaved ZCS-PWM boost converter with reduced auxiliary switch RMS current stress was proposed. The reduction in stress was achieved by the novel implementation of a transformer in the auxiliary circuit that allowed the converter to have additional advantageous features, one of these being a reduction in voltage stress as well. Since the current and voltage stress of the auxiliary circuit components are lower than what is found in other previously proposed auxiliary circuits, the auxiliary circuit can be operated at higher power levels that what has been previously reported in the literature. As a result, the proposed interleaved converter can operate with just a single auxiliary circuit can operate at higher power levels that other similar type interleaved converters that have just one auxiliary circuit.
- The technology proposed in Chapters 2 and 3 can be implemented in buck and multiport converters and is not limited to just for boost converters. This is often not the case for other ZCS-PWM converters, which are suitable only as boost converters or as buck converters.
- An AC-DC two-module ZCS-PWM interleaved buck converter was proposed to improve the entire load range efficiency of a standalone wind power system. Real time information of a small wind turbine in Chatham Ontario was acquired by using HOMER software to demonstrate how frequently the wind turbine operates at light loads. The energy savings that can be achieved by using the proposed converter was confirmed by calculating the kWh energy that can be saved by operating it with softswitching at normal loads and hard-switching at light loads. To the best of the author's knowledge, this is the first time that the operation of a PWM converter was correlated with real time information from a wind turbine to determine the cost that can be saved by improving the efficiency of the power electronics in a wind energy conversion system.
- A DC-DC multiport ZCS-PWM converter was proposed to improve the entire load range performance of a DC nanogrid system. It was shown that the proposed converter

can operate in different configurations with soft-switching and that it is an attractive solution as a power electronic interface in DC nanogrid.

• The steady-state characteristics of all the power converters that were proposed in this thesis were determined as a result of extensive mathematical analysis. With these characteristics, design procedures that can be used by others were established and confirmed with results obtained from experimental prototypes.

6.5 Future Work

The following are suggestions for future work that can be performed, based on the work done in this thesis:

- The auxiliary circuits that have been proposed in this thesis were for various industrial applications such as for AC-DC converters and as interfaces for renewable energy systems powered by solar and wind. Work can be done to investigate the use of the technology proposed in this thesis for other applications or for similar applications under different operating conditions. For example, the energy analysis that was performed in Chapter 4 was done for a particular set of operating conditions. Work can be done to see the results of an energy analysis under different operating conditions.
- In this thesis, it has been suggested to use 30-40 % of the rated power as the crossover point between soft-switching and hard-switching. A closed loop controller can be developed to disengage the auxiliary switch when it operates with less than 30 % of the rated power, using information obtained from some sort of sensing mechanism.
- The current flowing in an AC-DC converter during a line cycle varies as there is less current in the converter when the input AC voltage is near a zero-crossing than when it is near its peak. Work can be done to operate the proposed AC-DC converter in Chapter 3 with the auxiliary circuit engaged only during parts of the line cycle when the input AC voltage is at its peak. This would reduce losses that are created by the auxiliary circuit during the zero-crossings of the input AC voltage. It should be noted that this type of switching is different than what has been proposed in this thesis, which is the engage or disengage the auxiliary circuit based on load conditions.

• AC-DC converters are generally used as the front-end converter in two-stage AC-DC converters where the first stage is the AC-DC converter stage and the second stage is a DC-DC converter stage that converts the DC output of the first stage into the DC output that is required by an isolated load. The second DC-DC stage is typically implemented with a DC-DC full-bridge converter for higher power applications. Work can be done to implement the first stage of a two-stage AC-DC converter by using the technology proposed in this thesis and designing the auxiliary circuit transformer to send energy directly to the output instead of through a second converter stage. If this can be done, this would save energy as some of the energy from the input source would only need to be processed once instead of twice.

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Appendices

Appendix A: MATLAB program which used to generate Fig. 2.10.

IL1=9.6; vo=400; cr=4:24; le= 2220;

ze=sqrt(le./cr); vcrmax=(IL1*ze)+vo;

plot(cr,vcrmax)

Appendix B: MATLAB program which used to generate Fig. 2.11.

z=10:24; ip=400./z;

plot(z,ip)

Appendix C: MATLAB program which used to generate Fig. 2.12.

lr11=0.000005; lr21=0.000004; lr22=0.00000425; lr23=0.0000045; lr24=0.00000475; lr25=0.000005; lr26=0.00000525; cr=0.00000012;

z1=sqrt(lr21/cr);le1=lr11*lr21/(lr11+lr21);

we1=sqrt(1/(le1*cr)); z2=sqrt(lr22/cr); le2=lr11*lr22/(lr11+lr22);

we2=sqrt(1/(le2*cr)); z3=sqrt(lr23/cr); le3=lr11*lr23/(lr11+lr23);

we3 = sqrt(1/(le3*cr)); z4 = sqrt(lr24/cr); le4 = lr11*lr24/(lr11+lr24);

we4=sqrt(1/(le4*cr)); z5=sqrt(lr25/cr); le5=lr11*lr25/(lr11+lr25);

we5=sqrt(1/(le5*cr)); z6=sqrt(lr26/cr); le6=lr11*lr26/(lr11+lr26);

we6=sqrt(1/(le6*cr)); t=0:0.00000001:0.0000007;

 $I11=18-(400/z1)*(le1/lr11)*(1-cos(we1*t)); \quad I12=18-(400/z2)*(le2/lr11)*(1-cos(we2*t));$

I13=18-(400/z3)*(le3/lr11)*(1-cos(we3*t)); I14=18-(400/z4)*(le4/lr11)*(1-cos(we4*t));

I15=18-(400/z5)*(le5/lr11)*(1-cos(we5*t)); I16=18-(400/z6)*(le6/lr11)*(1-cos(we6*t));

plot(t,I11,'r') hold on; plot(t,I12,'k') hold on; plot(t,I13,'g') hold on;

plot(t,I14,'m') hold on; plot(t,I15,'b') hold on; plot(t,I16,'c') grid on;

Appendix D: MATLAB program which used to generate Fig. 2.13.

lr11=0.000005; lr21=0.000004; lr22=0.00000425; lr23=0.0000045; lr24=0.00000475; lr25=0.000005; lr26=0.00000525; cr=0.00000012;

z1=sqrt(lr21/cr);	le1=lr11*lr21/(lr11+lr21);	we1=sqrt($1/(le1*cr)$);		
z2=sqrt(lr22/cr);	le2=lr11*lr22/(lr11+lr22);	we2=sqrt(1/(le2*cr));		
z3=sqrt(lr23/cr);	le3=lr11*lr23/(lr11+lr23);	we3=sqrt(1/(le3*cr));		
z4=sqrt(lr24/cr);	le4=lr11*lr24/(lr11+lr24);	we4=sqrt(1/(le4*cr));		
z5=sqrt(lr25/cr);	le5=lr11*lr25/(lr11+lr25);	we5=sqrt(1/(le5*cr));		
z6=sqrt(lr26/cr);	le6=lr11*lr26/(lr11+lr26);	we6=sqrt(1/(le6*cr));		
t=0:0.00000001:0.0000007;				
I21= $(400/z1)-(400/z1)*(le1/lr21)*(1-cos(we1*t));$				
I22=(400/z2)-(400/z2)*(le2/lr22)*(1-cos(we2*t));				
$I23 = (400/z3) - (400/z3) * (le3/lr23) * (1 - \cos(we3 * t));$				
I24= $(400/z4)$ - $(400/z4)$ * $(le4/lr24)$ * $(1-cos(we4*t))$;				
$I25 = (400/z5) - (400/z5) * (le5/lr25) * (1 - \cos(we5*t));$				
I26=(400/z6)-(400/z6)*(le6/lr26)*(1-cos(we6*t));				
plot(t,I21,'r') hold of	on; plot(t,I22,'k') hold o	on; plot(t,I23,'g') hold on;		
plot(t,I24,'m') hold	on; plot(t,I25,'b') hold of	on; plot(t,I26,'c')		

Appendix E: MATLAB program which used to generate Fig. 2.14.

```
z4=sqrt(lr21/cr);
                   le4=lr14*lr21/(lr14+lr21);
                                                 we4=sqrt(1/(le4*cr));
z_{5}=sqrt(lr_{21}/cr);
                   le5=lr15*lr21/(lr15+lr21);
                                                 we5=sqrt(1/(le5*cr));
                   le6=lr16*lr21/(lr16+lr21);
                                                 we6=sqrt(1/(le6*cr));
z6=sqrt(lr21/cr);
t=0:0.00000001:0.0000007;
I11=18-(400/z1)*(le1/lr11)*(1-cos(we1*t)); I12=18-(400/z2)*(le2/lr12)*(1-cos(we2*t));
I13=18-(400/z3)*(le3/lr13)*(1-cos(we3*t)); I14=18-(400/z4)*(le4/lr14)*(1-cos(we4*t));
I15=18-(400/z5)*(le5/lr15)*(1-cos(we5*t)); I16=18-(400/z6)*(le6/lr16)*(1-cos(we6*t));
plot(t,I11,'r') hold on;
                          plot(t,I12,'k') hold on;
                                                      plot(t,I13,'g') hold on;
plot(t,I14,'m') hold on;
                          plot(t,I15,'b') hold on;
                                                      plot(t,I16,'c')
```

Appendix F: MATLAB program which used to generate Fig. 2.15.

lr11=0.0000038; lr12=0.0000040; lr13=0.0000042; lr14=0.0000044; lr15=0.0000047; lr16=0.000005; lr21=0.000004; cr=0.00000012;

z1=sqrt(lr21/cr);	le1=lr11*lr21/(lr11+lr21);	we1=sqrt(1/(le1*cr));	
z2=sqrt(lr21/cr);	le2=lr12*lr21/(lr12+lr21);	we2=sqrt(1/(le2*cr));	
z3=sqrt(lr21/cr);	le3=lr13*lr21/(lr13+lr21);	we3=sqrt(1/(le3*cr));	
z4=sqrt(lr21/cr);	le4=lr14*lr21/(lr14+lr21);	we4=sqrt(1/(le4*cr));	
z5=sqrt(lr21/cr);	le5=lr15*lr21/(lr15+lr21);	we5=sqrt(1/(le5*cr));	
z6=sqrt(lr21/cr);	le6=lr16*lr21/(lr16+lr21);	we6=sqrt(1/(le6*cr));	
t=0:0.00000001:0.0000007;			
I21= $(400/z1)-(400/z1)*(le1/lr21)*(1-cos(we1*t));$			

I22=(400/z2)-(400/z2)*(le2/lr21)*(1-cos(we2*t));

 $I23 = (400/z3) \cdot (400/z3) \cdot (1e3/lr21) \cdot (1-\cos(we3 \cdot t));$

I24=(400/z4)-(400/z4)*(le4/lr21)*(1-cos(we4*t));

I25 = (400/z5) - (400/z5) (le5/lr21) (1 - cos(we5*t));

I26=(400/z6)-(400/z6)*(le6/lr21)*(1-cos(we6*t));

plot(t,I21,'r') hold on; plot(t,I22,'k') hold on; plot(t,I23,'g') hold on; plot(t,I24,'m') hold on; plot(t,I25,'b') hold on; plot(t,I26,'c')

Appendix G: MATLAB program which used to generate Figs. 3.11-3.18

lr1=0.000005; lr2=0.0000049; cr=0.000000012; vo=400; n=5; vx=vo/n;

vcm = 440; iin=18;

le=lr1*lr2/(lr1+lr2); ze=sqrt(le/cr); z2=sqrt(lr2/cr); z1=sqrt(lr1/cr);

we=sqrt(1/(le*cr)); w1=sqrt(1/(lr1*cr)); w2=sqrt(1/(lr2*cr));

%%% Mode 2 %%%

%Initial Vcr=Vcrm , ilr2=0

t2=0:1e-9:pi/(2*w2); $t_2=pi/(2*w2);$

vcr2=vcm*cos(w2.*t2); ilr22=(vcm/z2)*sin(w2.*t2);

vcr_2=vcm*cos(w2*t_2); ilr2_2=vcm/z2;

icr_2=-1*ilr2_2; ism=ilr2_2;

%%% Mode 3 %%%

%Initial ilr2= vcm/z2

 $t_3 = pi/we;$

B=((we^2)*vcm*ze)/((w1^2)*vx*z2); %% Time for Mode 3 + mode 4

 $t_4=(2*(pi-atan(B)))/we;$ %% Time for Mode 3 + mode 4

 $a=(vcm*le)/(z2*lr1); b=(vx*le)/lr1^2; z=((vx*le)/lr1^2)-(vx/lr1);\%\%$ Time in which Is1 and Is2 reach to their minimum value

 $t_41 = real(-(log((z*1i + (a^2*we^2 + b^2 - z^2)^(1/2))/(b*1i - a*we))*1i)/we); \%\%$ Time in which Is1 and Is2 reach to their minimum value

 $t41=0:1e-9:real(-(log((z*1i + (a^2*we^2 + b^2 - z^2)^{(1/2)})/(b*1i - a*we))*1i)/we); \%\%$ Time

vcr41=(((vx*(w1^2))*(cos(we*(t41))-1))/(we^2))-(ilr2_2*ze*sin(we*t41)); %% Time

 $is141=iin-((((vcm*le)/(z2*lr1))*(1-cos(we*t41)))+(((vx*le)/(lr1^2))*(t41-((sin(we*t41))/we)))-((vx*t41)/lr1));\%\%$ Time

 $ilr141 = ((((vcm*le)/(z2*lr1))*(1-cos(we*t41)))+ (((vx*le)/(lr1^2))*(t41-((sin(we*t41))/we)))- ((vx*t41)/lr1));$

```
ilr241 = (vcm/z2) - (((vcm*le)/(z2*lr2))*(1-cos(we*t41))) - (((vx*(w1^2))/((we^2)*lr2))*(t41 - ((sin(we*t41))/we)));
```

 $isa41 = (vcm/z2) - (((vcm*le)/(z2*lr2))*(1-cos(we*t41))) - (((vx*(w1^2))/((we^2)*lr2))*(t41-((sin(we*t41))/we)));$

vlr141=-vcr41-vx;

 $ilr2_41 = (vcm/z2) - (((vcm*le)/(z2*lr2))*(1-cos(we*t_41))) - (((vx*(w1^2))/((we^2)*lr2))*(t_41-((sin(we*t_41))/we)));$

isa_41= (vcm/z2)-(((vcm*le)/(z2*lr2))*(1-cos(we*t_41)))-(((vx*(w1^2))/((we^2)*lr2))*(t_41-((sin(we*t_41))/we)));

$$\label{eq:linear} \begin{split} &ilr1_41=((((vcm*le)/(z2*lr1))*(1-cos(we*t_41)))+(((vx*le)/(lr1^2))*(t_41-((sin(we*t_41))/we)))-((vx*t_41)/lr1)); \end{split}$$

 $is1_41 = iin-((((vcm*le)/(z2*lr1))*(1-cos(we*t_41)))+(((vx*le)/(lr1^2))*(t_41-((sin(we*t_41))/we)))-((vx*t_41)/lr1));$

 $vcr_41 = (((vx^*(w1^2))^*(cos(we^*(t_41))-1))/(we^2)) - (ilr_22^*ze^*sin(we^*t_41));$

vlr1_41=-vcr_41-vx;

c=(vcm*le)/(z2*lr2); d=(vx*w1^2)/(we^2*lr2); %% Time in which Isa reachs to its minimum value

 $t_4a = (pi + asin(d/(c^*we)))/we; \%\%$ Time in which Isa reachs to its minimum value

 $r=(vx*w1^2)/(we)$; h=(vcm*ze*we)/(z2); %% Time in which Is1 reachs to zero, or Vlr1 reaches to its maximum value

 $t31=0:1e-9:(2* (atan((r-sqrt(r^2+h^2))/h))+pi)/we; \%\%$ Time

 $t_31=(2* (atan((r-sqrt(r^2+h^2))/h))+pi)/we;$ %% Time in which Is1 reachs to zero, or Vlr1 reaches to its maximum value

vcr_31=(((vx*(w1^2))*(cos(we*(t_31))-1))/(we^2))-(ilr2_2*ze*sin(we*t_31));

vcr31=(((vx*(w1^2))*(cos(we*(t31))-1))/(we^2))-(ilr2_2*ze*sin(we*t31));

vlr131=-(((vx*(w1^2))*(cos(we*(t31))-1))/(we^2))+(ilr2_2*ze*sin(we*t31))-vx;

$$\label{eq:linear} \begin{split} & \text{ilr1}_31 = ((((vcm*le)/(z2*lr1))*(1-cos(we*t_31))) + (((vx*le)/(lr1^2))*(t_31-((sin(we*t_31))/we))) - ((vx*t_31)/lr1)); \end{split}$$

m=vcr_31+vx; f=ilr1_31/(cr*w1);

t_4main=t_41-t_31; t4main=0:1e-9:t_4main;

vcr4main=(vcr_31+vx)*cos(w1*t4main)+(ilr1_31/(cr*w1))*sin(w1*t4main)-vx;

```
vcr_4main=(vcr_31+vx)*cos(w1*t_4main)+(ilr1_31/(cr*w1))*sin(w1*t_4main)-vx;
```

%%% Mode 5 %%%

t_5=t_41-t_31; t5=0:1e-9:t_5;

vcr5=(vcr_4main+vx)*cos(w1.*t5)+(ilr1_41/(cr*w1))*sin(w1.*t5)-vx;

 $ilr15 = ((-cr^*w1)^*(vcr_4main+vx)^*sin(w1.^*t5)) + (ilr1_41^*cos(w1.^*t5));$

vlr15=-vcr5-vx;

 $vcr_5 = ((vcr_4main+vx)*cos(w1*t_5))+((ilr1_41/(cr*w1))*sin(w1*t_5))-vx;$

 $ilr1_5 = ((-cr*w1)*(vcr_4main+vx)*sin(w1*t_5))+(ilr1_41*cos(w1*t_5));$

vlr1_5=-vcr_5-vx;

%%% Mode 6 %%%

% t_6=(1/w1)*(acot((w1*cr/ilr1_5)*(vcr_5+vx-vo)));

g=-(w1*cr)*(vcr_5+vx-vo); k=-ilr1_5;

t_6=(atan(k/g)+pi)/w1; t6=0:1e-9:t_6;

vcr6=(vcr_5+vx-vo)*cos(w1*t6)+(ilr1_5/(cr*w1))*sin(w1*t6)-vx+vo;

ilr16= (-cr*w1)*(vcr_5+vx-vo)*sin(w1*t6)+ilr1_5*cos(w1*t6);

 $vcr_6 = ((vcr_5 + vx - vo)*cos(w1*t_6)) + ((ilr1_5/(cr*w1))*sin(w1*t_6)) - vx + vo$

 $ilr1_6 = (-cr^*w1)^*(vcr_5+vx-vo)^*sin(w1^*t_6)+ilr1_5^*cos(w1^*t_6);$

% t5=(((pi/we)+(pi/(2*w2)))+(pi/we)-((1/we)*acos(1-((iin*z2*lr1)/(vcm*le))))):1e-9:((((pi/we)+(pi/(2*w2)))+(pi/we)-((1/we)*acos(1-((iin*z2*lr1)/(vcm*le)))))+(1/w1)*(acot(((vcr_4*w1)-(399*w1))/(ilr_4/cr))));

% t_5= $(1/w1)*(acot(((vcr_4*w1)-(399*w1))/(ilr_4/cr)));$

% vcr5=(400*(1-cos(w1.*t5)))+(vcr_4*cos(w1.*t5))+((ilr_4/(cr*w1))*sin(w1.*t5));

% vcr_5=(400*(1-cos(w1*t_5)))+(vcr_4*cos(w1*t_5))+((ilr_4/(cr*w1))*sin(w1*t_5))

%%%%In order to have zcs for main and auxiliary switches, the following conditions should be satisfied respectively:

%%%% (pi/we)-((1/we)*acos(1-((iin*z2*lr1)/(vcm*le))))>0;

%%%% (pi/we)-((1/we)*acos(1-(lr2/le)))>0

% T1=(pi/we)-((1/we)*acos(1-((iin*z2*lr1)/(vcr_5*le))));

% Ta=(pi/we)-((1/we)*acos(1-(lr2/le)));

% is1=iin-((vcr_5/z2)*(le/lr1)*(1-cos(we*t_3)));

% isa=(vcr_5/z2)-((vcr_5/z2)*(le/lr2)*(1-cos(we*t_3)));

Curriculum Vitae

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Post-secondary Education and Degrees:	University of Science and Research Kermanshah, Iran 2011-2013 MSC
	The University of Western Ontario London, Ontario, Canada 2017-2017 MSC
	The University of Western Ontario London, Ontario, Canada 2018-2021 Ph.D.
Honors and Awards:	MITACS Scholarship 2018-2021 (8 consecutive scholarships)
	Graduate student award for excellence in research, Western University London, Ontario, Canada 2019-2021
	Engineering award recipient, Western University London, Ontario, Canada 2019-2020
	Engineering award recipient, Western University London, Ontario, Canada 2020-2021
Related Work Experience	Teaching Assistant The University of Western Ontario 2017-2021
	Developing NZEBs by using HDERs The University of Western Ontario- AVL Manufacturing 2018-2021

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