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Power Management and Control to Balance Residential Microgrids with Individual Phase-wise Generation and Storage

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Abstract

The past decade has seen a significant rise in proliferation of roof-top photovoltaic (PV) systems with storage units at residential sites. This has affected the way power system engineers and researchers have previously studied distribution systems as passive networks. With the introduction of these local distributed energy resources, a distribution system has become part of an active network. This modernization of the power distribution network, brings along with itself a number of key issues that need to be pro-actively tackled by the local utilities.

In North America, with family-owned roof-top PV systems, storage devices and electric vehicles, the concept of central generation has transformed to local distributed generation (DG). With this phenomenon reshaping the current perspective of distribution networks, the local generation and storage capacities, with their respective controllers, allow for these DG units to be grouped together to form single-phase microgrids most commonly referred to as *residential microgrids*. This thesis looks into the two key issues pertaining to residential microgrids i.e. accommodating multiple embedded generation and energy storage units while balancing the generation and loading in each phase to achieve overall three-phase system balance.

A benchmark distribution system model is proposed in this thesis to study residential microgrids both in grid-connected and islanded modes. Limitations in existing distribution network models have been identified along with possible architectures for these residential microgrids. The configuration parameters of the benchmark model have been carefully selected after consultation with the London Hydro (local power utility in Lon-

don, Ontario). Several case studies have been presented to show that the proposed benchmark model can be used to represent a particular architecture of the residential microgrids.

Mathematical foundations of balancing residential microgrids through back-to-back converters have been developed in this thesis, which lay the foundation stone of the subsequent contributions with regards to this thesis. An online toolkit is developed in LabVIEW from the derived mathematical formulations.

Two power management strategies for single-phase residential microgrids, namely *intra-phase* and *inter-phase* power management strategies have been proposed which cater for the coordinated control of these single-phase microgrids to balance generation and loading in all of the three-phases seen from a primary feeder.

An operational control strategy has been later studied for optimal selection of power surplus phase(s) to mitigate the deficit(s) in other phase(s). This allows the system to transfer power from the surplus phase(s) to power deficient ones to achieve an overall balance, despite diverse load demand profiles in each phase.

An experimental validation of the proposed control strategies has been carried out with laboratory-scale design and development of the back-to-back converter along side single-phase sources, loads and a control platform to mimic a typical residential microgrid. From the experimental results, it is concluded that phase imbalance can be mitigated by the transfer of surplus power from a phase to the power deficit phase.

This work on power balancing single-phase residential microgrids can potentially open up new areas of research in the field of microgrids, especially with an unprecedented growth of roof-top PV panels.

Keywords: Single-phase microgrids, intra-phase power management, inter-phase power management, unbalanced systems, back-to-back converters.

Summary for Lay Audience

In North America, with roof-top PV systems, storage devices and electric vehicles, the concept of central generation has transformed to local distributed generation. With this phenomenon reshaping the current distribution networks, the local generation and storage capacities with their respective controllers allow for these generation units to be grouped together to form single-phase microgrids most commonly referred to as residential microgrids. The thesis looks into the two key issues pertaining to residential microgrids i.e. accommodating multiple embedded generation and energy storage units while balancing the generation and loading in each phase to achieve overall three-phase system balance. An experimental validation of the proposed control strategies has been carried out with laboratory-scale design and development of the back-to-back converter and a control platform to mimic a typical residential microgrid. This work on power balancing single phase residential microgrids can potentially open up new areas of research in the field of microgrids.

Dedication

To,

My parents; without their prayers I am nothing.

My brothers; who are always there in time of need.

My wife; for her patience and faith in me, because she always understands me.

My sons; their unyielding love has always inspired me to push forward every time.

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I would also like to acknowledge the efforts that my wife has made over the last many years. Her support and encouragement during the most tumultuous moments has left an indelible mark in my life, which I will remember for a long time. She gave me two beautiful children during this time. Their cute smiles are enough to reinvigorate my spirits for the final push.

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Declaration

The contents of Chapters 3, 5 and 6 are previously published IEEE papers of author and have been used as such. IEEE has allowed the use of these papers for the purpose of using it in this thesis.

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List of Abbreviations, Symbols, and Nomenclature

Chapter 1

PV:	Photovoltaic
DG:	Distributed Generation
RERs:	Renewable Energy Resources
MEG:	Microgrid Exchange Group
DOE:	Department of Energy
CHP:	Combined Heat and Power
LV:	Low Voltage
FC:	Fuel Cell
VSC:	Voltage Source Converter
SMES:	Superconducting Magnetic Energy Storage
SOC:	State of Charge
EMS:	Energy Management System

PCC:	Point of Common Coupling
ω:	Angular frequency
D_P:	Droop coefficient of real power
D_Q:	Droop coefficient of reactive power
ΔP:	Incremental change in real power
$\Delta\delta$:	Incremental change in angle
$\Delta\omega$:	Incremental change in angular frequency
G:	Feed-forward gain
K_p:	Proportional gain
R/X:	Ratio of resistance and reactance
VPD:	Voltage-real Power Droop
FQD:	Frequency-reactive Power Droop
THD:	Total Harmonic Distortion
LAN:	Local Area Network
$MPPT$:	Maximum Power Point Tracking
RES:	Renewable Energy Source
SDC:	Switching Droop Control
URC:	Urban Residential Customers
LDC:	Local Distribution Company
FIT:	Feed-In Tariff
RL:	Residential Load
$STATCOM$:	Static Synchronous Compensator

BTB: Back-To-Back

SMC: Sliding Mode Control

Chapter 2

V_P: Primary winding voltage of transformer

V_S: Secondary winding voltage of transformer

I_P: Current flowing in the primary winding

I_S: Current flowing in the secondary winding

N_P: Number of turns on the primary coil

N_S: Number of turns on the secondary coil

ϕ: Phase

$EMTDC$: Electro-Magnetic Transients including DC

Chapter 3

R_p: Resistance of primary feeder

X_p: Reactance of primary feeder

$ACSR$: Aluminum-Copper Steel Reinforced

r_N: Service drop cable resistance for Nth customer

Δr_N: Change in cable resistance for the Nth customer

R_A: Resistance of cable serving customers on Phase A

X_A: Reactance of cable serving customers on Phase A

CFL: Compact Fluorescent Lamps

Chapter 4

ΔP_{PV}: Incremental change in PV power

ΔP_{Batt}: Incremental change in battery power

ΔP_{Droop}: Incremental change in power of droop unit

P/f: Power and frequency droop characteristics

PI: Proportional Integral

$=$: Balanced condition in phases

$\rightarrow$: Power transfer from current phase to other phases

$\leftarrow$: Power received from another phase

¤: Drawing more power from sub-station transformer or load shedding

V_{an}: Voltage in Phase A

V_{bn}: Voltage in Phase B

V_{cn}: Voltage in Phase C

V_0: Zero sequence voltage

V_1: Positive sequence voltage

V_2: Negative sequence voltage

z_a: Impedance in Phase A

z_b: Impedance in Phase B

z_c: Impedance in Phase C

z_n: Impedance in neutral

z_y:	Base impedance in each phase
Δz_{y1}:	Incremental change in impedance in Phase A
Δz_{y2}:	Incremental change in impedance in Phase B
Δz_{y3}:	Incremental change in impedance in Phase C
I_a:	Current flowing in Phase A
I_b:	Current flowing in Phase B
I_c:	Current flowing in Phase C
P_{ϕ_z}:	Power delivered to one of the three-phases
$I_{L_{\phi_C}}$:	Line current flowing in Phase C
$I_c^{'}$:	Surplus current flowing in Phase C
$cos\theta_L$:	Power factor
m_C:	Modulation index of the back-to-back converter for ϕ_C
V_{DC}:	Voltage across DC link capacitor
m_A:	Modulation index of the back-to-back converter for ϕ_A
$E_{B2B_{\phi_A}}$:	Enabling signal for the back-to-back converter
η:	Power loss factor of the converters
n:	Power ratio between the power deficiency to power surplus
$P_{surplus,A}$:	Surplus power in Phase A
$P_{total,A}$:	Total available power in Phase A
$P_{pv,A}^{max}$:	Maximum capacity of PV unit in Phase A
$P_{batt,A}^{max}$:	Maximum capacity of battery unit in Phase A
$P_{droop,A}^{max}$:	Maximum capacity of droop unit in Phase A

$P_{\phi A}^{intra}$: Intra-phase power in Phase A

$f_{batt,A}$: Droop frequency of battery in Phase A

f_0: Nominal frequency

$f_{droop,A}$: Frequency of droop unit in Phase A

$P_{load,A}$: Load power in Phase A

$Priority_{pv}$: Priority of power contribution from PV unit

$Priority_{batt}$: Priority of power contribution from battery unit

$Priority_{droop}$: Priority of power contribution from droop unit

$P_{B2B_{\phi_A}}^{ref}$: Power reference for back-to-back converter connecting Phase A

$P_{B2B_{\phi_B}}^{ref}$: Power reference for back-to-back converter connecting Phase B

$P_{\phi_A}|PT$: Surplus power transfer from Phase A

$P_{\phi_B}|PT$: Surplus power transfer from Phase B

$P^{sup}|_{\phi_z}$: Surplus power in a phase

$P_{loss}|_{\phi_z}$: Power loss in a phase

$P^{req}|_{\phi_y}$: Power required in a phase

$P_{loss}^{B2B}|_{\phi_x}$: Power loss in a back-to-back converter

Tfr_{loss}: Losses in the transformer

P_{loss}^{cap}: Power loss across the DC link capacitor

P_{con} : Conduction losses due to switching of gates

$P_{B2B_{\phi_A}\&_{\phi_C}\rightarrow\phi_B}$: Surplus power transfer from Phase A to Phase B

Chapter 5

L:	Inductance
C:	Capacitance
$\frac{d\bar{i_L}}{dt}$:	Average rate of change of current flowing in inductor
$\frac{d\bar{v_0}}{dt}$:	Average rate of change of voltage across the capacitor
V_i:	Input voltage
$\bar{v_0}(t)$:	Average output voltage
R:	Resistance
$\bar{v_L}$:	Average voltage across the inductor
d:	Duty cycle
$\bar{i}_C(t)$:	Average capacitor's current
r_{pv}:	Dynamic resistance of PV array
r_{pv-cs}:	Dynamic resistance in the current source region
r_{pv-vs}:	Dynamic resistance in the voltage source region
V_{batt}:	Battery's voltage across terminals
V_{B-C}:	Battery voltage
C_B:	Capacity of battery
i_B:	Charging current of battery
V_{B-D}:	discharge cycle of battery
T:	Transformation matrix
T^{-1}:	Inverse transformation matrix
α:	alpha-axis quantities

β: beta-axis quantities

d: d-axis quantities

q: q-axis quantities

$P^{max}_{exhange,\phi}$: Maximum power that can be transferred between phases

Chapter 6

K_c: Gain of PI controller for current control loop

K_i: Integral gain of PI controller for current control loop

K_v: Gain of PI controller for voltage control loop

K_{vi}: integral gain of PI controller for voltage control loop

f_{min}: Minimum frequency of single-phase residential microgrid

SOC_{min}: Minimum state-of-charge of battery

SOC_{max}: Maximum state-of-charge of battery

$E_{B2B_{\phi_A}}$: Enable signal of the back-to-back converter connecting Phase A

$E_{B2B_{\phi_B}}$: Enable signal of the back-to-back converter connecting Phase B

$i^*_{\phi_A}$: Current reference of back-to-back converter for Phase A

$i^*_{\phi_B}$: Current reference of back-to-back converter for Phase B

$i^*_{\phi_C}$: Current reference of back-to-back converter for Phase C

K_1: Gain constant

K^1_p: Gain of PI controller

K^1_i: Integral gain of PI controller

L_x: Load step change

$e(t)|_x$: Net real power required by the deficit phase

Chapter 7

$P^x_{surplus}$: Surplus power in Phase x

$P_{B2B_{\phi A,B,C}}$: Power reference of the back-to-back converters

$P_{req_{\phi x}}$: Power required by Phase x

P^{ref}_{grid}: Power reference for the grid

Chapter 8

DCB: Direct Copper Bonded

CMOS: Complementary Metal-Oxide Semiconductor

TTL: Transistor-Transistor Logic

TI: Texas Instruments

R_{thsa}: Thermal resistance of the heat sink

G_{cl}: Feed-forward loop gain of back-to-back converter

$e(\infty)$: Steady state error

T_r: Rise time

T_p: Peak time

T_s: Settling time

$\%O.S$: Percentage Overshoot

$\%U.S$: Percentage Undershoot

ESR: Effective Series Resistance

E_{on}: Turn on energy loss

E_{off}: Turn off energy loss

FFT: Fast Fourier Transform

Chapter 1

Introduction

1.1 Motivations

According to World Bank's report, approximately 11.1% of the total world population is without electricity [1]. This lack of electricity access is a critical global issue, which is undermining the progress of nation states. Human development and economic indicators including the growth in gross domestic product (GDP) are all linked with how well a country is connected through electricity. Unfortunately, off the remaining 89% of global population that do have access to electricity, some suffer with extended power outages in both urban and rural areas. This is mainly due to lack of electricity generation resources, aging transmission/distribution infrastructure, climatic conditions, increased network losses and load demand.

To increase the global access of electricity, there is a global policy shift of encouraging utilities to move from localized and conventional power production to a more distributed power generation network, relying more and more on renewable energy sources e.g. photovoltaic (PV). In this essence, there is growing proliferation of roof-top PV and household energy storage systems at residential sites [2]. The residential market of PV installations has experienced annual growth in the USA. According to "U.S Solar Market Insight Re-

port", the first quarter of 2019 saw 603 MW of residential PV installations [3]. This figure is a reflection of 6% annual growth in roof-top PV installations.

In Canada, the population is growing and so is the annual demand for electricity. According to government of Canada, the electricity demand is expected to grow at an annual rate of 1% between 2014 and 2040 [4]. In this respect, the power utilities are encouraging their customers to make use of solar power for residential needs. There are several advantages for customers to use PV systems in their homes. Firstly, a solar system can meet 20 to 100% of the annual power needs to run a home. With the incentives given by local provincial governments, the cost of electricity from roof-top PV systems will be close to buying power from the Hydro utilities. It is anticipated that the cost of solar electricity will get cheaper every year [5]. Secondly, a solar system typically yields 5-10% rate of return on the cash invested. Finally, the local PV generation provides cost of electricity independence to the customers. Rising utility cost will not affect these customers in the same way.

With the proliferation of PV systems at the residential level, the landscape of distribution system is changing rapidly. Several issues arise with this unprecedented growth. Reverse power flow in the distribution network is a major issue due to resultant voltage rise during light loading and high PV generation conditions [6–8]. Traditionally, the distribution systems are capable of handling impacts of low bus voltage. Therefore, voltage control is necessary under high proliferation of PV systems, which has become a popular area of research.

Increase in PV generation at the residential sites, will cause phase balancing issues at the distribution side, which are expected to receive significant interest in the future [9,10]. Phase unbalance is allowed to a certain degree in the distribution network i.e. between 1.3% up to 2% of negative phase sequence [11]. The current practice is to conduct a load profile assessment associated with the distribution transformer, and then distribute the loads among three phases. Since loads are changing all the time, no perfect balance

can ever be achieved during operation. If design is properly performed, the mismatch should remain to be small. However, with proliferation of single-phase distributed power generation, the imbalance could be too significant to bear. For example, two streets, say X and Y, are connected to two separate phases, roof-top PVs installed on street X receives more sun shine in the morning than that on street Y. The difference in PV production on these two streets will create an imbalance. Similar situation can happen if one street has more electric vehicles than the other one. These 'modern' apparatuses increase the uncertainties for distribution system planning and operation.

Moreover, the rapidly evolving trend of installing PV systems in residential areas, has forced local utility companies to carry out extensive planning, load-forecasting, for both steady-state and dynamic capacity studies, and reliability assessment of their distribution system's infrastructure [12]. Needless to say, that to carry such studies, it is imperative to have a more detailed realistic model of the distribution network, which is able to simulate and capture this ever-changing landscape in distribution systems.

Furthermore, with the future of distribution networks moving towards smart grid technology, the electricity consumers have become a very important part of the power market. In fact, with local distributed generation, like that at residential roof-tops, the term '*consumers*' will not be a valid term in the future. In the envisioned future electricity markets, hundreds of thousands of independently operating residential producers will allow for a significant increase in distributed renewable energy resources to be integrated into the nation's electric grid [13]. Hence, today the consumers have become *prosumers* (producers and consumers of electricity), and will be key stakeholders in the future power market. In this respect, the utilities may need to come up with infrastructural changes to their distribution network to allow for these prosumers to integrate.

To solve some of the problems stated above, microgrids were proposed as a way forward to integrate a high penetration of renewable energy resources with the grid. This is a paradigm shift from conventional grids in order to reduce harmful emissions from

fossil fuels and combine the advantages of distributed generation (DG) sources. The DG units are known for reducing power losses in the distribution network, provide ancillary services to the grid and possess local voltage and frequency support [14, 15]. Increasing the participation of DG units has an effect on reducing the microgrids operational cost and allowing the network operators the ease of integrating renewable energy resources (RERs) [16].

1.2 Microgrids

Microgrid Exchange Group (MEG) of the U.S. Department of Energy (DOE) defines microgrid as: "A group of interconnected loads and distributed energy resources (DERs) within clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid. A microgrid can connect and disconnect from the grid to enable it to operate in both grid-connected or islanded mode" [17]. There are three aspects of this definition. Firstly the elements included in a microgrid are various DERs (solar, wind, micro-turbines and CHPs) connected with local loads. Secondly the microgrid must form one unit that can be controlled with respect to the grid. The formation of one unit is through a hierarchy of control layers, each with different functions. Finally, the definition points to the two operating states of a microgrid. The main advantage of setting up a microgrid is its ability to operate in islanded mode through the various layers of control strategies, while observing IEEE 1547 standard for interconnecting DERs [18].

The advantages of microgrids are two folds; both from the customer's and grid operator's point of view. For the customer, microgrids can provide electricity needs especially in times of potential black outs upstream in the transmission system. For the grid operator, by considering a microgrid as a controllable entity within a power system, a particular microgrid can be operated as a single aggregated load or generator. This synergy of local loads and micro source generations allows a microgrid to provide economic, technical,

environmental and social benefits to different stakeholders.

1.2.1 Distributed generations

As microgrids are setup at LV distribution, it is expected that the generators used will be of low power ratings, typically less than 200 kW [19]. Most of the DG units used in microgrids are not suitable for direct connection to the PCC because of the form of power they produce. For example, the output from photovoltaic (PV) is DC while from micro turbines and wind generators it is unregulated AC [20–22]. Hence, they have to be interfaced with power electronic converters. DG units that are AC sources are interfaced with AC-to-DC converters while DC sources are interfaced through DC-to-DC converters. These converters also cause decoupling of the rotating dynamics hence imparting minimal inertia. The type of generators that are used are micro turbines, wind generators, PV, fuel cells (FC) and CHPs. While gas and diesel generators can provide backup support to the microgrid in case of emergencies [23].

1.2.2 Electrical energy storage devices

A microgrid can operate both in grid connected and in islanded mode. In grid connected mode, the voltage and frequency are regulated by the main grid but in islanded mode, the two quantities need to be supported by the microgrid itself, usually through synchronous generators. For a microgrid without synchronous generators, one way of maintaining voltage and frequency is by voltage source converter (VSC) interfaced energy sources. The intermittent nature of power delivered by renewable resources in a microgrid causes difficulties in controlling accurately the generated power [24, 25]. Hence the use of energy storage systems becomes even more important. These systems can provide the power difference between the generation and the load demand in situations of intermittency of renewable energy resources and also during load switching [26]. Some of the common types of energy storage systems are batteries, super capacitors, flywheels

or superconducting magnetic energy storage (SMES).

1.2.3 Primary control issues in microgrids

As stated earlier, the microgrids can operate in both grid connected and islanded modes. Operating in these two modes require a number of primary concerns to be addressed appropriately. To summarize the requirements for microgrid control are [27, 28]:

Voltage and frequency regulation for grid connected and islanded modes

The control systems for inverters must ensure that the voltage and frequency for the microgrid is regulated during both the grid connected and islanded mode. Voltage control must ensure that there are no large circulating reactive power between sources. Without local voltage control, microgrids with high penetration of micro sources could experience voltage and/or reactive power oscillations. This is analogous to conventional systems with synchronous generators. The difference being that in conventional systems generators have large impedance and hence circulating currents are not present [29]. In a microgrid, on the other hand, low and/or no impedance between sources means that these circulating currents pose a significant problem. Small deviations in voltage set-points can cause the circulating current to exceed the ratings of micro sources. Hence there is a need for suitable voltage vs. reactive power droop control strategy.

As with the voltage regulation, the principle behind frequency control in microgrids can again be compared with conventional synchronous generator based systems. As is the case with voltage control, where voltage vs. reactive power droop control is used, for frequency regulation; frequency vs. active power droop strategy is utilized. A conventional synchronous generator can change its output power in response to the system requirements by varying the frequency using the droop control. The difference in frequencies between two points in the system allow for power exchange. As a consequence, the two different system frequencies tend to move towards a common frequency until the

new steady state is achieved. This relationship between active power and frequency need to be implemented for the inverter interfaced sources.

Distributed energy resource (DER) coordination

With multiple RERs connected together, one of the important issues is their coordination. Typically we have three basic methodologies for this purpose. Firstly, the master-slave topology, where one inverter regulates the voltage. The master acts as a voltage source, while all other inverters work as current sources. The main features of this topology include simplicity of control algorithm, requirement for supervisory control and high communication requirement. Due to the trade off in communication requirements, the system can become difficult to expand. Hence this topology becomes unsuitable because of high dependency on communication links and the need for supervisory control.

A multi-master control scheme on the other hand, allows the inverters to set their instantaneous active and reactive power references based on the droop functions described earlier. There is a still a requirement for supervisory control, but its functionality is limited to setting set-points for frequency, voltage or droop slopes. Hence, the need of expensive communication links between the sources is significantly reduced. The advantages of this topology include flexible system expansions, increased reliability of the system as compared to master-slave topology, and simpler objectives for supervisory control layer.

Power management between the grid and the microgrid

Non-dispatchable sources require adequate weather conditions and/or fuel requirements to produce power, which may not always be the case. Energy storage devices are required to be connected with these sources. Power management strategy helps i) to control the power output of individual DG units, ii) to regulate the voltage and frequency of microgrid, iii) to have optimum cost, iv) power sharing v) maintain the balance between

the power generation and the power demand and vi) allows for adequate means to use non-dispatchable sources along with storage devices to serve the loads both in grid connected in islanded modes. Power management of a resilient and sustainable power infrastructure is a challenging one which provides a reliable and efficient power supply [28]. This strategy is needed for quick operation of a microgrid with multiple DG units particularly in autonomous mode. The main concerns include the power management strategies to be employed either centralized or decentralized, communication interface for centralized control, reactive power sharing amongst units and conservation of batterys state of charge (SOC).

Microgrid synchronization with the main grid

Operation of microgrid in islanded mode may be temporary and hence there is a need for reconnection of the system with the main grid. Islanded microgrids cannot be reconnected with the grid immediately after the fault is cleared because it may have consequences over the frequency and voltage due to difference in generations in the two systems (grid and islanded microgrid) and the loads that are being served. In order to have a smooth transition, the phase angle and frequency of the two systems must match. This will further require the coordination of all the inverters. Power oscillations may be experienced during the transitioning phase, but these can be minimized depending upon the synchronization process of the inverters and droop set-points communicated to them through the supervisory control layer.

As can be seen from section 1.2.4 that voltage and frequency need to be regulated in both the grid connected and islanded modes, the interconnection of DG units require proper coordination, a power management strategy has to be established between the grid and the microgrid and synchronization of islanded microgrid with the main grid. The literature review will look at PV and battery based islanded microgrids and will introduce the primary concerns of these microgrids to lay the basis for residential micro-

grids. Critical analysis of the literature in this domain will be carried out in terms of control strategies that were adopted in each case for system stability and reliability.

1.3 Background

The concept of microgrids is relatively new with the earliest literary contribution in this field coming at the turn of the century. Since then, a lot of research work has been performed in this field with respect to a number of issues related to its control and integration with the conventional grid. The primary concerns as discussed in the previous section will be control of voltage and frequency, coordination of DERs, power management between the grid and the microgrid and the synchronization of the system with the main grid. With the added advantage of these microgrids to go islanded or autonomous, these concerns become even more crucial to tackle.

In this section, the issues concerning the control of PV/battery based microgrids (both in grid and islanded modes) will be discussed with particular focus on autonomous operation, followed by their power management strategies in both three-phase and single-phase microgrids. The final section will be dealing with seamless synchronization issues of microgrids. This will lead to identifying a particular area in microgrids which requires further research and development in the future.

1.3.1 PV arrays as DG sources

Amongst the DG sources, PV is a preferred source for residential microgrids mainly because the related technology has reached an advanced stage and the government is giving numerous subsidies which has made power production through PV an economical option [30]. The output power from the PV array largely depends on solar irradiance, temperature, and the output voltage. In literature, mathematical models of individual components of the PV system are represented and simulated for better understanding of

their performance [31]. The parameters related to the PV array should be calculated for mathematical modeling as these parameters are usually not included in the manufacturer data sheet. The integration of PV array to the DC bus is usually performed by an intermediate DC-DC converter [32].

1.3.2 Primary concerns

Section 1.2.3 highlighted the general concerns in microgrids. Building on these PV/battery based islanded microgrids have further primary requirements to be catered for. These have been summarized below,

1. Power generation through PV is dependent upon irradiance and temperature. Hence atmospheric conditions play a key role in determining the power output from this source. For islanded microgrids, intermittent energy sources like PV can be connected in different topologies with backup battery reserve. This includes i) deploying them as separate units [33,34], b) PV and battery forming a hybrid unit [35,36] or c) with droop controlled converter units [37,38].

2. The battery's SOC must not exceed maximum SOC while charging or decrease below minimum SOC while discharging [39,40].

3. The PV/battery units within a microgrid need to be controlled through droop controlled based converters so that the frequency and voltage can be regulated. It is also demonstrated that PV arrays alone can perform frequency regulation. This is performed by power curtailment at the inverter side and has been field tested to demonstrate its effectives [41].

4. Battery is a critical reserve and must only be in operation when the power generation from PV is unable to support the load and during the transient stage of sudden load changes [37,40].

5. Coordination of multiple units must be handled by central or decentralized energy management system (EMS), which sets power references for these units [22, 42].

1.3.3 Grid connected microgrids

A considerable amount of work has already been performed for grid connected mode and the theoretical backgrounds for control strategies have been soundly established. The earliest and substantial contribution in this respect is given in [20]. The primary control generally provides the references for the inner current loops and outer voltage loops. These loops are referenced to zero and primarily used as PQ control in grid connected mode. In this control type, the real and reactive powers are regulated on pre-determined points and provides references for the inner loops. Here voltage source converter (VSC) is operated in current control mode. The DC link voltage is used to regulate the real power while the q-axis component of the output current is used for the reactive power control.

1.3.4 Islanded microgrids

Autonomous mode of microgrids refers to the situation when the system is off the grid at the PCC; either intentionally or unintentionally. As a result, the power has to be supplied from the generating units that are within the confines of the microgrid [43, 44]. The advantage being that the locally connected loads can still operate without any interruption caused due to faults on the grid side. The breaker at the PCC operates and isolates the microgrid from the fault scenario. The backup energy storage devices provide the net power to the load and are vital for such configurations. Being an advantage that a microgrid can run autonomously, the control becomes increasingly complex and essential for stability of the system. The control of VSC switches from current control mode to voltage mode control. The voltage references are obtained from the well-known droop characteristics relating it to reactive power while the frequency reference is obtained

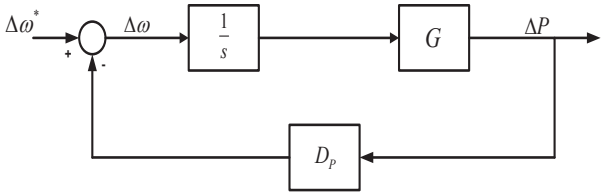


Figure 1.1: Small signal model of the conventional power control.

through its relationship with real power. In autonomous mode, the utility will not have direct prerogative in maintaining the microgrids voltage and frequency and hence these issues must be dealt by controllers that are local to the microgrid itself. They will solely be responsible in maintaining the power balance and power quality within the microgrid. The transition of these microgrids from islanded mode to grid connected mode should adhere to IEEE 1547 standard [18].

1.3.5 Droop control in autonomous microgrids

This control technique has been widely used in literature due to its inherent decentralized control properties [20, 45–50]. With multiple DER units, the droop coefficients should also follow the constraint of limiting the deviations of frequency and voltage to their maximum allowable values [51].

For a given converter connected to the PCC through an impedance , the complex power can be written as,

$$S = V_{PCC} \times I^* = \frac{V_{PCC}E\angle\theta - \delta}{Z} - \frac{V_{PCC}^2\angle\theta}{Z} \tag{1.1}$$

From above, the real and reactive power can be derived as,

$$\begin{aligned} P &= \frac{V_{PCC}E}{Z}\cos(\theta - \delta) - \frac{V_{PCC}^2}{Z}\cos(\theta) \\ Q &= \frac{V_{PCC}E}{Z}\sin(\theta - \delta) - \frac{V_{PCC}^2}{Z}\sin(\theta) \end{aligned} \tag{1.2}$$

The relationship between frequency and voltage is given as,

$$\omega = \omega^* - D_P P$$
$$V = V^* - D_Q Q \tag{1.3}$$

Where, ω^* and V^* are the DER output voltage RMS value and angular frequency at the no-load respectively while D_P and D_Q are droop coefficients. These coefficients are determined based on the converter power rating and the maximum allowable voltage and frequency deviations.

Linearizing equations (1.2) and (1.3) gives,

$$\Delta P = G\Delta\delta$$
$$\Delta\omega = \Delta\omega^* - D_P\Delta P \tag{1.4}$$

Where,

$$G = \frac{V_{PCC0}E_0}{Z}\cos(\theta_0)$$
$$\Delta\delta = \int \Delta\omega dt \tag{1.5}$$

Hence,

$$\Delta P(s) = \frac{G}{s + D_P G}\Delta\omega^*(s) \tag{1.6}$$

The conventional droop control can be implemented without communication links. However, there are some disadvantages of using this technique which are listed below,

1. It is observed that every droop characteristic has one control variable, hence with multiple units it would be impossible to satisfy all control objectives in this case [52, 53]. The block diagram as shown in Fig.1.1 can be modified to tune the characteristics of this strategy, based on the time constant of the control system [52].

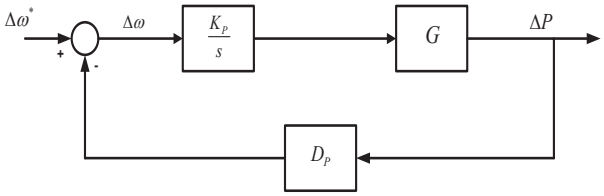


Figure 1.2: Small signal model of the adjustable active power control.

By making the phase angle of VSC a function of integral gain, the deviations in real and reactive power become functions of these gains. This modification in the droop strategy allows for improved voltage regulation, robust performance even if there is a variation in the system parameters and voltage and frequency controls are not compromised by adjusting the controller speed. Using this strategy, the voltage regulation can degrade when handling non-linear loads.

This is also shown in Fig.1.2. The modification in the droop strategy allows for improved voltage regulation, robust performance even if there is a variation in the system parameters and voltage and frequency controls are not compromised by adjusting the controller speed. Using this strategy, the voltage regulation can degrade when handling non-linear loads.

2. The conventional method requires adjustment for microgrids where the R/X ratio is $>> 1$ [27, 54]. Voltage-real power droop (VPD) and frequency-reactive power droop (FQD) strategy has been proposed as a consequence in [55]. When the line impedance essentially becomes resistive at LV distribution system, the relationship between droop coefficients as given in (3) can be written in terms of voltage-real power and frequency-reactive power terms. This improved droop strategy becomes easy to implement with the assumption that the line is highly resistive. Similar to the earlier modification, changing the controller time constant does not affect the voltage and frequency controls. This technique suffers from high dependence on system parameters and can only work for highly resistive transmission lines. The voltage regulation is also affected when handling non-linear loads. The short falls

of VPD/FQD technique can be overcome by using the transformation methodology as suggested by [56–58]. The transformation matrix that is used is an orthogonal matrix which causes the real and reactive powers to become independent of the line impedances. This decoupling of powers requires prior knowledge of the system parameters especially the impedance. This technique still is unable of handling non-linear loads and suffers from voltage regulation problems. Another affect that can be observed is that the control loop time constant and the voltage/frequency regulation now have been compromised by this methodology. The use of virtual output impedance is yet another way of adjusting the output impedance of VSC as suggested in [27, 59, 60]. In this configuration the output voltage of VSC is proportionally drooped with respect to the output current. The advantage of this methodology is that it can handle non-linear loads as the harmonic currents can be shared appropriately. Also this method does not have dependency on the system parameters. It has been observed that adjusting the control loop time constant may result in undesired deviation in the DER voltage and frequency.

3. The voltage is not a global variable so reactive power control may affect the voltage regulation of critical loads [54]. The conventional droop control scheme need to be modified as such to make it adaptive. This can be done by compensating the original voltage-reactive power droop as in (3) to include the voltage drop in the across the feeder impedance. The voltage imbalance in single-phase systems is mitigated through this methodology. Although this resolves the issue of voltage regulation, it inherently becomes a function of the real power. In this case, the droop coefficients will no longer be constant values, instead it will become a non-linear function of real and reactive power. This technique may not handle non-linear loads, requires prior knowledge of feeder parameters, and adjusting the time constants of the controller may cause unnecessary deviations in voltage and frequency.

4. The conventional strategy cannot distinguish between load current harmonics from circulating current. It has to be modified such that the total harmonic distortion of the output voltage is reduced [61–64]. Two approaches were identified for this modification. In the first methodology, the DERs equally share the linear and non-linear loads. The current harmonics are sensed and are used to calculate the corresponding droop voltage harmonics. As a result of this technique, the THD of the output voltage is significantly improved. In the second methodology, the conventional droop method is modified to compensate for the harmonics of the DER output voltage. These harmonics are generated to the distorted nature of the load current. These methodologies are affected by system parameters. For precise reactive power sharing, there may be poor voltage regulation. Finally, the time constant of the controller can affect the voltage and frequency controls.

   The modified droop control techniques are summarized in Table 1.1.

1.3.6 Power management in PV/Battery based islanded microgrids

Power management strategies have been discussed in [35,37,68–72]. These control strategies can be centralized are termed as Energy Management System (EMS) and are highlighted in [68–70, 73, 74]. A central EMS needs to dispatch power output references to each unit connected in an islanded microgrid over a communication channel. This channel can be either wired using protocols for Local Area Network (LAN) (IEEE standard 802.3) or through wireless interface using standard WiMAX protocols as set in IEEE 802.16 [75, 76]. The advantage of having a central EMS allows ease in power management and resynchronization with the grid before microgrids transition from islanded to grid connected mode. The most glaring disadvantage in this case will be the single point of failure. A breakdown in the operation of EMS may compromise the operation of the

Table 1.1: Summary of Droop Control Techniques

Droop Methodology	**Advantages**	**Disadvantages**
Conventional droop method [65, 66]	• Ease of implementation	• Affected by system parameters. • Only functional for highly inductive transmission lines. • Cannot handle non-linear loads. • Voltage regulation is not guaranteed. • Adjusting the controller speed for the active and reactive power controllers can affect the voltage and frequency controls.
Adjustable load sharing method [52]	• Adjusting the controller speed for the active and reactive power controllers without compromising the voltage and frequency controls. • Robust to the system parameter variations. • Improved voltage regulation.	• Cannot handle non-linear loads.
VPD/FQB droop method [53]	• Ease of implementation • Adjusting the controller speed for the active and reactive power controllers without compromising the voltage and frequency controls.	• Affected by the system parameters. • Only functional for highly resistive transmission lines. • Cannot handle non-linear loads.
Virtual frame transformation method [56–58]	• Ease of implementation • Decoupled active and reactive power controls	• Cannot handle non-linear loads. • Prior knowledge of line impedances is required. • Adjusting the controller speed for the active and reactive power controllers can affect the voltage and frequency controls. • Voltage regulation is not guaranteed.
Virtual output impedance [59, 60, 67, 68]	• Ease of implementation • Not affected by the system parameters. • Functional for both linear and non-linear loads. • Mitigates the harmonic distortion of the output voltage. • Can compensate for the unbalance output voltages of DERs.	• Adjusting the controller speed for the active and reactive power controllers can affect the voltage and frequency controls. • Voltage regulation is not guaranteed.
Adaptive voltage droop method [54]	• Improved voltage regulation. • Not affected by the system parameters.	• Cannot handle non-linear loads. • Adjusting the controller speed for the active and reactive power controllers can affect the voltage and frequency controls. • Prior knowledge of system parameters is required.
Non-linear load sharing techniques [62, 63]	• Properly shares the current harmonics between the DERs and consequently cancels out the voltage harmonics.	• Affected by system parameters. • Poor voltage regulation for the case of precise reactive power sharing. • Adjusting the controller speed for the active and reactive power controllers can affect the voltage and frequency controls.

microgrid. Another disadvantage is the failure in the communication links between the units. A communication malfunction may cause irregular power references to be set and hence leads to destructive consequences in the long term reliability of the microgrid. On the other hand, the decentralized control structure does not have a central controller and the system operation is handled by local controllers at the DG units. In this way, the

physical limitation of setting up a central EMS system can be overcome but when the number of distributed units increase coordination issues with these units may increase complexity in decentralized control structure.

An SOC based battery management system for microgrids is introduced in [39]. The considered configuration only consists of the battery as a means of supporting the loads at the PCC, without any other sources of generations. The disadvantages of the control strategy employed in this work are the high dependency on the battery and that such configurations are generally not used for an islanded microgrid. As per the control algorithm, if the battery's SOC is below its minimum limit, while the system is in islanded mode, the battery gets disconnected from the system, causing a system shut down.

The control strategy as adopted in [73], suits the microgrid configuration under consideration. The microgrid consists of single battery storage, micro turbine, FC and PV units, and generations are directly connected to local loads. This microgrid setup can be classified under remote microgrid where the loads are near to the generation units themselves. The management system as considered makes the battery to work with the FC to meet the load demand when the DG units are unable to meet it. When the battery's SOC reaches its minimum value, the FC unit supplies for load demand while in other cases, both battery and FC unit will share the load demand. Hence the operating cycles of FC unit is compromised for low SOC of battery. The microgrid considered by authors in [74] consists of FC which regulates the DC link voltage of the converter. The battery is there to reduce the operating cycles of FC. The model predictive control strategy adopted prevents overcharging of the battery by curtailing the PV generation. The drawback with this strategy comes when the state space formulation of the system is considered. The moment the system is linearized with the assumption that the dynamics of the PV control system is slow, it will introduce prediction errors which may cause erroneous control signals to be sent to the converters. The control strategy proposed requires a fast sampling rate and hence there is a trade-off between complexity of control

design and the prediction accuracy as proposed in this work.

In order to avoid a central EMS, a power management scheme is proposed in [72], where a central battery bank is used with other DG units and are interfaced through a hybrid converter. The control algorithm that was proposed, prevented over charging of the battery. The issues with this strategy is concerning the hybrid converter itself. As the battery overcharges, the system frequency drops below the requirements for an islanded microgrid, consequently it may take the PV unit out of service. This will put additional constraint on the battery to serve the load during this period.

A decentralized power management control scheme is discussed in [77]. The system makes use of a single battery resource with multiple PV units to regulate the microgrids frequency. The droop strategy employed becomes a master-slave problem, where the battery, being the master, uses the information of SOC to direct the PV units to curtail power (PV slave operation) or to shed unnecessary loads (load slave operation). As the battery's SOC reaches its maximum value, the system frequency keeps increasing, until maximum allowable frequency deviation is reached. This signal is used by PV to move from MPPT state to start curtailing power. The energy storage system makes use of finite droop slope for this signaling. The loads in this configuration need to have priorities that need to be set earlier. All critical loads remain are given higher priority and remain in the system while all other loads may need to shed if the generation and battery is unable to support unnecessary loads. The drawback of this scheme lies in the master-slave operation itself, where the frequency and voltage regulation is performed by the unit designated as 'master'. Hence there exists a single point of failure.

A new approach towards decentralized coordination of RES was proposed in [71] where the DG units were connected to the PCC with two battery energy storages. The conventional droop scheme is modified to include control mode switching for both the DG units and the energy storage systems from maintaining constant voltage (voltage control mode) to transferring constant power (power control mode). This action is taken

discretely and is governed by system frequency and SOC of the batteries while for the PV units it is dependent upon frequency and real power produced. Since the modes are switched discretely, the control strategy is named switching droop control (SDC). Due to its characteristics, the transitioning from one mode to the other is not smooth as referred by the authors. The simulation results clearly show that the system suffers from large transients.

A complete decentralized power management approach is discussed in [37]. The tasks of power management are regulated amongst PV, battery and other droop units. The main focus is on the managing real power while maintaining fixed reference for the reactive power. The mode transitioning of units from power control mode to voltage mode control and vice versa as stated in [71], is performed in a reliable and efficient manner in this work. The battery is conserved such that it only meets peak load demand according to the microgrids real power-frequency characteristics. In this way, it can contribute to maintaining system frequency based on its SOC information. The control strategy is elegant as simple PI controllers are utilized for the inner and outer loops.

1.3.7 Residential microgrids

Residential microgrids is a relatively new domain in the area of microgrids with the first literary work appearing in 2010. As compared to the conventional three phase microgrids, these are single phased. It should be emphasized that such microgrids do exist in practice, e.g. residential customers in rural areas, multiple neighbouring communities or business districts [78]. Customers in remote rural areas suffer from low power quality and reliability because of long distances and weak transmission lines. Solar panels can be setup in these areas close to load points, which can be adequate to serve these loads. It should be noted that these resources are geographically bounded.

The provisions of setting up of PV on roof tops for urban residential customers (URC) are more relaxed in developed countries. Utilities have realized that distributed gener-

ation is a preferable solution to conventional methods of electricity generation, when faced with communities that oppose large transmission lines in their neighbourhoods. Local distribution companies (LDCs) in Ontario have introduced feed-in tariff (FIT) and micro-FIT programs, which set prices for electricity produced from renewable energy [79]. In this way, the customers can setup local PV units, which will serve to provide power for local loads and in scenarios where local generation exceeds the load demand, this can then be exported to the utility on a set price fixed under FIT.

1.3.8 Primary concerns for residential microgrids

Section 1.3.2 focused on the primary concerns with PV/battery based microgrids. With community based microgrids, which can be setup at distribution level the customers are capable of generating their own power through roof top PV connections. These are composed of small per phase microgrids, usually community based, which can island and synchronize with the grid. Along with the issues discussed in section 1.3, several other concerns have to be addressed for stable operation of such islanded microgrids, which are going to be addressed as 'Residential Microgrids' from here forth.

- Coordination amongst individual units in the same phase to regulate voltage and frequency at the PCC.
- Power balance amongst phases especially when the generation in one phase is more than its own load requirement and other phases can use the excess the power to meet their own local demand.

1.3.9 Control aspects in residential microgrids

Distribution transformers supply power to a community having center tapped secondaries which allows residential loads (RLs) to operate both at 110/120V (between phase and neutral) and 220/240V (between two phases). The DG units connected at residential scale can thus be coordinated together to form a small scale microgrid, in which the

energy sources will be operating at single phase. The coordination of DG units can take place locally i.e. within the community microgrids boundary and/or between two single-phase microgrids.

As mentioned previously, a lot of work has been performed for power management of three phase microgrid systems. This is not the case residential microgrids. Control strategies have been proposed for the reactive power compensation for these single phase microgrids using STATCOMs in [80,81], but the microgrids considered are only grid connected. It is also investigated that back-to-back converters can be used as an interface in single phase microgrids. The control strategy proposed allows the back-to-back converters to share power amongst phases in 3-phase distribution network, based on load requirements [78,82–84]. The back-to-back converter interface as suggested in [78], limits the power flow in one direction. It is assumed that one of the phases of microgrid always function as a load center with no local generation. The control strategy in this work depends on the communications, with a complex back-stepping based sliding mode control (SMC). Along with control complexity, this management scheme suffers from additional cost due to communication overhead. In [85], a hierarchical approach of power management issues in single phase roadway microgrids for operating traffic lights is discussed. This work assumes that the generation is the same in all the three phases for all case studies which does not provide a practical view, as the local generation may vary at any given instant of time. A summary of the work performed in the domain of residential networks is tabulated in Table 1.2.

1.4 Problems Under Investigation

This section presents a brief description of the problems under investigation in this thesis. Individual chapters in this work have detailed problem statements relating to the idea presented in that chapter.

Table 1.2: Summary of Power Management Techniques for Residential Microgrids

References	Features	Problem(s) Addressed
Sun et.al. [78]	• Per phase microgrids interfaced with back-to-back converters. • The back-to-back converters are controlled through modified sliding mode controller. • Individual inverters at each phase are droop controlled. • Low bandwidth communication is used for power management. • Individual microgrids can operate in both grid and autonomous mode. • The power flow is limited due to the back-to-back interface. • The control strategy employed has high communication dependence which may result in single point of failure.	• Power sharing • Power flow control
Majumder et.al. [80, 86]	• Single phase DGs interfaced with H-bridge to the PCC. • Distribution STATCOM (DSTATCOM) used to reduce the power oscillations while interacting with the grid to compensate for reactive power. • Operation of microgrid is limited to grid connected mode only.	• Power balance • Power quality
Majumder et.al. [82]	• Single phase DGs interfaced with back-to-back converters to the utility. • The system can run both in grid connected and autonomous modes. • The loads considered can be linear or non-linear.	• Power flow control • Power quality
Jiao et.al. [87]	• Hierarchical approach of solving power management problem amongst phases. • Local generations and loads are assumed to be the same amongst phases. • The loads considered are pole mounted traffic signals.	• Power sharing

The main question addressed in this thesis is how to coordinate and balance the real power generated from DG sources in individual phases, forming single-phase residential microgrids, in a distribution network.

Based on the state of the art, currently there are no benchmark distribution net-

work models that can allow researchers to perform simulations for residential microgrids. Hence, the first step is to introduce a benchmark system that is a reflection of a typical North American distribution network. This is introduced in Chapter 3. Furthermore, this model will allow to introduce residential microgrids in the system to perform various phase balancing techniques that are introduced in Chapters 5 and 6.

It is also pertinent to mention that a mathematical analysis for balancing single-phase residential microgrids needs to be performed. This will involve deriving steady state equations for the system and then compare them with the simulation results. From the literature survey it is found that such an analytical formulation of the problem has not been performed before.

Coordination of DG sources for single-phase residential microgrids also requires improved control strategies that were previously proposed in the literature and discussed in section 1.3.9. Since, the idea presented in this thesis relates to balancing phases in terms of real power flow, the introduction of back-to-back converters between the phases is seen as one of the solutions. Hence, the main idea now revolves around not only coordinating individual DG sources in a phase but also controlling the power flow between phases through the back-to-back converter. The solution to these two problems have been introduced in Chapters 5 and 6.

Although, the back-to-back converters between phases can resolve the issue of phase balancing, it is also necessary to operate this system of single-phase residential microgrids in an optimal manner. Therefore, it is also necessary to device an operational control strategy, which can allow this. This will involve selecting an appropriate power surplus phase(s) to contribute towards power sharing with the deficit phase. In a scenario, where all phases are in power deficit, appropriate action is taken to import power from the grid as well. The solution to this problem is introduced in Chapter 7.

Finally, the problem of inter-phase power management needs to be validated through experimental validation, as performed in Chapter 8, that can prove the validity of different

concepts introduced in Chapters 6 and 7.

1.5 Research Objectives and Scope

Following up from the discussion in sections 1.3.8-1.3.9, the proposed research will address the following issues concerning,

- Coordination of islanded single-phase residential microgrids is the main objective of this work. Within a phase, this will deal with coordinating individual DG units in the same phase through various control structures. This will primarily include the contribution from the primary and secondary control layer.
- In the scenario with limited battery back-up reserve and low PV generations, strategy for conserving battery energy and coordination with other DG sources in a community will be studied.
- For the condition, where a phase is deficit in power, the coordination of single or multiple residential microgrids through back-to-back converters will be investigated.
- Adequate control of back-to-back converter to deliver real power to the deficit phase is necessary and will be discussed in detail.
- An operational control strategy is required to select an appropriate phase for power sharing between phases. This will be developed also, which will allow optimal phase selection during power transfer.
- Experimental validation for power between the surplus phase and the power deficient phase will be highlighted to validate the concepts from the previous objectives listed in this section.

1.6 Contributions

A list of contributions from this work are summarized below,

- This study provides an extensive control architecture for residential microgrids to re-

duce the phase imbalance created with the introduction of renewable energy sources like PV and battery at the distribution network's level.

- A benchmark distribution network model has been developed that can be used to study the control and stability of single-phase residential microgrids.
- For the residential microgrids, control strategies are developed to control and coordinate DGs within a phase using the proposed modified vector control and the improved multi-segment droop control schemes. The overall control of DG units through these strategies has been given the name of 'intra-phase power management strategy'.
- The coordination of single or multiple phases through back-to-back converter has been developed in this work. The back-to-back converter allows the real power to flow from the power surplus phase to the power deficient phase, under controlled scenarios as formulated for improved multi-segment droop control strategy. This controlled power flow between phases to mitigate phase imbalance in distribution networks has been given the name of 'inter-phase power management strategy'. This is first time that such strategies are proposed.
- Strategy for optimal selection of power surplus phase(s) during inter-phase power management has been developed. This has greatly improved the power availability of these single-phase residential microgrids.
- A laboratory-scale back-to-back converter is developed to successfully test and validate the proposed inter-phase power management strategy.

1.7 Thesis Organization

The thesis is organized into the following chapters:

Chapter 2 deals with an overview of distribution systems and the various architectures used in the implementation of distribution networks. The details of distribution transformers and service entrance are added to fully understand the present day lay-

out of a typical North American distribution network from the utility to customers. A literature review on balancing three-phase systems, especially with high proliferation of roof-top PVs and storage devices (including electric vehicles), is later provided to identify the previously used techniques for balancing three-phase systems and how the proposed work provides another dimension towards balancing three-phase systems.

In Chapter 3, a benchmark distribution system is developed for investigating control and energy management of distributed generation (DG) at a residential level in the form of three single-phase microgrids. The benchmark is derived from a typical distribution network architecture with common parameters found in North-America systems including wiring specifications, line impedances and connection details for rooftop PV systems. This benchmark system can accommodate microgrids operating in both grid-connected and islanded modes. Within this benchmark, multiple single-phase DG sources located in different phases can be coordinated to form a dynamically balanced three phase system under different load and generation profiles in different phases.

While different techniques have been investigated to resolve the imbalance situations in distributed networks, there is lack of adequate theoretical foundation to support such works.

Chapter 4 provides a detailed analysis for a typical residential community with phase-wise generation, storage, and large-size random loads. The analysis has laid mathematical foundations for a class of such situations and provides essential theoretical basis for different techniques for re-balancing among three-phases with options for incorporating different energy management strategies. To simplify the adoption process of this important result, detailed mathematical formulations have been developed to provide explicit links among the net power required for transfer from power surplus phases to power deficient ones to achieve an overall dynamic balance among all three phases. Furthermore, an easy to use on-line training site has been developed for potential users to assess their own application scenarios. Six representative case studies have also been included for

illustration purposes.

In Chapter 5, the modeling, design and simulation results of a power control and management strategy for islanded residential microgrids is presented; termed as 'intra-phase power management'. The proposed intra-phase power control and management system uses a modified vector control with a multi-segment (P/f) droop strategy. To demonstrate the effectiveness of the strategy, a detailed three-phase residential microgrid model is developed in PSCAD/EMTDC environment, including switching models of the back-to-back converters. The results have shown that the proposed strategies can effectively maintain desired voltage and frequency profiles, and power balance in each phase can be effectively managed for stable operation.

The power management strategy developed in Chapter 5 does not completely address the issue of power balancing in residential microgrids. In the case where such a balance cannot be maintained locally within a phase, Chapter 6 introduces a secondary control strategy; termed as 'inter-phase power management strategy' using a back-to-back converter between phases. The modeling, design and simulation results using PSCAD/EMTDC are presented in this chapter.

An operational control strategy for residential microgrids in islanded/grid connected single-phase residential microgrids is presented in Chapter 7. It makes use of the control strategies developed in Chapters 5 and 6. Each phase utilizes its local energy balance control system, which communicates its status of generation, SOC of battery and load demand with a community energy balance control system, using low bandwidth communication link. For the scenario, in which the available power generation in a particular phase is unable to support the loads, the developed control strategy enables the power exchange between phases, which is based on the decision made by the community energy balance control system. This is carried out through the control of interconnecting single-phase back-to-back converters. Detailed switching model for the residential microgrid is developed in PSCAD/EMTDC platform and the proposed control strategy is validated.

Chapter 8 includes the validation of the proposed work through laboratory-scale experimental setups. The design stage of the back-to-back converter is explained followed up with details of other hardware including voltage and current sensors and the microcontroller. The software control module is developed in MATLAB/Simulink with a communication protocol for sensing appropriate system signals. The experimental setup is used to validate the proposed modified vector control strategy and the inter-phase power management strategy.

The conclusions and future work constitute Chapter 9, followed by bibliography and appendices.

Chapter 2

Distribution Systems; An Overview

An introduction to residential microgrids was presented in Chapter 1, with emphasis that such a system is formed at the distribution side of the power network. To this end, it is important to familiarize with the basic concepts of distribution systems. Therefore, this chapter introduces the concepts, design details, circuit layouts and standards that are followed in a typical North American distribution network.

The distribution system comes under the category of 'sub-transmission systems' which delivers power from large transmission substations to the customers. In general, a distribution network consists of (a) Sub-transmission system, (b) Substation, (c) Primary feeders, (d) Transformers, (e) Secondary circuits and (f) Service drops. The details of these sub-components are described next.

2.1 Sub-Transmission

The sub-transmission section of a distribution network delivers power from bulk power sources. The circuits may consist of overhead or underground cables. The voltage levels of these circuits varies from 12.47 to 245 kV. The design of these distribution systems vary from simple radial systems to a more complex networked designs. The design selection or a combination of system designs depend upon the need of the manufacturing process.

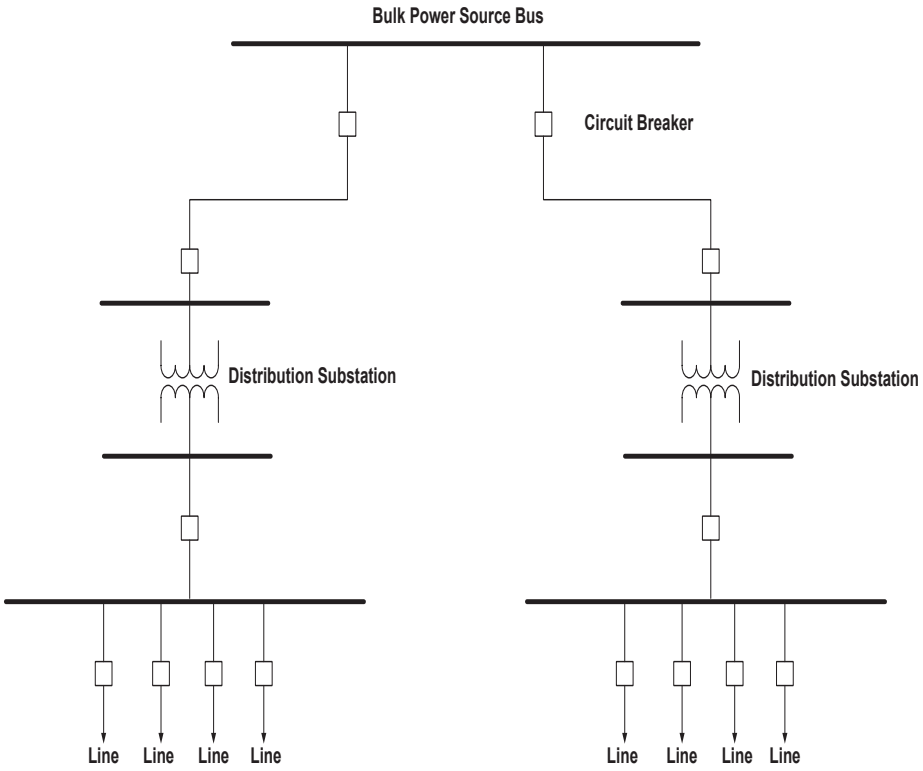


Figure 2.1: A simple radial system.

In general, the system cost increases with system reliability, if the component quality is equal. In particular there are four main types of distribution system designs and they are named as follows,

- Radial
- Improved radial
- Loop type system
- Network type system

2.1.1 Radial and improved radial sub-transmission

In a radial system, as the name suggests, the circuits radiate from the bulk power stations to the distribution substations. The radial system is simple and has a low initial cost. A radial system is shown in Fig.2.1. An improved radial system, on the other hand, allows for relatively faster service restoration when a fault occurs on one of the distribution

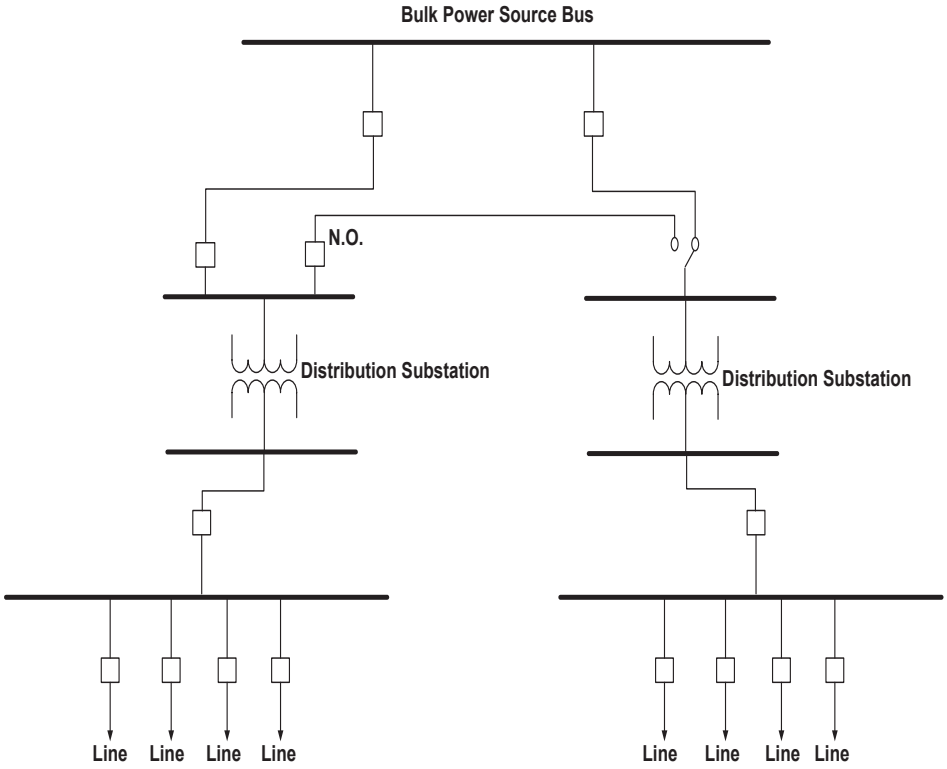


Figure 2.2: An improved radial system.

circuits. This is shown in Fig.2.2.

2.1.2 Loop type system

For greater service reliability, the distribution system is designed as loop circuits or multiple circuits. A loop type distribution system is shown in Fig.2.3. In this design, a single circuit originating from a bulk power bus runs through a number of substations and returns to the same bus.

2.1.3 Network type system

The network type system has multiple circuits as shown in Fig.2.4. The distribution substations are interconnected and the design may have more than one bulk power source. Even though it is highly reliable, it requires costly control of power flow and relaying.

Hence, the primary feeder design will be governed by IEEE standards for distribution

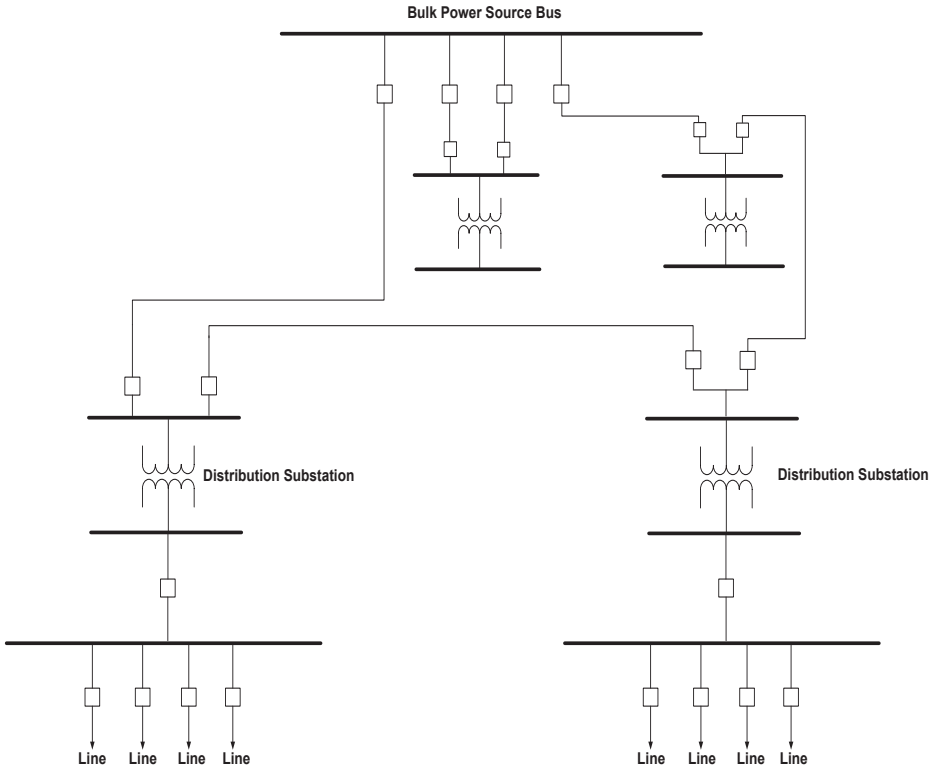


Figure 2.3: A loop type distribution system.

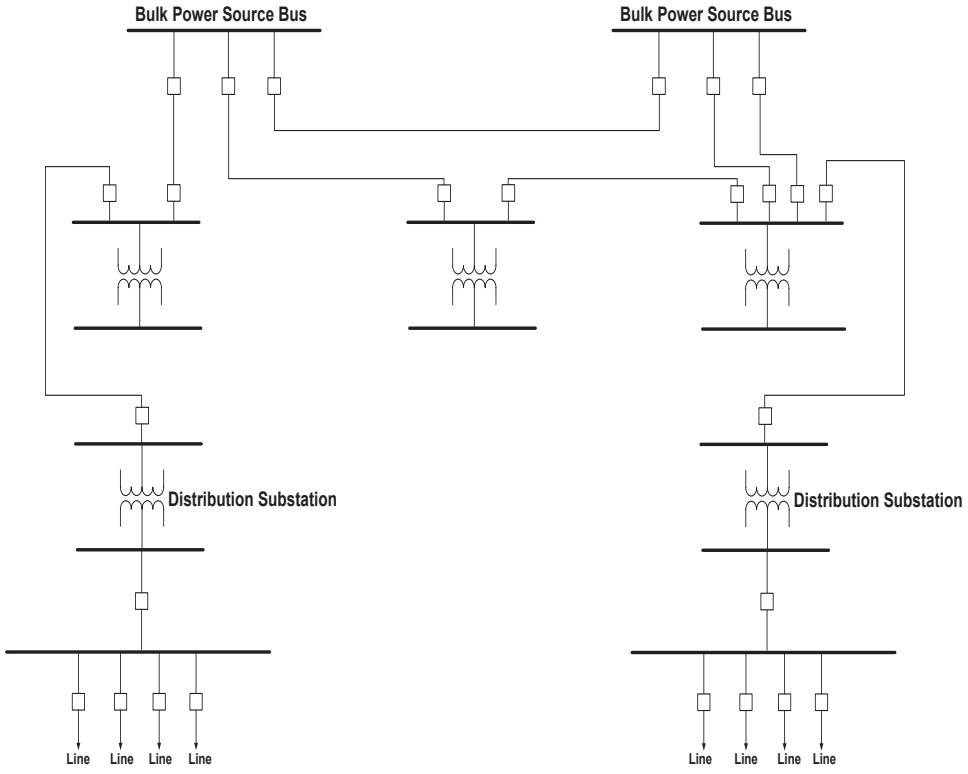


Figure 2.4: A network type distribution system.

Table 2.1: Economical load reach distances for overhead 3-phase lines

Primary Voltage(kV)	Economic Reach (miles)
4.2	1.3
12.5	3.6
13.8	4.0
24.9	7.1
34.5	9.7

systems, where the length of the feeder will depend upon primary voltage. For various voltages of feeders, the respective economic reach is tabulated in Table 2.1. The design will also vary on the geographical location where a particular feeder has to serve a load center [88]. The feeder construction can be overhead or underground and its rating will also be determined by the load density.

For accurate model of the primary feeder, the type of conductor to be used is also important as this will contribute to the X/R ratio of the distribution system. According to IEEE red book on Distribution Systems, if a 600 A feeder rating is used, the R and X values in $m\Omega$/100ft for aluminium and copper conductors is tabulated in Table 2.2 [11].

In North America, the local distribution company (LDC) provides information on the ratings of primary feeders, average length of primary feeder, average number of feeders per substation and the topology followed at the distribution level. This information is tabulated in Table 2.3 for BC Hydro, as an example [89].

2.2 Distribution Transformers

A typical transformer consists of two or more coils interlinked through an iron core. The iron core is used to confine the magnetic flux and to link the coils together. Mathemati-

Table 2.2: IEEE conductor standards

Resistance	**Al**		**Cu**	
	R	**X**	**R**	**X**
mΩ/100ft	2.56	0.99	2.28	1.68
mΩ/ft	0.0256	9.9e-3	0.0228	0.0168
mΩ/km	83.98	32.48	74.8	55

Table 2.3: Information regarding a section of distribution system from BC Hydro

Ratings of Primary Feeder	Average Length of Primary Feeder	Total # of Substations	Total # of Feeders	Average # of Feeders	Distribution Topology
12.5-22 kV	38.5	234	1482	6.3	Radial

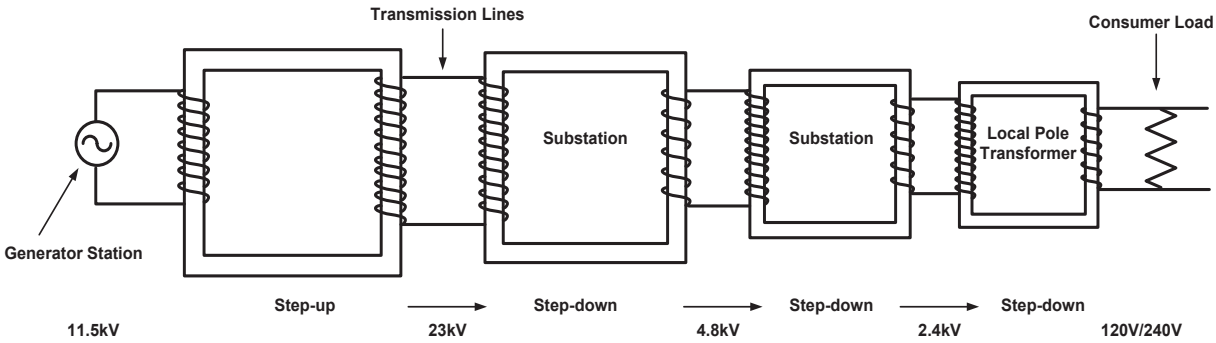


Figure 2.5: A chain of transformers linking the generator station to the customer.

cally, the primary voltages and currents are related to the number of turns on both coils using,

$$\frac{V_P}{V_S} = \frac{N_P}{N_S} \tag{2.1}$$

and

$$\frac{I_P}{I_S} = \frac{N_S}{N_P} \tag{2.2}$$

where, V_P and V_S are the primary and secondary voltages, I_P and I_S are the primary and secondary currents while N_P and N_S are the number of turns on the primary and secondary coils.

The power delivered to the end customer is routed through a number of transformers as shown in Fig.2.5. The last distribution transformer is near the service drop out which can either be a residential or commercial building as shown in Fig.2.6. A particular distribution transformer is designed with service ratings as tabulated in Table 2.4.

Table 2.4: Design specifications of transformers

No. of Wires	Phase	Voltage	Comments
2	Single	120	These installations are no longer made
3	Single	120/240	Most common residential service
4	Three	120/208	
4	Three	120/240	

2.2.1 Three wire-single-phase systems

A *phase* refers to the angle between AC voltage and current. For example in a three-phase system, each of the voltages generated are out of phase by 120°. Single-phase and three-phase systems are abbreviated as 1ϕ and 3ϕ respectively. For residential electrification, three wire-single phase system is usually used. In this system, there are two ungrounded and one grounded conductors as shown in Fig.2.7. One of the ungrounded conductor is usually black and the other is red. The grounded conductor uses the yellow color code. The purpose of using two ungrounded conductors and one grounded conductor, provides the $120V$ and $240V$ voltage rating at the secondary of distribution transformer. The use of these two voltage ratings will depend upon how the branch circuit is connected within the distribution panel.

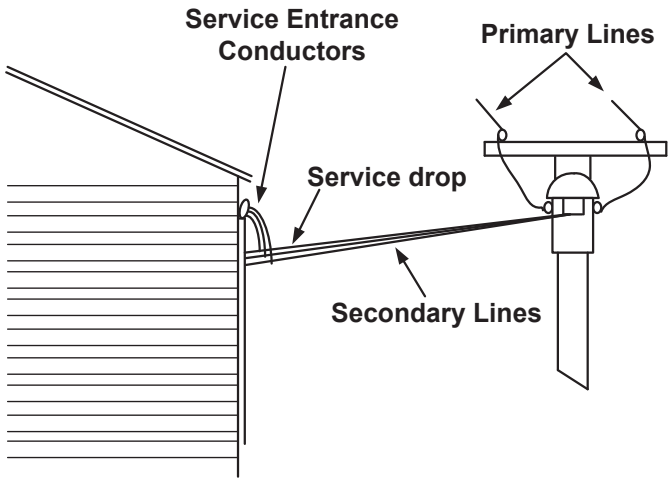


Figure 2.6: Step down transformer with overhead conductors providing the last link to the customer's service wires at the service point.

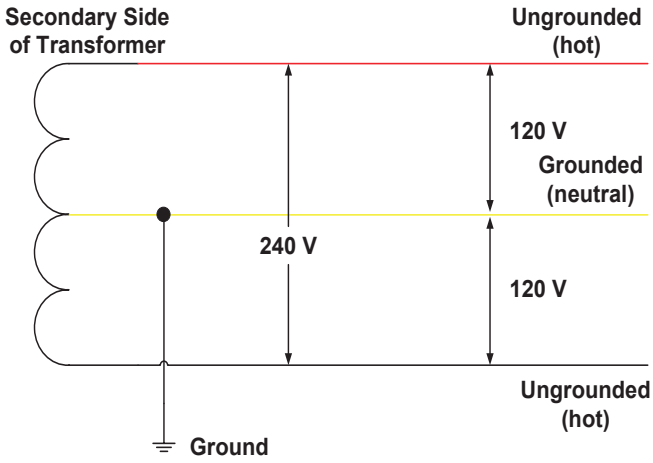


Figure 2.7: A three wire-single-phase system with two ungrounded conductors and a grounded conductor.

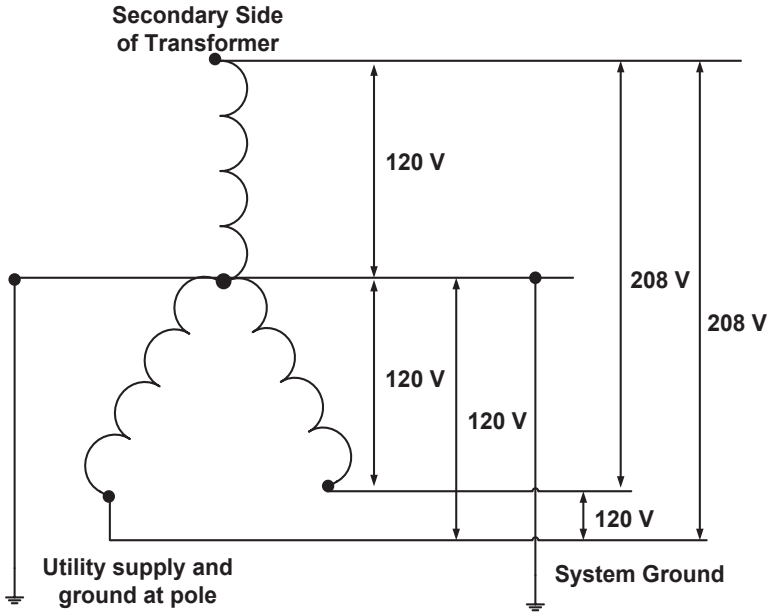


Figure 2.8: A wye-connected four-wire-three-phase system providing $120V/208V$.

2.2.2 Multi-phase systems

There may be situations where a homeowner requests a system with more than one phase. This is a multi-phase system that is usually installed to power heavy-duty or special equipment such as a milling machine or a lathe. There are two main types of multi-phase systems that are used. They are wye-four-wire-three-phase systems and delta-four-wire-three-phase systems.

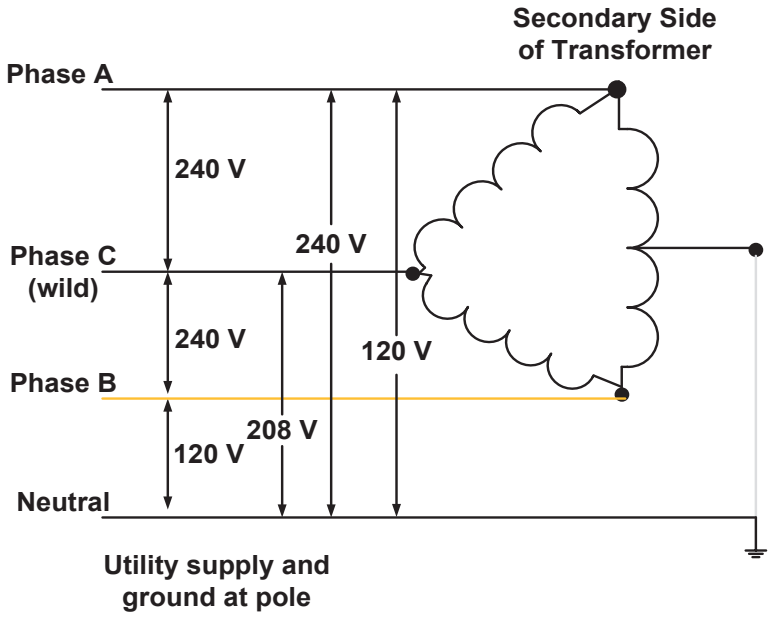


Figure 2.9: A delta-connected four-wire-three-phase system providing $120V/208V/240V$.

2.2.3 Wye-four-wire-three-phase systems

A wye-connected four-wire three-phase, $120/208V$, arrangement is shown in Fig.2.8. Such a system can supply both single-phase $120V$ circuits and three-phase $208V$ circuits. In this type of panel, there are three hot bus bars. Each has $120V$ to ground when connected to the neutral. For $120V$ circuits, the circuit breaker connections are the same as in three-wire single-phase services.

The black (hot) circuit wire goes to the circuit breaker terminal and the white neutral circuit wire is connected to the neutral bus bar. As with single-phase systems, the $120V$ circuits should be balanced or equally arranged among the three hot buses. Two-pole circuit breakers are also installed in the same manner as with three-wire, single-phase service panels. That is, the double-pole breaker is attached to any two of the three hot bus bars.

2.2.4 Delta-four-wire-three-phase systems

Another service alternative is the delta-connected four-wire three-phase, $120/240V$ system. A schematic for this type is illustrated in Fig.2.9. It can provide $120V$ single-phase

$240V$ single-phase and $240V$ three-phase power. The panel connections are made as follows [90]:

- For $120V$ single-phase circuits, one circuit wire (white) is connected to the neutral and the other (black) to an ordinary single-pole breaker attached to phase A or C only. The breaker must not be attached to phase B for this type of circuit since this would provide $208V$. Equipment designed for $120V$ operation would be ruined in this case. The phase B wire of this system is often called "high leg" or "wild leg" and must be identified as such at all accessible points with an orange-colored indicator. At the panel, wire B is connected to the center bus bar.
- To derive power at $240V$ single-phase, both circuit wires need to be connected to a double-pole circuit breaker attached to any two phases. Neutral wire is not included in this circuit.
- For $240V$ three-phase circuits, three wires are connected to a three-pole breaker attached to all three phases.

2.3 Local Distribution Transformer to Customers

As discussed previously, the topology from bulk power sources to a distribution network can vary from a simple radial system to more complex network configurations, the primary feeders still serve a locality or a geographical area from the local substation. The primary feeder can branch out into several circuits or laterals. These laterals can be in single-phase form and sub-laterals may be tapped out subsequently, if necessary. These laterals can be located in residential or rural areas, and normally consist of a single-phase conductor and a neutral. Larger loads, such as those of schools, community centers, local industrial sites may be served by either dedicated underground or overhead primary feeders. They are mainly in three-phase.

Each phase in the primary feeder serves a group of residential units. A split single-

Table 2.5: Rating and percentage impedance of distribution transformers

Secondary Unit Substation Transformers (V)	kV Rating	Percent Impedance Voltage
2400-13800	112.4-224	Not less than 2.0
2400-13800	300-500	Not less than 4.5
2400-13800	750-2500	6.75
22900	All	6.75
34400	All	6.75

phase pole transformer is often used to step down the voltage even further to meet the voltage level for residential, commercial and industrial users. The split phase transformers are available in both 120 V and 240 V with a common neutral to customers as shown in Fig.2.7. The local transformer steps down the feeder voltage from 13.8 kV to 120 V/240 V [88]. The ratings and percentage impedance of distribution transformers is tabulated in Table 2.5 [11].

2.4 Service Entrance

The term service entrance refers to all equipment, wires and metering devices that are required to carry power from the utility's pole or underground transformer to the customer. The purpose of service entrance equipment is to protect, meter and distribute power to the local branch circuits in the building or residential unit.

The cables brought to a commercial building or residential site for the nearby transformer can be either overhead connections or underground. The overhead connections are called service drops (as shown in Fig.2.10) while the underground ones are called service laterals (as shown in Fig.2.11).

Typically, a building or residential unit will have a single service drop or lateral. There may be exceptions to this rule given the following circumstances,

- A secondary service may be connected in a building in order to supply power to emergency equipment like that in hospitals, fire stations or to commercial and public sites, which may be considered as critical loads for the local utility. An example of this is

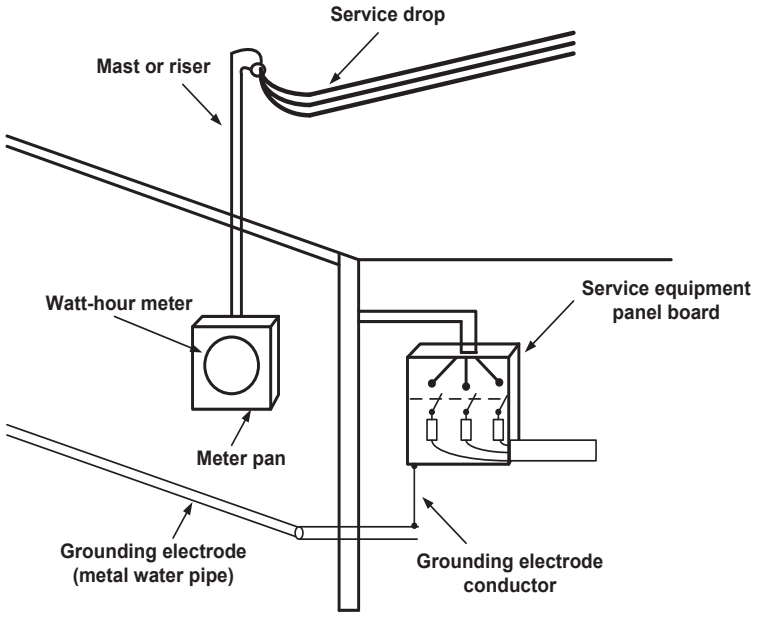


Figure 2.10: An overhead service drop with other equipment as seen at a typical residential site.

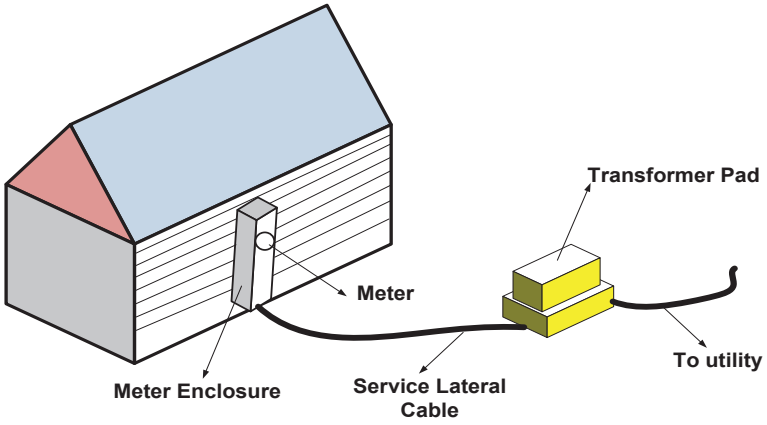


Figure 2.11: An underground installation for a service entrance.

shown in Fig.2.12.

- If a significantly large load in a community cannot be supported by a single service, a secondary supply may be provided for this unexpected load.
- Electrical power provided by other renewable sources like solar, wind or small generators, may share part of the load with the grid in a building or residential site.

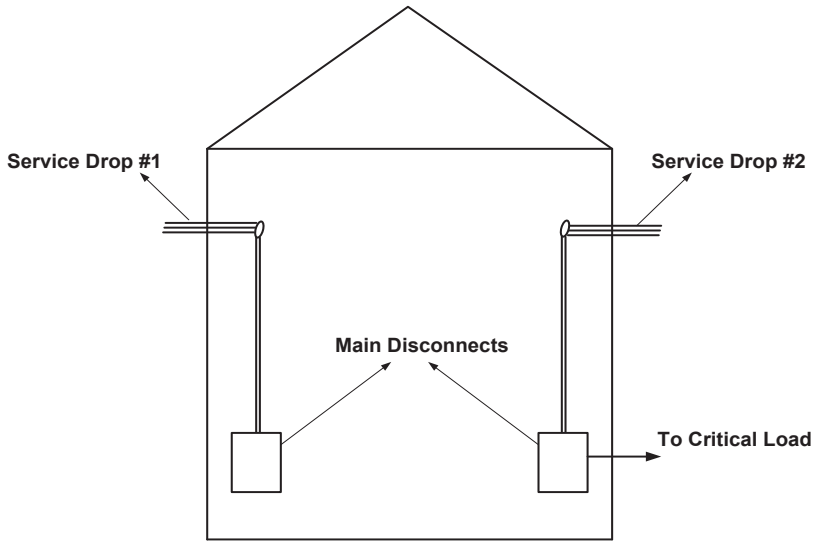


Figure 2.12: A separate service drop is provided to the critical loads.

2.5 Service Entrance Conductors

The service entrance conductors are typically run through a conduit or cable assembly. In a conduit type architecture, all the conductors are insulated. The cable assembly is similar except for the fact that neutral wire is bare. The different types of entrance conductor assemblies depend upon a number of reasons which include, customer preference, site's structure and local utility's codes and specifications. An example of service entrance cable is shown in Fig.2.13.

Typically, the conductors that are used for residential areas with their capacities and cable resistances are tabulated in Table 2.6 [11].

Table 2.6: Cables with their ampacity and resistance used in residential circuits

AWG Cables	Current Ratings (A)	Resistance (Ω/m)
#14	15	0.00829
#12	20	0.00521
#10	30	0.00838
#8	40	0.00206
#6	55	0.00138

In order to simulate a real-life scenario of a residential microgrid, a radial type system is used because of its simple implementation. Complex relaying as used in loop type and

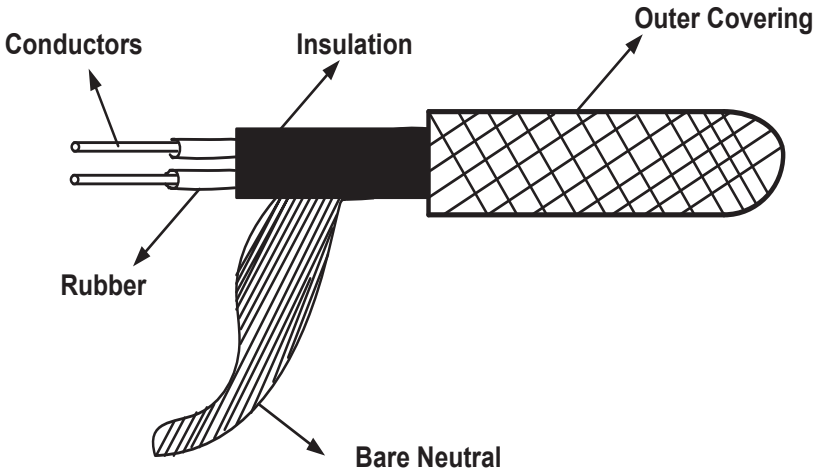


Figure 2.13: Service entrance cable with bare stranded neutral.

network type distribution systems becomes out of scope for this work. The data listed in this section is used in Chapter 3 to model a section of a distribution system, which is a close approximation of the existing systems in North America.

2.6 Reasons for Phase Unbalance in Distribution Systems

The nature of distribution networks in North America is that MV main feeders are the main back bone of the system, from which single-phase laterals are tapped to customers. Phase unbalance is deeply widespread in North American systems and is one of the main causes of failures for single-phase transformers as well as overheating of induction motors for industrial plants. It is pertinent to mention here the reasons why phases unbalance occurs in the system. Some of the main reasons include:

1. There is an inherent structural asymmetry, when single-phase laterals are tapped from 3-phase LV mains. This results in the presence of self and mutual inductances, which lead to causing phase unbalance in terms of voltages and currents for each phase [91, 92].

2. The second reason behind phase unbalance is the erratic load behavior of customers. The unbalance in the system is aggravated due to the presence of local generation and storage, say roof-top PV systems with lead acid batteries. Those customers that do possess such systems have an entirely different load profile as compared to those that do not. This means that within a phase itself there can be high phase unbalance in terms of generation and storage. With the emergence of electric vehicles (EVs), the already stressed distribution networks have now become even more unbalanced. The irregular charging cycles for these EVs results in further imbalance of the system.

3. Another cause of phase unbalance is the irregular distribution of customers on the 3-phase LV feeder. This comes down to the inadequate planning of the distribution network. When new customers are allocated a phase, they may be assigned a random single-phase connection. This randomness in phase allocation also results in undue phase unbalance, which is avoidable with proper planning [93, 94].

2.7 Results of Phase Unbalance in Distribution Systems

An unbalanced network can have far-reaching impact on the distribution company as well as the customers. Some of these consequences are listed below:

1. Under utilization of the feeder's capacity is one of the consequences of phase unbalance. For a typical 3-phase LV feeder, if the capacity of heavily loaded single-phase lateral is completely utilized, the capacity of other phases cannot be shifted to this heavily loaded phase. Ultimately, the equipment and cables will need to be redesigned according to the load profile of the heavily loaded phase. This will incur additional cost on top of maintenance of this distribution network [95–97].

2. Another major concern from an unbalanced system is the energy losses that occur in the neutral wire. Ideally, under balanced conditions, the neutral wire should not carry any current. Under unbalanced conditions the neutral wire is the carrier of negative sequence current caused by the imbalance of one or more phases. The additional energy losses occur at both the distribution feeder and transformer [98–100].

3. Irregular load shedding is one of the results of phase unbalance in the system. The negative sequence current in the neutral wire can cause tripping of the protection devices at the substation, resulting in taking the primary feeder off the network [97].

4. For the 3-phase loads in the distribution network, e.g. motor loads, the negative sequence current causes overheating, energy losses and some times failures for these motors. This premature failure of these loads results in additional cost for the customers [101, 102].

2.8 Solutions to Phase Unbalance

Some of the solutions available for an unbalanced systems in the literature revolve around allocating a different phase to the loads, which can be performed both online and offline. A dynamic re-phasing strategy is developed in [103]. At a certain time of the day when the unbalance in the system crosses a certain threshold, the loads are allocated a different phase through re-phasing switches. Heuristic techniques have been used in [95, 104–107] to solve the problem of phase unbalance. In [104,105], genetic algorithm is used, whereby an optimal solution for the unbalanced condition is solved using the information of phase connection of the local distribution transformer to the primary feeder. In [106, 107], expert systems have been developed to minimize the number of re-phasing iterations and reducing the negative sequence current in the neutral wire. The problem of reducing the cost of re-phasing is solved in [95] by using simulated annealing. Although, these

solutions may be easily implemented and are cost effective, they do suffer from reliability issues. This is because all these heuristic techniques are dependent on the training data that has been used. Once trained, the algorithm will basically work like a black box. The output variables may not be optimal from these algorithms for a different operating point.

Other solutions proposed for an unbalanced system include the use of power electronic converters, typically known as phase balancers [108–111]. The use of a static balancer is introduced in [108], to mitigate the effects of phase unbalance. This makes use of a star connected autotransformer to achieve the desired objective. A power factor correction based converter is used in [109]. The control strategy therein uses current sharing method to minimize the unbalance in the system. Another solution is to incorporate a static var compensator (SVC) in the system as proposed in [110]. A SVC connected to an unbalanced system will absorb the reactive power caused by the negative sequence current to balance the system. On similar grounds distributed static synchronous compensators (DSTATCOMs) can also be used as proposed in [111]. The use of phase balancers and other FACTs devices at the distribution network's level will incur a large capital and maintenance cost. They are therefore categorized as more academic rather than practical solutions to the problem. Furthermore, the efficiencies of these systems is less than 95% because of the switching losses in power electronic converters. Also, the reliability of phase balancers is not guaranteed. If a series connected balancer is tripped, it will cause an outage of all the customers in that particular phase, which is undesirable.

Other works include the use of energy storage to re-balance the system in a microgrid based scenario [112–114]. In [112], a control strategy is developed to make use of the battery to balance a phase in a 3-phase system under varying loading conditions. A similar control strategy with single-phase PV system is introduced in [113]. A reactive power support through single-phase PV systems is developed in [114]. This use of storage systems to balance a microgrid at the LV side of the distribution network, can balance a

single phase. The problem arises when multiple phases are unbalanced and each phase is equipped with PV and battery based systems. In that case, the coordination and control of these DG units becomes imperative and a control strategy needs to be developed where individual phases can participate to balance the system. Also, to the best knowledge of the author, there are no benchmark systems that can be used for research purposes when it comes to phase balancing in microgrids. Furthermore, the operation and maintenance cost still remain a hurdle in using such systems for phase balancing.

2.9 Summary

In this chapter, an overview of distribution systems has been presented with emphasis on the various system architectures and design details which are typically followed in a North American network. The details of the service entrance cables is later explained. Towards the end, the reasons for phase unbalance in distribution systems is stressed upon, followed up by the results for such a system. The previous works in solving the problem of imbalance in the system are summarized with their limitations. It is concluded that there is a need for a benchmark system that can be used to study microgrids in general and residential microgrids in particular for research purposes. Furthermore, there is a need to develop an efficient control strategy that can be used to balance phase(s), without the use of heuristic techniques and flexible AC transmission systems (FACTs) based power electronics converters that have a large footprint. The material presented in this chapter is a stepping stone of simulating a typical distribution network and a residential microgrid in PSCAD/EMTDC.

Chapter 3

A Benchmark Distribution System Model for Residential Microgrids

This chapter introduces a benchmark distribution system developed for investigating control and energy management of distributed generation (DG) at a residential level in the form of three single-phase microgrids. The benchmark is derived from a typical distribution network architecture with common parameters found in North-America systems including wiring specifications, line impedances and connection details for rooftop PV systems, as given in Chapter 2. This benchmark system can accommodate microgrids operating in both grid-connected and islanded modes. Within this benchmark, multiple single-phase DG sources located in different phases can be coordinated to form a dynamically balanced three-phase system under different load and generation profiles in different phases. It is expected that this benchmark system will facilitate investigation of impacts posed by proliferation of single-phase distributed generation devices and local storage systems in private residences. Case studies have been carried out to demonstrate the versatility and effectiveness of this benchmark system.

3.1 Introduction

Even though distribution system is a well-studied field, most are focusing on steady state analysis and network reconfiguration in a multi-bus environment [115–117]. Since distributed generation is dynamic in nature, power management and control studies have to deal with transient behaviors of the system at this low voltage (LV) residential environment. Local rooftop PV systems and battery storages can be connected to form as a residential microgrid connecting to a primary feeder on a single phase. In this respect, a generic configuration, which can accommodate a residential microgrid, is not only important, but also necessary for various studies in distribution networks.

Even though many microgrids have been developed to work at distribution level in the literature, many cannot be directly used for residential applications. A distribution network is introduced in [118] to study an adaptive critic-based approach for grid connected microgrids. It consists of a single point of common coupling (PCC) with multiple 3-phase feeders from a local substation. The microgrid has several DG units with 3-phase loads aggregated as secondary feeder loads. With the provision of local generation at the customer end, the need to accommodate details of local distribution transformer and customer loads becomes an integral part of the system model. Furthermore, the distribution network used for the study, can only be used for coordinating DG units in a three-phase microgrid environment without having additional features of coordinating these units for single-phase residential microgrids.

In other studies, microgrids are connected directly to a grid without due consideration of transformer interface at substations, nor reactance associated with feeders [119–121]. For example, transitions of a three-phase microgrid from an islanded to a grid-connected modes have been investigated in [119] with focus on synchronization procedures. The associated distribution system has been simplified to a direct connection to the grid at the PCC. Furthermore, only aggregated constant resistive loads are considered.

The microgrid considered in [120] consists of three power electronics-interfaced DG

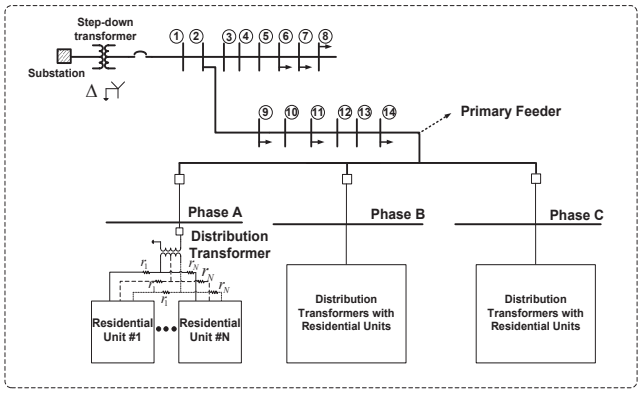


Figure 3.1: A simple radial distribution system with residential units.

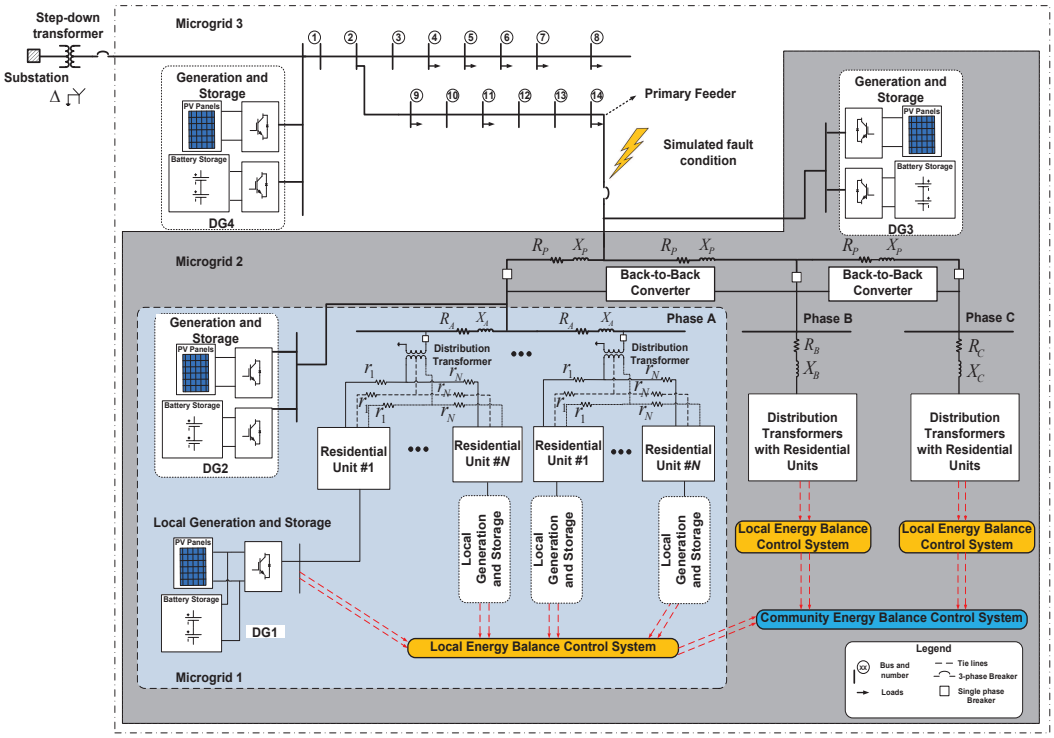


Figure 3.2: A radial distribution system with possible structures for residential microgrids.

units connected to an IEEE 5-bus system. The IEEE x-bus standards (where $x < 13$) are typically used, where key features of a LV distribution networks are omitted for simplicity. As a result, this model is not detailed enough to meet the needs in residential microgrid studies, where the central point is coordination of multiple DG units using different power management strategies at a customer level.

The microgrid explored in [121] is composed of a multi-bus system with renewable energy sources connected to individual buses. The system architecture considers aggre-

gated loads at the feeders and interconnection among the studied microgrid, the utility network, and at individual buses serving local loads without considering transformers or other interfacing devices. Furthermore, the renewable energy sources are assumed to operate as centralized units on a bus, rather than being distributed as in realistic residential microgrids. Hence, this architecture does not represent a realistic distribution system in residential microgrids with generation sources and storage devices located at different phases.

Residential microgrids have been investigated in [122–124]. A laboratory-scaled single-phase radial microgrid is considered in [122] with generators and loads connected to local nodes. The architecture is more suited for three-phase microgrids with small micro-turbines as DG sources that serve a residential community. No coordination among DG sources has been considered in the study. Furthermore, some of the losses in key system components, such as distribution transformers, are not taken into account. This network architecture would not provide an effective framework for residential microgrid related studies.

A hybrid PV/battery system for a single household is examined in [123]. A PV/battery system and local loads are connected to a household distribution panel only. However, the distribution system topology, primary feeder and transformers have not been considered neither the potential coordination with DG units nearby, such as devices from the next door neighbor on the same local distribution network.

An energy management strategy has been considered for a grid-connected residential microgrid in [124]. The system consists of multiple DG sources connected to a three-phase network at the PCC. The local and central energy management systems allow for coordination of local generation and storage in residential units to achieve a state-of-charge (SOC) equalization. This avoids prolonged load shedding for some customers under an islanded condition with insufficient supply. For this coordination strategy to work, the customers need to be on the same phase as the primary feeder. In a residential

microgrid, different customers can be fed from different phases on a same primary feeder. Consequently, such system architecture and associated control strategies are not suitable for realistic situations in a distribution system.

An islanded hybrid single- and three-phase microgrid has been considered in [78]. This single-phase microgrid has DG units with local loads on two of the phases while the other phase is dedicated to loads only. Only single phase loads have been considered. Despite of this unique feature, this architecture cannot be adopted where single phase sources and loads are located in all three phases. Furthermore, the control objectives are based on unidirectional power flow between phases, they are not suited for power sharing studies in residential microgrids among different phases, where the power flow among phases can be bi-directional. The actual direction and the amount of power transfer depend on the availability of surplus power and power mismatch among phases.

To investigate control and power management issues for single- and three-phase microgrids with individual DG sources, storage devices, and loads in different phases at a distribution level, it is imperative to develop a benchmark model with versatile, yet flexible architectures. Since structure and parameters of distribution systems are country and region dependent, the current work will focus on those commonly found in North America.

The developed benchmark model is flexible enough to simulate a section of a distribution system by considering details of feeder reactance, different transformer configurations and wiring conventions of residential loads including roof-top PV systems and battery storage devices in the laterals of a primary feeder. This feeder can also supply power to common three-phase loads; say, a school, or a local community center. As compared to those in the literature, the current benchmark model provides a more realistic environment. In an islanded operating mode, the system has the capability of exchanging power among phases through a power management unit based on a back-to-back converter configuration, which is discussed in more detail in Chapters 4 and 6.

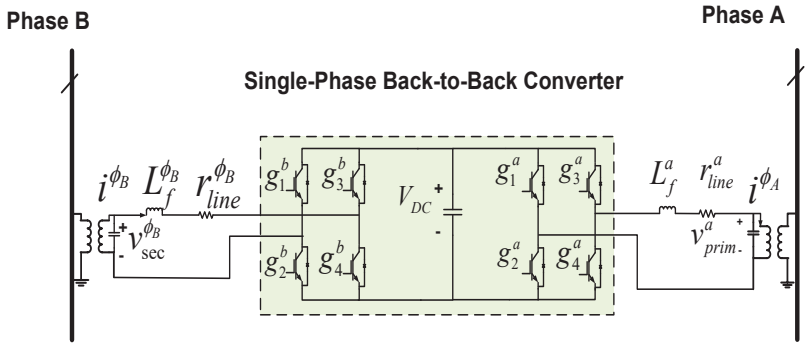


Figure 3.3: Structure of the back-to-back converter

3.2 Distribution Networks in North America

A simple radial distribution system from the local substation to customers with residential loads is illustrated in Fig.3.1 while the same network with DG units is shown in Fig.3.2. In Fig.3.2, the PV and storage units are located at roof-tops of houses. These units can also be either central to the phase, primary feeder or to the distribution network. The back-to-back converters interconnect the three phases through isolation transformers. The structure of the back-to-back converter is shown in Fig.3.3. The key features of a distribution network are discussed in this section. For the sake of simplicity, residential loads connected to bus#14 only are shown here.

3.2.1 Local substation To local distribution transformer

Even though the topology from bulk power sources to a distribution network can vary from a simple radial system to more complex network configurations, the primary feeders still serve a locality or a geographical area from the local substation. As shown in Fig.3.1 the primary feeder can branch out into several circuits or laterals. These laterals can be in single-phase form and sub-laterals may be tapped out subsequently, if necessary. These laterals can be located in residential or rural areas, and normally consist of a single-phase conductor and a neutral. Larger loads, such as those of schools, community centres, local industrial sites may be served by either dedicated underground or overhead primary feeders. They are mainly in three-phase.

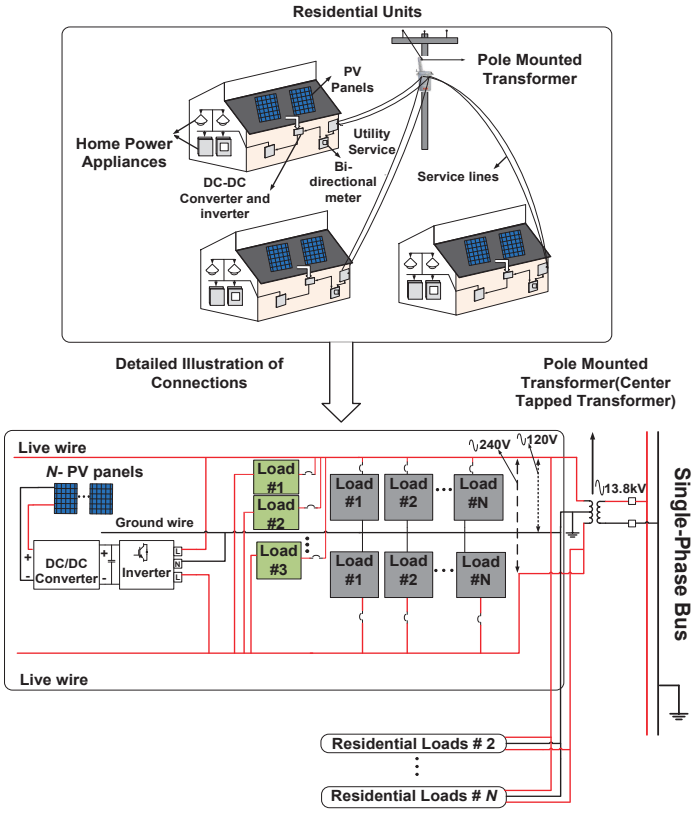


Figure 3.4: A per-phase diagram from distribution transformer to customers

3.2.2 Local distribution transformer to customers

Each phase in the primary feeder serves a group of residential units. A split single-phase pole transformer is often used to step down the voltage even further to meet the voltage level for residential, commercial and industrial users as shown in Fig.3.4. Such split phase transformers are available in both 120 V and 240 V with a common neutral to customers. The local transformer steps down the feeder voltage from 13.8 kV to 120 V/240 V [88].

3.2.3 At customer's end

The voltages of the power source at a customer site can be either 240 V or 120 V from outlets routed from a local split phase transformer. These dual voltage outputs are obtained conveniently between two phases (240V), and between a phase and the ground (120 V). A single line diagram showing this layout is highlighted in Fig.3.4.

3.2.4 PV connection at residential units

At residential sites, customers can set-up their own PV units to off-set their household consumption or export to the grid. A single line diagram of a typical PV connection at a residential site is shown in Fig.3.4. After the converter stage, the PV inverter output can be connected to the primary panel board through an AC disconnect switch. As depicted in Fig.3.4, the primary panel board is connected to a bidirectional utility meter, which measures the net usage for accounting purposes.

3.3 Limitations in Existing Distribution Network Models

The current models of the distribution network are simply too limited when dealing with newly introduced DGs for microgrid studies. Introduction of high number of DG units, as shown in Fig.3.2, requires enhancements to existing distribution network models. In essence, the following limitations have been identified for the existing distribution network models:

1. Most of the microgrid studies in the literature (as discussed in section 3.1) tend to focus on three-phase systems. With proliferation of PV and battery units at residential levels, there is a need for a benchmark network model that can be used to study effects of these DG units in single-phase active distribution networks;

2. With installation of phase-wise generation and storage units, single-phase microgrids can be formed on individual phases. The existing distribution network models do not support such single-phase configuration scenarios for coordination control and energy management within each phase and between two different phases;

3. There exists no distribution system models available in the literature that can accommodate realistic situations where multiple singe-phase DG units installed in

different phase(s) and then connected on to a primary feeder;

4. The network model with its coordination control strategy should ensure that the voltage and frequency in each phase are maintained by balancing generation and consumptions under different conditions in that particular phase, while trying as much as possible towards balancing the three phases. This feature is not supported in the existing distribution system models;

5. Community based power sharing using controllable power electronic devices is a novel idea for single-phase microgrids, as studied in [125, 126]. Currently, there is no standard distribution system model that can provide a unified framework to investigate power and load sharing among different microgrids in separate phases;

6. At present, the system utilized by distribution utilities can give the operators real time visualization of current state of the network, fault zones or regions under maintenance etc. The proposed system is a step towards deployment of these residential microgrids whereby, the system operators can simulate their jurisdiction's network off-line. This will later help them to deploy such microgrids in the future; and

7. By making use of the proposed benchmark distribution network with its various configuration parameters, the ratings of back-to-back converters, the potential system unbalance with multiple DG sources and the control parameters can be determined.

3.4 Single-phase Residential Microgrid Studies

The proposed benchmark model overcomes the identified deficiencies in the existing distribution system models as mentioned in section 3.3. This new benchmark model is capable of supporting ever-increasing number of DG units introduced at individual consumer levels. Without loss of generality, three regions of interest are identified in Fig.3.2:

1. At the left corner of Fig.3.2, a set of local PV generation and storage units has been referred to as DG1. The generation and storage that is located centrally with respect to phase A, is referred to as DG2. This serves the customers that are connected to this phase through multiple distribution transformers. PV/storage at each residence (DG1) can be used together with central generation (DG2) to form Microgrid # 1. This configuration or its variation can be repeated in phase B and/or phase C.

2. Microgrid # 2 overlaps some region of Microgrid # 1 as is evident from Fig.3.2 Microgrid # 2, referred to as DG3 in Fig.3.2, has its generation and storage installed on the primary feeder at bus#14 , which is central to its three phases. If a fault occurs on bus#14, the loads on this feeder can be served through this architecture.

3. Finally, DG4 serves the distribution system from the substation onwards. The PV generation and storage units are placed next to the first serving bus. It can serve as a temporary source, should a fault occurs in the substation or on the incoming transmission line. The location of DG4 is strategic with respect to the entire distribution network under the current consideration. With DG4, Microgrid # 3 has been formed, which incorporates both Microgrids # 1 and # 2 within its jurisdiction.

Some of the salient features of this proposed benchmark distribution network model are discussed next.

3.4.1 Coordination of DG units in grid connected mode

The proposed benchmark distribution system can be used to study various scenarios in grid-connected residential microgrids. These may involve the coordination of several microgrid structures within a distribution network. Due to the presence of phase-wise generation and storage units, the benchmark allows for some of the local loads to be sup-

ported by the grid, while others by the local PV/battery hybrid systems. This segregation of supplies for loads between the utility and local DG sources is usually dependent upon a specific configuration of connection and accounting arrangements of a customer [79].

3.4.2 Coordination of DG Units in an islanded mode

For islanded residential microgrids, the coordination of DG units is more complex as compared to that in grid-connected systems, because one can no longer use the grid as the reference for voltage and frequency regulation. The situation becomes even more complicated when single-phase DGs and loads are considered. By referring to the structure for residential microgrids in Fig.3.2, the following control and coordination issues should be investigated:

1. In Microgrid #1, the DG1 at each customer's home, needs to be coordinated with DG2. Control strategies can take on either a master-slave or a multi-master arrangement. If a master-slave approach is chosen, DG2 can be designated as the 'master unit' to regulate the voltage and frequency in Microgrid # 1, while the DG1 will be run as a slave unit. These units will be operated as power controlled sources. In a multi-master configuration, two or more identified DG units can be used to regulate the frequency and the voltage profile in Microgrid # 1. This can be achieved if the units are arranged in droop controlled modes. Since it is necessary to maintain local power management within a phase, such schemes are referred to as intra-phase power management. Detail coverage of a modified vector control and improved multi-segment droop control scheme adopted for the intra-phase power management module can be found in [125, 126].

2. The system originated from the primary feeder has been designated as Microgrid # 2 as shown in Fig.3.2. Even though this microgrid contains three phases, they are made up with a single-phase microgrid with nested DG units. The control strategy

Table 3.1: Parameters of a step down transformer at a local substation

Transformer type	$\Delta - Y$
Primary winding (L-L RMS)	69 kV
Secondary winding (L-L RMS)	13.8 kV
3-ϕ transformer (MVA)	100 MVA
Operating frequency	60 Hz
Positive sequence leakage reactance	0.0675 p.u
Air core reactance	0.2 p.u
Knee voltage	1.17 p.u
Magnetizing current	2%

allows individual phases to share power under islanded condition according to their load demands, capacities of DG units and state of charge of the battery storage units. In this way, it is possible to achieve a balanced three-phase system even through each phase can have very different local characteristics. This is achieved by the inter-phase power management scheme, known as 'Community Energy Balance Control System'.

3. Since Microgrid # 2 is connected with Microgrid # 1, DG 3 in Microgrid # 2 will have to be coordinated with DG 1 and DG 2 in Microgrid # 1 as well. By a similar token, Microgrid # 3 will also need to be coordinated with Microgrids # 1 and # 2. Such nested configuration makes control and power management challenging, but at the same time, makes this model more versatile to adapt to various realistic system configurations.

3.5 Benchmark Distribution System Model for Residential Microgrids

A section of radial distribution network of Fig.3.2 from the local substation to a customer residences in Fig.3.4 is taken as an example in the following analysis. The substation in the current study steps down voltage from 69 kV to 13.8 kV. The parameters adopted for the substation step down transformer are presented in Table 3.1 [11].

Table 3.2: Parameters of a primary feeder

Length of primary feeder	8 km
Height of pole	30 m
Horizontal spacing between conductors	1 m
Vertical offset of central conductor	0.5 m
Shunt conductance	1x10^{-11} mho/m
Resistivity	1 ohm*m
Resistance of conductor (R_p)	2.311 $m\Omega/100ft$ or 0.0758 $m\Omega/m$
Reactance of conductor (X_p)	3.314 $mH/100ft$ or 0.109 $m\Omega/m$

The primary feeder adopted in this model corresponds to an overhead three-phase transmission line, supported by utility poles with the length varying between 1.61 and 24 km. According to ABB, the reactance (R_p and X_p shown in Fig.3.2) of a 1000 kcm primary feeder cable, are given in $m\Omega/100ft$ [127]. For a 13.8 kV primary feeder, the parameters, including the values of reactance used are tabulated in Table 3.2.

3.6 Configuration Parameters of the Benchmark Distribution Network

The local distribution transformer used is a centrally tapped transformer, which further steps the voltage down from 13.8 kV to 120/240 V. The parameters of a local distribution transformer used in the model are laid out in Table 3.3. In this study, 10 residential units have been assigned a phase from the primary feeder. Adding more residential units per phase produces a memory error in the simulation software; in this case PSCAD/EMTDC. It is assumed that all the houses covered by one phase are situated at a distance of 10 m from each other. This distance will add to the resistance of electric cables, that are laid for each unit. Typically 1/0 Aluminum-Copper Steel Reinforced (ACSR) cable is used for underground service connections to residential units. In older communities, overhead connections are still used. In these cases, the parameters may need to be adjusted. The values for the cable resistance in each phase are denoted by r_1 and r_N, where N represents the total number of houses served on a phase as shown in Fig.3.2. The resistance of 1/0

Table 3.3: Parameters of a local distribution transformer

Transformer type	Central tapped
Primary winding (L-L RMS)	13.8 kV
Secondary winding (L-L RMS)	120/240 V
Transformer (MVA)	0.075 MVA
Operating frequency	60 Hz
Positive sequence leakage reactance	0.02 p.u
No load losses	0.0075 p.u
Air core reactance	0.2 p.u
Knee voltage	1.17 p.u
Magnetizing current	1%

Table 3.4: Load signatures at a residential unit

Load	Rating	V, I	PF	Z
Washing machines	2100 W	220 V, 9.35 A	0.9358	$25.67\angle 20.64°$
Microwave	1350 W	220 V, 6.25 A	0.9	$38.40\angle 25.844°$
Refrigerator	87.42 W	220V, 0.667 A	0.546	$359.81\angle 56.90°$
Fan (low speed)	50 W	110 V, 0.421 A	0.80	$285.04\angle 8.11°$
Fan (high speed)	70 W	110 V, 0.614 A	0.95	$195.44\angle 18.20°$
CFL	4 W	110 V, 0.056 A	0.6	$2142\angle 53.13°$

ACSR cable is $5.22 \times 10^{-4}\Omega/m$. Assuming that the maximum permissible voltage drop in the service cable from the transformer to the Nth house is 2%, thus, the maximum drop in voltage can be calculated as $V_D = 120 \times 2\% = 2.4V$. The power panel boards at each home are commonly rated at 100 A. Therefore, the resistance of the service cable can be derived as: $\Delta r_N = 2.4V/100A = 0.024\Omega$. This corresponds to approximately 45m of additional service cable for the Nth house as compared with the house nearest to the distribution transformer. The local distribution transformer and residential units on phase A of the primary feeder can be repeated for other two phases, given that the loading in each phase is similar. Otherwise, transformers with different MVA ratings need to be used as per regulations.

As shown in Fig.3.2, the three-phase primary feeder is routed to serve local residential units. For a typical #4 AWG cable, the reactance represented by R_A and X_A in Fig.3.2 is taken as $27.4 + j10.45m\Omega/100ft$. The advantage of using these parameters in the model can be appreciated when single phase laterals are loaded with multiple groups of residential units which are separated by some distance. The reactance will cause voltage drops along the lateral. The amount of such voltage drops will depend on actual loading

Table 3.5: Harmonic content of loads

Type of Load	Harmonic Content (Amps RMS)			
	$\mathbf{3}^{rd}$	$\mathbf{5}^{th}$	$\mathbf{7}^{th}$	$\mathbf{9}^{th}$
Washing machines	0.45	0.175	0.15	0.13
Microwave	0.5	0.5	0.1	0.2
Refrigerator	$4.6\text{x}10^{-5}$	$8.0\text{x}10^{-6}$	$4.0\text{x}10^{-6}$	$3.0\text{x}10^{-6}$
Fan (low speed)	0.023	0.0225	0.013	$7.0\text{x}10^{-3}$
Fan (high speed)	0.026	0.011	$8.0\text{x}10^{-3}$	$9.0\text{x}10^{-3}$
CFL	0.45	0.175	0.15	0.13

of the residence, quality of the cable used and the number of homes served by the primary feeder.

The residential units in Fig.3.2 have the same electrical layout as shown in Fig.3.4. Each unit is assumed to have some typical household electrical apparatus namely, microwave oven, television set, washing machine, refrigerator, compact fluorescent lamps (CFLs), high and low speed fans, as listed in Table 3.4. Their typical signatures in terms of ratings, voltage and current requirements, power factor and impedance are also listed. These loads are connected to electrical outlets where voltage can be both 120 and 240 V. #AWG-14 cables are used for electrification of each unit, which has a rating of 15 A [128]. The harmonic content of these loads is also tabulated in Table 3.5.

3.7 Case Study

To validate the performance of the benchmark distribution system, the architecture of Microgrid # 1, as shown in Fig.3.2, is used for grid-connected and islanded scenarios of residential microgrids. It is assumed that one of the primary feeders from the local substation is equipped with a hybrid PV/battery unit and a droop controlled unit in each phase. A solution time step of $0.5\mu s$ is used in the PSCAD/EMTDC simulations.

To investigate the system behaviors during a transition from a grid-connected mode to an islanded mode, bus#14 is simulated with a three-phase to ground fault, which is non-recoverable in a typical 5 cycles time period. The DG units in the residential microgrid (hybrid PV/battery system) will serve the loads under this scenario. The simulation results are presented in Fig.3.6.

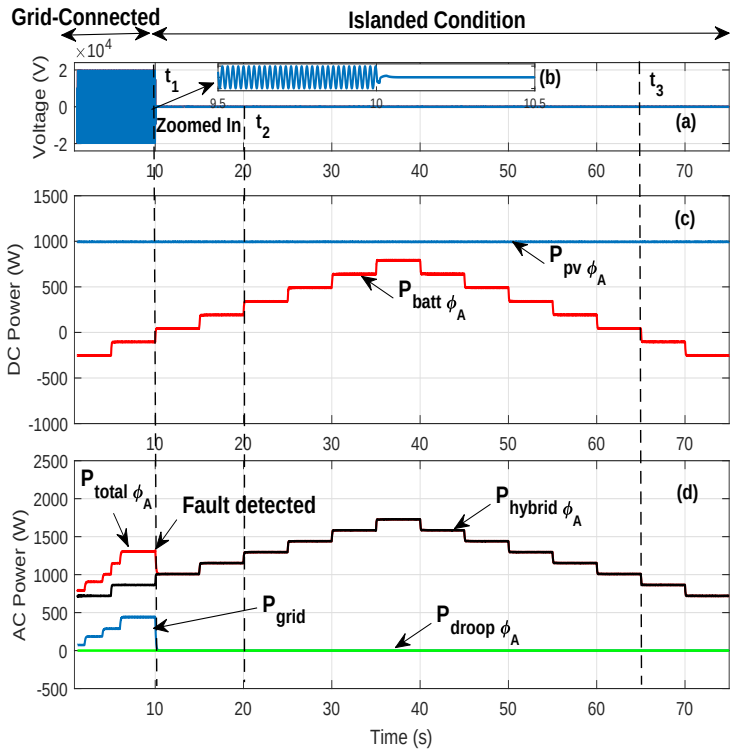


Figure 3.5: Voltage and power variations during a transition from a grid-connected to an islanded mode using the benchmark distribution system model.

Prior to $t_1 = 10s$, the grid is operating normally with the primary feeder operating at $f = 60Hz$ and $V_{rms} = 13.8kV$, as evident from the Fig.3.5(a). A zoomed-in version of the same figure is also shown, for visualization purposes. Fig.3.5(b), shows the DC power profile of the system. For the duration of the simulation run i.e. $75s$, it is assumed that the PV power generation is constant at $1000W$. This is represented by $P_{pv_{\phi_A}}$. The respective charging and discharging of the battery in the hybrid unit is represented by $P_{batt_{\phi_A}}$ and by the state-of-charge (SOC) in Fig.3.6(a). Since some of the loads in the residential microgrid will be handled by the grid and others by the PV/battery hybrid unit, the AC power profile in Fig.3.5(c) illustrates this by the grid and the hybrid unit's contribution in serving the loads.

At $t_1 = 10s$, an extended three-phase to ground fault is detected. At this point, the grid becomes unavailable. Hence, the total load is taken up by the hybrid unit, as shown in Fig.3.5(c). After $t_1 = 10s$, the load transitions are simulated by step changes

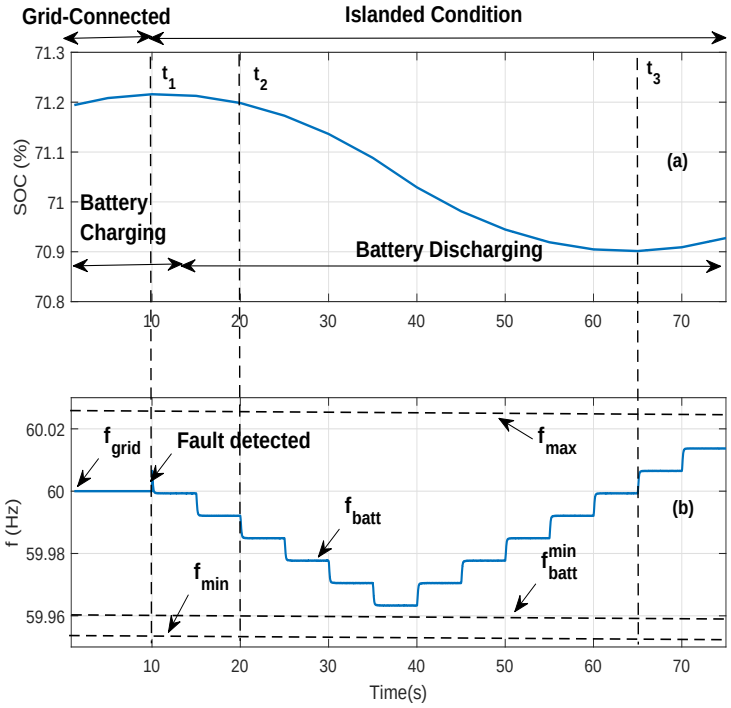


Figure 3.6: Variations in the SOC and the system frequency at the transitions from a grid-connected to an islanded mode using the benchmark distribution system model.

of $144W$. At this stage, any additional PV power available will be used to charge the battery. This is illustrated between $t_1 = 10s$ and $t_2 = 20s$ in Fig.3.5(b). Between $t_2 = 20s$ and $t_3 = 65s$, both the PV and battery units contribute towards the loads. This is shown by the battery discharging in Fig.3.5(b) with the respective change in SOC in Fig.3.6(a). After $t_3 = 65s$ till the end of the simulation run, the battery starts charging again. This is because the loading deceases below the PV power. At this time, only the PV unit will serve the loads while the battery charges.

From these simulation studies, it can be concluded that the benchmark distribution system is capable of operating both in grid-connected and islanded operating conditions. The system is also capable of coordinating a hybrid PV/battery unit with the local loads.

3.8 Summary

A new benchmark distribution system model capable of supporting studies of residential microgrids has been developed. This model supports both grid-connected and islanded

systems, and transitions from one to the other. A unique feature of this model is that it allows for integration of multiple single-phase DG sources to be located in a particular phase, yet, it also supports coordination of these units within their respective phases or across different phases. This proposed benchmark model will allow researchers and utility personnel to investigate the impact of ever increasing installation of roof-top PV units and residential energy storage units. A case study has been carried out using this newly developed benchmark to illustrate its effectiveness.

Chapter 4

Mathematical Foundations for Balancing Single-Phase Residential Microgrids in a Three-Phase Distribution System

With increased installation of single-phase rooftop PV systems, in-house battery storages, and high-power plug-in loads (i.e. EVs) at single-phase residential sites, it is prevalent that more and more residential distribution systems are becoming severely unbalanced causing power quality problems and thermal risks at distribution sub-stations. While different techniques have been investigated to resolve this issue, there is still lack of adequate theoretical foundation to guide these approaches. In this chapter, detailed analytical analysis has been carried out for a typical North American residential community having single-phase power generation, storage, and high-power randomly plug-in loads. This analysis has laid mathematical foundations for a class of operating scenarios and provided essential theoretical basis to unify different techniques for dynamically balancing single-phase microgrids connected with three-phase distribution systems. Detailed

formulations have been developed for the first time to draw explicit power transfer relationships among power surplus phases and power deficient ones to achieve an overall dynamic balance. A user-friendly interactive on-line tool has also been developed for potential users to evaluate their own application scenarios.

4.1 Introduction

There has been a tremendous surge in installation of residential rooftop PV systems (with local storage) over the past few years [129]. Since these systems are often connected to one phase of a three-phase system, conventional residential distribution networks have gradually evolved into active networks with a high degree of phase imbalance [114]. With sufficient local generation and storage, distribution companies are strategizing by grouping a number of houses to form a residential microgrid [130], while power from all three phases is used to support local community and shopping centers, which are predominately three-phase loads. The power imbalance among different phases can be reduced or eliminated by making use of interfacing back-to-back converters for power transfer from power surplus phases to power deficient phases. Hence, these power rebalancing techniques have become a necessity for distributions networks connected with small-scale local generation in the form of microgrids [131, 132].

A configuration of a typical of residential microgrid can be illustrated in Fig.4.1. The system allows customers to connect their PV generation and battery storage to the single-phase network local to them. The three single phases are connected through respective back-to-back converters, which can be used for dynamic power balancing. Each single-phase microgrid has a three-tiered hierarchical control strategy to maintain voltage and frequency stability within its phase, as well as power transfer among different phases. Within such a control strategy, the primary and the secondary control layers, referred to as intra-phase power management [125, 126, 133], are mainly used for control

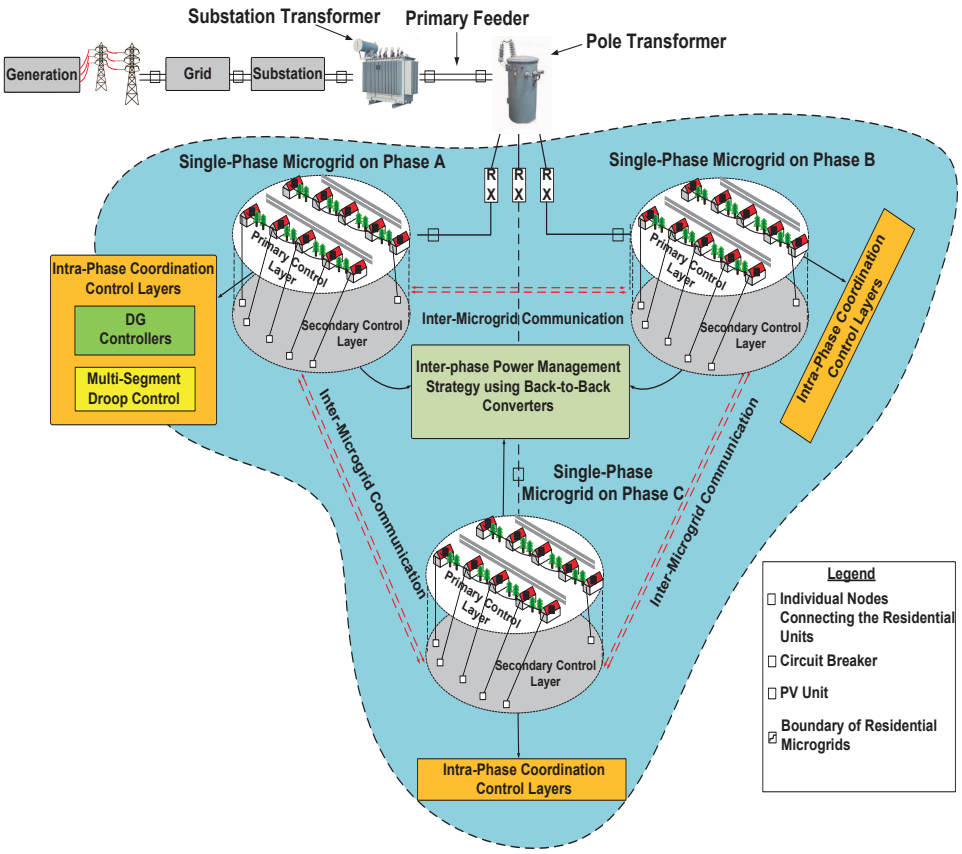


Figure 4.1: Single-phase microgrids with DG units in a three-phase system with a central EMS, back-to-back converters and a network controller.

and power management within a respective phase. The tertiary layer takes on the task of phase balancing by determining the amount of power transfers in real-time among different phases. As such, this layer is referred to as inter-phase power management in [125,126,133], which involves activating and managing appropriate power flow through the back-to-back converters.

Balancing techniques for three-phase microgrids have been proposed in [134, 135]. In [134] a repetitive controller is developed to deal with unbalanced loads and to reduce harmonics. While in [135], a robust controller is proposed for the same purpose. These type of controllers can only be used to reduce the effects of positive and negative sequence currents caused by the unbalanced loads. Hence, they cannot be used to re-establish the power balance in three phases, as are the above-mentioned cases. Other power balancing topologies relying on converters have also been investigated in [136–142]. An active

power filtering technique to inject the harmonic current for compensating the non-linear loads at the DC link is introduced in [136]. Improved converter topologies using mid-point capacitors [137, 138], four-leg inverter [139, 140] or a three H-bridge single-phase inverter topology [141, 142] proposed an active filter for balancing non-linear loads in microgrids. The control strategies discussed in [136–142] can only deal with systems with a common DC link, in particular, with centralized PV generation and battery reserve. These techniques cannot be easily adopted for residential microgrids due to absence of a common DC link for group of houses connected in a single-phase.

Power management strategies for 3-phase balanced microgrid systems have been studied in [35, 37, 71, 77, 143]. Various control strategies have been developed to coordinate different Distributed Generation (DG) units with energy storage systems. One of these techniques is to use a multi-segment droop control strategy [35, 37, 143]. However, this strategy works only for balanced three-phase systems and its effectiveness is limited for residential microgrids with diverse, independent power generation, distributed storage, and different load profile on each phase.

Coordination of the three individual single-phase microgrids, consisting of three separate PV/battery hybrid systems, has been proposed by using back-to-back converters. The control of these converters between a microgrid and a grid connection is explored in [82]. The DG units in each microgrid support its own local load as much as possible. However, whenever the load demand in a particular phase increases beyond the capacity of its own DG units, the utility provides the additional power through the back-to-back converters. When the local demand is lower than the local generation, the back-to-back converter will export the surplus power to the grid.

The control of an islanded hybrid single and three-phase microgrid through back-to-back converters is highlighted in [78]. The proposed architecture is a close depiction of a distribution system with single-phase loads connected with local DG units. As such, phases A and B constitute DG units and local loads, while phase C is considered as

the load center only. The power exchange between phases is carried out by controlling the inter-tied back-to-back converters among the three phases with unidirectional power flow to the load center. An extensive control model using a back-stepping technique is proposed in [78]. Although not all system level equations are elaborated, it does provide possible scenarios for single-phase residential microgrids [78]. It will be shown that the proposed mathematical formulation can indeed be applied to some of the scenarios described in [78] with minor modifications. Such modifications are due to the fact that one phase in [78] is a pure load center absence of any local generation and storage.

Although the primary and secondary control layer strategies for single-phase residential microgrids have been developed by the same authors [125, 126, 133], those control strategies have not considered scenarios where the phases with power surplus can transfer certain amount of power to phases with power deficiency. To achieve this objective, it is important to have a supervisory control layer, which can manage the power transfer among different phases to achieve an overall dynamically balanced three-phase system. To unify different approaches, it is important to develop an underlying mathematical formulation to represent different phase balancing scenarios through power transfers among different phases. This constitutes the sole objective of this chapter. It lays a foundation for unifying several existing techniques. Furthermore, the formulation is also technology neutral, and is not be tied to any specific implementation details.

More specifically, the main contribution of this chapter is the derived mathematical formulation to investigate the relationship between an unbalanced three-phase microgrid with its three single-phase microgrids, and to determine the amount of power needed to be transferred to re-balance the system. The formulation is developed such that it can be easily realized through the three back-to-back converters connecting the three phases. Furthermore, these mathematical derivations are later simulated to analyze their correctness.

The advantage for such residential microgrids may be evident, where the generation

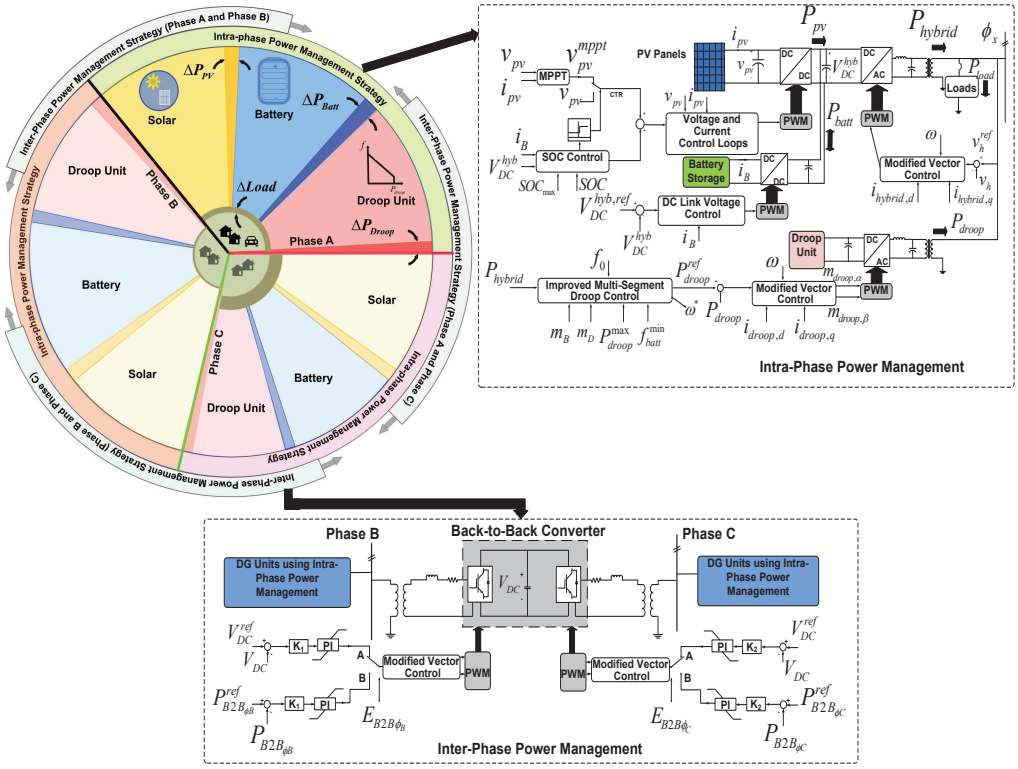


Figure 4.2: Power circle representation of three single-phase residential microgrids connecting to a three-phase substation transformer along with the inner controls of intra-phase power management strategy.

and storage available in one phase could be significantly higher than that in other phases. This could occur for several reasons, which include the alignment of the PV units where some of them may get affected by shading effects from the surroundings, or storage unit(s) operating near threshold boundaries, or the DG units having reached their power capacity limits [37, 144]. Therefore, the power imbalance in the phases can effectively be reduced through inter-phase power transfer.

To demonstrate the effectiveness of such formulation, six case studies have been presented. Interested readers are also invited to an on-line tool kit site. By putting in the parameters associated with their unbalanced distribution systems, DG, and storage units, they can calculate the amount of power transfers needed to achieve phase balance for their own application scenarios.

4.2 Relationship Among Three Single Phases

As shown in Fig.4.1, the three single-phase microgrids are connected to their respective phases on the secondary side of the sub-station transformer. To minimize the stress inflicted to the transformer by the unbalance currents drawn by these single-phase microgrids, it is desirable for the three single-phase microgrids to operate in a balanced form. Unlike traditional passive networks where the balance condition can be established through impedance matching, the current microgrids have their own local generation, energy storage devices, and unique load profiles, such as randomly plugged-in heavy loads. These unique operating characteristics have made the phase balancing a much challenging task. This condition can be intuitively represented by a power circle as shown in Fig.4.2. The power circle consists of three independently operated microgrids in each of the three phases. This configuration is a true representation of an existing residential distribution system, where different phases are allocated to different streets. Take Phase A for example, it has its own local loads, PV generation, battery storage, as well as droop based control system for power management as represented by ΔP_{PV}, ΔP_{Batt} and ΔP_{Droop} in Fig.4.2. Similar situations can be seen in the other two phases. The individual phases are able to support their own loads, as much as possible through the modified vector control strategy and the improved multi-segment droop strategy that are previously proposed by the same authors in [125, 126, 133].

The multi-segment droop control strategy allows for frequency regulation in ϕ_x, which is described in more detail in Chapter 5. The control structure for the strategy is shown in Fig.4.2. This results in proper coordination of PV/battery with droop units under various operating conditions, the status of the battery and the capacities of the DG units.

Due to uneven local generation and consumption, it is seldom the case that these three microgrids have identical operating conditions. Therefore, viewing from the substation transformer, these three single-phase microgrid appears to be unbalanced loads.

They all draw different amount of currents from the transformer. However, it is possible to achieve dynamic phase balancing if power is allowed to be exchanged among these three phases. The coordination of power exchanges can be done through inter-phase power management strategy as shown in the outer arches in Fig.4.2, using an improved multi-segment droop strategy as proposed earlier by the same authors [125, 126, 133].

The use of inter-phase power management strategy is not limited between only two phases. In fact, the phase with surplus power can provide necessary power to two power deficit phrases simultaneously so that neither phases have to draw additional power from the sub-station transformer. Hence, a dynamic balanced system can be achieved. The back-to-back converters are controlled through multi-loop PI control stages comprising of the previously proposed modified vector control strategy by the same authors as shown in Fig.4.2 [125, 126, 133]. This control strategy is explained in detail in Chapter 5.

For the purpose of this study, some assumptions have been taken. It is assumed that all back-to-back converters are in working conditions and that the supervisory layer with its communication links to each phase of the residential microgrid are fail safe.

4.2.1 Operating scenarios and management of power exchanges

Even though the power circle in Fig.4.2 has illustrated the basic concept of dynamic balancing among three single-phase microgrids, it is important to consider unique conditions under different operating situations. In total, there are six possible scenarios as illustrated in Table 4.1. Note that the following symbols are used to represent modes of operations among the six scenarios: "=" means a balanced condition with no need for any power transfer, "→" means power transferred from the current phase to other phases; "←" power received from another phase; and finally, "¤" stands for drawing more power from the sub-station transformer or shedding some local load. Similar scenarios but with different phases are also applicable, which are not repeated herein for brevity.

4.2.2 Objectives

With the establishment of the six operating scenarios, the important questions are: for a given situation where some phases have surplus power and other phases may have power deficiency, how much power should be transferred between phases so that a balanced three-phase system can be achieved dynamically? To be more specific, this question can be divided into three sub-questions:

1. How much power need to be transferred from one phase to another phase?
2. How much power need to be transferred from one phase to the two other phases? and
3. How much power need to be transferred from the two surplus phases to the power deficient phase?

These questions arise when the local intra-phase power management is unable to support the loads. Thus, the objective of this paper is to provide comprehensive answers to the above fundamental questions through detailed analysis.

4.3 Mathematical Foundations for Power Transfer Among Phases

The mathematical derivations in this section are performed for the scenario when the local intra-phase power management is unable to support the load and the intra-phase power management has to intervene to balance the phases. To this end, the purpose is to find the required power for the deficit phase and the contribution from the power surplus phases to balance the power deficit phase. Given a balanced three-phase wye system with impedance z_y in each phase, the magnitudes of phasor voltages in each phase are given by V_{an}, V_{bn} and V_{cn}, where each phasor is displaced by 120° angle, as shown in Fig.4.3(a).

Table 4.1: Six operating scenarios of three single-phase microgrids

Sr.	**Scenario**	$\phi_{\mathbf{A}}$	$\phi_{\mathbf{B}}$	$\phi_{\mathbf{C}}$
1.	$\begin{cases} P_{Gen_{\phi_A}} = P_{Load_{\phi_A}} \\ P_{Gen_{\phi_B}} = P_{Load_{\phi_B}} \\ P_{Gen_{\phi_C}} = P_{Load_{\phi_C}} \end{cases}$	$=$	$=$	$=$
2,3.	$\begin{cases} P_{Gen_{\phi_A}} > P_{Load_{\phi_A}} \\ P_{Gen_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} > P_{load_{\phi_C}} \end{cases}$	$\leftarrow$	$\leftarrow$	$\rightarrow$
4.	$\begin{cases} P_{Gen_{\phi_A}} > P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} = P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} < P_{load_{\phi_C}} \end{cases}$	$\rightarrow$	$=$	$\leftarrow$
5.	$\begin{cases} P_{Gen_{\phi_A}} > P_{Load_{\phi_A}} \\ P_{Gen_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} < P_{load_{\phi_C}} \end{cases}$	$\rightarrow$	$\leftarrow$	$\leftarrow$
6.	$\begin{cases} P_{Gen_{\phi_A}} < P_{Load_{\phi_A}} \\ P_{Gen_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} < P_{load_{\phi_C}} \end{cases}$	¤	¤	¤

The zero, positive and negative sequence voltages can be represented as,

$$\begin{aligned} V_0 &= \frac{1}{3}\left(V_{an} + V_{bn} + V_{cn}\right) \\ V_1 &= \frac{1}{3}\left(V_{an} + aV_{bn} + a^2V_{cn}\right) \\ V_2 &= \frac{1}{3}\left(V_{an} + a^2V_{bn} + aV_{cn}\right) \end{aligned} \tag{4.1}$$

Under a balanced condition, the zero and negative sequence voltages will be zero, while the positive sequence voltage will be equal to the phase voltage. The phasor voltages in

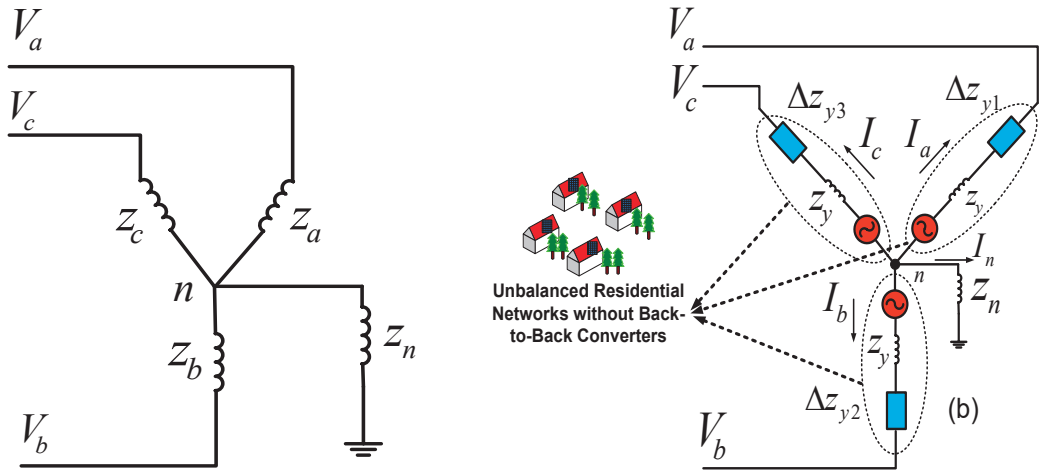


Figure 4.3: (a) Balanced and (b) Unbalanced wye-networks with impedances in the neutral.

terms of impedances and currents are given by,

$$\begin{aligned} V_{an} &= z_y I_a + z_n I_n \\ &= z_y I_a + z_n \left(I_a + I_b + I_c\right) \end{aligned} \tag{4.2}$$

Similarly

$$V_{bn} = z_n I_a + \left(z_y + z_n\right) I_b + z_n I_c \tag{4.3}$$

$$V_{cn} = z_n I_a + z_n I_b + \left(z_y + z_n\right) I_c \tag{4.4}$$

Rewriting (4.2)-(4.4) in a matrix form gives,

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} (z_y + z_n) & z_n & z_n \\ z_n & (z_y + z_n) & z_n \\ z_n & z_n & (z_y + z_n) \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{4.5}$$

where, z_n is the impedance in the neutral wire and I_a, I_b and I_c are line currents.

For an unbalanced wye-network with local generation and storage, a single line diagram can be shown in Fig.4.3(b). The local DG sources are at the front end of a voltage controlled single-phase inverter, which are shown as AC sources in all of the three phases

in Fig.4.3(b). For this case, consider a delta impedance in each phase, as illustrated by Δz_{y_1}, Δz_{y_2} and Δz_{y_3} in Fig.4.3(b), where these delta impedance can either be positive or negative. The non-zero value is indicative of mismatch between the generation and the local load consumption within that particular phase. Rewriting the equations in the form of impedance,

$$V_{an} = (z_y + \Delta z_{y_1} + z_n) I_a + z_n I_b + z_n I_c \tag{4.6}$$

Similarly,

$$V_{bn} = z_n I_a + (z_y + \Delta z_{y_1} + z_n) I_b + z_n I_c \tag{4.7}$$

$$V_{cn} = z_n I_a + z_n I_b + (z_y + \Delta z_{y_1} + z_n) I_c \tag{4.8}$$

When local load changes, $\Delta z_{y_{1,2,3}}$ in each phase will change, as a result,

$$V_{an} \neq V_{bn} \neq V_{cn} \tag{4.9}$$

4.3.1 All phases are balanced

Considering, the first scenario in Table 4.1, where all phases are balanced, given $\Delta z_{y_z} = 0$. The power delivered to individual loads in each phase is given by,

$$P_{\phi_z} = \frac{V_{zn}^2 cos\theta_L}{(z_y + \Delta z_{y_z})} \tag{4.10}$$

where, ϕ_z represent one of the three-phases of the residential microgrid.

4.3.2 A power surplus phase transferring power to a power deficit phase

In order to balance such a system without the need of increasing the capacity of neutral current, the proposed methodology involves the implementation of interfacing back-to-

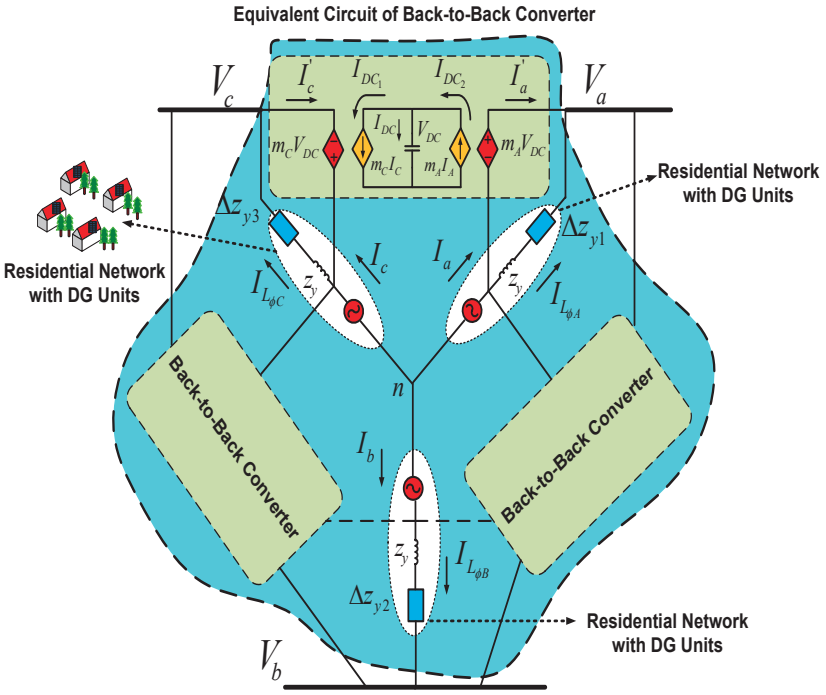


Figure 4.4: Proposed interfacing back-to-back between phases with its equivalent circuit.

back converters between phases. A single-line diagram of a such an implementation is shown in Fig.4.4, where the back-to-back converter is shown as an equivalent circuit diagram.

Without loss of generality, assuming that ϕ_A is a power surplus phase while ϕ_C is a power deficient phase, the single-phase power in ϕ_C can be written in terms of the line current and the phase voltages as,

$$I_{L_{\phi_C}} = I_c + I_c^{'} \tag{4.11}$$

where, $I_{L_{\phi_C}}$ is the load current, I_c is the line current and $I_c^{'}$ is the surplus current from ϕ_A through the back-to-back converter. The single-phase power in ϕ_C can then be written as,

$$P_{\phi_C} = V_{cn} I_{L_{\phi_C}} cos\theta_L \tag{4.12}$$

where, $cos\theta_L$ is the line power factor. Substituting (4.11) in (4.12), gives,

$$P_{\phi_C} = V_{cn} I_c cos\theta_L + V_{cn} I_c^{'} cos\theta_L \tag{4.13}$$

where from Fig.7.2, $I_c^{'}$ and I_c can be derived as,

$$I_c^{'} = \frac{m_C V_{DC}}{z_y + \Delta z_{y_3}} \tag{4.14}$$

and

$$I_c = \frac{V_{cn}}{z_y + \Delta z_{y_3}} \tag{4.15}$$

where, m_C is the modulation index of the back-to-back converter for ϕ_C and V_{DC} is the voltage across DC link capacitor in the back-to-back converter. Substituting (4.14) and (4.15) into (4.13), one gets:

$$P_{\phi_C} = \frac{V_{cn}^2}{z_y + \Delta z_{y_3}} cos\theta_L + \frac{V_{cn} m_C V_{DC}}{z_y + \Delta z_{y_3}} cos\theta_L \tag{4.16}$$

Simplifying (4.16) leads to:

$$P_{\phi_C} = V_{cn} cos\theta_L \left[\frac{V_{cn} + m_C V_{DC}}{z_y + \Delta z_{y_3}} \right] \tag{4.17}$$

For the ϕ_A part of back-to-back converter, the $m_A V_{DC}$ product can be written as,

$$\begin{aligned} m_A V_{DC} &= I_a^{'} \left(z_y + \Delta z_{y_1} \right) \\ V_{DC} &= \frac{I_a^{'} \left(z_y + \Delta z_{y_1} \right)}{m_A} \end{aligned} \tag{4.18}$$

Substituting (4.18) in (4.16) with proper simplification, it can be shown as,

$$P_{\phi_C} = V_{cn} cos\theta_L \left[\frac{V_{cn}}{z_y + \Delta z_{y_3}} + \frac{I_a^{'} m_C}{m_A} \left(\frac{z_y + \Delta z_{y_1}}{z_y + \Delta z_{y_3}} \right) \right] \tag{4.19}$$

Separating the terms in (4.19) gives,

$$P_{\phi_C} = \underbrace{\frac{V_{cn}^2 cos\theta_L}{(z_y + \Delta z_{y_3})}}_{Intra-phase} + \underbrace{\frac{V_{cn} I_a^{'} m_C cos\theta_L}{m_A} \left(\frac{z_y + \Delta z_{y_1}}{z_y + \Delta z_{y_3}}\right) E_{B2B_{\phi_A}}}_{Inter-phase} \tag{4.20}$$

where, the factor $\left(\frac{z_y+\Delta z_{y_1}}{z_y+\Delta z_{y_3}}\right)$ in (4.20) represents the imbalance between phases and $E_{B2B_{\phi_A}}$ is the enabling signal for the back-to-back converter connecting ϕ_A and ϕ_C. In order to write (4.20) in terms of individual power contributions from each of the DG units, (4.18) can be rewritten as,

$$\begin{aligned} m_A V_{DC} &= \eta V_t \\ \frac{m_A V_{DC}}{\eta} &= \frac{n \cdot P_{surplus,A}}{I_a^{'}} \end{aligned} \tag{4.21}$$

where, η is the power loss factor of the converters, n is the power ratio between the power deficiency in one phase to the power surplus in another phase, which determines the amount of power transferred by the inter-phase power management scheme. Furthermore, (4.21) can be written as,

$$m_A I_a^{'} = -\frac{\eta \cdot n \cdot (P_{total,A} - P_{load,A})}{V_{DC}} \tag{4.22}$$

where, the negative sign indicates the opposite direction of $I_a^{'}$. Expanding (4.22) further gives,

$$m_A I_a^{'} = -\frac{\eta \cdot n \cdot \left(P_{pv,A}^{max} + P_{batt,A}^{max} + P_{droop,A}^{max} - P_{load,A}\right)}{V_{DC}} \tag{4.23}$$

where, $P_{pv,A}^{max}$, $P_{batt,A}^{max}$ and $P_{droop,A}^{max}$ represent the maximum power delivery capacities of the PV, battery and the droop units, which are known for a given microgrid. Assuming that the power loss factor between phases is the same, and that $I_a^{'}$ is in the opposite direction

to that of I_c then,

$$m_C I_c = \eta \left[\frac{P_{\phi C}^{intra}}{V_{DC}} + \frac{n \cdot \left(P_{total,A} - P_{\phi A}^{intra} \right)}{V_{DC}} \right] \tag{4.24}$$

The intra-phase power management in ϕ_A is governed by the following criteria:

$$P_{\phi_A} = \begin{cases} P_{pv,A}, \quad \text{if} \quad P_{load,A} \leq P_{pv,A} \\ P_{batt,A} = \frac{f_{batt,A} - f_0}{m_{batt,A}} + P_{pv,A}^{max} \\ \qquad\qquad \text{if} \quad P_{pv,A} < P_{load,A} \leq P_{batt,A} \\ P_{droop,A} = \frac{f_{droop,A} - f_{batt,A}^{min}}{m_{droop,A}} \\ \quad \text{if} \quad (P_{pv,A} + P_{batt,A}) < P_{load,A} \leq P_{droop,A} \end{cases} \tag{4.25}$$

where, $P_{pv,A}$ is the PV power production, which is dependent on the time of the day and environmental conditions. $P_{batt,A}$ is the power supplied by the battery. It is also dependent upon its state-of-charge, while $P_{droop,A}$ is the power supplied by the droop unit. These DG units are operating under the improved multi-segment droop control strategy, which is discussed in detail in Chapter 5. Based on (4.25), the priority for power contribution from these DG units is set to be,

$$\text{Priority}_{\text{pv}} > \text{Priority}_{\text{batt}} > \text{Priority}_{\text{droop}} \tag{4.26}$$

Taking the ratio of $m_C I_c$ and $m_A I_a$, gives,

$$P_{\phi_C} = \frac{V_{DC} m_C I_c^{'}}{\eta} - n \cdot (P_{total,A} - P_{load,A}) \tag{4.27}$$

Hence, total power in ϕ_C can be shown as,

$$P_{\phi C}^{inta} + n \cdot (P_{total,A} - P_{load,A}) = \frac{m_C I_c^{'} V_{DC}}{\eta} \tag{4.28}$$

The variables on the LHS of (4.28) can be substituted in place of the control variables in (4.20).

Generally, the inter-phase power transfer component from ϕ_A can be represented as,

$$P_{\phi_A}|_{PT} = P^{ref}_{B2B_{\phi_A}} = \frac{V_{cn}\left(I_a - I_{L_{\phi_A}}\right) m_C cos\theta_L}{m_A} \cdot \left(\frac{z_y + \Delta z_{y_1}}{z_y + \Delta z_{y_3}}\right) \cdot E_{B2B_{\phi_A}} \tag{4.29}$$

4.3.3 Two phases share power equally/unequally with deficit phase

For the scenario, where multiple phases can contribute to balance the power deficient phase, (4.20) and (4.29) need revision. Again assuming that ϕ_C is the power deficit phases while ϕ_A and ϕ_B are the power surplus phases, (4.20) and (4.29) can be written as,

$$\begin{aligned} P_{\phi_C} = \; & \frac{V^2_{cn} cos\theta_L}{\left(z_y + \Delta z_{y_3}\right)} + \frac{V_{cn} I_a^{'} m_C cos\theta_L}{m_A}\left(\frac{z_y + \Delta z_{y_1}}{z_y + \Delta z_{y_3}}\right) E_{B2B_{\phi_A}} \\ & + \frac{V_{cn} I_b^{'} m_C cos\theta_L}{m_B}\left(\frac{z_y + \Delta z_{y_2}}{z_y + \Delta z_{y_3}}\right) E_{B2B_{\phi_B}} \end{aligned} \tag{4.30}$$

$$\begin{aligned} P_{\phi_A}|_{PT} \quad + P_{\phi_B}|_{PT} = & \frac{V_{cn} E_{B2B_{\phi_A}}\left(I_a - I_{L_{\phi_A}}\right) m_C cos\theta_L}{m_A} \cdot \\ & \left(\frac{z_y + \Delta z_{y_1}}{z_y + \Delta z_{y_3}}\right) + \frac{V_{cn} E_{B2B_{\phi_A}}\left(I_b - I_{L_{\phi_B}}\right) m_B cos\theta_L}{m_A} \cdot \\ & \left(\frac{z_y + \Delta z_{y_2}}{z_y + \Delta z_{y_3}}\right) \end{aligned} \tag{4.31}$$

Also,

$$P_{\phi_A}|_{PT} + P_{\phi_B}|_{PT} = P^{ref}_{B2B_{\phi_A}} + P^{ref}_{B2B_{\phi_B}} \tag{4.32}$$

where, $P_{\phi_A}|_{PT}$ and $P_{\phi_B}|_{PT}$ are the power transferred from ϕ_A and ϕ_B respectively while, $P^{ref}_{B2B_{\phi_A}}$ and $P^{ref}_{B2B_{\phi_B}}$ are the power references for the back-to-back converters connecting

ϕ_C with ϕ_A and ϕ_B. The amount of power delivered by the power surplus phases will depend upon the local net power conditions within a phase.

For the case where there are two power deficient phases, the power transfer equations for balancing can be written as,

$$P_{\phi_y} = \frac{V_{yn}^2 cos\theta_L}{(z_y + \Delta z_{y_2})} + n.\Big\{\frac{V_{yn} I_x^{'} m_y cos\theta_L}{m_x} \cdot \cdot \left(\frac{z_y + \Delta z_{y_x}}{z_y + \Delta z_{y_2}}\right) E_{B2B_{\phi_x}}\Big\} \tag{4.33}$$

$$P_{\phi_z} = \frac{V_{zn}^2 cos\theta_L}{(z_y + \Delta z_{y_3})} + m.\Big\{\frac{V_{zn} I_x^{'} m_z cos\theta_L}{m_x} \cdot \cdot \left(\frac{z_y + \Delta z_{y_x}}{z_y + \Delta z_{y_3}}\right) E_{B2B_{\phi_x}}\Big\} \tag{4.34}$$

where n and m are the ratios of power deficit in the two phases to the power surplus phase.

4.4 Power Loss in the Power Transfer Process

It is important to point out that the formulas in Table 4.1 are derived under ideal conditions, and power losses during the course of power transfer have not been considered. In practice, any power transfer would incur losses that have to be taken into consideration. Consider a scenario, where ϕ_x has surplus power, $P^{sup}|_{\phi_x}$, and ϕ_y requests power, $P^{req}|_{\phi_y}$, to be exchanged, the power loss in this transfer process can be expressed as,

$$P^{sup}|_{\phi_x} - P_{loss}|_{\phi_x} - P_{loss}|_{\phi_y} = P^{req}|_{\phi_y} \tag{4.35}$$

The above equation can further be expanded to,

$$\begin{aligned} P^{sup}|_{\phi_x} = P^{req}|_{\phi_y} &+ \left[\left(I^2 R_x\right)|_{\phi_x} + P_{loss}^{B2B}|_{\phi_x} + Tfr_{loss}\right] \\ &+ \left[\left(I^2 R_y\right)|_{\phi_y} + P_{loss}^{B2B}|_{\phi_y} + Tfr_{loss}\right] \end{aligned} \tag{4.36}$$

where R_x and R_y are the resistances of the transfer lines, as well as the service line going to individual residential units. The power loss in the back-to-back converter, P_{loss}^{B2B}, in (4.36) is composed of two components:

$$P_{loss}^{B2B}|_{\phi_x} = P_{loss}^{cap} + 2P_{con} \tag{4.37}$$

where,P_{loss}^{cap}, is the loss across the DC link of the back-to-back converter and is dependent upon its equivalent series resistance, while P_{con} is the conduction losses due to switching of gates in the dc-to-dc converters. For power exchange between residential units that are on different phases, the power loss equation (4.35) can be written as,

$$-P^{sup2}|_{\phi_x} K_1 + P^{sup}|_{\phi_x} = P^{req}|_{\phi_y} + K_2 \tag{4.38}$$

Solving for $P^{sup}|_{\phi_x}$ leads to:

$$P^{sup}|_{\phi_x} \approx P^{req}|_{\phi_y} + K_3 \tag{4.39}$$

where K_1, K_2 and K_3 are constants accounting for losses in capacitor, gate-switching and transformer at ϕ_y. The power loss factor (η) can then be calculated as:

$$\eta = 1 - \frac{K_3}{P^{sup}|_{\phi_x}} \tag{4.40}$$

The parameter provides an overall efficiency of the power sharing operation among different phases in achieving dynamic phase balance for the three single-phase microgrids.

4.5 Demonstrating Dynamic Phase Balancing by Simulation

This section presents demonstrations of local power balancing for the scenarios considered in Table 4.1. Detailed residential microgrids with hybrid PV/battery droop units

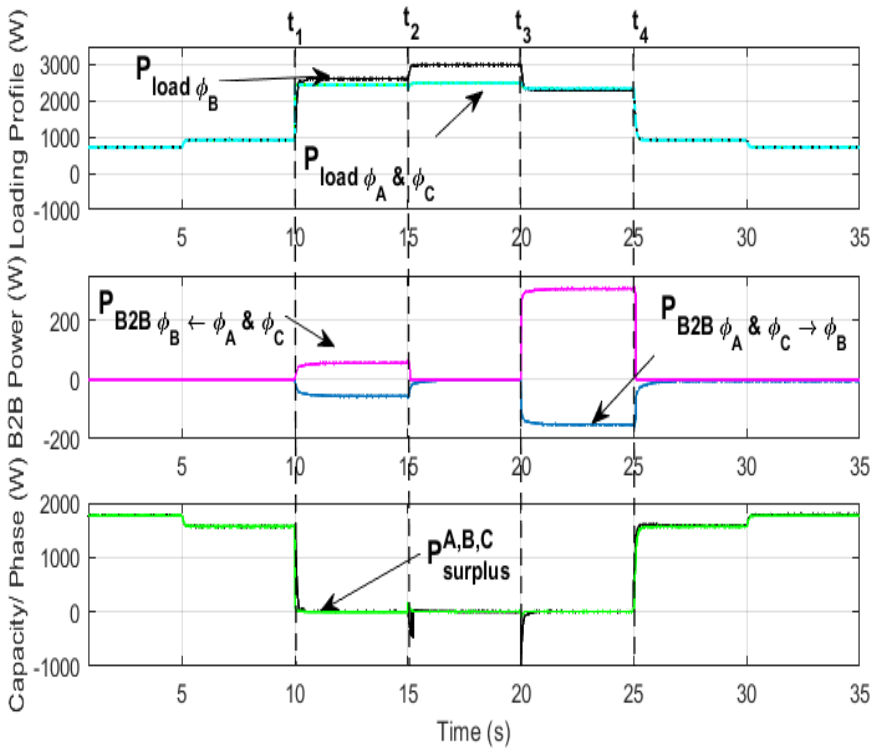


Figure 4.5: Simulation results for initial phase balance condition, two phases sharing power equally/unequally with the deficit phase and importing power from the grid conditions.

in each phase, with interconnecting back-to-back converters, have been simulated in PSCAD/EMTDC. The simulation time step is kept at $0.5\mu s$. The results are shown in Figures 4.5 and 4.6.

4.5.1 All phases are balanced

Assume that initially all three-phases are operating in a steady-state and each phase has sufficient capacity to meet its load demand prior to a load change as shown in Fig.4.5. Between $t = 0s$ and $t = t_1$, the PV and battery units, in each phase, are capable of supporting the loads through the intra-phase power management strategy. As the load profile increases in each phase, the generation and storage capacity of these phases decreases but with respect to the local distribution transformer, the phases appear to be balanced. Since, local generation and storage is sufficient to serve the loads, there is no need for inter-phase power management, through the tertiary layer. Hence $P_{B2B_{\phi_A \& \phi_C \rightarrow \phi_B}} = 0W$

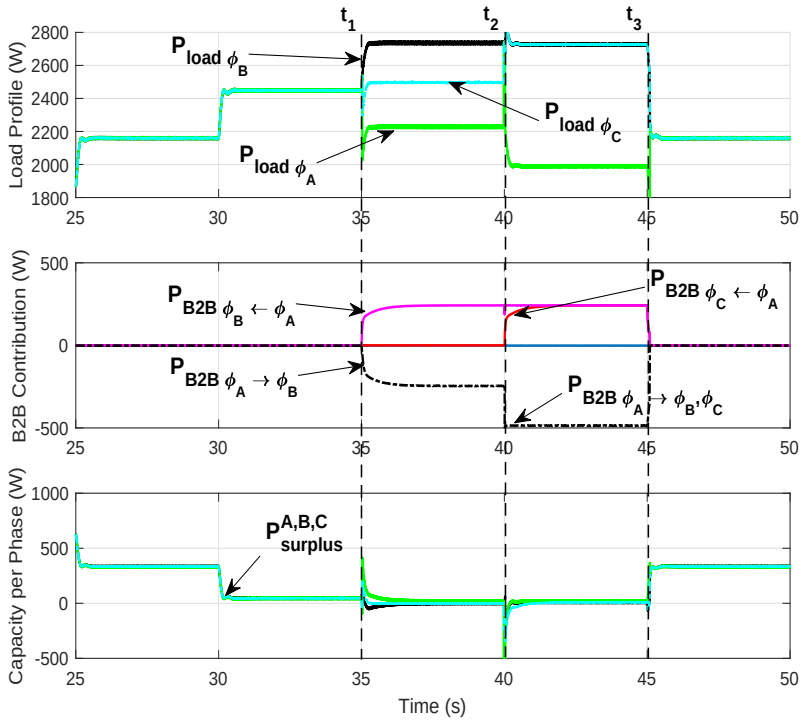


Figure 4.6: Simulation results for a power surplus phase sharing power with deficit phase(s).

as shown in Fig.4.5. This validates case#1 as listed in Table 4.1.

4.5.2 Two phases share power equally/unequally with deficit phase

Following from the previous case, at $t = t_1$, the loading in ϕ_B abruptly increases beyond the total generation capacity of that phase, as illustrated in Fig.4.5. There is a net power requirement of $106W$ in ϕ_B, as represented by $-106W$ in the phase capacity graph. At $t = t_1$, the load profiles of ϕ_A and ϕ_C are such that these phases possess surplus power. The back-to-back converters connecting the power surplus phases with the deficit phase are enabled. The power transferred from both ϕ_A and ϕ_C is represented by $P_{B2B_{\phi_A \rightarrow \phi_B}}$ and $P_{B2B_{\phi_C \rightarrow \phi_B}}$ in Fig.4.5. The total power received by ϕ_B is represented by $P_{B2B_{\phi_B \leftarrow \phi_A, \phi_C}}$. At this stage, all the three-phases possess, $106W$ in surplus generation capacity and appear to be balanced from the local distribution transformer standpoint. This validates cases#2 in Table 4.1. With different loading profiles in ϕ_A and ϕ_C, it can be shown that unequal power sharing from surplus power phases takes place with ϕ_B, which is cases#2

and 3 in Table 4.1.

4.5.3 Power surplus phase shares power with deficit phase(s)

The simulation results for this scenario are illustrated in Fig.4.6. For this case, it is assumed that the SOC of batteries in each phase is operating well below the $SOC_{\phi_x}^{max}$. Before $t = t_1$, the load profile in each phase is supported by local generation and storage. At $t = t_2$, there is a sudden change in loading for all the three-phases. ϕ_B is in deficit by $242W$, ϕ_A has excess $242W$ available while the loading in ϕ_C is completely supported by local generation and storage. Instead of balancing the system through the grid, the phases are able to do this task by triggering the enable signal, $E_{B2B_{\phi_A}}$, and setting $P_{B2B_{\phi_A}}^{ref}$=$242W$. The excess power transferred from ϕ_A to ϕ_B is represented by $P_{B2B_{\phi_A \rightarrow \phi_B}}$ in Fig.4.6 while $P_{B2B_{\phi_B \leftarrow \phi_A}}$ is the deficit power received by ϕ_B from ϕ_A. Between $t = t_1$ and $t = t_2$, the available capacity in each phase reaches zero after this exchange but the phases are autonomously balanced with respect to the local distribution transformer and without the intervention from the grid. This validates case#6 in Table 4.1. At $t = t_2$, a sudden load change in both ϕ_B and ϕ_C causes these phases to require $242W$ from the ϕ_A. In this scenario, only ϕ_A is available for sharing power with ϕ_B and ϕ_C. This sets the enable signal, $E_{B2B_{\phi_A}}$. The power that is transferred to both ϕ_B and ϕ_C is represented by $P_{B2B_{\phi_A \& \phi_C}}$, while $P_{B2B_{\phi_B \leftarrow \phi_A}}$ and $P_{B2B_{\phi_C \leftarrow \phi_A}}$ is the excess power received by the deficit phases in Fig.4.6. It is illustrated that ϕ_A is capable of sharing power with multiple phases if required. This validates cases#4 and 5 in Table 4.1.

4.5.4 All phases are in power deficiency

In this scenario, all three phases have power deficiency. As a result, neither intra-phase nor inter-phase power management strategies alone will be able to support the loads. Hence, load shedding needs to take place or grid support is required. This situation corresponds to case#6 in Table 4.1.

4.6 Online Tool Using LabVIEW

An online tool kit is developed based on the formulae derived in this chapter to mimic the operation of residential microgrids. The overall architecture is shown in Fig.4.7. The tool kit allows users to set the operating conditions for a residential microgrid in a particular phase. This is shown in Fig.4.8. Using the voltage vs current characteristics of a PV panel, the user can set the initial conditions for PV power. Similarly, the initial SOC of battery is set. Furthermore, P_{batt}^{max}, P_{droop}^{max} and the base load in a particular phase is then set. After these initial conditions are entered in the program, the system computes the surplus power available from each DG source and displays the dominant power management strategy. For the case shown in Fig.4.9, the intra-phase power management strategy is used to support the local loads. The block diagram for this is shown in Fig.4.10.

In the scenario, where a phase(s) do not have sufficient generation and storage to support the local loads, the inter-phase power management strategy is used. In this scenario, power surplus phase(s) is identified according to its current power availability. A snippet of the power management cases developed in LabVIEW is shown in Fig.4.11. A detailed demonstration of this tool kit is also available online and is accessible using the url: `https://www.youtube.com/watch?v=g_dgDHL2Suw&t=571s`.

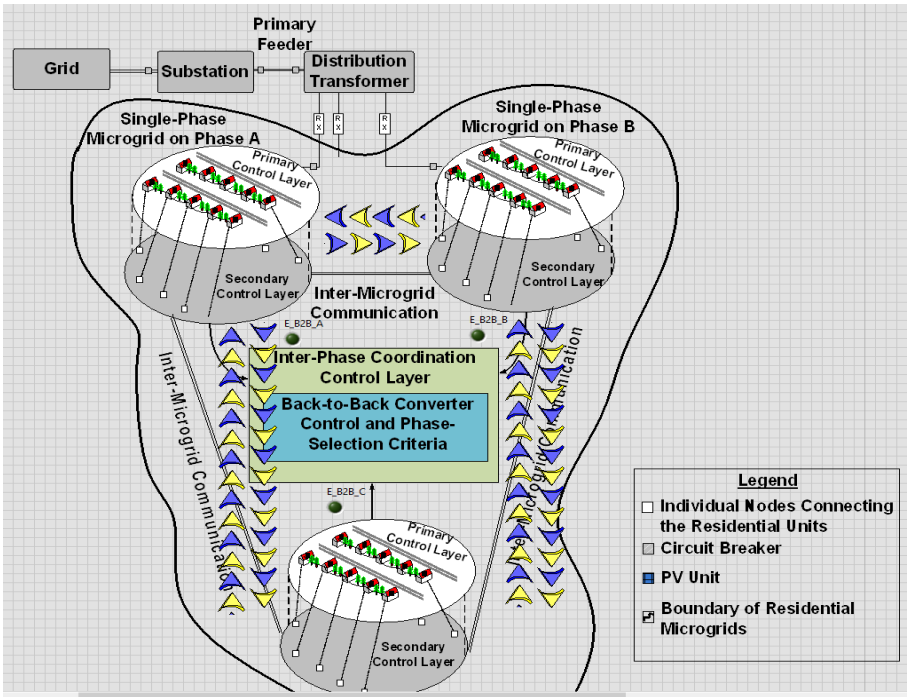


Figure 4.7: The structure used for LabVIEW simulation for intra-phase and inter-phase power management.

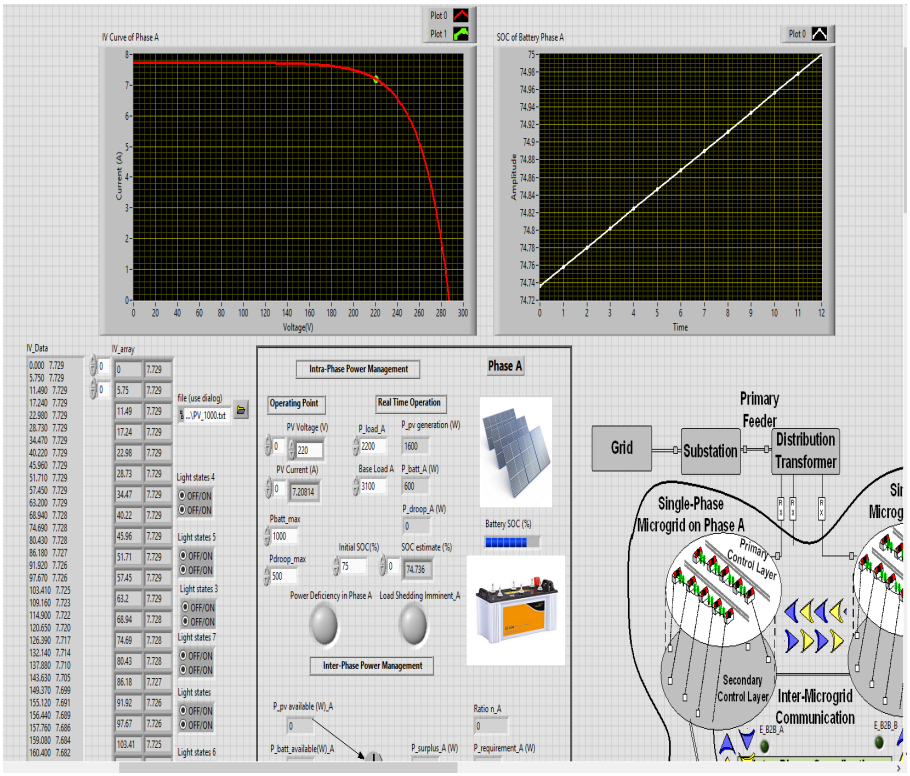


Figure 4.8: Visualizing the amount of power required from PV, battery and droop unit for intra-phase power management, while setting the operating points at the start of the simulation.

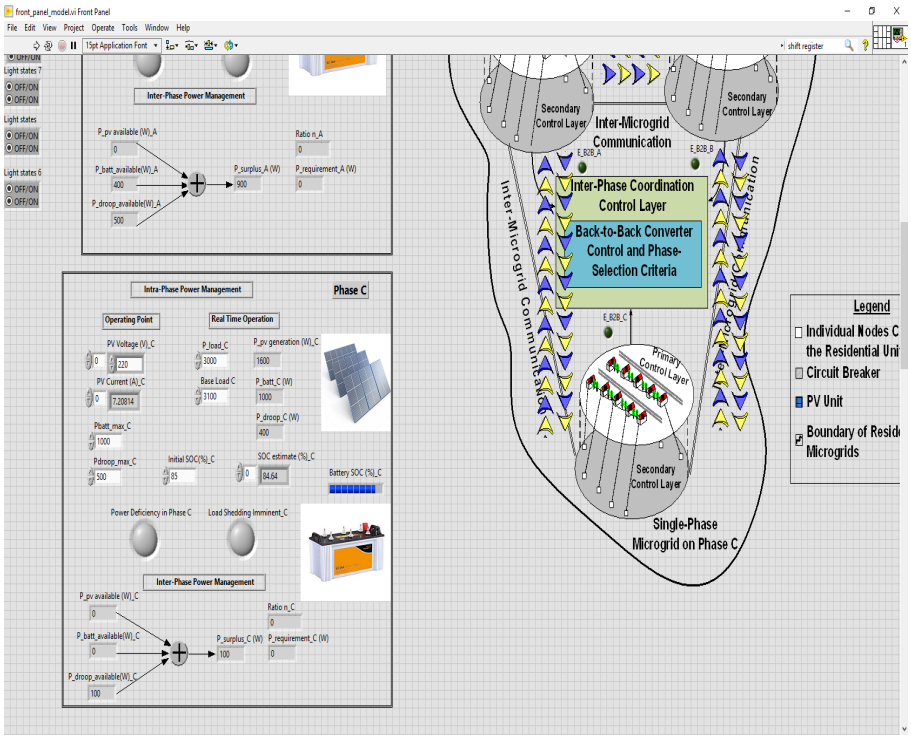


Figure 4.9: Power measurements for recording the surplus power available in each phase while inter-phase power management is taking place.

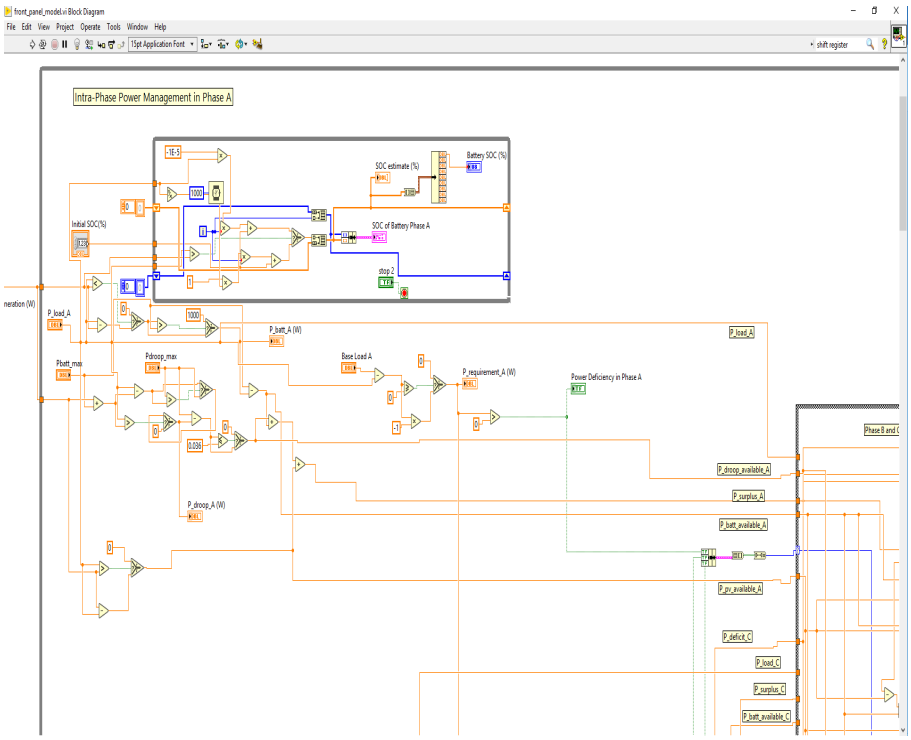


Figure 4.10: Snippet of intra-phase power management case.

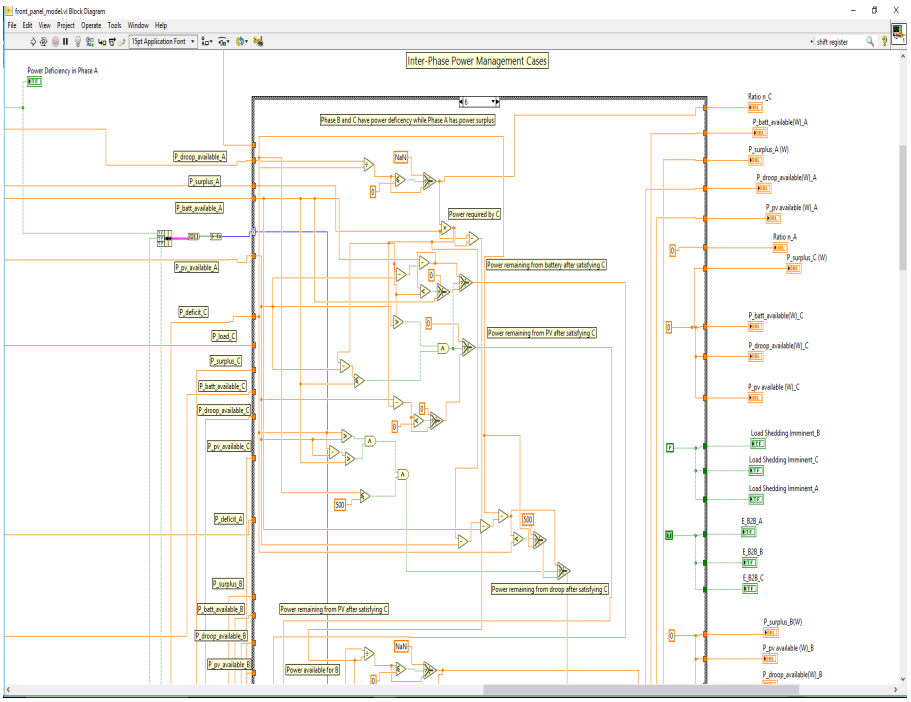


Figure 4.11: Snippet of a single inter-phase power management case.

4.7 Summary

To deal with phase balancing in the presence of single-phase generation and energy storage in residential microgrids, power transferred among different phases using back-to-back converters has been considered as one of the effective solutions. This chapter has systematically analyzed the fundamental relations behind this approach by establishing mathematical formulations for six potential operating scenarios. These formula have formed the basis to achieve dynamic balancing among three single-phase microgrids under various load and generation profiles to form a dynamically balanced three-phase system. It is believed that this is the first time that such relationships have explicitly been represented. Furthermore, a user-friendly interactive on-line tool kit has also been developed in LabVIEW, for interested readers to evaluate the power transfer requirements for their own system configurations and operating scenarios.

Chapter 5

Intra-Phase Power Management in Residential Microgrids

A power control and management strategy for islanded residential microgrids is presented in this chapter. Within each phase, there are PV systems, battery storage devices and droop controlled dispatchable units. Connections among phases are made through back-to-back converters to allow for power transfer between the phases. Hence, voltage and frequency control and power management must be carried out at intra-phase level, which is the main area of interest for this chapter. The intra-phase power control and management system uses a modified vector control with a multi-segment (P/f) droop strategy. To demonstrate the effectiveness of the strategy, a detailed three-phase residential microgrid model is developed in PSCAD/EMTDC environment. The results have shown that the proposed strategies can effectively maintain desired voltage and frequency profiles for each phase-wise and power balance in each phase can be effectively managed for stable operation.

5.1 Introduction

As previously discussed, single-phase residential microgrids call for new approaches to deal with power management within and between phases. An example of such configuration is illustrated in Fig.5.1, where the PV generation and battery storage are limited to individual phases with their respective loads. Without loss of generality, it is assumed that end consumers have rooftop PV systems and storage installed in their houses. There are sufficient number of such installations in each phase so that the phase can run as a single-phase microgrid.

The proposed architecture, as shown in in Fig.5.1, needs to address two issues for system's safety and reliability. This includes the *intra-phase power management*, where the proposed control strategy allows for power management within a phase. Finally, the *inter-phase power management*, where power exchange among phases takes place to achieve real-time dynamic phase balancing. For this chapter, the intra-phase power management strategy is discussed in detail.

With the proliferation of distributed energy resources, such as rooftop PVs [114] and high-power devices such as electric vehicles [145] at the customer's level, phase balancing has become an important issue for the local distribution companies. Balancing techniques for three-phase systems with unbalanced loads have been previously proposed in [136–142]. The topologies discussed therein, focus on active power filtering by injecting the harmonic current to compensate the non-linear loads at the DC link, with capacitor midpoint topology [137, 138], four-leg inverter topology [139, 140] or the three H-bridge inverter topology [141, 142]. The control strategies discussed in [136–142] can only deal with systems with a common DC link, in particular, with centralized PV generation and battery reserve. These techniques cannot be applied directly to residential microgrids, whereby each residential unit may have its own generation and storage. Some commercial products on phase balancing have started to appear. These include products for load balancing at data centers and at the distribution level [146,147]. However, these products

may not provide the flexibility required to cope with distributed energy resources causing phase imbalance at the residential level.

In single-phase microgrids, the control of converters through the typical 3-phase vector control schemes is infeasible. This is because of the absence of quadrature control variables [148]. The use of proportional resonant controller is proposed in [149, 150]. Through this control scheme, the odd harmonics are damped via cascaded compensator networks. Although this solution is capable of compensating for the lower order harmonics, but the additional cascaded networks makes the control strategy complex [151]. The single-phase converter's output current also needs to be controlled indirectly [152]. Hence, an effective control strategy needs to be developed for single-phase converters to achieve the required goals of power management under the proposed architecture.

For power management, a decentralized strategy for a single-phase microgrid is proposed in [153]. The coordination between the PV and battery units is based on a state-machine, where each state represents the operational condition of these units. A major drawback is the existence of chattering during load transitions. This can reduce the life of the power electronic components due to excessive heating generated. A more effective approach is to use droop control to manage PV production and battery charge/discharge automatically.

A droop control power management strategy for single-phase microgrid is introduced in [78]. In this scenario, any changes in the load demand results in the frequency and voltages references to be adjusted. The changes in ambient conditions and state-of-charge of the battery makes the proposed control strategy in [78] inapplicable for PV and battery units in residential microgrids. An improvement upon the conventional droop control through multi-segment droop strategy can provide an alternative solution to the problem. This will allow for residential loads to be supported by local generation and storage as well as other droop units, within a phase, to perform the desired intra-phase power management.

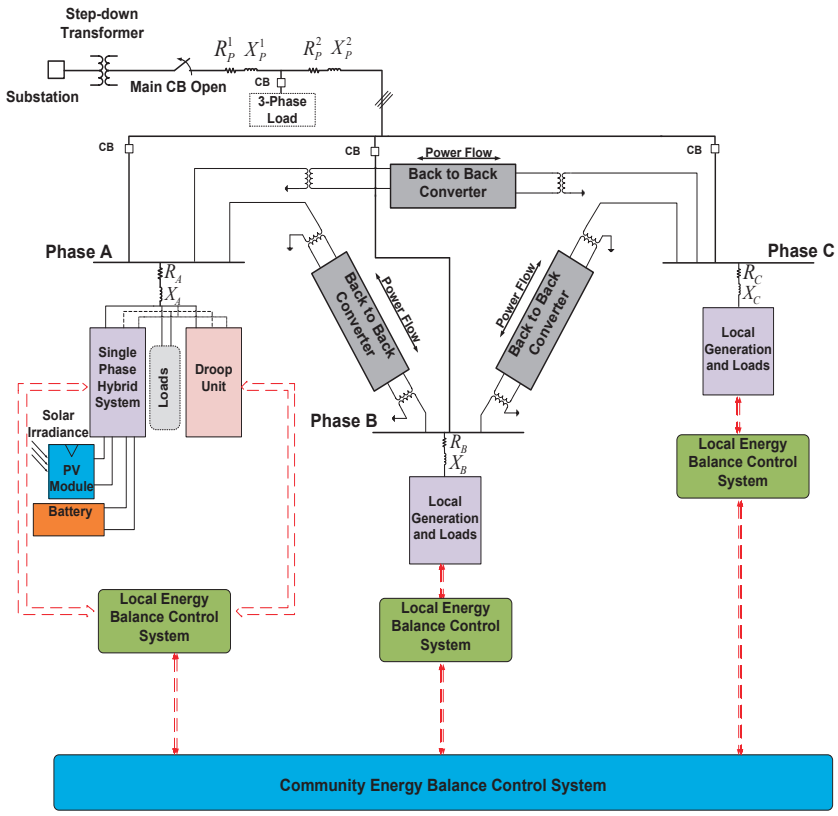


Figure 5.1: System architecture for residential microgrids with local DG units and inter-phase connection via back-to-back converters for power exchange.

Moreover, power management strategies for 3-phase systems have been studied in [35, 37, 71, 77, 143]. A control architecture to coordinate RES and energy storage for islanded microgrids is presented therein. Multi-segment droop control strategies are introduced to coordinate these DGs in [35, 37, 143]. The control strategies proposed therein are dependent upon the capacities of the DG units. Any further increase in load demand beyond the system capacity, will introduce forced load shedding which is undesirable in residential microgrids. The droop control strategies for batteries and RES in [71] is based on a look-up table to determine the droop coefficients. In order to avoid switching transients among system states, low-pass filters are used in the control loop. In [77], an autonomous active power management strategy is introduced for an islanded microgrid with a centralized battery reserve, operating as the master unit, and distributed PV systems, operating as slave units. The local controller for the battery is responsible for regulating the frequency at the PCC by using droop control based on the state of

charge of the battery. However, the control strategies implemented in both [71, 77] are unable to cater for scenarios when different RES and battery storage units are located in different phases. Within some phases, the local capacity may not be sufficient to support the load in their respective phases. In such cases, some loads may have to be shed.

A hierarchical coordination of an islanded single-phase community based microgrid is presented in [154]. The control strategy presented therein focuses on multiple microgrids, aggregated at a single bus. Power sharing is controlled based on the frequency deviation of the droop controlled DG units. This control strategy, therefore, can be used for situations where microgrids have dispatchable DG units. This ensures that a power requirement in the other microgrid(s) will be initially satisfied by sharing the power available among these DG units. The rest of the microgrids contribute only when the former reaches its rated generation capacity. In the case of residential microgrids, the decision criteria for power sharing will require both intra- and inter-phase coordination of DG units, supervised by the energy management systems (EMSs) at each phase. The network controller can use the information from each EMS to make decisions on the direction and the amount of the power transfer.

This chapter describes in detail the various aspects of DG units in terms of their modeling and the proposed modified vector control and improved multi-segment droop control strategies. The single-phase converters in these residential microgrids make use of a modified vector control approach, which effectively combines the advantages of 3-phase vector control for a single-phase system. The droop control strategy with a local EMS supervises the power management operation within each phase. This also ensures that the load and demand balance is maintained through the cooperative operation of PV and storage units. The interfacing converters for the PV and battery units are mathematically modeled and simulated in PSCAD/EMTDC with detailed switching models to test the efficacy of the proposed control strategies.

5.2 System Architecture and Objectives

The single-phase residential microgrids with its system architecture is shown in Fig.5.1. A single PV/battery hybrid unit is considered along with a droop unit in each phase. For simplicity, the details are shown explicitly for phase A only. The loads considered in this study are typical single-phase residential loads. The back-to-back converters are used in the architecture to connect the three phases. The details of which follow in Chapter 6. When the main 3-phase breakers at the substation are open, these residential microgrids are essentially operating in an islanded mode. However, such microgrids can reestablish connections to the grid when transitioning from an islanded to a grid-connected mode [155] with proper voltage, frequency phase sequence synchronization and closure of the breakers at the point of common coupling (PCC). It should be noted that it is not always realistic to consider using a pure single-phase network for the distribution network. This is because local schools, shopping and other community centers all require a 3-phase supply due to extensive use of three phase motor drives. This scenario is represented by the 3-phase load connected to the residential microgrids as shown in Fig.5.1.

In a grid-connected mode, the grid sets the voltage and frequency references for the rest of the system in Fig.5.1 [156]. While in an islanded mode, the voltage and frequency of each microgrid have to be controlled either through master-slave or multi-master topologies [157]. This results in each microgrid operating at its own respective voltage and frequency. Of course, a re-synchronization step has to be initiated to ensure all three single-phase microgrids are operating at the rated voltage and frequency, and with the appropriate phase sequence, before the onset of reconnection [158].

The advantage for such residential microgrids may be evident, where under an outage; the power available in one phase could be significantly higher than that in other phases. This could occur for several reasons, which include the alignment of the PV units where some of them may get affected by shading effects from the surroundings, or storage

unit(s) operating near threshold boundaries, or the DG units having reached their power capacity limits [37, 144].

In a practical system, one may have other issues to consider, such as billing concerns and customers' priority issues during power sharing. These administrative issues can be handled through a local energy balance control system in the form of agreed regulations for a specific installation. They are not real-time operational issues, and are hence not discussed in this paper.

In Fig.5.1, R_p^1, X_p^1, R_p^2 and X_p^2 are the resistances and reactances of the primary feeder. R_A, R_B and R_C are the per phase cable resistances while X_A, X_B and X_C are the per phase cable reactances and are chosen to match a typical North American distribution system [127]. Each phase also consists of its own local energy balance control system, which manages the phase generation from PV and battery storage units. This system can communicate with other phases through the community energy balance control system. The local energy balance control system relays the operating information about that particular phase to the community energy balance control system for inter-phase coordination.

Following the discussion in previous sections, the functionalities of the proposed intra-phase power management strategy can be stated as:

1. At a per-phase level, if the combined capability of the hybrid PV/battery and the droop units is sufficient to meet the local load demand, the load will be self-supported within its phase. As such, each phase operates virtually independently. There is minimal intervention by the network controller.

2. The voltage and frequency in each phase are maintained within the safety limits based on specific operating conditions in that phase.

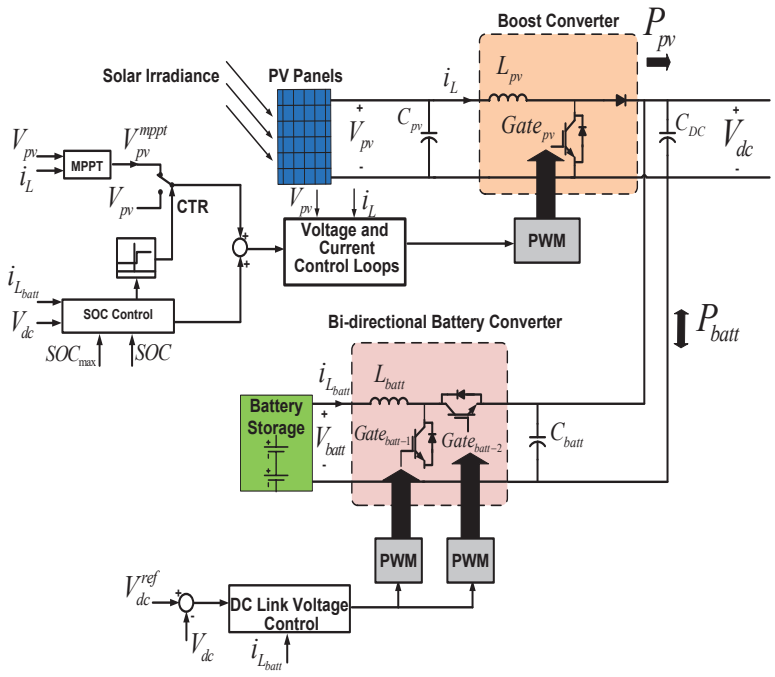


Figure 5.2: PV and battery hybrid architecture for residential microgrids with local stage-wise controllers.

5.3 Mathematical Modeling and Control of Converters

In order to achieve the objectives as listed in the previous section, the initial steps require mathematical models and designing of controllers for the DG units and their converters. The system architecture for residential microgrids as introduced in Chapters 3 and 4 consist of a hybrid PV/battery system, located at a customer's house. This is shown in Fig.5.2. For this chapter, the PV system, its boost converter, battery and its bi-directional converter is modeled in detail along with their respective control stages. This is followed up by a brief description of the droop unit, single-phase inverter and their control strategies that are used in the modeling stage for a particular phase.

5.3.1 Modeling of PV system

Ideally, photovoltaic arrays can be considered as current sources in parallel with one or two diodes [31, 144, 159]. A PV module consists of series and parallel arrays of semi-

conductor based cells with the output current from the arrays dependent on the photovoltaic current, I_{ph}, saturation current of the diode, I_{sd} and series and parallel resistances, R_s and R_{sh} in these arrays given by the following equation:

$$I_{pv} = I_{ph} - I_{sd}\left(exp\left(\frac{q\left(V_{oc} + IR_s\right)}{AkT}\right) - 1\right) - \frac{V_{oc} + IR_s}{R_{sh}} \tag{5.1}$$

where, q is the electron charge, k is the Boltzmann's constant, A is the diode quality factor, T is the temperature (°K) and V_{oc} is the open circuit voltage. The photovoltaic current, I_{ph} is given by,

$$I_{ph} = \frac{Ir}{Ir_n} I_{ph_n}\left(1 + k\left(T - T_0\right)\right) \tag{5.2}$$

where, Ir is the irradiance (W/m^2), Ir_n, T_0 and Ir_n are the irradiance, temperature and photovoltaic current in standard test conditions (STC). The saturation current of diode is then given by,

$$I_{sd} = I_{sd_0}\left(\frac{T}{T_0}\right)^3 exp\left(\frac{qE_g}{Ak}\left(\frac{1}{T_0} - \frac{1}{T}\right)\right) \tag{5.3}$$

where, I_{sd_0} is the saturation current under STC and E_g is the band gap energy. Finally R_s and R_{sh} in (5.1) is given by,

$$\begin{aligned} R_s &= C_1 + \frac{C_2}{Irr} + C_3 T \\ R_{sh} &= R_{sh_0} exp\left(-C_4 T\right) \end{aligned} \tag{5.4}$$

where $C_1 - C_4$ are constants and R_{sh_0} is the nominal shunt resistance under STC. The MPPT controller as shown in Fig.5.2, uses the well known perturb and observe methodology. This allows the PV unit deliver maximum power available based on the atmospheric conditions. The variation of PV power against voltage at various irradiance levels is shown in Fig.5.3, while the PV current variation with respect to voltage is shown in Fig.5.4.

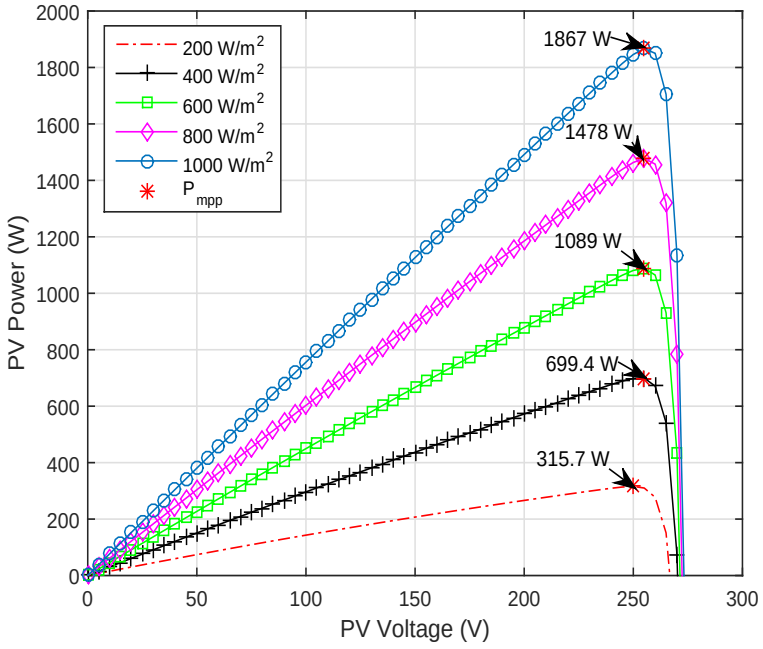


Figure 5.3: PV power against voltage variation for a PV unit at various irradiance levels.

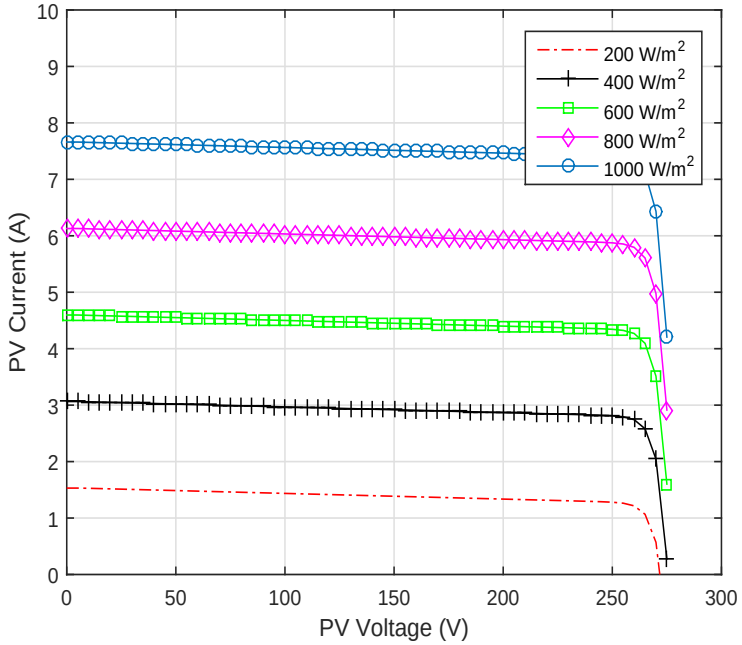


Figure 5.4: PV current against voltage variation for a PV unit at various irradiance levels.

5.3.2 Modeling of PV boost converter

The boost converter is used for the PV unit, as shown in Fig.5.2. Considering the average model, the 'On' and 'Off' state equations in terms of system components, inductor

current, input and output voltages are derived in this section. In the 'On' state, the system equation can be written as,

$$\begin{aligned} L_{PV}\frac{d\bar{i_L}}{dt} &= V_{PV} \\ C_{DC}\frac{d\bar{v_0}}{dt} &= -\frac{\bar{v_0}(t)}{R} \end{aligned} \tag{5.5}$$

where, L_{PV} is the converter inductance, C_{DC} is the output capacitance, i_L is the inductor current, V_{PV} is the voltage across C_{PV}, v_0 is the output voltage across C_{DC} and R is the effective load which is experienced by the boost converter. The averaged terms are represented by $^-$. In the 'Off' state, the system can be represented as,

$$\begin{aligned} L_{PV}\frac{d\bar{i_L}}{dt} &= V_{PV} - \bar{v_0}(t) = \bar{v_L} \\ C_{DC}\frac{d\bar{v_0}}{dt} &= \bar{i_L}(t) - \frac{\bar{v_0}(t)}{R} \end{aligned} \tag{5.6}$$

where, $\bar{v_L}$, is the average voltage across the inductor, L_{PV}. Taking the average of $v_L(t)$ over Ts gives,

$$\begin{aligned} \bar{v}_L(t) &= \frac{1}{T_s}\int_t^{t+T_s} v_L(\tau)d\tau \\ &= \frac{1}{T_s}\left[dT_s\left(V_i\right) + \left(1-d\right)T_s\left(V_{PV} - \bar{v}_0\right)\right] \\ &= dV_i + \left(1-d\right)\left(V_{PV} - \bar{v}_0\right) \end{aligned} \tag{5.7}$$

where d is the duty cycle of the converter and T_s is the time period. The above equation can be simplified to,

$$L_{PV}\frac{di_L}{dt} = v_L(t) = V_{PV} - \left(1-d\right)v_0 \tag{5.8}$$

The output capacitor current i_C can now be written by taking the average of $i_C(t)$ over

T_s gives,

$$\begin{aligned}\bar{i}_C(t) &= \frac{1}{T_s}\int_t^{t+T_s} i_C(\tau)d\tau \\ &= \frac{1}{T_s}\left[dT_s\left(-\frac{v_0}{R}\right) + (1-d)\,T_s\left(\bar{i}_L - \frac{\bar{v}_0}{R}\right)\right] \\ &= -d\frac{\bar{v}_0}{R} + (1-d)\left(\bar{i}_L - \frac{\bar{v}_0}{R}\right)\end{aligned} \tag{5.9}$$

The above equation can be simplified to,

$$C\frac{dv_0}{dt} = i_c(t) = (1-d)\,i_L - \frac{v_0}{R} \tag{5.10}$$

Making use of dynamic resistance of PV array in the current and voltage source regions, (5.8) and (5.10) can be written in their linearized form to form a state space representation as shown in (5.11).

$$\begin{aligned}\begin{bmatrix}\dot{\hat{i}}_L \\ \dot{\hat{v}}_{pv}\end{bmatrix} &= \begin{bmatrix}0 & \frac{1}{L} \\ -\frac{1}{C} & \frac{1}{r_{pv}C}\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_{pv}\end{bmatrix} + \begin{bmatrix}-\frac{V_{dc}}{L} \\ 0\end{bmatrix}\hat{d} \\ y &= \begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_{pv}\end{bmatrix}\end{aligned} \tag{5.11}$$

where, $\hat{i}_L$ and $\hat{v}_{pv}$ are the linearized components of the inductor current and input PV voltage, perturbed around the operating point and $v_0 = V_{dc}$. Taking Laplace transform of (5.11),

$$\begin{aligned}s\hat{i}_L(s) &= \frac{1}{L}\hat{v}_{pv}(s) + \frac{V_{dc}}{L}\hat{d}(s) \\ s\hat{v}_{pv}(s) &= -\frac{1}{C}\hat{i}_L(s) + \frac{1}{r_{pv}C}\hat{v}_{pv}(s)\end{aligned} \tag{5.12}$$

With the duty cycle, $\hat{d}(s)$ as input and inductor current, $\hat{i}_L(s)$ as output, the inner

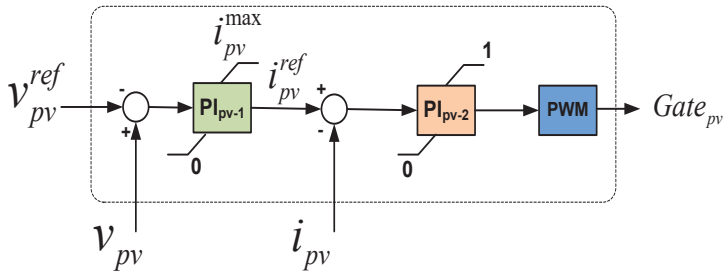


Figure 5.5: PV boost converter control strategy

current control loop transfer function can be derived as,

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{(sr_{pv}C - 1)\,V_{dc}}{s^2 L r_{pv} C - sL + r_{pv}} \tag{5.13}$$

With the inductor current, $\hat{i}_L(s)$ as input and PV voltage, $\hat{v}_{pv}(s)$ as the output, the voltage control loop transfer function can be derived as,

$$\frac{\hat{v}_{pv}(s)}{\hat{i}_L(s)} = -\frac{r_{pv}}{sr_{pv}C - 1} \tag{5.14}$$

The combined feed-forward gain from (5.13) and (5.14) will be simply the multiplication of the two transfer functions,

$$\frac{\hat{v}_{pv}(s)}{\hat{d}(s)} = \frac{\hat{v}_{pv}(s)}{\hat{i}_L(s)} \times \frac{\hat{i}_L(s)}{\hat{d}(s)} \tag{5.15}$$

The overall structure with PI controls for both the voltage and current loops are shown in Fig.5.5. The designing of the PI controller will be performed using the frequency response of the system. The open loop frequency response of the system without PI controller is shown in Fig.5.6. With low gain and phase margins, this system will have significant overshoots and steady state error.

The PI controllers are chosen as,

$$G_{PI_{pv-1}}(s) = \frac{0.5s + 250}{s} \tag{5.16}$$

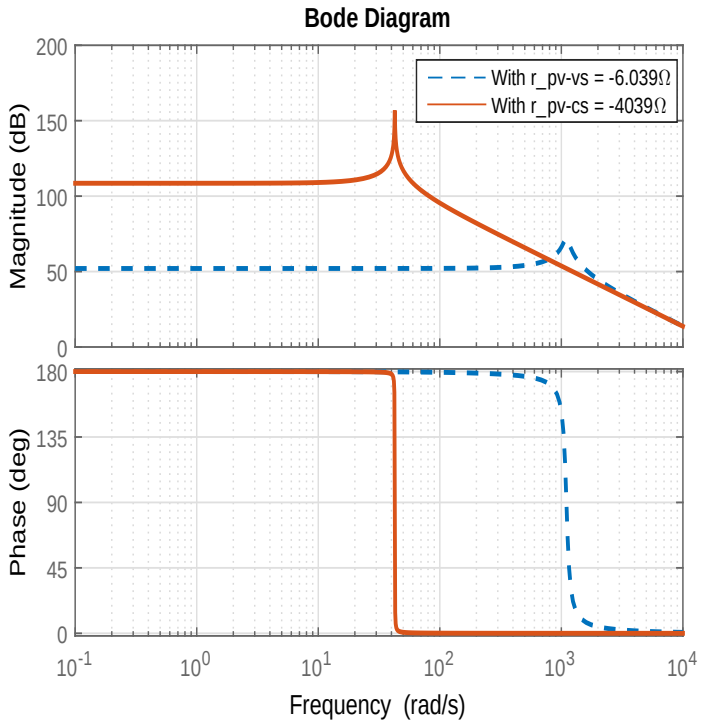


Figure 5.6: Open loop frequency response without PI controller for boost converter

$$G_{PI_{pv-2}}(s) = \frac{0.01s + 50}{s} \tag{5.17}$$

The PI controllers have been tested for stability with extrema of dynamic resistances using the open loop frequency response. Using the two extremities of resistances i.e. using r_{pv-cs} (dynamic resistance in the current source region) and r_{pv-vs} (dynamic resistance in the voltage source region), the gain and phase margin only vary slightly. This is shown in Fig.5.6. This illustrates the robustness of the controller against large changes in r_{pv}. The root locus for both the open and closed loop system is shown in Fig.5.8.

With these controllers in the voltage and current loops, the step response of the system is studied with and without the controllers. This is shown in Fig.5.7. From the figure the characteristics of frequency response are validated. Without the control stage, the system has high overshoots and steady state error and is unable to reach the v_{dc}^{ref}. With PI controller stage as stated in (5.16) and (5.19), the boost converter control scheme, works as an under-damped system, with minimum overshoot and least settling time.

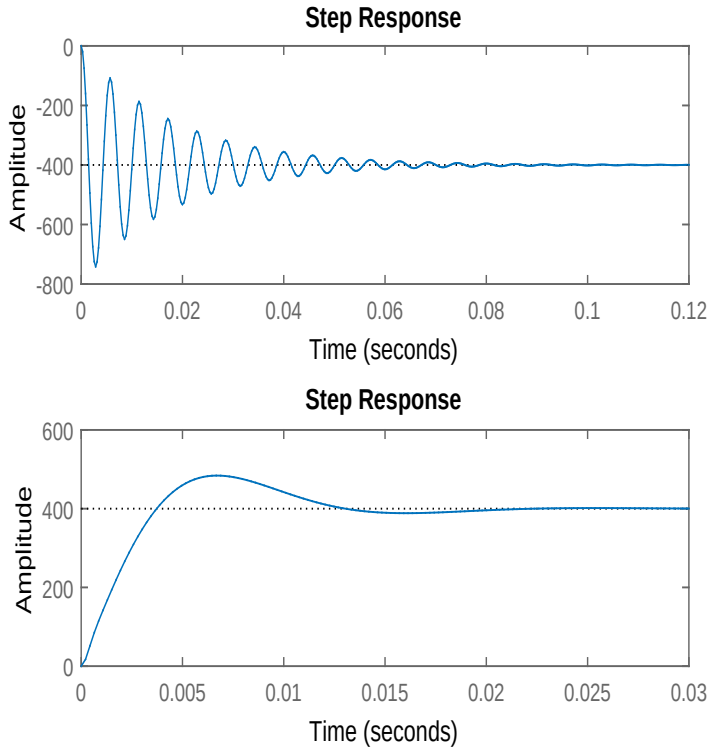


Figure 5.7: Step response of system with and without PI controller for the boost converter

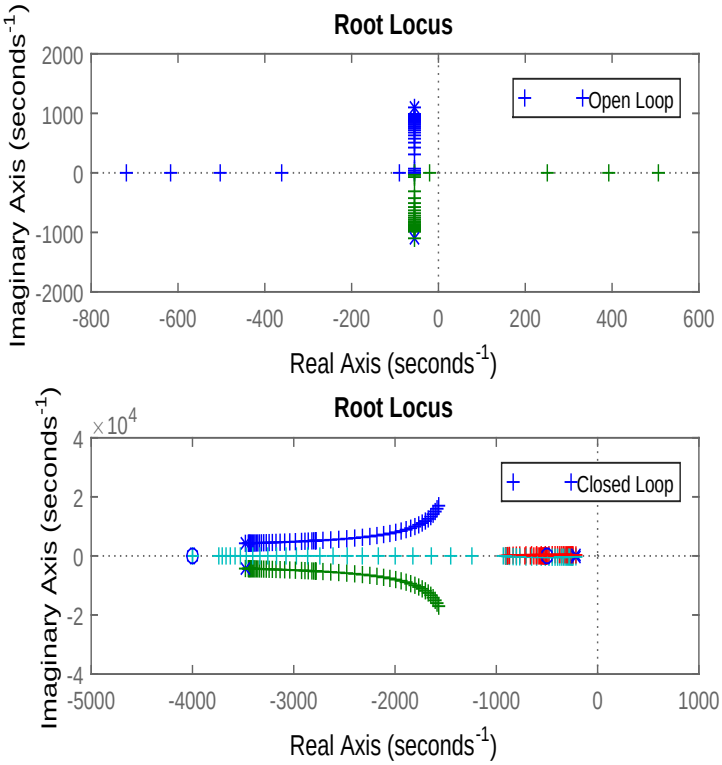


Figure 5.8: Root locus for open and closed loop boost converter

5.3.3 Modeling of bi-directional battery converter

The bi-directional converters are used for the to and fro power flow of the battery; in this case through the charging and discharging states of the battery. For the boost mode, the lower gate and the higher end transistor's body diode will be conducting. This is represented by,

$$L_{batt}\dot{i_{L_{batt}}} = V_{batt} \tag{5.18}$$

where L_{batt} is the converter inductance, $i_{L_{batt}}$ is the inductor current and V_{batt} is the input battery voltage. When the lower gate is in 'Off' state and the higher end transistor is also conducting, the system equation can be represented as,

$$L_{batt}\dot{i_{L_{batt}}} = V_{batt} - V_{dc} \tag{5.19}$$

where V_{dc} is the output voltage across C_{DC}. Taking the average of voltage across the inductor; $v_L(t)$ over T_s gives,

$$\begin{aligned} \bar{v}_{L_{batt}}(t) &= \frac{1}{T_s}\int_t^{t+T_s} \bar{v}_{L_{batt}}(\tau)d\tau \\ &= \frac{1}{T_s}\left[dT_s\left(\bar{v}_{batt}\right) + (1-d)\,T_s\left(\bar{v}_{batt} - \bar{v}_{dc}\right)\right] \\ &= \bar{v}_{batt} - (1-d)\bar{v}_{dc} \end{aligned} \tag{5.20}$$

where $^-$ represents the average of the states. This is simplified as,

$$L\frac{di_L}{dt} = v_L(t) = \bar{v}_{batt} - (1-d)\bar{v}_{dc} \tag{5.21}$$

Linearizing (5.21),

$$\begin{aligned} L_{batt}\left(\dot{i_{L_{batt}}} + \Delta\dot{i_{L_{batt}}}\right) = &(v_{batt} + \Delta v_{batt}) - (1 - (d + \Delta d))\cdot \\ &(v_{dc} + \Delta v_{dc}) \end{aligned} \tag{5.22}$$

This gives,

$$L_{batt}\Delta\dot{i_{L_{batt}}} = -(1-D)\Delta v_{dc} + dV_{dc} \tag{5.23}$$

When the lower IGBT is 'On', the system is represented as,

$$C_{batt}\frac{dv_{CB}}{dt} = -\frac{V_{dc}}{R} \tag{5.24}$$

where C_{batt} is the output capacitance of the bi-directional converter, v_{CB} is the output voltage across the capacitor and R is the seen impedance of the inverter. When lower IGBT is 'Off', the system is represented as,

$$C_{batt}\frac{dv_{CB}}{dt} = i_{L_{batt}} - \frac{V_{dc}}{R} \tag{5.25}$$

Taking the average of $i_{CB}(t)$ over T_s gives,

$$\begin{aligned}\bar{i}_{CB}(t) &= \frac{1}{T_s}\int_t^{t+T_s} i_{CB}(\tau)d\tau \\ &= \frac{1}{T_s}\left[dT_s\left(-\frac{v_{dc}}{R}\right) + (1-d)\,T_s\left(\bar{i}_{L_{batt}} - \frac{\bar{v}_{dc}}{R}\right)\right] \\ &= -d\frac{\bar{v}_{dc}}{R} + (1-d)\left(\bar{i}_{L_{batt}} - \frac{\bar{v}_{dc}}{R}\right)\end{aligned} \tag{5.26}$$

Simplifying the above equation gives,

$$C_{batt}\frac{dv_{0B}}{dt} = i_{CB}(t) = (1-d)\,i_{L_{batt}} - \frac{v_0}{R} \tag{5.27}$$

where v_{0B} is the output voltage across the capacitance. Linearizing (5.27) gives,

$$C\Delta\dot{v_{dc}} = (1-D)\Delta i_{L_{batt}} - \frac{v_{dc}}{R} - dI_{L_{batt}} \tag{5.28}$$

Here C is a parallel combination of C_{batt} and C_{DC} i.e. $C = C_{batt} + C_{DC}$. Forming the state-space from (5.23) and (5.28) gives,

$$\begin{bmatrix} \dot{\hat{i}}_{L_{batt}} \\ \dot{\hat{v}}_{dc} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{dc} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{L} \\ -\frac{I_L}{C} \end{bmatrix} \hat{d}$$
$$y = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{dc} \end{bmatrix} \tag{5.29}$$

Taking Laplace transform of (5.29),

$$\begin{aligned} s\hat{i}_{L_{batt}}(s) &= -\frac{(1-D)}{L_{batt}}\hat{v}_{dc}(s) + \frac{V_{dc}}{L_{batt}}\hat{d}(s) \\ s\hat{v}_{dc}(s) &= \frac{(1-D)}{C}\hat{i}_{L_{batt}}(s) - \frac{1}{RC}\hat{v}_{dc}(s) - \frac{I_{L_{batt}}}{C}\hat{d}(s) \end{aligned} \tag{5.30}$$

With $\hat{d}(s)$ as input and the battery's inductor current, $\hat{i}_L(s)$ as output, the inner current control loop transfer function can be derived as,

$$\frac{\hat{i}_{L_{batt}}(s)}{\hat{d}(s)} = \frac{sRCV_{dc} + [(1-D)I_{L_{batt}}R + V_{dc}]}{s^2 L_{batt}RC + sL_{batt} + R(1-D)^2} \tag{5.31}$$

With $\hat{i}_L(s)$ as input and battery's voltage, $\hat{v}_{dc}(s)$, as output, the transfer function can be derived as,

$$\frac{\hat{v}_{dc}(s)}{\hat{i}_{L_{batt}}(s)} = \frac{-sRLI_{L_{batt}} + V_{dc}R(1-D)}{sRCV_{dc} + [V_{dc} + R(1-D)I_{L_{batt}}]} \tag{5.32}$$

The combined feed-forward gain from (5.31) and (5.32) will be simply the multiplication of the two transfer functions and is given by,

$$\frac{\hat{v}_{dc}(s)}{\hat{d}(s)} = \frac{\hat{v}_{dc}(s)}{\hat{i}_{L_{batt}}(s)} \times \frac{\hat{i}_{L_{batt}}(s)}{\hat{d}(s)} \tag{5.33}$$

The PI controllers are chosen as,

$$G_{PI_{batt-1}}(s) = \frac{1s + 250}{s} \tag{5.34}$$

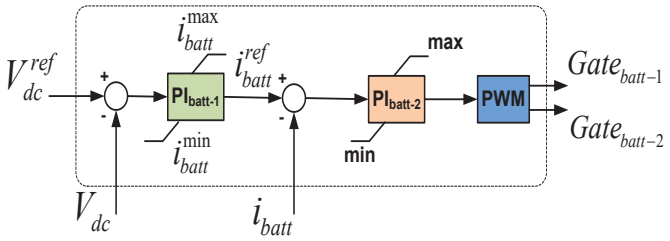


Figure 5.9: Control strategy for bi-directional battery converter.

$$G_{PI_{batt-2}}(s) = \frac{0.03s + 30}{s} \tag{5.35}$$

The overall control strategy for the bi-directional battery converter is shown in Fig.5.9, with the appropriate references for both the inner and outer control loops. The response of the system with and without the PI controller is shown in Fig.5.10. It can be seen that without controller the system becomes unbounded. While with the controller, the system has minimum overshoot with least settling time. The PI controller design is performed through the frequency response from the open and closed loop of the system. With sufficient gain and phase margin, the controller performs satisfactorily. This is shown in Fig.5.11. The root locus for both the open and closed loop system is shown in Fig.5.12.

By making use of the control strategies for both the PV and battery system, and other system details including the DC link voltage, state-of-charge (SOC) of the battery and the operating point of the PV system, the overall contribution of PV and battery power, denoted as P_{pv} and P_{batt} in Fig.5.2, can be adjusted. The outer control loops shown in Fig.5.2, make sure that the PV system is always operating at the maximum power using the MPPT controller. Furthermore, the SOC control block assures that the battery's state-of-charge remains within the range $SOC_{min} < SOC < SOC_{max}$. The reason to incorporate this control block is to either avoid overcharging of the battery when SOC is close to SOC_{max} or avoid deep discharge of the battery when SOC is near the lower threshold of SOC_{min}.

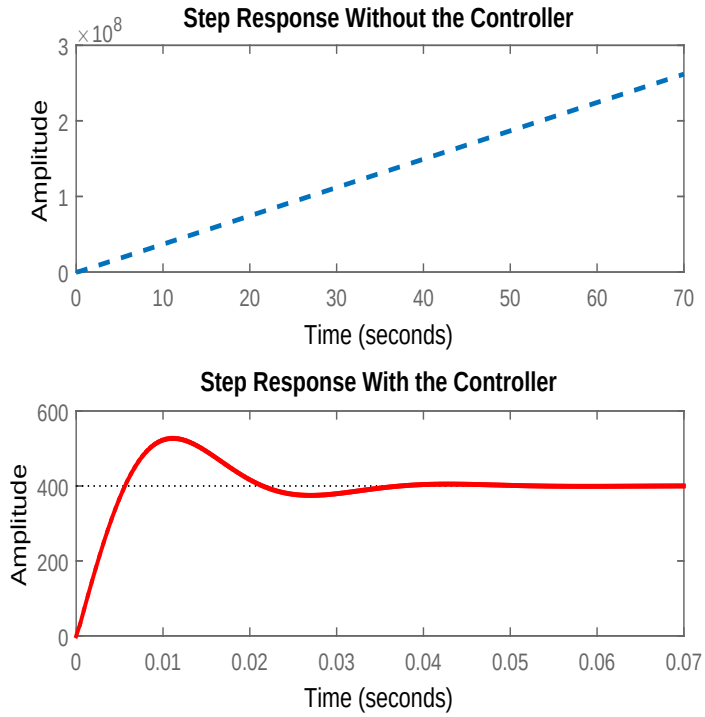


Figure 5.10: Step response of system with and without controller for buck-boost converter

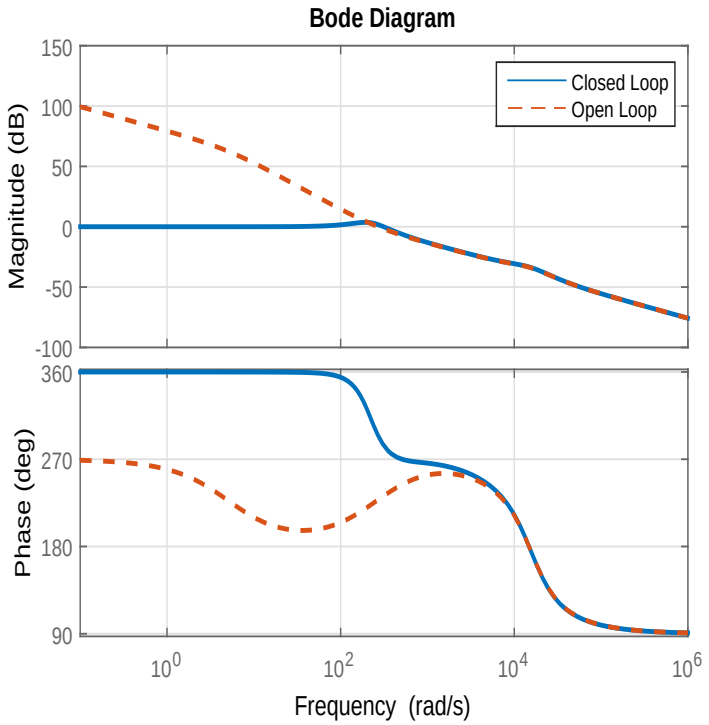


Figure 5.11: Open and closed loop bode plot for buck-boost converter with gain and phase margins

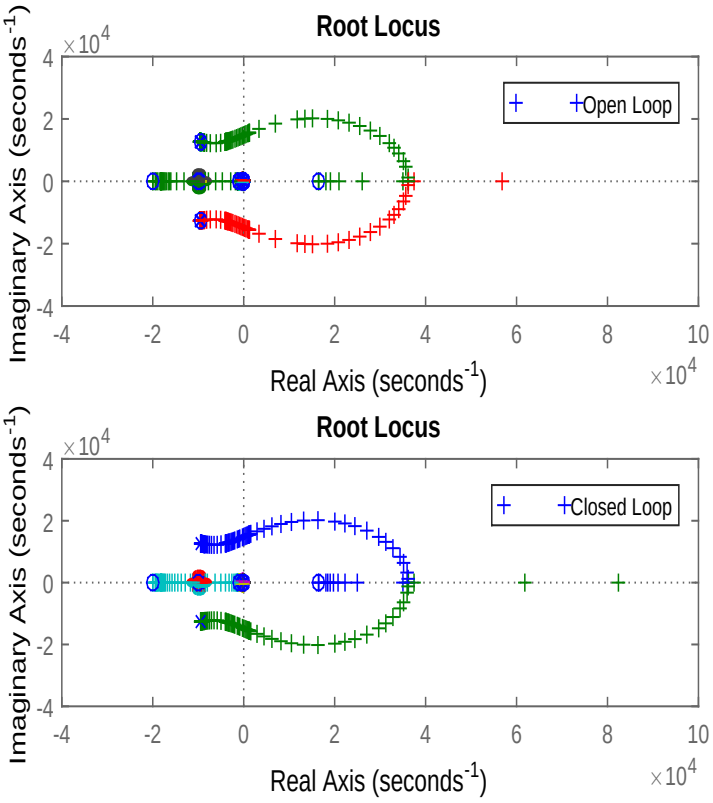


Figure 5.12: Root locus for open and closed loop buck-boost converter

5.3.4 CIEMAT battery model

The CIEMAT chemical model of a lead acid battery is used in this work [160], whereby the charging model is given by,

$$V_{B-C}(t) = [2 - 0.16SOC(t)] + \frac{i_B(t)}{C_B}\Big(\frac{6}{1 + i_B(t)^{0.86}} + \frac{0.48}{(1 - SOC(t))^{1.2}} + 0.036\Big) \times (1 - 0.025\Delta T) \tag{5.36}$$

where, C_B, i_B and V_{B-C} are the capacity, charging current, and voltage of the battery respectively. The SOC is calculated using,

$$SOC(t) = \frac{1}{C_B \times 3600}\left[\int_0^{\tau} i_B(t)\ dt\right] \times 100\% \tag{5.37}$$

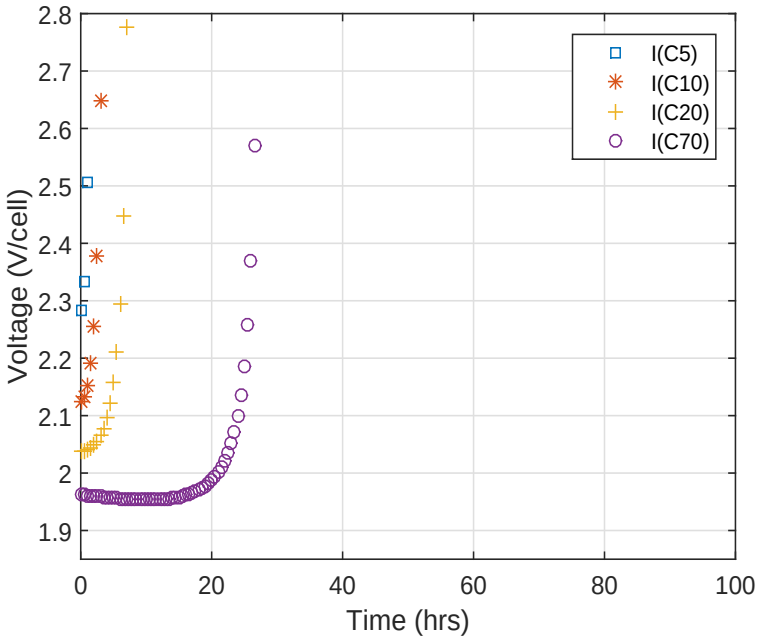


Figure 5.13: Charge cycle for various capacities of lead acid battery using the CIEMAT model.

where, τ is the time constant. The discharge cycle of battery is given by,

$$V_{B-D}(t) = [2.085 - 0.12(1 - SOC(t))] - \frac{i_B(t)}{C_B}\Big(\frac{4}{1 + i_B(t)^{1.3}} + \frac{0.27}{SOC(t)^{1.5}} + 0.02\Big) \times (1 - 0.007\Delta T) \tag{5.38}$$

where, V_{B-D} is the battery's discharging voltage.

The charge and discharge cycles of various capacities of lead acid batteries using the CIEMAT model are shown in Figures 5.13 and 5.14.

5.3.5 Modeling of droop unit

The droop unit used for the simulation is a typical inverter based source that is capable of delivering power to the local loads when the PV and battery system is unable to. This is because the limit of maximum power that can be delivered from these sources has been reached. The system architecture with the droop unit is shown in Fig.5.15. It is considered as a back-up resource for the local loads, when the residential microgrids are

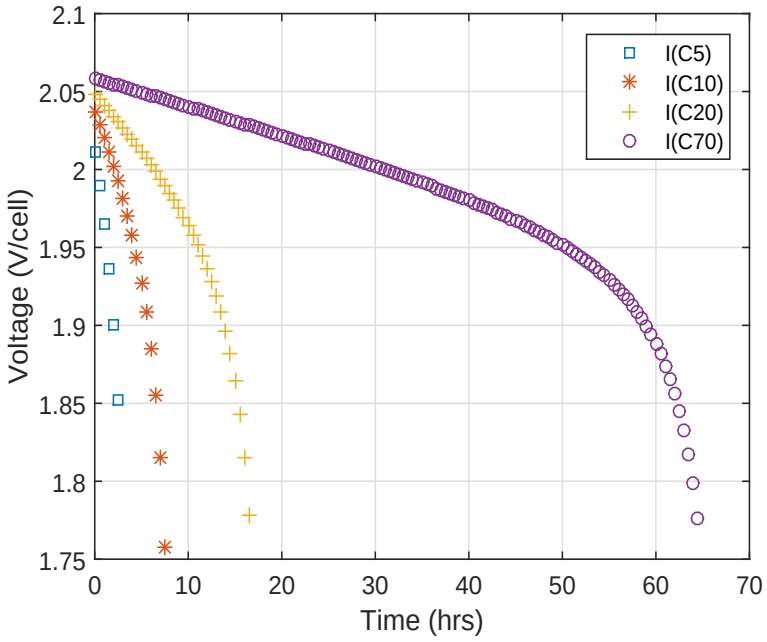


Figure 5.14: Discharge cycle for various capacities of lead acid battery using the CIEMAT model.

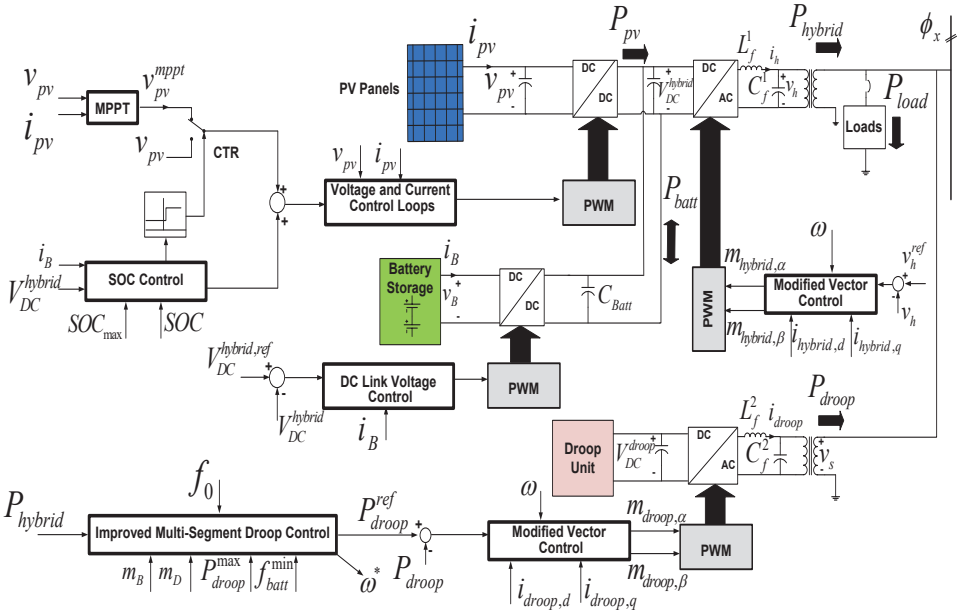


Figure 5.15: Phase-wise DG units along with their respective controllers.

operating in an islanded mode. The combination of hybrid PV/battery system and droop unit form one complete single-phase residential microgrid in a phase, which is represented by ϕ_x in Fig.5.15. The coordination of DG units in this configuration is undertaken by the improved multi-segment droop control strategy which is shown in Fig.5.16.

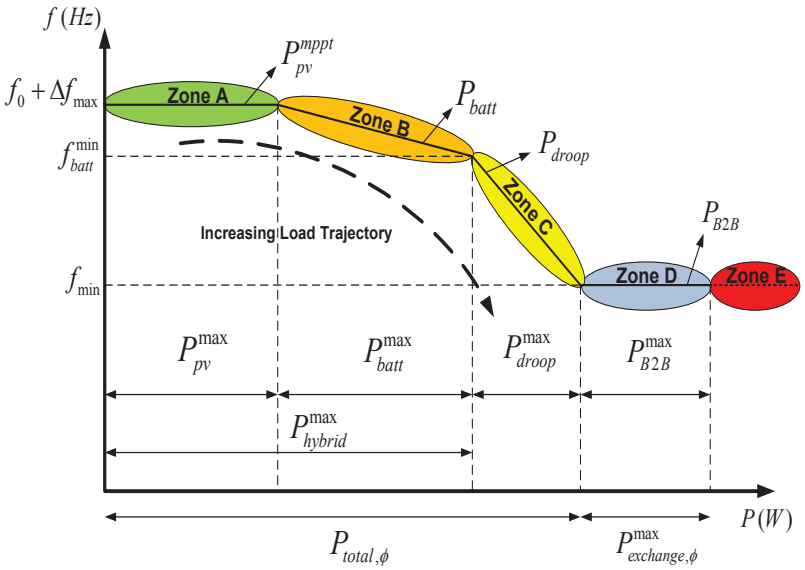


Figure 5.16: The improved multi-segment droop control strategy with its P/f characteristics for different power sources.

The droop strategy is based on the previous works in the literature [35, 37, 68, 143]. The term 'improved' is added to coordinate the transfer of power between phases using these DG units through back-to-back converters, which is discussed in Chapter 6. The multi-segment droop control strategy allows for frequency regulation in ϕ_x by monitoring the phase frequency. This results in proper coordination of PV/battery with droop units under various operating conditions, the status of the battery and the capacities of the DG units. Zone A represents the region where the PV unit is supplying maximum power till its capacity is reached. Beyond this region, the battery takes over to supply power to the local loads. The system therefore enters Zone B and remains in this particular zone until minimum frequency for the hybrid unit is reached. This is represented by f_{batt}^{min} in Fig.5.16. At this point, the battery is supplying its maximum power, P_{batt}^{max}. Once the power capacity of the hybrid PV/battery system is reached, the droop unit is activated to transfer the deficit power to the local loads. This is represented by Zone C in Fig.5.16. Maximum droop power, P_{droop}^{max}, corresponds to the minimum frequency for that phase, f_{batt}^{min}. Beyond this region, the system cannot support local loads and will require assistance from other phases. The control structure for the strategy is shown in

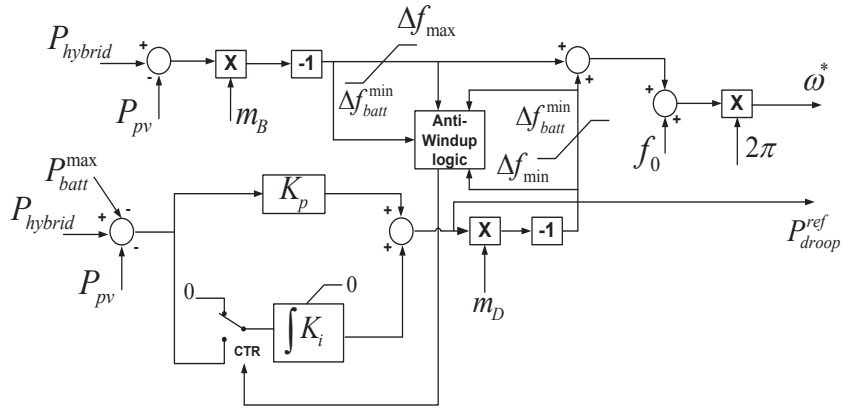


Figure 5.17: The proposed intra-phase power management strategy with multi-segment droop control.

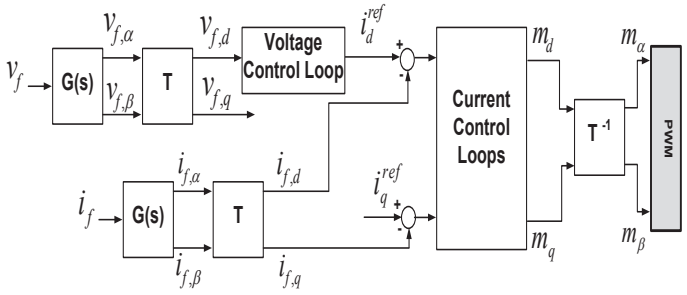


Figure 5.18: Modified vector control for a single-phase converter.

Fig.5.17. The anti-windup logic utilized in this structure allows the maintain appropriate frequency for the phase by receiving information of the power contributions from PV, battery and droop units.

5.3.6 Control of single-phase inverter

The DG units and their controllers as described in the previous sections, are then connected to a single-phase inverter. This then connects to the main phase bus bar. The control of a single-phase inverter is not trivial as compared to normal three-phase inverters. The control of single-phase inverter must insure that the voltage and frequency is maintained at the reference levels, while operating the residential microgrid in islanded mode. This is achieved after receiving system information from the various DG units. For this purpose a modified vector control strategy is proposed, which is described next.

5.3.7 Modified vector control strategy

For a typical three-phase system, the implementation of vector control makes use of the inherent presence of orthogonal components for AC voltages and currents. It uses conventional PI controllers in the voltage and current control loops, which is relatively easier to implement over the PR controller for three-phase systems. However, in single-phase circuits, the presence of only real components, causes the orthogonal components are to be generated. The proposed solution is to use a pre-filter stage, which is a modification over the conventional vector control for three-phase systems. It is referred here as the modified vector control and is shown in Fig.5.18, i_f and v_f are the converter's output voltage and current. The transfer function of the filter, $G(s)$ is given by,

$$G(s) = \frac{-s + \omega_0}{s + \omega_0} \tag{5.39}$$

where, ω_0 is the system's nominal frequency in rad/s. The filter characteristics include its unity gain and 90° phase shift of the real components. The quadrature components are then evaluated through this strategy to form the $\alpha - \beta$ frames for single-phase systems. The reference frames can be interchanged between $\alpha - \beta$ and $d - q$ by using (2) [161]. For a conventional three-phase system, there is no requirement for this pre-filtering stage.

$$\begin{bmatrix} d \\ q \end{bmatrix} = T \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \Leftrightarrow \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = T^{-1} \begin{bmatrix} d \\ q \end{bmatrix} \tag{5.40}$$

where, T and T^{-1} are the well-known transformation matrices to switch between $\alpha - \beta$ and $d - q$ reference frames, which are typical of three-phase systems. The $d - q$ components derived from this strategy are then used for voltage and current control loops of single-phase converters. This is illustrated in Fig.5.18.

As compared to the proposed modified vector control, a non-vector based single-phase converter control requires a high switching frequency in the range of 10-100 kHz,

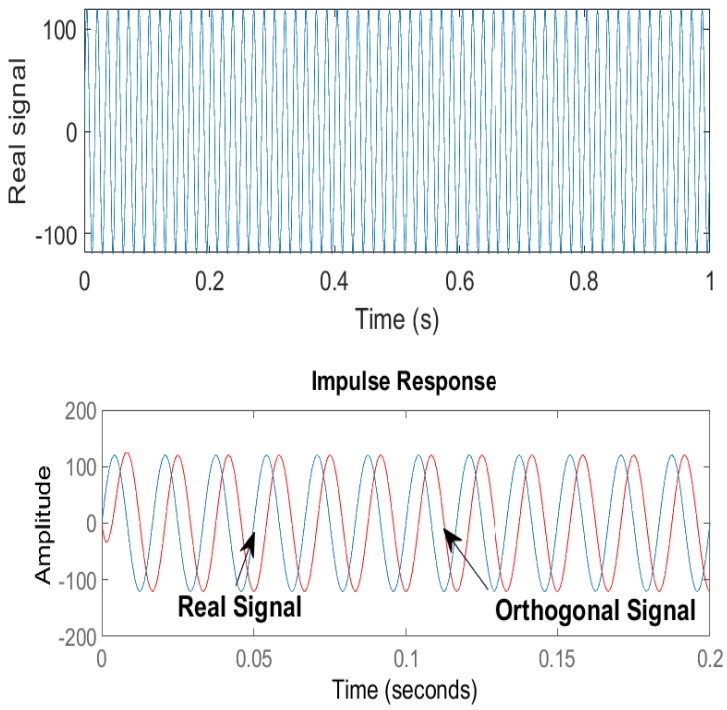


Figure 5.19: Real and imaginary voltage components through the all pass filter.

which results in heating losses. The overall cost of the converter also increases due to the requirement of designing more effective heat sinks [151]. Hence, the modified vector control for single-phase converters, combines the advantages of three-phase vector control, reduces the control complexity with a pre-filtering stage, and uses PI controllers for voltage and current loops in single- phase converter control.

5.4 Intra-phase Power Management

A multi-loop PI controller based intra-phase power management strategy for DG sources is shown in Fig.5.15. The DG sources include PV, battery and the droop units. The control strategy, illustrated in Fig.5.15, is for a particular ϕ_x, where x represents one of the phases A, B or C. The coordination and control of the hybrid PV/battery units with their respective droop units are dependent upon the local load demand in a phase, the available power generation and the battery's SOC. The total power available in a

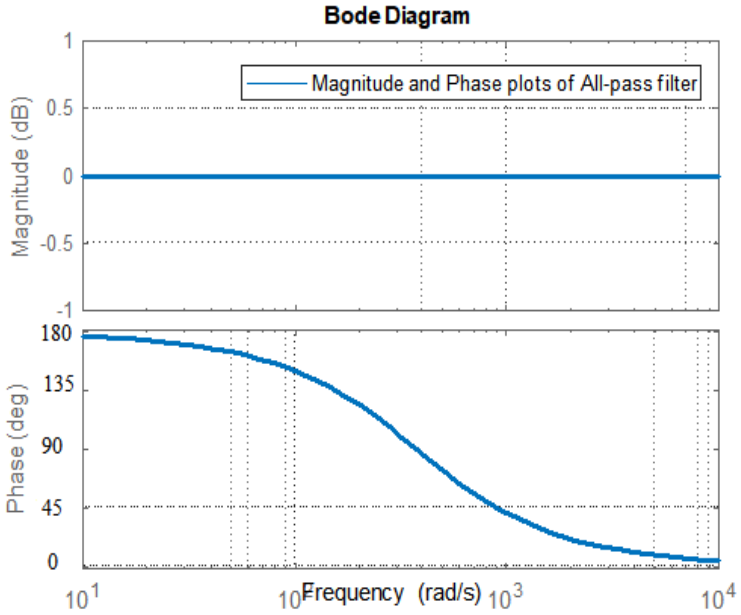


Figure 5.20: Bode plot of all-pass filter.

particular phase represented by $P_{total_{,\phi}}$ can be expressed as,

$$P_{total_{,\phi}} = P_{pv}^{max} + P_{batt}^{max} + P_{droop}^{max} \tag{5.41}$$

where, P_Z^{max} is the maximum power available from the DG unit, Z.

The loading conditions listed in Table 5.1 and the subsequent control objectives are detailed in the following subsections:

Scenario I: $P_{load}|_{\phi_x} < P_{pv}|_{\phi_x}$

Due to its renewable nature, the power from the PV unit should always be the first to support the load, P_pv. Therefore, this scenario is represented by zone A in the P/f characteristics of the multi-segment droop strategy in Fig.5.16. Any surplus power will be used to charge the battery, given that SOC is limited between SOC_{max} and SOC_{min}, until $SOC \rightarrow SOC_{max}$. As the battery is being charged, the system operates at $f_0 + \Delta f_{max}$, where Δf_{max} is the maximum allowable frequency deviation off the nominal, f_0.

Table 5.1: System's operating conditions and summary of control objectives for intra-phase power management

Scenario	Loading Conditions	Operating Frequency Range	Battery's SOC Status	Summary of Control Objectives
I.	$P_{load}\|_{\phi_x} < P_{pv}\|_{\phi_x}$	$f_0 < f < f_0 + \Delta f_{max}$	$SOC_{min} \leq SOC \leq SOC_{max}$ or $SOC \rightarrow SOC_{min}$	Intra-phase power management: • The load is handled by the PV unit only • The PV DC-DC converter operates at MPPT • The battery charges • No power sharing with the droop unit • This is illustrated by Zone A in Fig.5.16
II.	$P_{load}\|_{\phi_x} = P_{pv}\|_{\phi_x}$	$f = f_0$	$SOC_{min} \leq SOC \leq SOC_{max}$	Intra-phase power management: • The load is handled by the PV unit only • The PV DC-DC converter operates at MPPT • Floating state of the battery • No power sharing with the droop unit • This is illustrated by Zone A in Fig.5.16
III.	$P_{pv}^{mppt}\|_{\phi_x} < P_{load}\|_{\phi_x} \leq P_{batt}^{max}\|_{\phi_x}$	$f_{batt} < f < f_0$	$SOC_{min} \leq SOC \leq SOC_{max}$	Intra-phase power management: • Load is shared by the PV, battery and droop units • The PV DC-DC converter operates at MPPT • The battery discharges • No power sharing with the droop unit • This is illustrated by Zone B in Fig.5.16
IV.	$(P_{pv}^{mppt} + P_{batt}^{max})\|_{\phi_x} < P_{load}\|_{\phi_x} \leq P_{droop}^{max}\|_{\phi_x}$	$f_{batt}^{min} < f < f_{min}$	$SOC_{min} \leq SOC \leq SOC_{max}$	Intra-phase power management: • Load is shared by the PV, battery and droop units • The PV DC-DC converter operates at MPPT • The battery discharges • The battery power is limited at P_{batt}^{max} • This is illustrated by Zone C in Fig.5.16

Scenario II: $P_{load}|_{\phi_x} = P_{pv}|_{\phi_x}$

Under this scenario, if the load demand matches the PV generation, the PV will support the load, while the battery remains in a floating state. The proposed intra-phase control scheme in Fig.5.15, will make the PV unit operate off the maximum power point, by disengaging the MPPT function, through the SOC based control loop for PV DC-DC converter. The PV unit will then follow the load variations.

Scenario III: $P_{pv}^{mppt}|_{\phi_x} < P_{load}|_{\phi_x} < P_{batt}^{max}|_{\phi_x}$

As the load demand increases, the P/f trajectory enters the battery droop segment, whereby both the PV and the battery units support the load. The battery droop segment is represented by zone B in Fig.5.16. The system frequency drops either from f_0 or $f + \Delta f$, depending upon the previous operating scenario and battery's SOC. This scenario continues until $P_{batt} \rightarrow P_{batt}^{max}$, where P_{batt}^{max} is the maximum power battery power that can be delivered during discharge cycle.

Scenario IV: $P_{pv}^{mppt}|_{\phi_x} + P_{batt}^{max}|_{\phi_x} < P_{load}|_{\phi_x} < P_{droop}^{max}|_{\phi_x}$

During this scenario, the loads cannot be supported by the local PV and storage units. Therefore, the droop unit connected to ϕ_x will start supporting the load. At this stage, the P/f trajectory enters zone C as shown in Fig.5.16. The frequency of ϕ_x continues to drop due to the power contribution of the DG units until it reaches f_{min}, as shown in Fig.5.16. For intra-phase power management, the control strategy limits the frequency deviation of ϕ_x between $f_0 + \Delta f_{max}$ and f_{min}.

In summary, when only the hybrid unit is supporting the loads, the frequency is regulated between $f_0 + \Delta f_{max}$ and f_{batt}^{min}. At f_{batt}^{min}, the battery will supply the maximum discharge power, P_{batt}^{max}. The droop unit starts contributing only when the aggregated power is unable to meet the load demand. In Fig.5.17, the anti-windup control logic is used to limit the droop unit's real power contribution during load sharing. This uses the concepts developed in [143]. This ensures that the frequency is regulated between f_{batt}^{min} and f_{min} as illustrated in the P/f characteristics of Fig.5.16. At f_{min}, the droop unit operates at its rated capacity, P_{droop}^{max}. Hence, the preferred sequence of power sources in a phase, ϕ_x, is as following,

$$\text{Priority}_{\text{pv}} > \text{Priority}_{\text{batt}} > \text{Priority}_{\text{droop}} \tag{5.42}$$

Hence, the PV/battery hybrid units will serve the local loads until they reach their generation capacities. At this stage, further increase in load demand will be handled by the droop unit. Furthermore, the saturation blocks are used, as illustrated in Fig.5.17, to limit the frequency reference between $[f_0 + \Delta f_{max}, f_{min}]$, where f_{min} is the minimum allowable system frequency for safe and reliable operation of the residential microgrids. A summary of control objectives for various operating scenarios under intra-phase power management and control are listed in Table 5.1.

5.5 Validation of the Control Strategies

In this section, the microgrid under the operating scenarios and control objectives in Tables 5.1 are simulated in PSCAD/EMTDC. The PV model used in the simulation is data driven using the PV simulator available in the distributed generation laboratory. The data is then used in the software using a lookup table and using the PV unit as a dependent current source. In the case of battery storage unit, a dependent voltage source is used. The variations in the input voltage are dependent upon the charging and discharging cycles of the battery from the CIEMAT model, as described in section 5.3.4. The developed intra-phase control and power management strategy is validated.

The operating scenarios, as listed in Table 5.1, are covered under the intra-phase power management strategy. In order to illustrate the contributions of the DG units, a gradual step change of $288W$ is applied to the load demand. The simulations are run for $75s$. Other key variables, including the frequency, DC and AC phase power and battery's SOC are shown in Fig.5.21. For the purpose of illustration, results of only one phase are shown here. A constant PV generation of $1000W$ is assumed throughout the simulation run. This is represented by $P_{pv_{\phi_B}}$. The multi-segment P/f characteristics of these scenarios is shown in Fig.5.22.

The initial SOC of the battery is assumed to be approximately 71.2%. Since the load

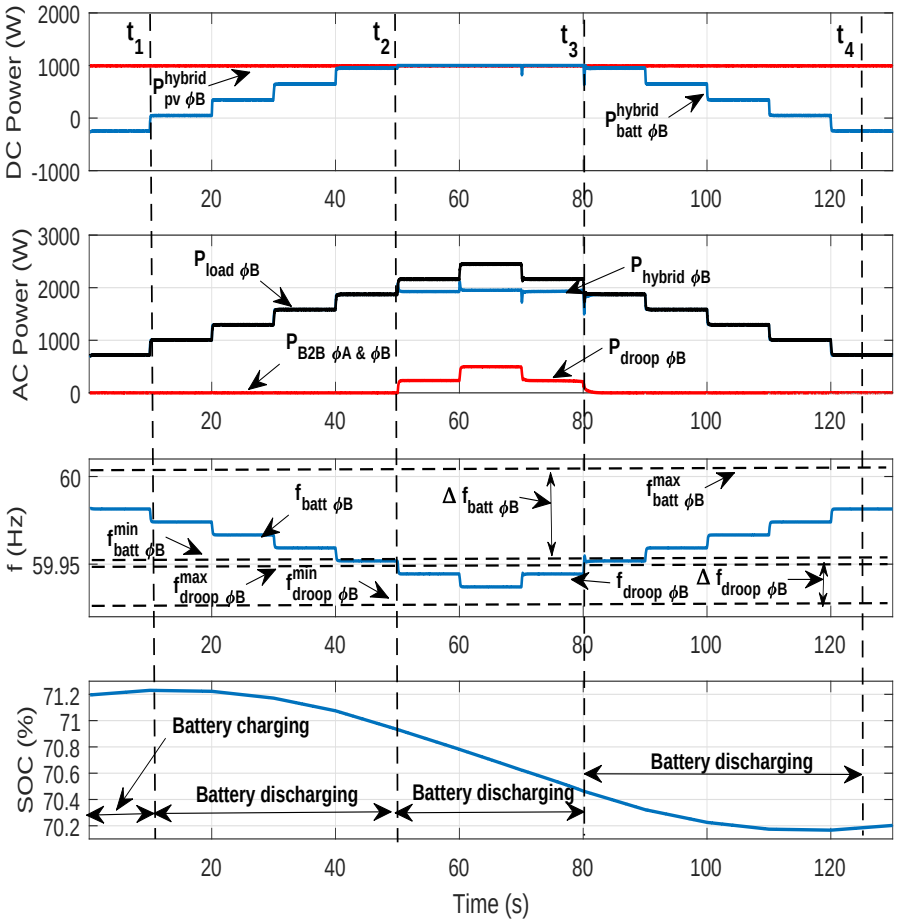


Figure 5.21: Performance of the intra-phase power management system.

demand at the start of simulation is low, the battery is charged with the available excess PV power in ϕ_B. This is due to initial SOC $< SOC_{max}$. The negative battery power between $t_1 = 0s$ and $t_2 = 5s$, illustrates the battery's charging state. As th battery is being charged, the system operates above the nominal frequency, f_0. This validates scenario #1 in Table 5.1.

The PV unit still supports the load between $t_2 = 5s$ and $t = 10s$. The lack of any excess power from the PV unit ensures that the battery is in floating state i.e. $P_{batt_{\phi_B}} = 0W$. Since $P_{pv_{\phi_B}} = P_{load_{\phi_B}}$, the battery does not participate in regulating power. The system continues to operate at f_0. This validates scenario #2 in Table 5.1.

As the load demands moves from zone A to zone B between $t = 10s$ and $t_3 = 25s$, both the PV and battery units start supporting the load. This is represented by positive

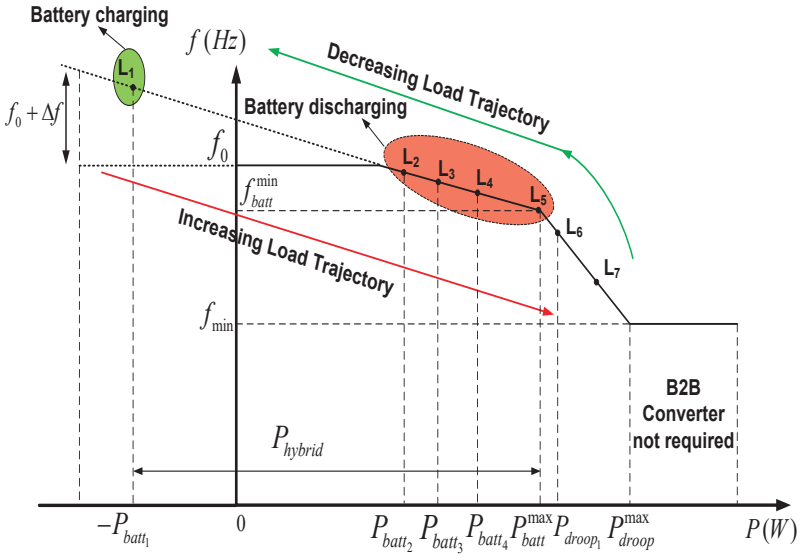


Figure 5.22: P/f characteristics for simulated scenarios in Table 5.1.

battery, $P_{batt_{\phi_B}}$, in Fig.5.21. Since both PV and battery units are handling the load at this stage, the system operates below the nominal frequency, f_0. This validates scenario #3 in Table 5.1.

At $t_3 = 25s$, the battery unit reaches its capacity, P_{batt}^{max}. The system starts operating at f_{batt}^{min}, corresponding to L_5 in Fig.5.22. At this stage, the battery's maximum discharge power is regulated at $1000W$. Further increase in load demand from L_5 to point L_6 will cause a power imbalance. Therefore, the net power will be supplied by the droop unit, represented by $P_{droop_{\phi_B}}$ in Fig.5.21. This validates scenario #4 in Table 5.1.

At the onset of decrease in load demand between $t_5 = 35s$ and $t_7 = 70s$, the contribution from the droop unit decreases to $0W$. This follows the supplier priority as given in (4). Once again the hybrid PV and battery unit start supporting the load. The battery charging resumes again at $t = 60s$, as the load demand falls below $P_{pv_{\phi_B}}$. This is illustrated by the increase in battery's SOC in Fig.5.21.

5.6 Summary

In response to ever-increasing installation of distributed generation units (PV and droop units) and battery storage devices in residential communities, a power management strat-

egy for residential microgrids is presented in this chapter. In this respect, a cooperative control and power management strategy is developed. Since most of the residential power supplies are single-phase in nature at the consumers' end, intra-phase power management has been considered within a phase. For intra-phase load-frequency control, a modified vector control is adopted with a multi-segment (P/f) droop based load-sharing. The proposed scheme has been validated by simulation with the detailed model of the microgrid and power electronic converters in PSCAD/EMTDC. The results have shown that the developed scheme can provide effective control and power management for intra-phase scenario in residential distribution microgrids with renewable energy resources and storage devices.

Chapter 6

Inter-Phase Power Management in Residential Microgrids

A power deficit scenario within single-phase residential microgrids will cause unnecessary load shedding of loads. This will happen if there is no assistance from the grid. In this situation, there is a need of some power electronics based converter, which can use the information of individual phase(s) and by using the improved multi-segment control strategy, as described in Chapter 5, transfer the deficit power from the surplus phase to the power deficient phase. This scenario has been coined the name of 'inter-phase power management strategy'. In this chapter, the layout and design of back-to-back converter is explained followed up with PSCAD/EMTDC simulations for typical scenarios where the inter-phase power management strategy will use the back-to-back converter to transfer power.

6.1 Introduction

An architecture of the three single-phase microgrids connected is shown in Fig.6.1, where the three single-phase microgrids are connected to their respective phases on the secondary side of a local distribution transformer [125, 126, 133]. With local phase-wise

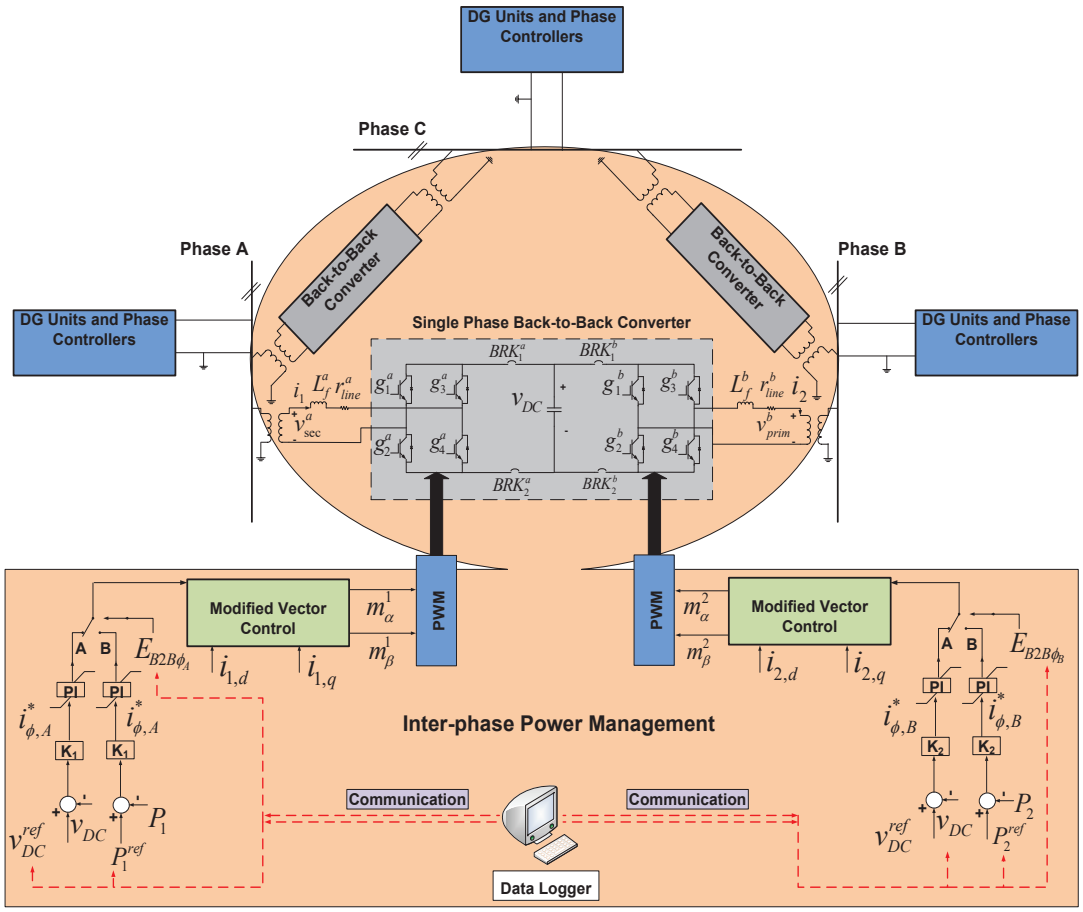


Figure 6.1: Overall architecture of single-phase residential microgrids with back-to-back converters between phases.

generation from rooftop PV panels and their varying irradiance levels, unique load profiles and diverse use of storage units at various levels of the state-of-charge (SOC), the negative sequence current can inflict a great deal of stress at the local transformer. With high penetration of renewable energy in each phase as well as diversified phase-wise loads in the single-phase microgrids may draw different level of currents from this local transformer leading to phase imbalance. Therefore, under these conditions, phase balancing has become a much significant task to ensure reliable operation of substation equipment and to provide high-quality power to all customers.

An equivalent circuit for the inter-phase power management for balancing individual phases using interconnecting back-to-back converters is introduced in Chapter 4 and is shown in Fig.6.2. For an unbalanced wye-network with local generation and storage,

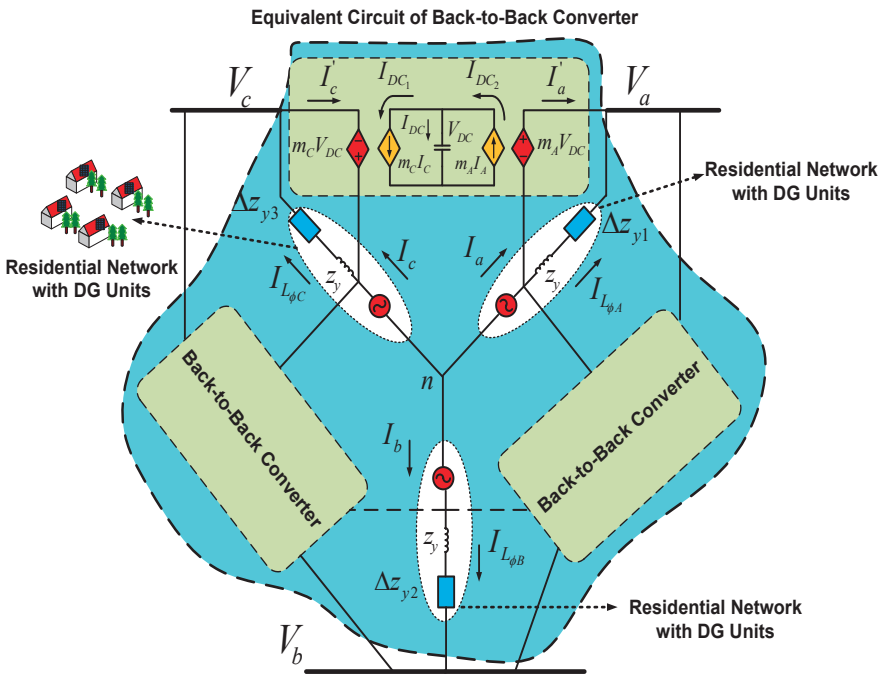


Figure 6.2: Proposed interfacing back-to-back between phases with its equivalent circuit.

the local DG sources are at the front end of a voltage controlled single-phase converter, represented by the three phases in Fig.6.2. Any mismatch between the generation and the local load consumption within a particular phase can be represented in terms of delta impedance, Δz_{y_1}, Δz_{y_2} and Δz_{y_3} in Fig.6.2, where these delta impedance can either be positive or negative.

This configuration has the advantage that the dynamic balancing of phases can take place locally within the single-phase residential microgrids. This is not limited between only two phases. In fact, the phase with surplus power can provide necessary power to two deficit phrases simultaneously so that the three singe-phase microgrids only collectively draw the minimum amount of balanced power from the local distribution transformer.

6.2 Design of the Back-to-Back Converter

The control of single-phase systems is not as trivial as that for three-phase systems. The control for such single-phase microgrids using intra-phase power management strategy

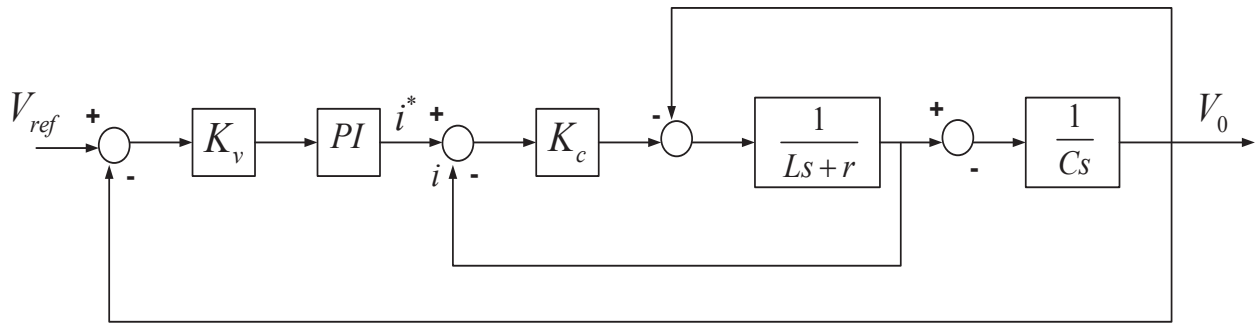


Figure 6.3: Simplified closed loop diagram for the control of back-to-back converter.

has been introduced in Chapter 5, where there is a need for the modified vector control strategy to introduce an orthogonal signal to make use of $\alpha\beta$-dq transformation. For the control of back-to-back converter, the modified vector control strategy is again utilized for the voltage and current control loops as shown in Fig.6.1. Furthermore, the LC filter required for such an architecture is comparatively larger in individual values for L and C as that for three-phase systems. The line inductance is selected to be $5mH$ while the filter capacitance is selected as $100\mu F$. This is because, there are inherent higher order harmonics that need to be suppressed.

The controller design of the back-to-back converter consist of designing the PI controller gains for the inner current loops and for the outer voltage control loops. A simplified closed loop diagram for the control of back-to-back converter is shown in Fig.6.3. From Fig.6.3, the first order plant's Laplace Transform for the inner current control loop is given by,

$$G_c(s) = \frac{K_c}{LCs^2 + rCs + 1} \tag{6.1}$$

whereby, L and r are the line inductance and resistance of the back-to-back converter, C is the filter capacitance and K_c is the feed-forward loop gain. Using the Routh-Hurwitz stability criteria, the closed loop system with the PI controller block can be written as,

Table 6.1: Routh-Hurwitz stability criteria for the control of back-to-back converter

s^3	LC	$(1 + k_p K_c K_v)$
s^2	$(rC + K_c C)$	$k_i K_c K_v$
s^1	$\frac{(rC+K_cC)(1+k_pK_c)-LC(K_ck_i)}{(rC+K_CC)}$	0
s^0	$K_c k_i$	0

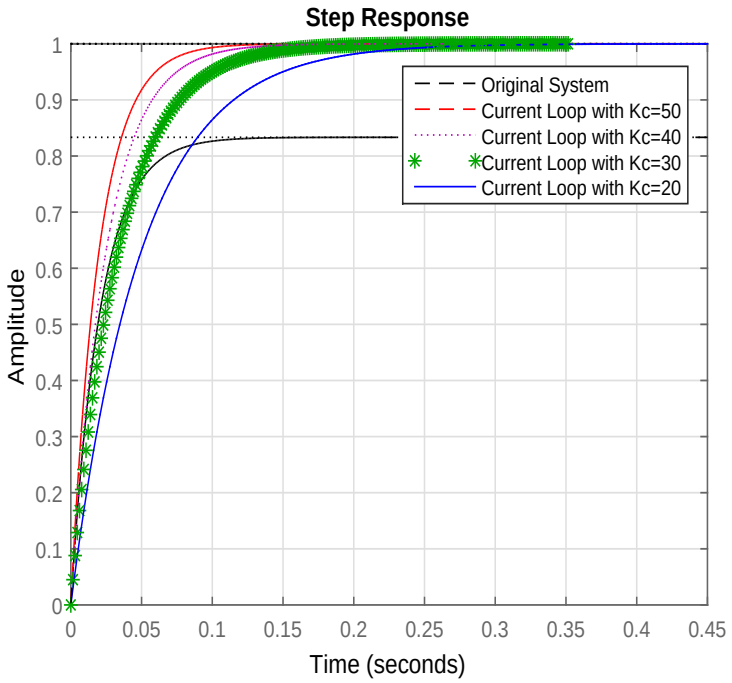


Figure 6.4: Step response by varying values of current loop gain, K_c.

$$G_{cl}(s) = K_v \cdot \frac{k_p s + k_i}{s} \cdot \frac{K_c}{LC^2 s^2 + rC^2 s^2 + K_c C s} \tag{6.2}$$

This is simplified to get,

$$G_{cl}(s) = \frac{K_v k_p K_c C s + K_v k_i K_c}{LC^2 s^3 + (rC + K_c C)s^2 + (1 + k_p K_c K_v)s + (k_i K_c K_v)} \tag{6.3}$$

The tabulated results from Routh-Hurwitz stability criteria are shown in Table 6.1.

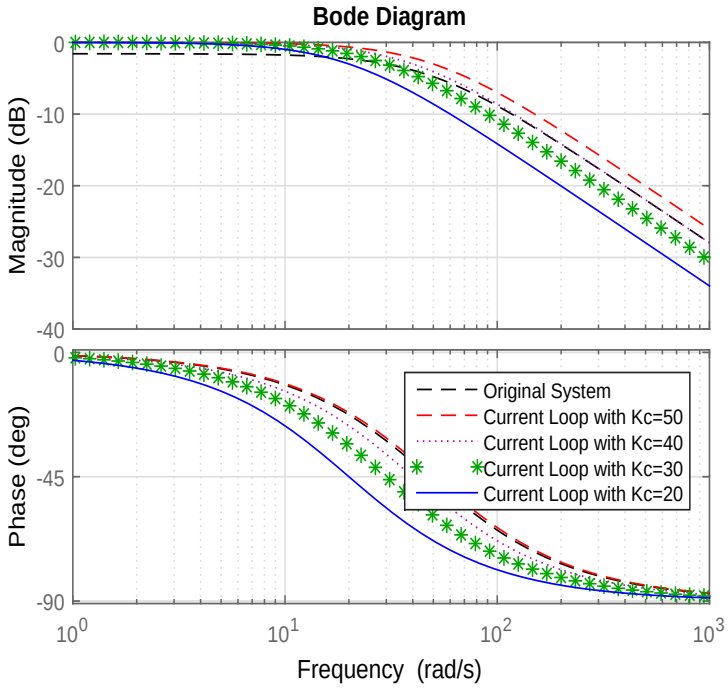


Figure 6.5: Bode plot by varying values of current loop gain, K_c.

By varying the values of K_c in Table 6.1, different inequalities relating to the gains of PI controller can be achieved. The step responses for the inner current control loop is shown in Fig.6.4, where K_c is varied between 20 to 50. It can be observed that with the original system without controller gains, the system is unable to reach the reference which is provided. The response of system becomes faster in terms of settling time as the values of K_c are increased from 20 to 50. The bode plots for the system are shown in Fig.6.5. It is observed that with $K_c = 50$, the designed controller has sufficient phase margin at the fundamental frequency of 60Hz. At this stage, the gain for the inner current control loop is set at 0.005 which is equal to the line inductance for the back-to-back converter. Using this value and the fact that K_c is set at 50, the root locus plot of dominant poles is plotted by varying the integral gain of the current loop's PI controller for a range of values. This is shown in Fig.6.6. It is observed that as the integral gain is increased from 0 to 0.5, the dominant poles cause the system to become under damped. Hence the integral gain is selected to be 0.2.

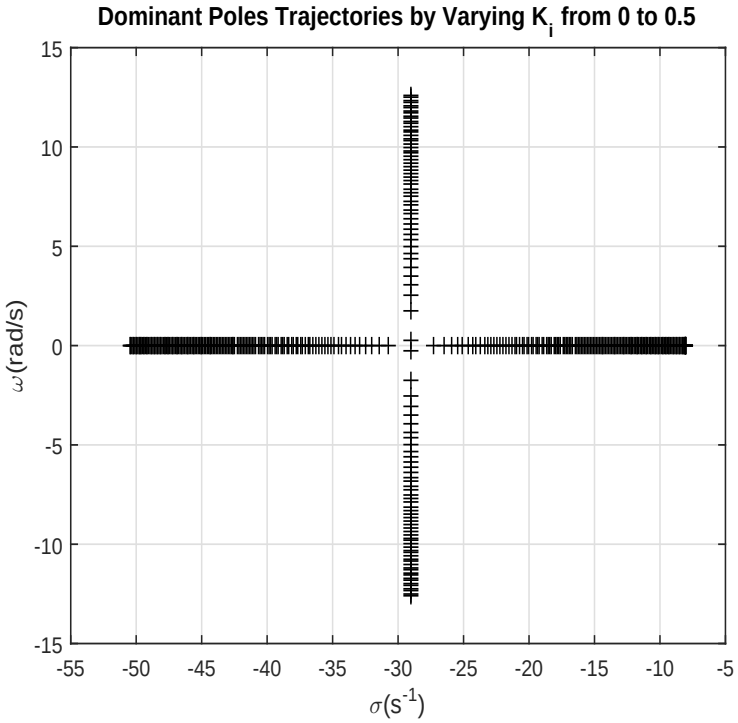


Figure 6.6: Trajectory of the dominant poles in the current loop by varying the integral gain, K_i.

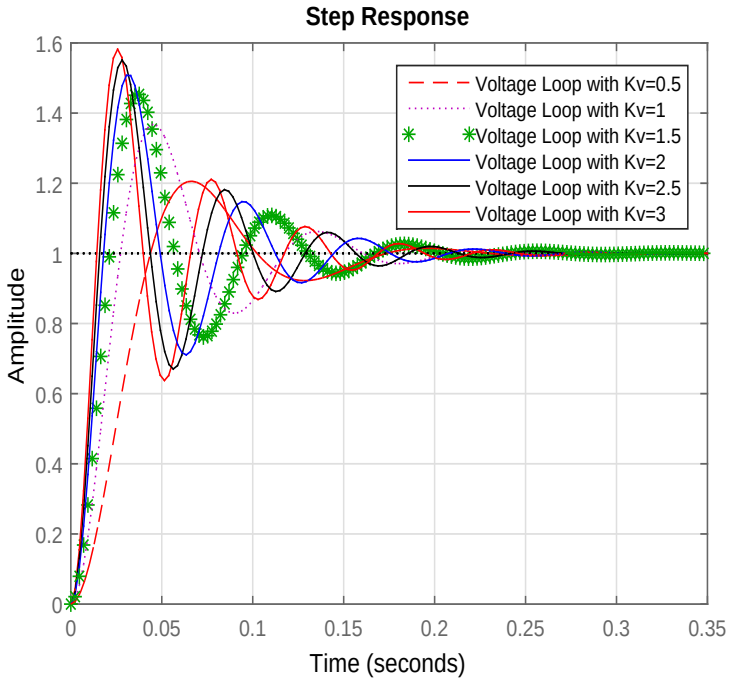


Figure 6.7: Step response by varying values of outer voltage control loop, K_v.

With the inner current control loop designed for the back-to-back converter, the same procedure is followed to design the outer voltage control loop. Using Ziegler-Nichols

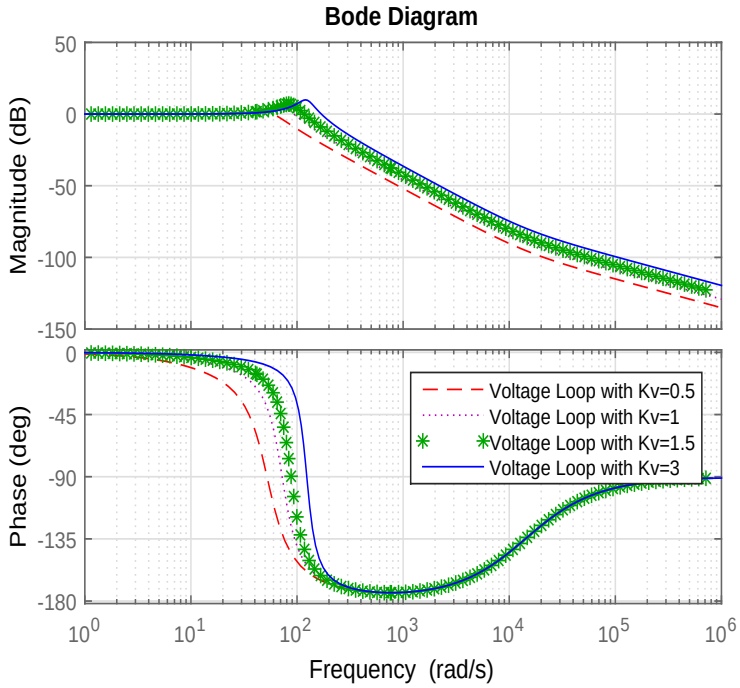


Figure 6.8: Bode plot by varying values of outer voltage control loop's gain, K_v.

method of tuning the PI controller, it is found out that the optimal values for $k_p = 0.007$ and that for $k_i = 100$. At this stage the gain for outer voltage control loop needs to be set. For this purpose, the value of K_v is varied from 0.5-3 and the step response of the system is observed. This is shown in Fig.6.7. As the value of K_v is increased, the settling time reduces. At the same time there is a slight overshoot as compared to other values. Hence, from the step response shown in Fig.6.7, K_v is selected as 3. The bode plots for the system are shown in Fig.6.8. It is observed that with $K_v = 3$, the designed controller has sufficient phase margin at the fundamental frequency of 60Hz. The root locus plot of dominant poles is plotted by varying K_v for a range of values. This is shown in Fig.6.9. It is observed that as the value of outer gain is increased from 0.01 to 10, the dominant poles cause the system to become under damped. Hence, it is confirmed that $K_v = 3$, will not cause the system to become unstable.

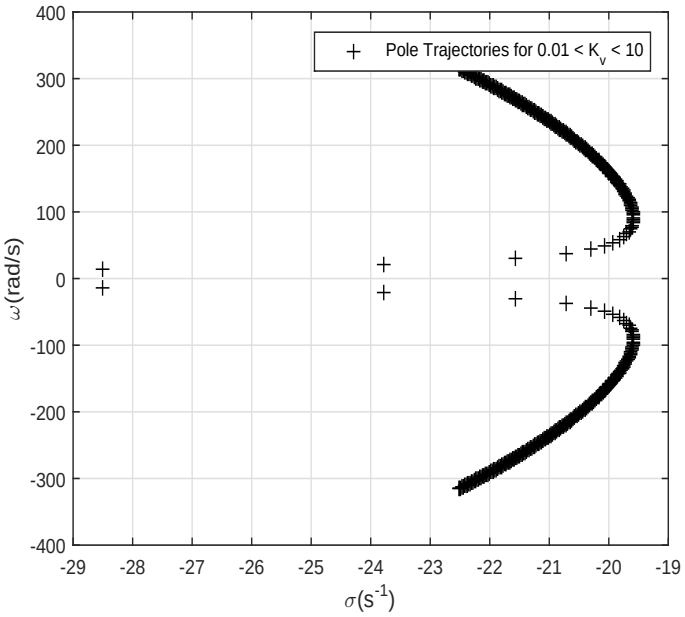


Figure 6.9: Trajectory of the dominant poles in the outer voltage control loop by varying the proportional gain, K_v.

6.3 Inter-phase Power Management

The control objective of the inter-phase power management ensures that the necessary back-to-back converters are activated during power transfer between phases as tabulated in Table 6.2. This scenario is represented by zone D in Fig.6.10 and is given by,

$$P_{load}|_{\phi_x} > (P_{pv}^{mppt}|_{\phi_x} + P_{batt}^{max}|_{\phi_x} + P_{droop}^{max}|_{\phi_x}) \tag{6.4}$$

During this scenario, the PV, battery and droop units reach their unit capacities and are unable to support the load. Based on the information collected from the local energy balance control system, the community energy balance control system makes a decision for the power contributing phase. Since the DG units, within a phase, are operating at their maximum capacities, the frequency of ϕ_x is regulated at f_{min}. The single-phase back-to-back converter with its control strategy is shown in Fig.6.1. Modified vector control is used for the inner current control loops.

The DC link voltage or the real power flow is regulated by the outer control loops.

Table 6.2: System's operating conditions and summary of control objectives for inter-phase power management

Scenario	Loading Conditions	Operating Frequency Range	Battery's SOC Status	Summary of Control Objectives
1.	$P_{load}\|_{\phi_x} > (P_{pv}^{mppt} + P_{batt}^{max} + P_{droop}^{max})\|_{\phi_x}$	f_{min}	$SOC_{min} \leq SOC \leq SOC_{max}$	Intra-phase power management: • Load is shared by the PV, battery and droop units • The PV DC-DC converter operates at MPPT • Following eq.(A.3) [160], the battery discharges • Limit battery power at P_{batt}^{max} Inter-phase power management: • The community energy balance control system makes the decision for power contributing phase • Setting of the required enable and logic signals • $P_{B2B}^{ref} = P_{hybrid} - P_{pv}^{mppt} - P_{batt}^{max}$ • Illustrated by Zone D in Fig.6.10

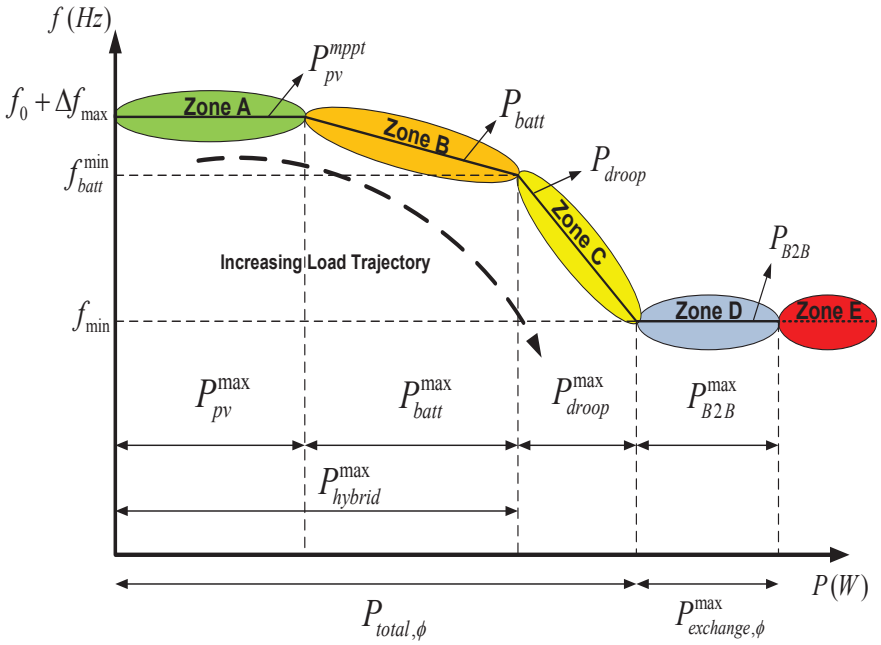


Figure 6.10: The improved multi-segment droop control strategy with its P/f characteristics for different power sources.

The control loop of mode A in Fig.6.1 is used by the power surplus phase to regulate the DC link voltage. This happens prior to the power sharing mode. During power transfer between phases, the control loop switches to mode B. This regulates the required real power flow between phases. The switching of control modes is determined by the digital

signals $E_{B2B_{\phi_A}}$ or $E_{B2B_{\phi_B}}$. These signals are shown in Fig.6.1, whereby,

$$E_{B2B_{\phi A}}, E_{B2B_{\phi B}} \quad \in \quad \{0,1\} \tag{6.5}$$

From Fig.6.1, the current references during power transfer are stated as,

$$\begin{aligned} i^*_{\phi,A}(t) &= K_1(e(t)_1) \times \left(k_p^1 + k_i^1 \int e(t)_1 \ \ dt\right) \\ i^*_{\phi,B}(t) &= K_2(e(t)_2) \times \left(k_p^2 + k_i^2 \int e(t)_2 \ \ dt\right) \\ i^*_{\phi,C}(t) &= K_3(e(t)_3) \times \left(k_p^3 + k_i^3 \int e(t)_3 \ \ dt\right) \end{aligned} \tag{6.6}$$

where, $i^*_{\phi,A}(t)$, $i^*_{\phi,B}(t)$ and $i^*_{\phi,C}(t)$ are the current references for each of the single-phase back-to-back converters during power transfer; $e(t)_1$, $e(t)_2$ and $e(t)_3$ denote the net real power required by the deficient phase from the power-surplus phase and is given by,

$$e(t)|_x = P_{load}|_{\phi_x} - P_{total,x} \tag{6.7}$$

where, $P_{load}|_{\phi_x}$ is the loading requirement in the power deficient phase, x. K_1, K_2 and K_3 in (6) are controller parameters. The required gating signals are generated through m^1_α,m^1_β,m^2_α and m^2_β. The system's operating conditions and a summary of the control objectives for the inter-phase power management scenario are listed in Table 6.2. It is assumed that while the power exchange between is taking place, the third phase operates independently with no inter-phase power transfer.

In the worst case scenario, where the load demand further increases and exceeds the local phase generation and storage capacities; as well as the maximum power that can be exchanged between phases, load shedding will be needed to maintain the safe and reliable operation of the system. This is represented by Zone E in Fig.6.10. However, introducing a load shedding technique is beyond the scope of this work.

6.4 Simulation Results

A detailed switching model of residential microgrids with a hybrid PV/battery unit and a droop unit in each phase, with interconnecting back-to-back converters, is simulated in PSCAD/EMTDC. The solution time step is kept at $0.5\mu s$.

Figures 6.11-6.18 show the simulation results for various scenarios of the proposed hierarchical control strategy. These include the cases; where (a) all phases are balanced through intra-phase power management, (b) one phase is power deficient and the other two phases share power equally or (c) unequally, (d) Only a single-phase shares power with the deficit phase and (e) a phase shares power with two power deficit phases. The load trajectory increases from L_1 - L_8, in steps of $288W$. The simulation is run for $75s$. In order to control the output voltage and frequency of a particular phase ϕ_x, the community energy balance control system (CEBCS) first identifies it as power deficient and polls other phases for surplus power for sharing. From the AC power simulation results, shown in Figures 6.12, 6.16 and 6.14, the net power requirement for a deficient phase, $P_{req_{\phi x}}$, is calculated.

6.4.1 All phases are balanced

The simulation results for intra-phase power management strategy is shown in Fig.6.11. The load trajectory increases in steps of $288W$. The simulation is run for $130s$, with step changes in loads after every $10s$. For this simulation run, it is assumed that the system is already operating in islanded condition. At $t_2 = 50s$, both PV and battery support the load, until the battery reaches P_{batt}^{max}. At this stage, the maximum discharge power of battery needs to be regulated at $1000W$ for any further increase in load trajectories. As the load increases from, the supplied power by the hybrid unit is not sufficient to support the load, hence the droop unit starts contributing. This is represented by $P_{droop_{\phi_A}}$ in Fig.6.11. Similar results can be obtained for other phases also. Since, local generation

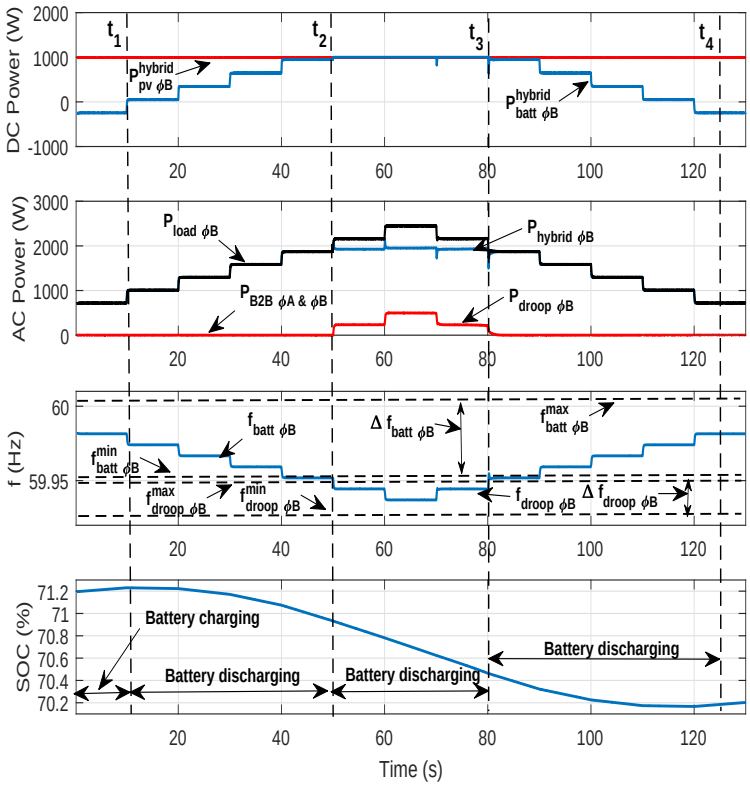


Figure 6.11: Performance of intra-phase power management for balancing a phase.

and storage is sufficient to serve the loads, there is no requirement for inter-phase power management. Hence $P_{B2B_{\phi_A \& \phi_B}} = 0W$ as shown in Fig.6.11.

6.4.2 Two phases share power equally with deficit phase

At $t_4 = 35s$, the CEBCS identifies that both phases ϕ_A and ϕ_C are available to share power with ϕ_B. If both phases are capable of sharing power equally with ϕ_B, then this will cause the enable signals, $E_{B2B_{\phi_A}}$ and $E_{B2B_{\phi_C}}$ to be set, and the reference power $P^{ref}_{B2B_{\phi_A}}$=$P^{ref}_{B2B_{\phi_C}}$=121W. The power that is transferred from both ϕ_A and ϕ_C is represented by $P_{transferred\ \phi_A\ \&\ \phi_C}$ in Fig.6.12. The total power, $P_{exchanged\ with\ \phi_B} = 242W$. Using the improved multi-segment droop strategy in [125, 126], the system frequency of ϕ_B reaches f_{min} before the back-to-back converters are triggered. This is because all the DG units in ϕ_B are operating at full capacities. During power transfer, the back-to-back converter's DC link voltage, $V^{B2B}_{DC_{\phi A}}$ and $V^{B2B}_{DC_{\phi C}}$, accordingly decreases to transfer

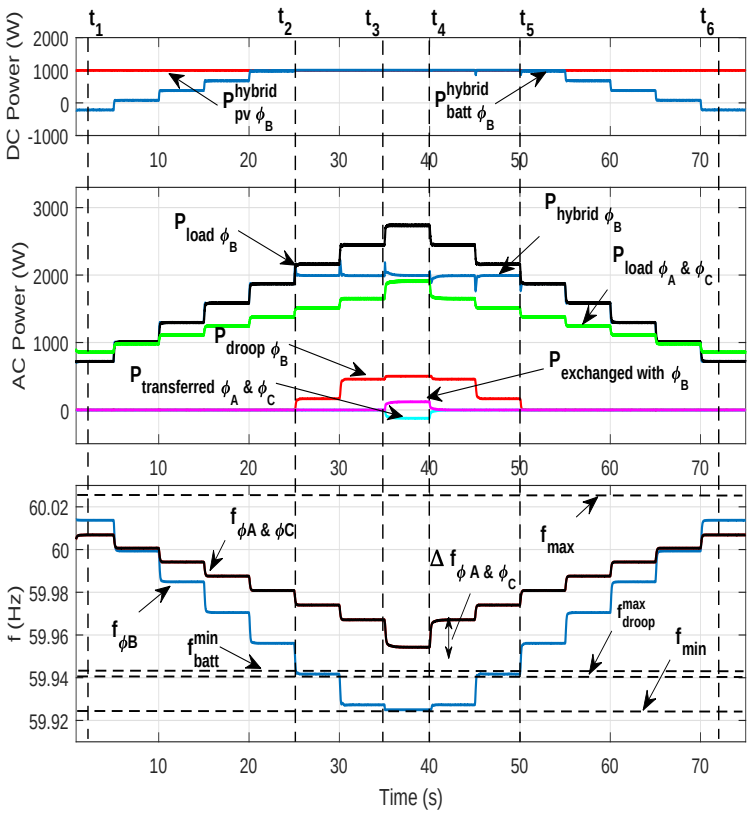


Figure 6.12: Simulation results for equal power sharing between phases.

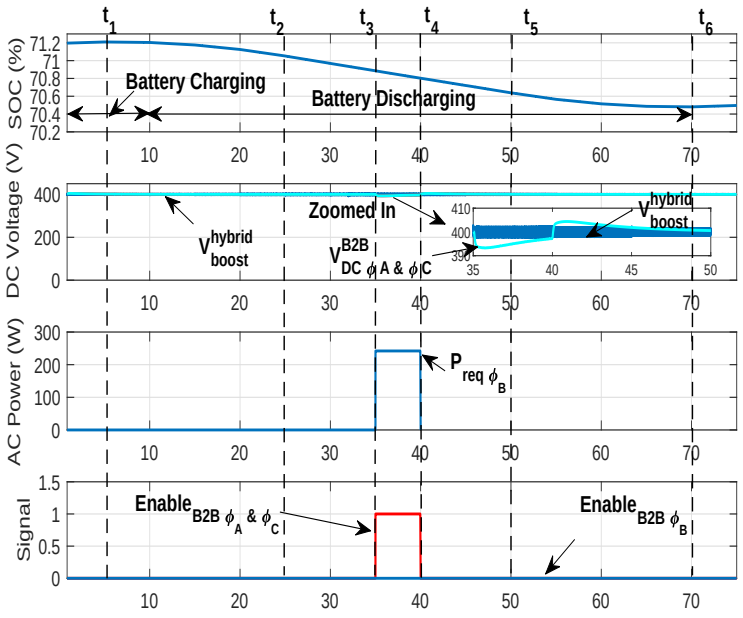


Figure 6.13: System's status signals during equal power sharing by two phases.

the required power to ϕ_B, as shown in Fig.6.13.

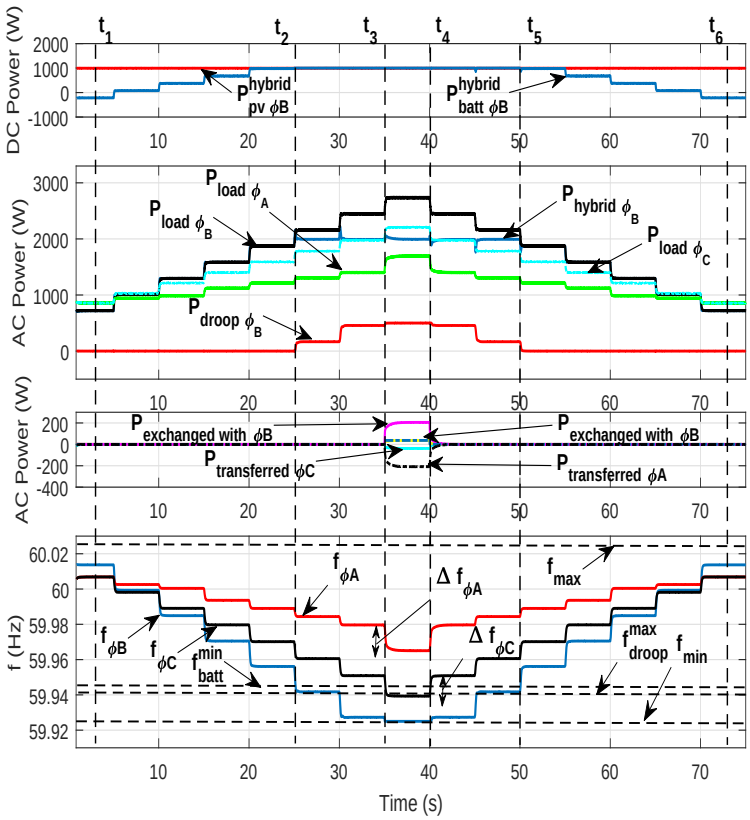


Figure 6.14: Simulation results for unequal power sharing by two phases.

6.4.3 Two phases share power unequally with deficit phase

In this scenario, the CEBCS identifies that both ϕ_A and ϕ_C are available for sharing power yet unequally. This may be due to differences in loading and generation in both the phases. This triggers the enable signals, $E_{B2B_{\phi_A}}$ and $E_{B2B_{\phi_C}}$. The power that is transferred from both ϕ_A and ϕ_C is represented by $P_{transferred\,\phi_A\,\&\,\phi_C}$ in Fig.6.14. It is illustrated that ϕ_A and ϕ_C share power unequally. The total power, $P_{exchanged\,with\,\phi_B} = 242W$. During power transfer, the back-to-back converter's DC link voltage, $V_{DC_{\phi A}}^{B2B}$ and $V_{DC_{\phi C}}^{B2B}$, accordingly decreases to transfer the required power to ϕ_B, as shown in Fig.6.15.

6.4.4 One phase shares power with deficit phase

For this case, the network controller identifies that only ϕ_A is available for sharing power at $t_4 = 35s$. This triggers the enable signal, $E_{B2B_{\phi_A}}$, and sets $P_{B2B_{\phi_A}}^{ref}$=$242W$. The power transferred from ϕ_A to ϕ_B is shown in Fig.6.16. The total power, $P_{exchanged\,with\,\phi_B}$ =

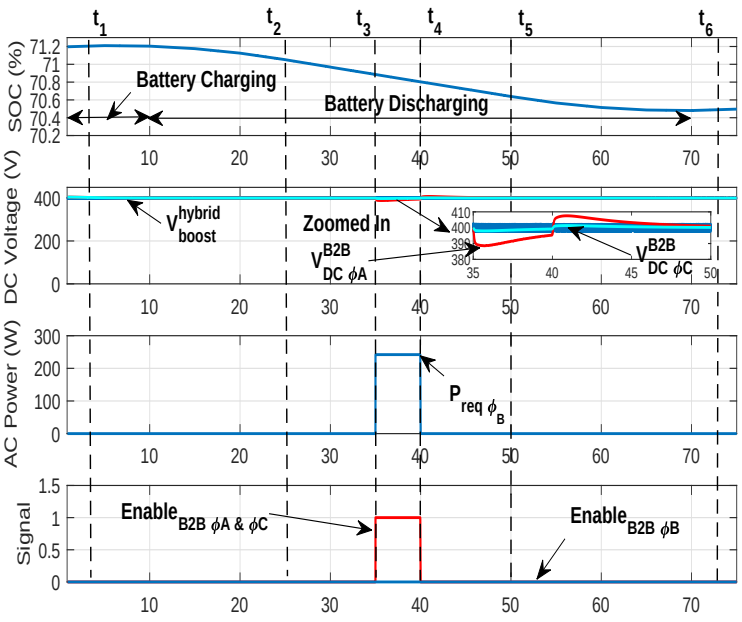


Figure 6.15: System's status signals during unequal power sharing by two phases.

$242W$. During power transfer, the back-to-back converter's DC link voltage, $V_{DC_{\phi A}}^{B2B}$ accordingly decreases to transfer the required power to ϕ_B, as shown in Fig.6.17. The DC link voltage for ϕ_C, $V_{DC_{\phi C}}^{B2B}$ is regulated at $400V$ during this time.

6.4.5 One phase shares power with deficit phases

In this scenario, the CEBCS identifies that only ϕ_A is available for sharing power with ϕ_B and ϕ_C. This triggers the enable signals, $E_{B2B_{\phi_A}}$. The power that is transferred to both ϕ_B and ϕ_C is represented by $P_{exchangedwith\phi_B}$ and $P_{exchanged\ with\ \phi_C}$ in Fig.6.18. It is illustrated that ϕ_A is capable of sharing power with multiple phases if required. The total power, $P_{transferred\ with\ \phi_A} = 745W$.

Between $t_5 = 40s$ and $t_7 = 70s$, for all case scenarios, the load demand starts decreasing in all of the cases shown above. The power sharing reference and the contribution from the droop unit decreases to $0W$, resulting in PV and battery to start handling the load [125, 126]. The back-to-back converter's DC link voltages regulate at $400V$. At $t = 60s$, the battery starts charging again as the load demand becomes less than $P_{pv_{\phi_B}}^{hybrid}$,

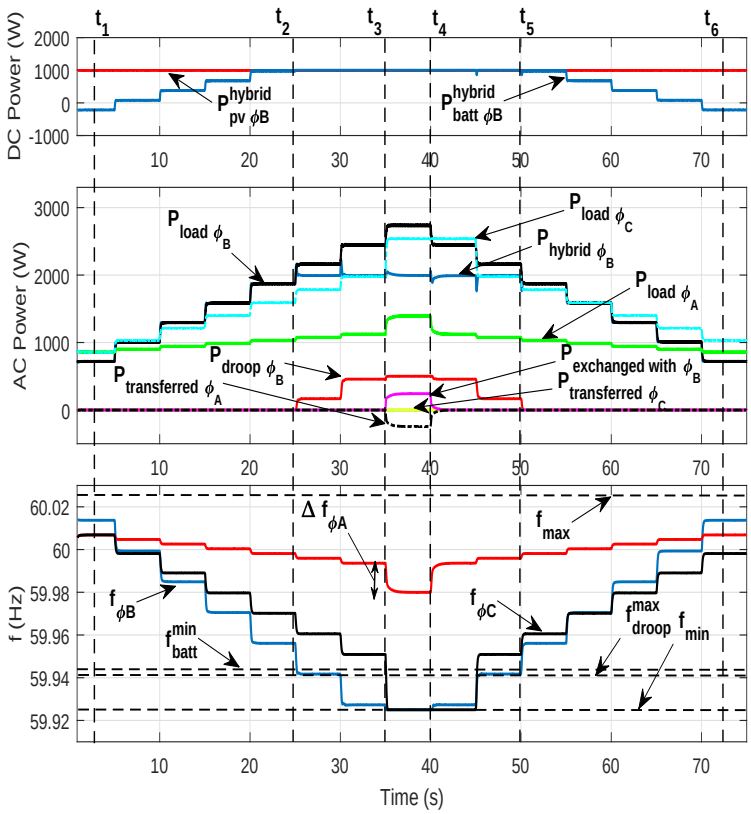


Figure 6.16: Simulation results for one phase sharing power with the deficit phase.

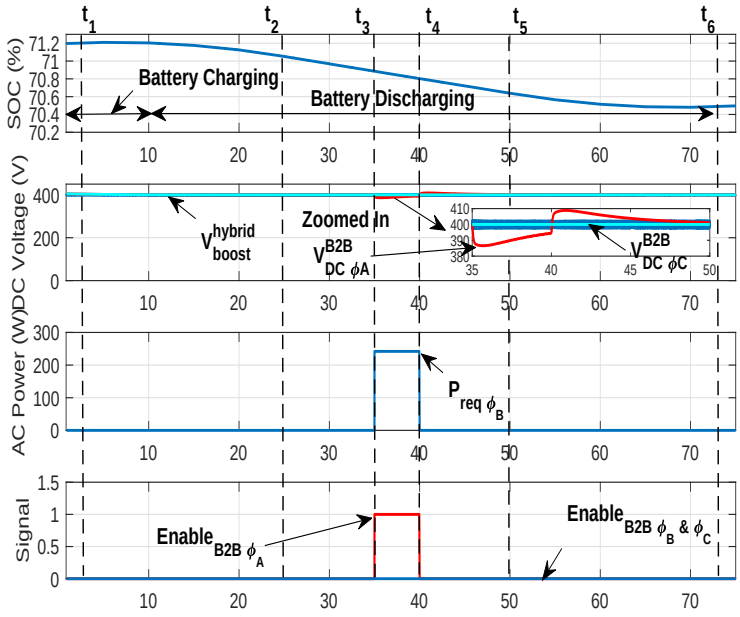


Figure 6.17: System's status signals during one phase sharing power with the deficit phase.

as shown in Figures 6.11, 6.13, 6.17, 6.15 and 6.18. Overall, the system operates between $f_0 + \Delta f$ and f_{min}. The results shown in this section are repeatable for other phases also.

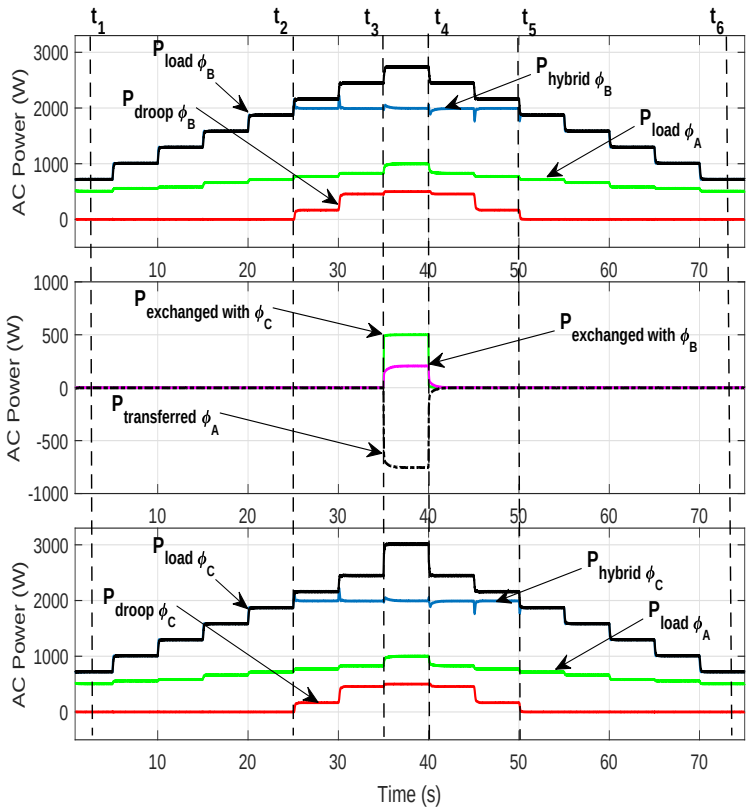


Figure 6.18: Simulation results for one phase sharing power with deficit phases.

6.5 Summary

This chapter deals with the inter-phase power management for single-phase residential microgrids by making use of three back-to-back converters that are placed between respective phases to allow for independent power transfer as requested by the network controller. The proposed scheme has been validated by simulations with the detailed model of the microgrid and power electronic converters in PSCAD/EMTDC. The results have shown that the developed scheme can provide effective control and power management for inter-phase scenarios in residential distribution microgrids with renewable energy resources and storage devices.

Chapter 7

Operational Modes and Control Strategies in Residential Microgrids

An operational and energy management strategy for balancing three single-phase residential microgrids is presented in this chapter. The strategy makes use of the previously developed intra- and inter-phase power management techniques to transfer power from the surplus phase(s) to power deficient ones to achieve an overall balance, despite diverse load demand profiles in each phase. This scheme is particularly useful in situations where phase-dependent generation, single-phase loads, and home-based storage devices are involved, such as roof-top PVs, electrical vehicles, and battery storage units. This scheme also opens up potential avenues for accommodating more advanced energy management schemes, such as peak shaving, load shifting, to minimize potential risks of overloading substation transformers or forced load shedding. Seven operating scenarios have been analyzed in this chapter with detailed switching models developed in PSCAD/EMTDC platform to validate the effectiveness of the proposed strategy.

7.1 Introduction

Installation of singe-phase residential roof-top PV systems has surged over the past few years [2]. As a result, the conventional passive distribution networks have now evolved into active networks that could suffer from a high degree of phase imbalance at the residential level [114,145]. With sufficient local generation and storage, the distribution companies are strategizing of grouping these dwellings to form residential microgrids [162]. A configuration of such a residential microgrid is shown in Fig.7.1. It is assumed that some of the local customers have installed PV panels on their roofs and battery storage at their homes, which are mainly single-phase. One characteristic of such a distribution system is that it consists of both three-phase balanced part and three single-phase part. The power in the three-phase part is often used to support local community centers, schools, or shopping complex, in which predominately the loads are in balanced three-phase, while single-phase parts are mainly associated with residential dwellings, which can be unbalanced. However, this phase imbalance issue can be rectified by transferring power among different phases to achieve internal balanced using back-to-back converters bridging different phases [125, 126, 133]. Hence, the need for developing affective operational and energy management strategies for such small-scale microgrids has become a necessity in current distributions networks [131, 132].

There are different control strategies to address phase balancing issues and to support local phase-wise loads through local generation and stored energy. This is known as intra-phase power management [125, 126, 133]. However, if the load demand exceeds the capacities of local phase-wise generation and storage, the proposed control scheme initiates power transfer from other power surplus phase(s) to make up the shortfall, or imports equal amount of minimum power through the substation transformer and then begin transferring power from the surplus phases. The latter enables the local distribution company to reduce the stress induced by the unbalanced power demand on the transformer. This power management strategy is referred to as inter-phase power

management [125, 126, 133].

Balancing techniques for three-phase microgrids have been proposed in [134, 135]. In [134] a repetitive controller is developed to damp the periodic harmonics caused by the unbalanced loads. While in [135], a robust controller is proposed for the same purpose. These type of controllers can only be used to negate the effects of positive and negative sequence currents associated with unbalanced loads. Hence, they are ineffective for power balancing scenarios. Other balancing topologies using converters have also been discussed in [136–142]. An active power filtering technique to inject the harmonic current for compensating non-linear loads at the DC link is introduced in [136]. Improved converter topologies using midpoint capacitors [137, 138], four-leg inverter [139, 140] or the three H-bridge inverter topology [141, 142] are all proposed for balancing non-linear loads in microgrids. The control strategies discussed in [136–142] can only deal with systems with a common DC link, in particular, with centralized PV generation and battery reserve.The effectiveness of these techniques is limited for residential microgrids due to absence of a common DC link within a group of residential houses connected to a phase.

Power management strategies for three-phase systems have been studied in [35, 37, 71, 77, 143]. Various control strategies have been proposed to coordinate the DG units with energy storage. One such technique is the use of multi-segment droop control strategy [35,37,143]. This strategy is limited by the capacities of renewable energy sources (RES). This drawback makes this strategy inefficient for residential microgrids, where in case of an islanded operation, the load demand may increase beyond the capacities of local generation and storage. This will introduce forced load shedding.

The coordination of these phase-wise microgrids has been made possible by a previously developed technique relying on back-to-back converters. The control of these converters at the interface of a microgrid is explored in [82]. The proposed architecture allows the microgrid to operate both in grid-connected and islanded modes. However, there are two operational constraints: (1) to give the priority to locally generated power

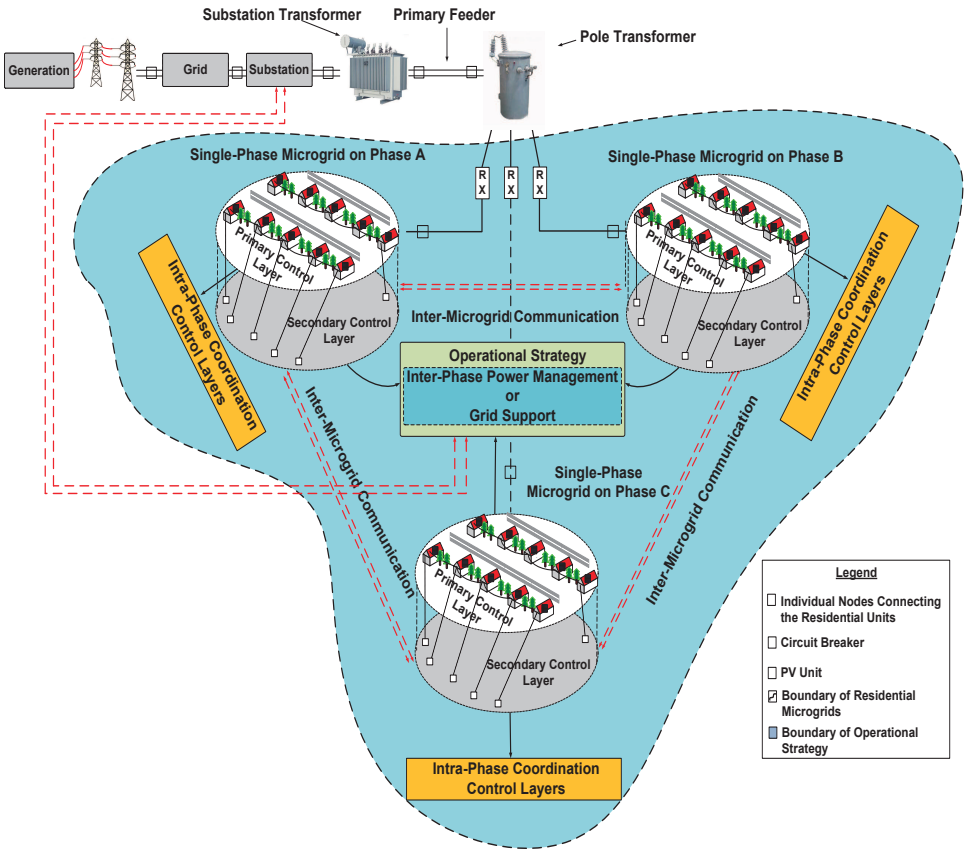


Figure 7.1: An architecture of a grid interfaced single-phase residential microgrids with local load, generation and back-to-back converters for power exchange.

for local consumptions; and (2) when grid power is needed to meet the demand, it is highly desirable to draw balanced three-phase power from the substation transformer. Therefore, this leads to two operating strategies: (1) If the total power available from all three phases is sufficient to meet the demand of loads in all three phases, the power management will be carried out internally within the three single-phase microgrids; and (2) if there is an identified power deficient, adequate amount of power will be imported from the grid in a balanced form; and the internal power management schedule is then used to balance the microgrids.

The control of an islanded hybrid single and three-phase microgrid through back-to-back converters is highlighted in [78]. The architecture therein is a close depiction of distribution system with single-phase loads connected with local DG units. Phases A and B constitute DG units and local loads while Phase C is considered as a load center only.

The power exchange between phases is carried out by controlling the inter-tied back-to-back converters of the three phases. This structure cannot be used for residential microgrids, as all three phases have local generation and loads. The power exchange in [78] is unidirectional, i.e. power flows from Phase A to Phase B, while both Phases A and B can transfer power to Phase C. Although this simplifies the control strategy significantly, this scheme cannot be used for power exchange amongst all phases back and forth.

Previous works from the authors have focused on the control strategies for the primary and secondary layers for single-phase residential microgrids [125, 126, 133]. The proposed control strategy therein does not cater for scenarios where multiple phases can balance the power deficient phase. Hence, there is a need for a supervisory control layer, which can manage the power flow from power-surplus phase(s) to power-deficit phase(s) to the all three phases from the point view of the sub-station transformer.

Further, the coordination of these microgrids based on economical dispatch and other decision-making criterion, using surplus power, voltage and frequency deviation at the PCC, has been studied in [154, 163, 164]. They are part of the tertiary control layer for microgrids [51,121,165]. In [154], the tertiary coordination is made to be dependent upon a dispatchable source that responds to variations in power exchange, as commanded by the microgrid controller. Since, this resource may or may not be existent in residential microgrids, the tertiary layer coordination, as proposed in [154], will not be effective for the architecture as presented in Fig.7.1.

A comprehensive tertiary coordination layer is proposed in [163]. This work involves the use of a weighted criteria and risk index matrices to determine a three-phase microgrid for power exchange. Since this work focuses primarily on the tertiary control layer, its effective coordination with the primary and secondary layers is not discussed. In addition, the coupling of microgrids for power exchange is carried out through the on/off position commands of the interconnecting breakers. This requires an additional stage of frequency

synchronization.

Although the control strategies in the primary and the secondary layers strategies have been developed for the single-phase microgrids by the same authors [125, 126, 133], those control strategies have not considered procedures and scenarios of selecting a phase(s) for transferring the net unbalance power in the deficient phase and the possibility of involving the grid in providing the minimum amount of emergency support based on information of individual phase-wise loadings and short-term load forecast for each phase. To achieve this objective, it is important to have a supervisory control layer, which can manage the power transfer among different phases as well as to and from the grid to achieve an overall dynamically balanced three-phase system with respect to the local distribution transformer. For this purpose, the main objective of this work is to develop and demonstrate an operational control strategy that can cater the physical balancing of a typical three-phase distribution network with/without requiring intervention from the grid side. This constitutes the sole objective of the current work.

7.2 Single-phase Residential Microgrids

An architecture of the three single-phase microgrids connected is shown in Fig.7.1, where the three single-phase microgrids are connected to their respective phases on the secondary side of a local distribution transformer. With local phase-wise generation from rooftop PV panels and their varying irradiance levels, unique load profiles and diverse use of storage units at various levels of the state-of-charge (SOC), the negative sequence current can inflict a great deal of stress at the local transformer. With high penetration of renewable energy in each phase as well as diversified phase-wise loads in the single-phase microgrids may draw different level of currents from this local transformer leading to phase imbalance. Therefore, under these conditions, phase balancing has become a much significant task to ensure reliable operation of substation equipment and to provide

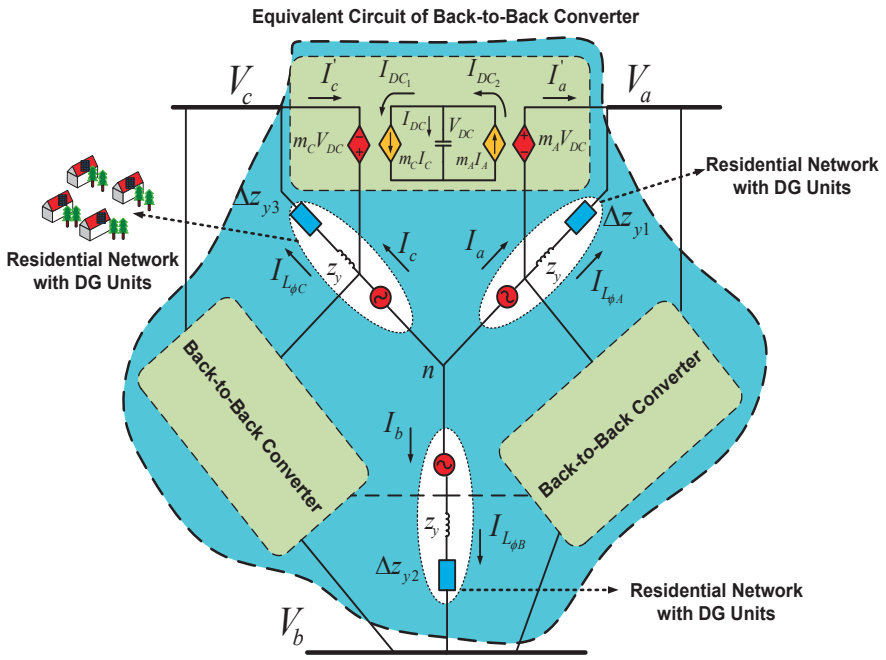


Figure 7.2: Proposed interfacing back-to-back between phases with its equivalent circuit.

high-quality power to all customers.

An equivalent circuit for the inter-phase power management for balancing individual phases using interconnecting back-to-back converters is shown in Fig.7.2. For an unbalanced wye-network with local generation and storage, the local DG sources are at the front end of a voltage controlled single-phase converter, represented by the three phases in Fig.7.2. Any mismatch between the generation and the local load consumption within a particular phase can be represented in terms of delta impedance, Δz_{y_1}, Δz_{y_2} and Δz_{y_3} in Fig.7.2, where these delta impedance can either be positive or negative.

This configuration has two major advantages. Firstly, dynamic balancing of phases can take place locally within the single-phase residential microgrids. This is not limited between only two phases. In fact, the phase with surplus power can provide necessary power to two deficit phrases simultaneously so that the three singe-phase microgrids only collectively draw the minimum amount of balanced power from the local distribution transformer. Whenever the three single microgrids collectively have surplus power, they can export desired amount of balanced power to the grid. Hence, a dynamically balanced three-phase is achieved. The tertiary control layer determines the surplus and deficient

phases and the offset power that needs to be imported from the other phase(s) to balance the system. This decision is made based on the criteria of available surplus power, SOC of the batteries, and short term load forecasting. Secondly, this layer also considers import of balanced power from the grid or export that to the grid.

In the current investigation, it is assumed that the local customers actively take part in the ancillary operation of balancing the residential microgrids of their community without bias to any local consumer. This includes aspects such as billing for power sharing, or priorities of receiving or exporting power. These administrative issues can be handled through an EMS in the form of regulations or contractual agreements. Even though important, they are not considered to be real-time operational issues, and therefore, are deemed to be outside the scope of the current investigation. Furthermore, it is assumed that the time taken for decision-making and the execution of the actual power transfer is much shorter than the time constants of load and generation changes in the phases.

7.2.1 Operating scenarios

In total, there are seven possible scenarios as summarized in Table 7.1. Herein, $P_{Gen_{\phi_x}}$ is the total power capacity in ϕ_x, where x is ϕ_A, ϕ_B or ϕ_C. $P_{grid_{\phi_x}}$ is the power imported from or exported to the grid by ϕ_x and $P_{load_{\phi_x}}$ is the loading in ϕ_x. Note that the following symbols are used to represent modes of operations for all the scenarios: "=" means a balanced condition with no need for any power transfer, "$\rightarrow$" means power transferred from the current phase to another phase; "$\leftarrow$" power received from another phase; and finally, "$\uparrow$" stands for exporting excess power to the grid and "$\downarrow$ for importing minimal amount of power from the grid through the local distribution transformer. Similar scenarios but with different phase combinations are also applicable, which are not repeated herein for brevity. The operating scenarios listed in Chapter 4 Table 4.1 did not take into account the grid support that can take place for possible phase balancing. Hence, the scenarios listed in Table 7.1, require a fresh analysis in terms of the strategies proposed

Table 7.1: Seven operating scenarios of three single-phase microgrids

Sr.	Scenario	ϕ_A	ϕ_B	ϕ_C
1.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} = P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} = P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} = P_{load_{\phi_C}} \end{cases}$	=	=	=
2.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} > P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} > P_{load_{\phi_C}} \\ P_{Gen_{\phi_A}} = P_{Gen_{\phi_C}} \end{cases}$	→	←	→
3.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} > P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} > P_{load_{\phi_C}} \\ P_{Gen_{\phi_A}} > P_{Gen_{\phi_B}}, P_{Gen_{\phi_C}} \end{cases}$	→	←	→
4.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} << P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} << P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} << P_{load_{\phi_C}} \end{cases}$	↓	↓	↓
5.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} >> P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} >> P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} >> P_{load_{\phi_C}} \end{cases}$	↑	↑	↑
6.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} > P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} = P_{load_{\phi_C}} \end{cases}$	→	←	=
7.	$\begin{cases} P_{Gen_{\phi_A}} + P_{grid_{\phi_A}} > P_{load_{\phi_A}} \\ P_{Gen_{\phi_B}} + P_{grid_{\phi_B}} < P_{load_{\phi_B}} \\ P_{Gen_{\phi_C}} + P_{grid_{\phi_C}} < P_{load_{\phi_C}} \\ P_{Gen_{\phi_A}} >> P_{Gen_{\phi_B}}, P_{Gen_{\phi_C}} \end{cases}$	→	←	←

in this chapter.

7.2.2 Objectives

With the seven possible operating scenarios established in Table 7.1, the core questions are:

1. How to select an appropriate phase(s) with surplus power to transfer the power to deficient phase(s)?

2. How much power is needed to be transferred from one phase to another phase?

3. How much power is needed to be transferred from one phase to the two other

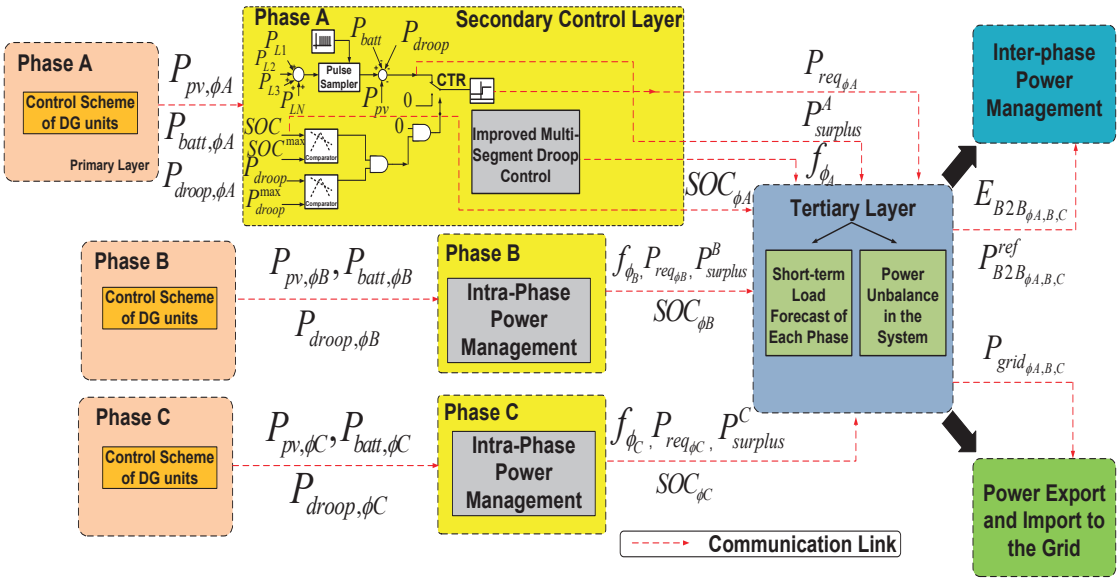


Figure 7.3: The proposed operational strategy over and above the primary and secondary control layer strategies.

phases?

4. How much power is needed to be transferred from the two power surplus phases to the power deficient phase?

5. How much power can be exported to the grid? and;

6. How much the minimal amount of power needs to be imported from the grid is required to balance the phases?

The objective of this chapter is to provide answers to the above questions by analyzing each scenario in Table 7.1 in detail within a framework of an operational strategy and also validate the effectiveness of these strategies through detailed simulation studies.

7.3 Operational Strategy for Balancing Residential Microgrids

A control and operational structure for single-phase residential microgrids is illustrated in Fig.7.3. It consists of a three tiered layers namely; primary, secondary and tertiary

layers. The primary control layer deals with the low level converter controls, which have been previously proposed by the same authors [125, 126, 133]. The secondary control layer makes use of the information of each DG unit from the primary layer and makes use of the previously developed improved multi-segment droop strategy to determine the frequency of each phase, SOC of the battery, the surplus power available in each phase or the power requirement in each phase. These key variables have represented by f_{ϕ_x}, SOC_{ϕ_x}, $P^x_{surplus}$ and $P_{req_{\phi_x}}$, where x represents either ϕ_A, ϕ_B or ϕ_C.

The tertiary control layer makes use of the information on the unbalance power in each phase to determine if a phase(s) can be balanced using either inter-phase power management alone, or with the help of power export/ import to the grid or both. If phases can be balanced by inter-phase power management only, the enabling and the power reference for the particular back-to-back converter are communicated through this layer. These signals are represented by $E_{B2B_{\phi A,B,C}}$ and $P^{ref}_{B2B_{\phi A,B,C}}$ in Fig.7.3. In fact, information on the short-term load forecast or generation can be incorporated at this stage to achieve more intelligent decision-making to anticipate the behaviors of the microgrids. If additional power is needed to be imported from the grid the power reference is set as $P_{grid_{\phi A,B,C}}$ by again taking into consideration the surplus phase(s) and the unbalance power required by the deficit phase. In the case of exporting power to the grid, the SOC of the batteries are evaluated against the maximum state-of-charge limits, denoted here as $SOC^{max}_{\phi_x}$. If the tertiary control layer detects that the battery has reached its SOC^{max}, any excess power from the PV unit can be exported to the grid. The logical flow of these concepts are illustrated in Fig.7.4.

Assuming that from the secondary layer it is determined that ϕ_B is unbalanced and requests the deficit power, $P_{req_{\phi B}}$, from the power surplus phase(s), as is shown in Fig.7.4. The selection of power surplus phase(s) that will contribute towards balancing ϕ_B is evaluated through power surplus variables in ϕ_A and ϕ_C, i.e. $P^A_{surplus}$ and $P^C_{surplus}$. This decision is made through a series of digital logic circuitry, as shown in the phase selection

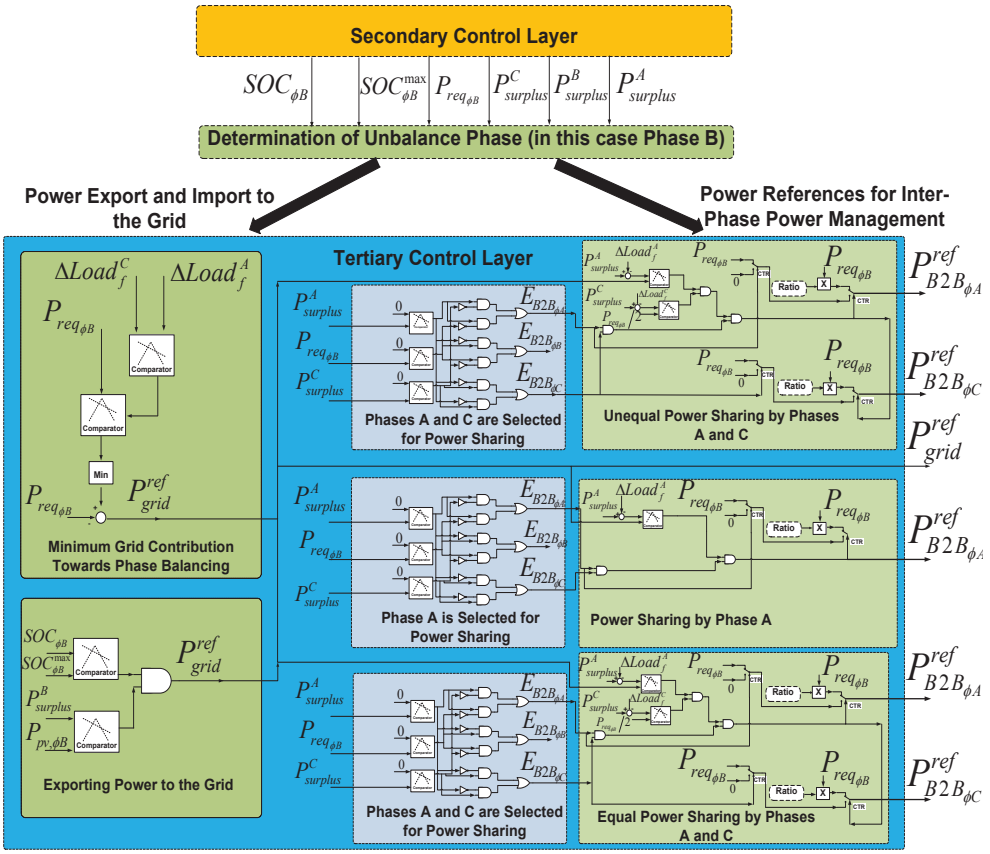


Figure 7.4: Detailed decision-making criteria of the proposed operational strategy for balancing residential microgrids.

blocks of Fig.7.4. At this stage, the enabling signals of the back-to-back converter(s), connecting the power surplus phase(s), are determined. Depending upon which phase(s) is selected, the power reference for the back-to-back converter is later calculated using the information of the short-term load forecast and the surplus power in the selected phase(s) and the deficit power in ϕ_B. This leads to either power sharing by one surplus phase or equal/unequal power contributions from the other phases. Furthermore, importing power from the grid is determined by the generation capacities of all the phases and their current loading profiles. If at any time instant, it is evaluated that the power surplus phase(s) previously contributing to ϕ_B, does not possess sufficient local generating power to balance ϕ_B, the equivalent power is requested from the grid. The grid reference, P^{ref}_{grid}, is set such that this power is delivered to each phase in equal amounts to keep the system balanced. Finally, if the battery's SOC in ϕ_B reaches $SOC^{max}_{\phi B}$, the surplus PV power is

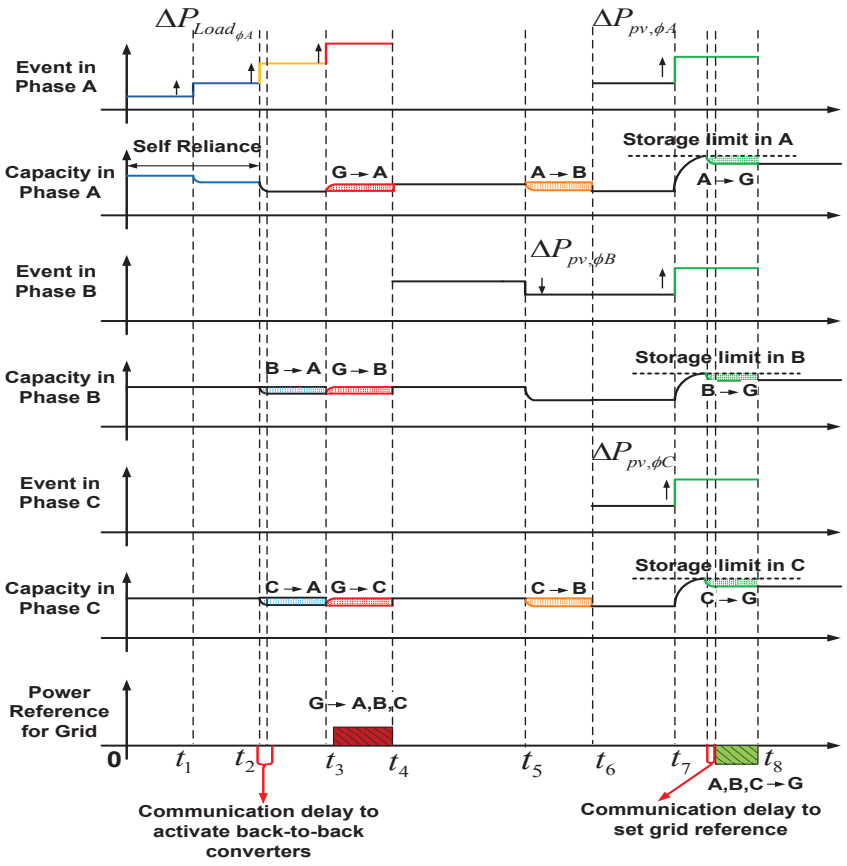


Figure 7.5: A timing diagram of the proposed hierarchical operational strategy illustrating the relative delays in processing the commands for intra- and inter-phase power management as well as the coordination with the grid.

then exported to the grid by setting the calculated reference power, P_{grid}^{ref}.

A holistic overview of the proposed operational strategy is shown in Fig.7.5. It illustrates the actions taken by both intra- and inter-phase power management strategies to balance a phase(s) as well as the relative communication delays in executing these actions. These concepts are shown for some of the cases that are tabulated in Table 7.1 but this can be considered as the basis for other cases as well except only with different operational conditions in each phase. The key variables in each phase are the changes in loading profile and atmospheric conditions, in terms of irradiance on the PV panels, with limitations on the storage capacities of the batteries in these phases. Changes in each of these variables are represented as an event in the three-phases. This operational structure also illustrates the communication delays in activating the back-to-back converters and setting the grid references for its contribution in balancing the system.

Between $t = t_1$ and $t = t_2$, the loading in ϕ_A increases by $\Delta P_{load_{\phi A}}$. In this scenario, the generation and storage in ϕ_A allows it to be self-reliant in handling this load change through the intra-phase power management. The capacity in ϕ_A reduces slightly as this load change is supported by the PV power available and the battery Hence, the primary and secondary control layers maintain the system operation, without any intervention of the tertiary layer.

Between $t = t_2$ and $t = t_3$, the loading in ϕ_A increases again, such that the generation and storage capacity in ϕ_A is unable to support this load change. This will trigger the tertiary control to coordinate the transfer of surplus power available in ϕ_B and ϕ_C to ϕ_A through the inter-phase power management. As a result, the capacities in the power surplus phases decrease to meet the power deficit in ϕ_A, while keeping the system balanced. The communication delay is inherent in the data flow from the secondary to the tertiary control layer and also from the latency in the network cables connecting the respective back-to-back converters. A typical network latency of $30ms$ is taken on top of data flow delays within each control layer.

As the load increases further between $t = t_3$ and $t = t_4$, the capacities in all the three-phases are unable to rectify the imbalance in ϕ_A. As a result, grid support is required to maintain system balance. The grid supplies power in equal amount, which is illustrated as increase in capacities in all the three phases. The communication delay in setting the grid references is again due to network latency as well as local frequency synchronization procedures before grid power can be imported.

At $t = t_5$, there is a sudden change in PV power available in ϕ_B. This can happen due to sudden cloud cover or shading from the surrounding structures. An increase in local phase loading can make ϕ_B unbalanced. In this scenario, excess power from other surplus phases can be used to balance ϕ_B by activating the back-to-back converters.

At $t = t_7$, there is a sudden rise in PV power in all the three-phases, resulting in the batteries to be charged to their storage limits. The excess PV power and storage capacity

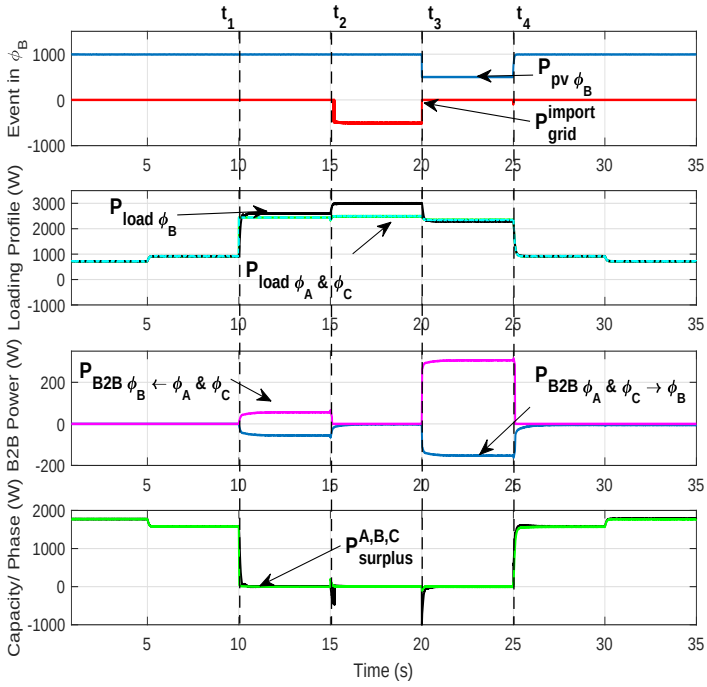


Figure 7.6: Simulation results for initial phase balance condition, two phases sharing power equally/unequally with the deficit phase and importing power from the grid conditions.

available in the system is now utilized by the tertiary layer to export it to the grid but in a balance way. This is represented by the negative power reference with respect to the grid, as shown in Fig.7.5.

7.4 Validation of the Strategies by Simulations

Detailed residential microgrids with hybrid PV/battery droop units in each phase, with interconnecting back-to-back converters, have been simulated in PSCAD/EMTDC. The simulation time step is kept at $0.5\mu s$. The simulations validates various scenarios as tabulated in Table 7.1, with the results shown in Figures 7.6-7.9 to validate the proposed hierarchical operational strategy. Step changes in loads are used in all cases.

7.4.1 All phases are in balance

Assume that initially all three-phases are operating in a steady-state and each phase has sufficient capacity to meet its load demand prior to a load change as shown in Fig.7.6.

Between $t = 0s$ and $t = t_1$, the PV and battery units, in each phase, are capable of supporting the loads through the intra-phase power management strategy. As the load profile increases in each phase, the generation and storage capacity of these phases decreases but with respect to the local distribution transformer, the phases appear to be balanced. Since, local generation and storage is sufficient to serve the loads, there is no need for inter-phase power management, through the tertiary layer. Hence $P_{B2B_{\phi_A \& \phi_C \rightarrow \phi_B}} = 0W$ as shown in Fig.7.6. This validates case#1 as listed in Table 7.1.

7.4.2 Two phases share power equally/unequally with deficit phase

Following from the previous case, at $t = t_1$, the loading in ϕ_B abruptly increases beyond the total generation capacity of that phase, as illustrated in Fig.7.6. There is a net power requirement of $106W$ in ϕ_B, as represented by $-106W$ in the phase capacity graph. At $t = t_1$, the load profiles of ϕ_A and ϕ_C are such that these phases possess surplus power. The tertiary layer identifies this and enables the back-to-back converters connecting the power surplus phases with the deficit phase, through the inter-phase power management. The power transferred from both ϕ_A and ϕ_C is represented by $P_{B2B_{\phi_A \rightarrow \phi_B}}$ and $P_{B2B_{\phi_C \rightarrow \phi_B}}$ in Fig.7.6. The total power received by ϕ_B is represented by $P_{B2B_{\phi_B \leftarrow \phi_A, \phi_C}}$. At this stage, all the three-phase possess, $106W$ in surplus generation capacity and appear to be balanced from the local distribution transformer standpoint. This validates cases#2 in Table 7.1. With different loading profiles in ϕ_A and ϕ_C, it can be shown that unequal power sharing from surplus power phases take place with ϕ_B, which is case#3 in Table 7.1.

A sudden cloud cover over the PV panels in ϕ_B is represented at $t = t_3$ in Fig.7.6. This loss in PV power causes ϕ_B to be short of $300W$ for its current load profile. ϕ_A and ϕ_C again have power surplus at this stage. Hence, the tertiary layer initiates the inter-phase power management to share this surplus power equally with ϕ_B. At this stage,

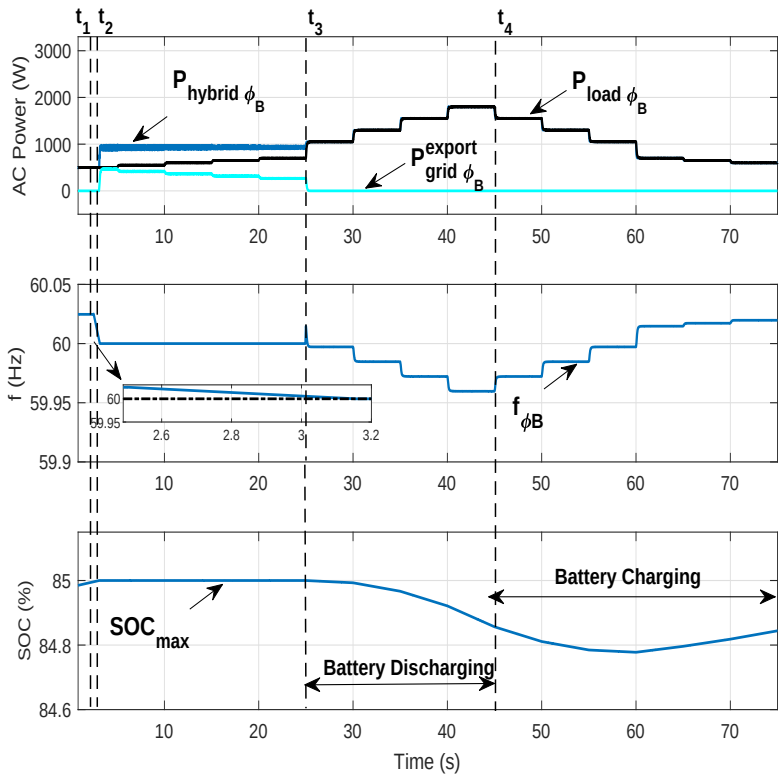


Figure 7.7: Performance of operational control strategy in exporting excess power from ϕ_B followed by intra-phase power management.

the phases are in balance again using the proposed operational strategy. From $t = t_4$ to $t = t_5$, the rated PV power is restored and the phases continue to balance themselves using the intra-phase power management strategy.

7.4.3 Importing power from the grid

At $t = t_2$, the loading in ϕ_B further increases, as shown in Fig.7.6. At this stage, the loading in ϕ_A and ϕ_C, exactly match the generation capacity of these phases. Hence there is no surplus power available to balance ϕ_B. At this stage, the tertiary layer prepares to import power from the grid. The net requirement of ϕ_B is $506W$. This power is imported from the grid and distributed equally amongst the three-phases. The surplus power now available in ϕ_A and ϕ_C is used to the charge the batteries, which are operating below their storage limits. This validates case#4 as tabulated in Table 7.1.

7.4.4 Exporting power to the grid

In this scenario, the SOC of battery in ϕ_B is close to SOC^{max} at the beginning of the simulation run. The results are shown in Fig.7.7. At $t = t_1$, the SOC reaches SOC^{max}, which is set at 85%. The loading at this instant is considerably low as compared to the PV power available, represented by P^{hybrid}_{pv,ϕ_B}. The tertiary control layer identifies that there is excess power available in ϕ_B and consequently initiates the process of transferring this power to the grid between $t = t_1$ and $t = t_2$. The frequency is regulated at 60Hz during this time, as shown in Fig.7.7. During this time, the power delivered to the grid is represented by P^{export}_{grid}. At $t = t_3$, the loading in ϕ_B increases such that both the PV and battery units need to support the load. The tertiary control layer, discontinues exporting power to the grid at this time. The frequency is regulated by the PV and battery hybrid unit as represented by $f_{\phi B}$. The battery starts discharging again and its SOC drops below SOC^{max}. At $t = t_4$, the load starts to drops further such the PV unit alone is capable of supporting the load. The excess power available during this time is used to charge the battery as shown in Fig.7.7. This validates case#5 as listed in Table 7.1.

A sudden increase in irradiance on the PV panels of all three-phases at $t = t_1$ can trigger the tertiary layer exporting power to the grid. Simulation results of ϕ_B are only shown in Fig.7.8. Considering that the storage limits of batteries in these phases is close to SOC_{max}, the excess PV power available is exported to the grid. The delay in exporting this power is due to the frequency synchronization of all the three-phases. Since the loading profile in all the three-phases is below the PV power available, the battery is in floating state after $t = t_2$ and does not contribute towards supporting the load.

7.4.5 Power surplus phase shares power with power deficit phase(s)

The simulation results for this scenario are illustrated in Fig.7.9. For this case, it is assumed that the SOC of batteries in each phase is operating well below the $SOC^{max}_{\phi_x}$. Before $t = t_1$, the load profile in each phase is supported by local generation and storage.

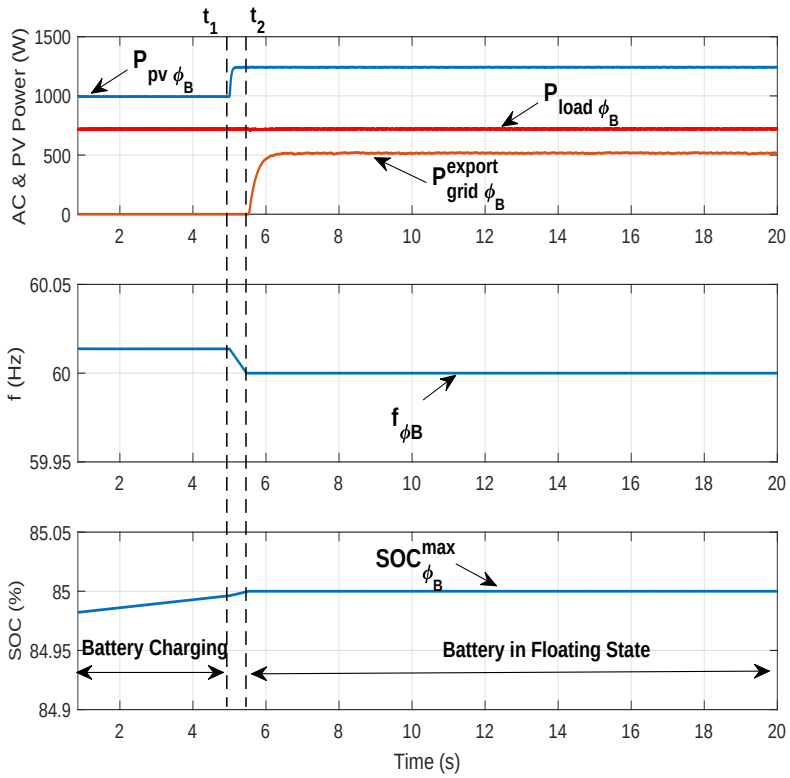


Figure 7.8: Performance of operational control strategy in exporting excess power from ϕ_B as a result of sudden change in PV power.

At $t = t_2$, there is a sudden change in loading for all the three-phases. ϕ_B is in deficit by $242W$, ϕ_A has excess $242W$ available while the loading in ϕ_C is completely supported by local generation and storage. The tertiary layer identifies that only ϕ_A is available for sharing power at $t = t_1$. Instead of balancing the system through the grid, the phases are able to do this task by triggering the enable signal, $E_{B2B_{\phi_A}}$, and setting $P^{ref}_{B2B_{\phi_A}}$=$242W$. The excess power transferred from ϕ_A to ϕ_B is represented by $P_{B2B_{\phi_A \rightarrow \phi_B}}$ in Fig.7.9 while $P_{B2B_{\phi_B \leftarrow \phi_A}}$ is the deficit power received by ϕ_B from ϕ_A. Between $t = t_1$ and $t = t_2$, the available capacity in each phase reaches zero after this exchange but the phases are autonomously balanced with respect to the local distribution transformer and without the intervention from the grid. This validates case#6 in Table 7.1.

At $t = t_2$, a sudden load change in both ϕ_B and ϕ_C causes these phases to require $242W$ from the ϕ_A. In this scenario, the tertiary layer identifies that again only ϕ_A is available for sharing power with ϕ_B and ϕ_C. This sets the enable signal, $E_{B2B_{\phi_A}}$.

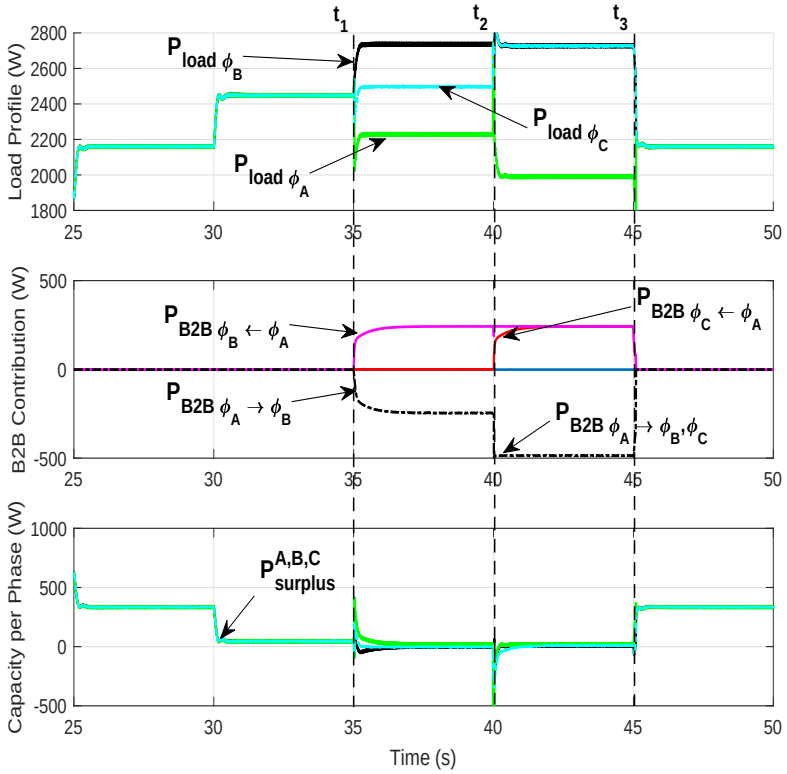


Figure 7.9: Simulation results for a power surplus phase sharing power with the deficit phase(s).

The power that is transferred to both ϕ_B and ϕ_C is represented by $P_{B2B_{\phi_A \& \phi_C}}$, while $P_{B2B_{\phi_B \leftarrow \phi_A}}$ and $P_{B2B_{\phi_C \leftarrow \phi_A}}$ is the excess power received by the deficit phases in Fig.7.9. It is illustrated that ϕ_A is capable of sharing power with multiple phases if required. This validates case#7 in Table 7.1.

7.5 Summary

This chapter has demonstrated that it is possible to achieve a dynamic phase balancing of residential microgrids with phase-wise PV and battery storages by using the back-to-back converter topology connecting among different phases. The phase balance can be achieved by allowing power sharing from power surplus phases to power deficient ones in a dynamic fashion with occasional minimal assistance from the grid. There are total of seven unique operating modes representing all possible scenarios considering different phase combinations. Furthermore, this configuration is flexible enough that, if the total

power production in the microgrids is more than the total load demands and no additional storages available, instead of curtailing the PV production, the surplus power can be exported to the grid in the balanced three phase form. Using this approach, regardless the load conditions, PV production, and state of battery storages in an individual phase, the three single-phase microgrids always appear to be balanced with respect to the substation. Therefore, the issues associated with phase imbalance in residential distribution networks can be avoided. The developed scheme has been validated through extensive computer simulation using full models of a distribution network and intermediate converters in PSCAD/EMTDC under all operating modes.

Chapter 8

Experimental Validation

To evaluate the performance of the developed back-to-back converter under different architectures, a series of experiments have been conducted. This chapter covers the development of such a converter at the laboratory scale. For this purpose, a step wise approach is taken before the main experiments are performed. The actual performance of the back-to-back converter is observed at system level test, through which the concept of transferring required power from the surplus phase to the deficit phase is validated.

8.1 Development of Back-to-Back Converter

The original architecture of the system as explained in Chapter 5 is show in Fig.8.1. This includes 3 back-to-back converters; one for each phase with phase-wise generation and storage. For the proof of concept, the experimental validation plan is devised in a way, whereby one back-to-back converter is developed to demonstrate the general concept of inter-phase power management strategy presented in this thesis. Furthermore, the DG sources and their control strategies are not implemented for simplicity purposes and to reduce the span of experimental validation stage. The supply connected to individual phases is a programmable AC supply, that acts as a voltage controlled source.

This section highlights the key elements used in the development of the back-to-back converter with their features and advantages.

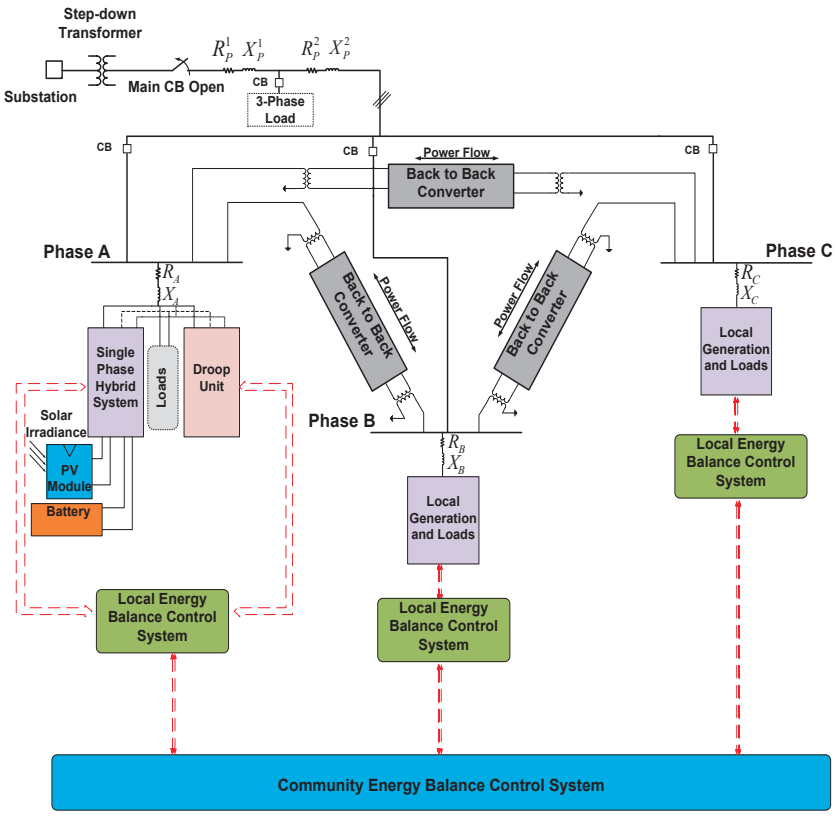


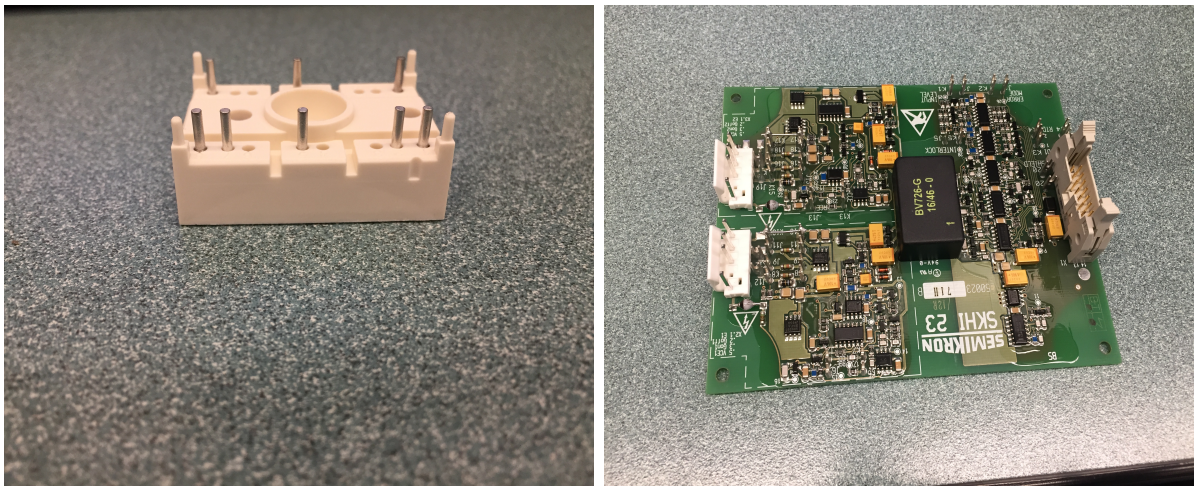
Figure 8.1: System architecture for residential microgrids with local DG units and inter-phase connection via back-to-back converters for power exchange.

8.1.1 IGBT module

The IGBT module used for the development of the back-to-back converter is SK25GH063 provided by SEMIKRON. Some of the main features of this module are that it is compact in design and allows for one screw mounting on to the heat sink or to the printed circuit board. This module has heat transfer and isolation through direct copper bonded aluminum oxide ceramic (DCB). This module consists of N-channel, homogeneous Silicon structure. It has relatively high short circuit capability. With a four IGBT stack, this module presents an ideal choice for the development of a low power back-to-back converter. A picture of SK25GH063 module is shown in Fig.8.2(a).

8.1.2 Gate driver board

The SK25GH063 IGBT module is compatible with SKHI23/12 gate driver board, shown in Fig.8.2(b). Its main features include; driving all SEMIKRON IGBTs with V_{CES} up to



(a) (b)

Figure 8.2: (a) SK25GH063 IGBT module and (b) SEMIKRON's SKHI23/12 gate driver that have been used for the development of the back-to-back converter.

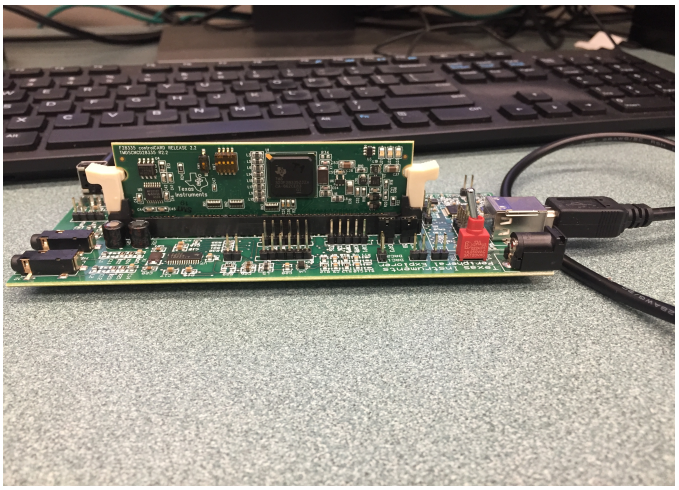


Figure 8.3: Texas Instruments (TI) microcontroller C2000 TMS320F28335

$1200V$. The on-board facilities include; double driver circuit for medium power IGBTs, also as two independent single drivers. It is compatible with both CMOS and TTL logic. The board processes short circuit protection mechanism. It provides isolation with on-board transformers, without using optocouplers. There is a supply under-voltage monitoring circuit available on the board as well. Driver interlock feature is also available on this board. The typical application, where this driver board can be used are for half and full bridge configurations.

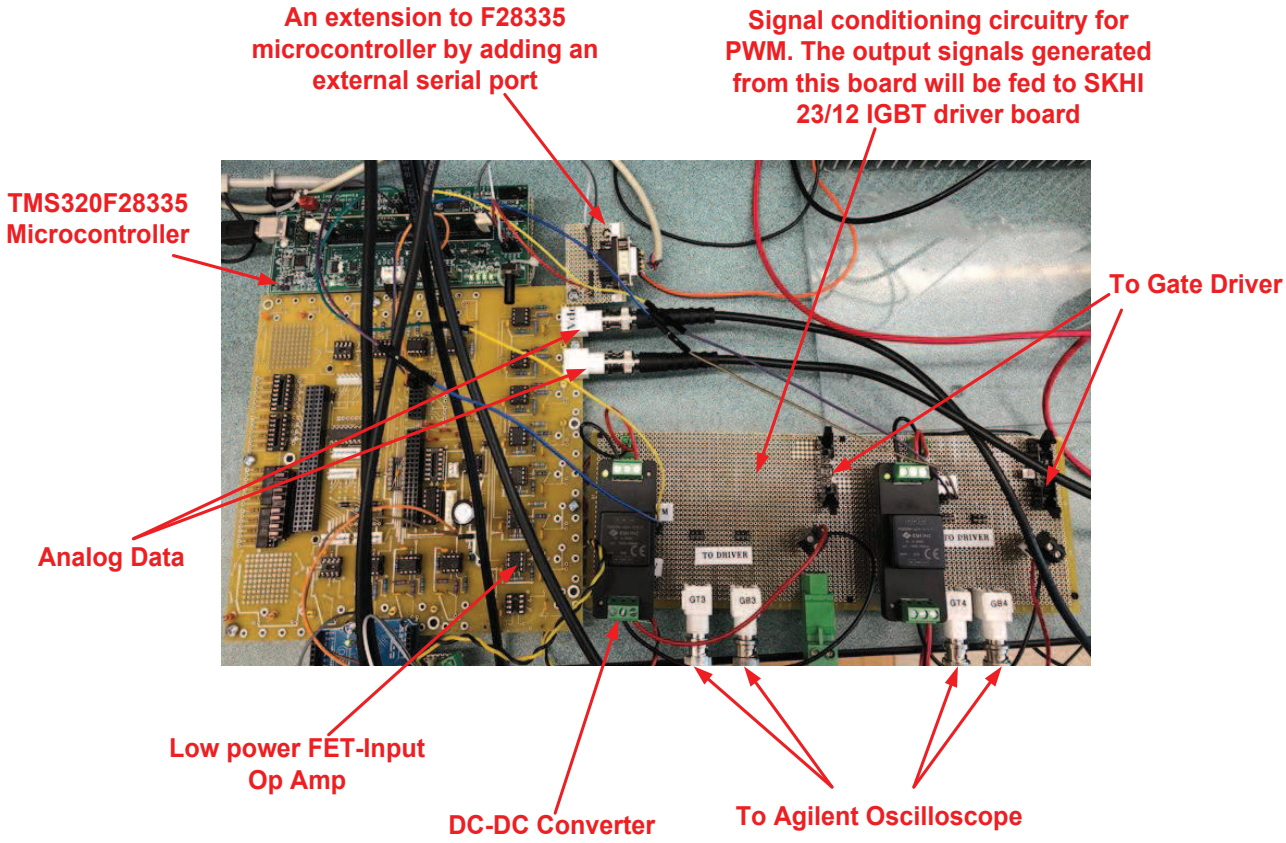


Figure 8.4: Signal conditioning board connected with F28835 microcontroller and analyzing the signals on the oscilloscope.

8.1.3 Texas Instruments (TI) microcontroller

The Texas Instruments (TI) C2000 series of a microcontroller based on Digital Signal Processing (DSP) is considered in this research, and is referred to as TMS320F28335 microcontroller. This 32-bit controller is optimized for processing, sensing and actuation to improve the closed-loop system performance in real-time control applications, such as those in the design and development of the back-to-back converter. This controller addresses some of the key elements required in for such a development including, analog-to-digital conversion (ADC) of input signal, comparators and pulse-width modulation (PWM) for gating signals. For the development of the back-to-back converter, the TMS320F28335 microcontroller makes use a modified vector control strategy to generate PWM signals to control the back-to-back converter. The personal computer running

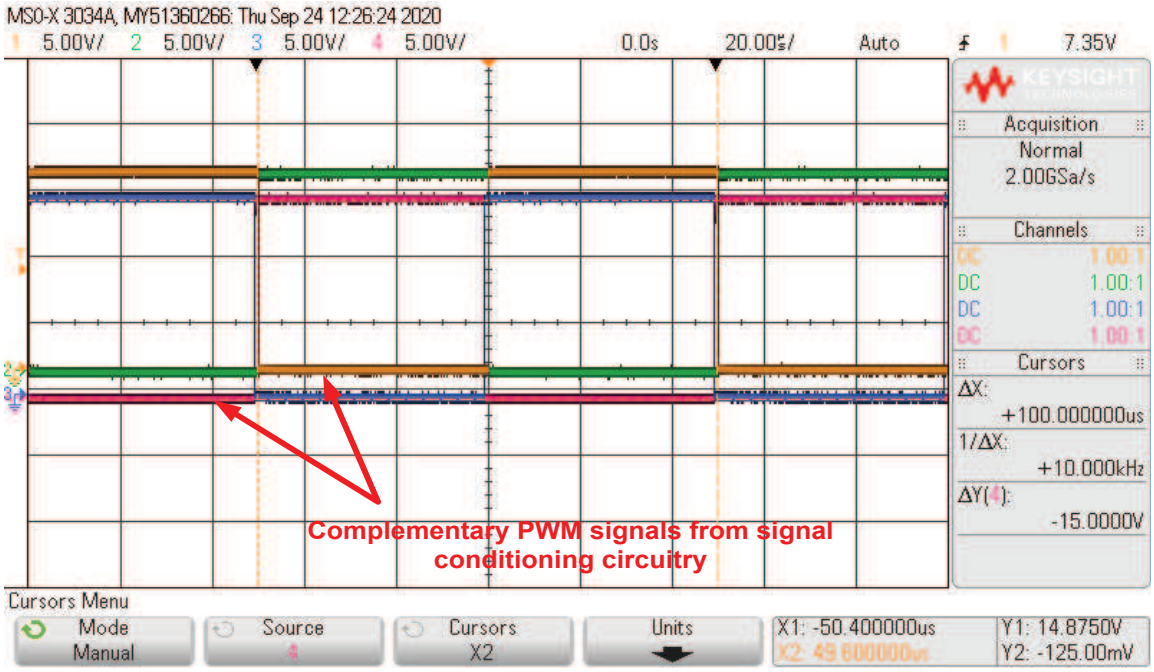


Figure 8.5: Results of 10kHz PWM signals level shifted to 0-15V as required by SKHI 23/12

MATLAB/Simulink for this purpose is referred to as Control Desk from here onwards.

8.1.4 Signal conditioning circuitry

The signal conditioning board for PWM signals is developed to make it compatible with SKHI 23/12 gate drivers for the IGBT modules. It is necessary that the gating signals are leveled at 0-15V instead of 0-3.3V as received from the TMS320F28335 microcontroller. In this respect, two boards are made (one for each side of the back-to-back converter). This is tested by making a simple complementary PWM signal generation program in Simulink and then power cycling the TMS320F28335 microcontroller. The interconnection of the circuitry is shown in Fig.8.4, while the converted PWM signals are shown in Fig.8.5.

8.1.5 Signal conditioning circuitry with SKHI23/12 gate driver

The signal conditioning board for PWM signals, that is described in section 8.1.4, is now used in coordination with the SKHI 23/12 gate driver board for the IGBT module. It

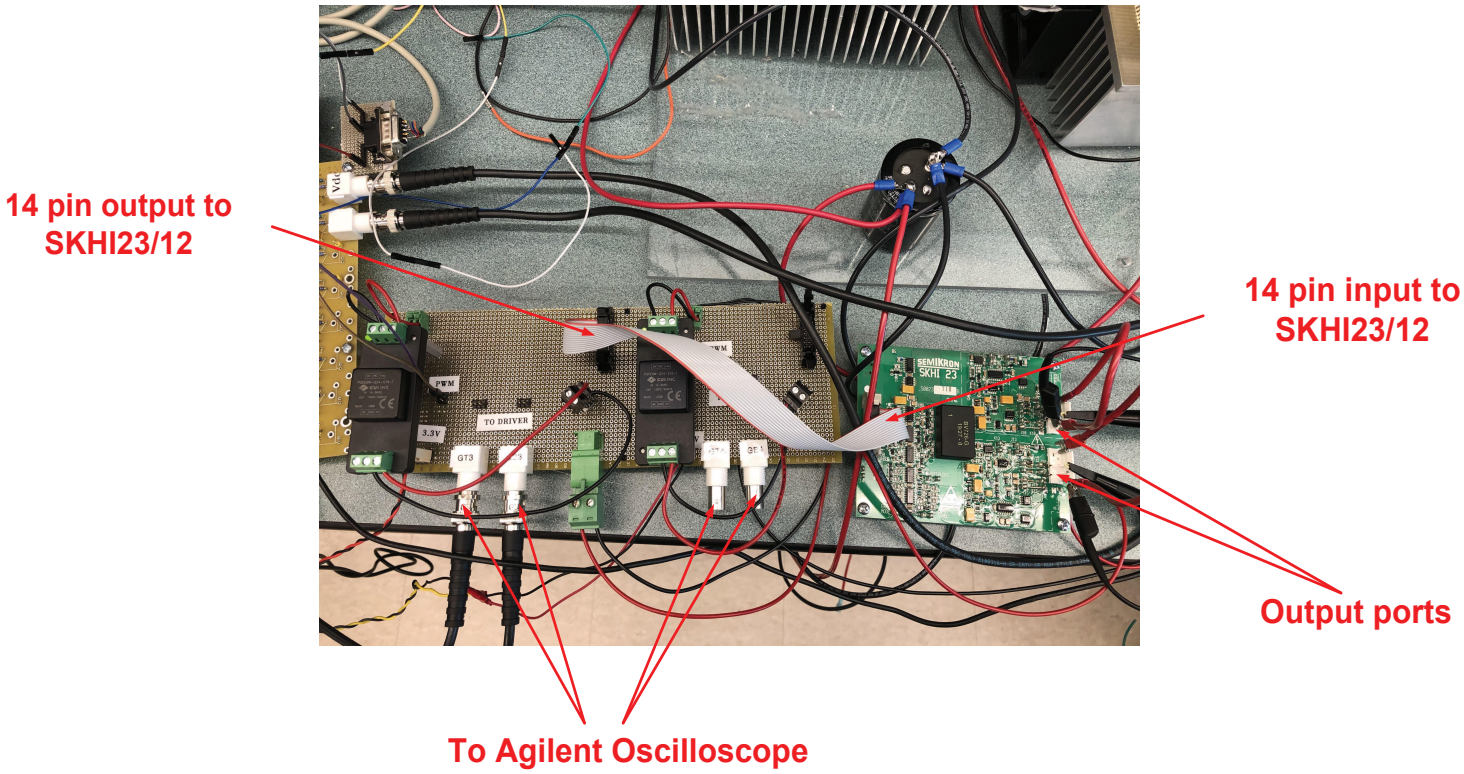


Figure 8.6: Signal conditioning board for SKHI23/12 gate driver.

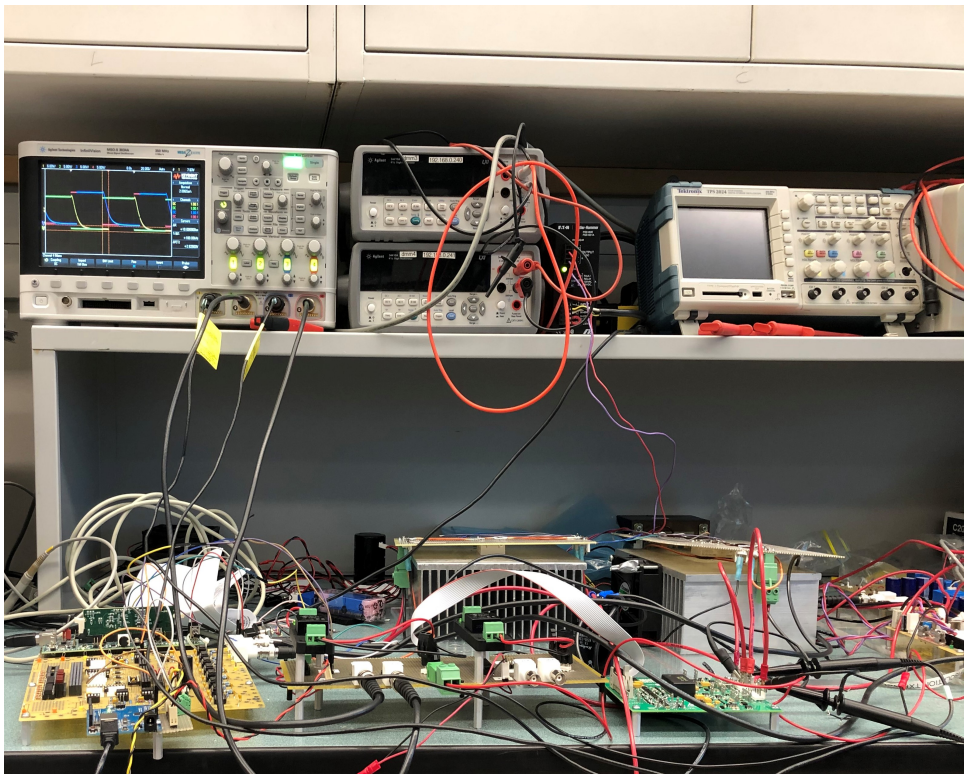


Figure 8.7: Signal conditioning circuit with SEMIKRON's SKHI23/12 gate driver.

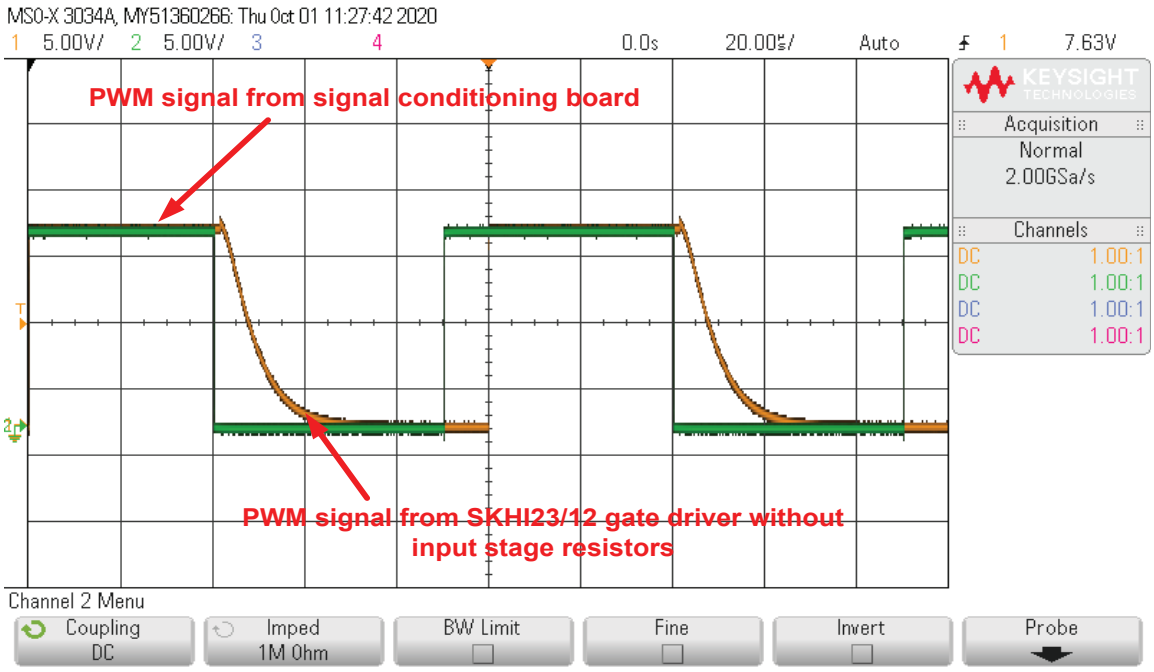


Figure 8.8: Results of 10kHz PWM signals level shifted to 0-15V and driver boards gating signals with dead time.

is necessary that the gating signals are leveled at 0-15V instead of 0-3.3V as received from the F28335 microcontroller. The functionality of the gate driver board is to provide the current drive capability to run IGBT module. It also provides isolation between the inputs to the SKHI23/12 driver board and the outputs to the IGBTs, using the on-board DC/DC converter. The setup for this experiment is shown in Figures 8.6 and 8.7. The results for the PWM generated from TMS320F28335 microcontroller and the output from gate driver are shown in Figures 8.8 and 8.9.

As it can be observed from Figures 8.8 and 8.9, the turn-off time introduced in the PWM signals is about $10\mu s$, as per the factory settings for the gate driver. This is later reduced to $0.9\mu s$ by adding additional resistors of $10k\Omega$ on the SKHI23/12 board on the input port, as suggested in the data sheet (see Appendix section 10.3).

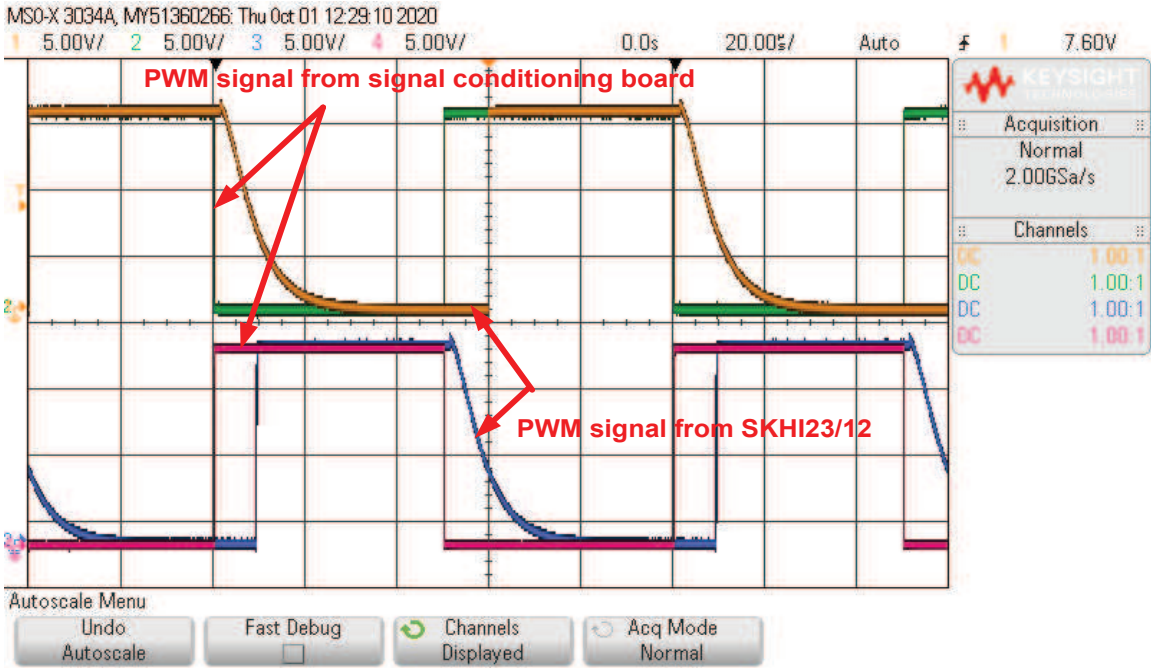


Figure 8.9: Results of 10kHz PWM complementary signals level shifted to 0-15V and driver board's gating signals with dead time.

8.1.6 Heat sink

The heat sink is determined based on the following steps:

1. The maximum ambient temperature that the IGBT can operate reliably is $125°C$ from the data sheet.

2. The assumption that the room temperature is $25°C$.

3. The temperature difference between junction and the room is $100°C$.

4. The junction to case thermal resistance is $0.23°C/W$ and the resistance between case and heat sink due to silicone compound is estimated to be $0.05°C/W$ (from the data sheet).

5. The power dissipation at the maximum current is 125.5 $°C$

6. The thermal resistance of the heat sink (R_{thsa}) is

$$R_{thsa} = \frac{125 - 25}{125.5} - (0.23 + 0.05) = 0.5168°C/W \tag{8.1}$$

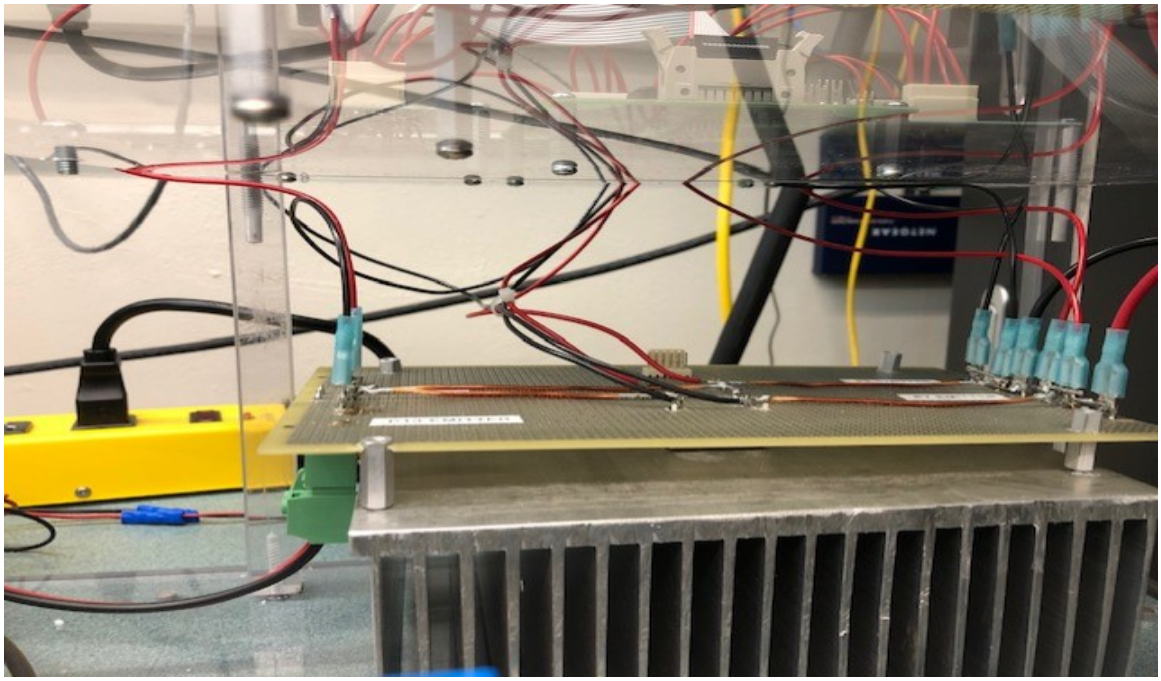


Figure 8.10: Mounting SK25GH063 IGBT module on the heat sinks.

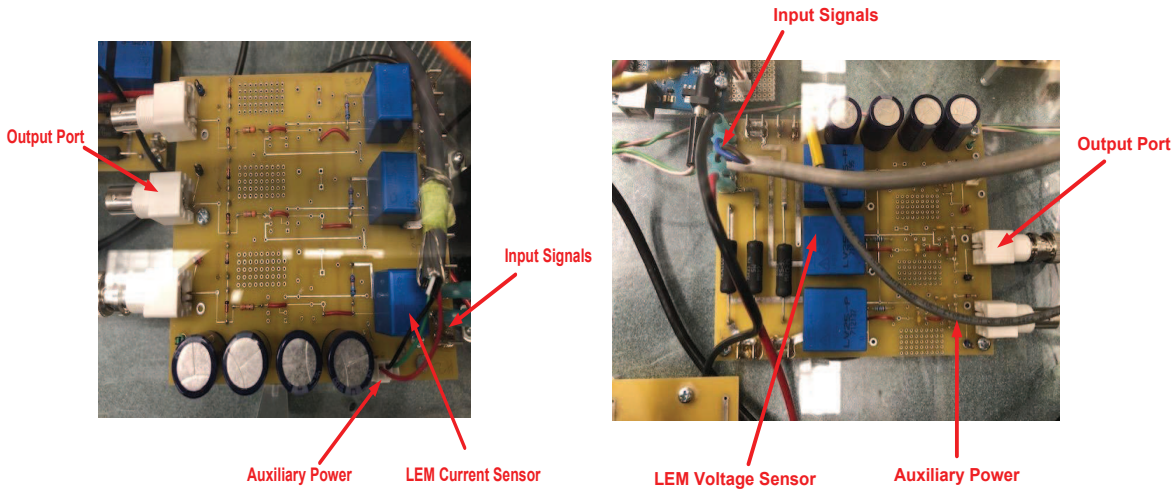
Therefore, a heat sink is selected with a thermal resistance or temperature rise less than $0.5168°C/W$ or $64.86°C$. Therefore, the heat sink provided by Wakefield-Vette 510-12U is used for this purpose, which has a thermal resistance of $0.24°C/W$.

8.1.7 Mounting SEMIKRON IGBT modules on heat sinks

The mounting of SEMKRON IGBT modules for the back-to-back converter is achieved by, firstly drilling a half an inch vertical hole into the heat sink to physically attach the module to it using a thin layer of heat sink compound. A perfboard is used for the interconnection of signals to the ports of IGBT module as shown in Fig.8.10. For stability purposes, 4 more holes were drilled into the heat sink for the spacers at each end of the perfboard.

8.1.8 Sensors

The voltage and current sensors are developed to measure the input and output voltage and current signals of the back-to-back converter. These are then interfaced with the



(a) (b)

Figure 8.11: (a) Current sensor board equipped with LA-20PB sensors and (b) Voltage sensor board equipped with LV-25P sensors.

TMS320F28335 microcontroller platform with proper signal conditioning circuitry. The current and voltage sensors make use of LEM sensors namely LA-20PB and LV-25P respectively and are shown in Fig.8.11. The voltage sensors are equipped with $5W$ power resistors of $5k\Omega$ for precise voltage readings to a maximum value of $175V$. For the voltage measurement of the DC link capacitor, this power resistor is rated at $6.5W$ and has a value of $40k\Omega$ for accurate readings to up to $440V$. In order to check the gains of LEM sensors, some experiments need to be performed. The following describes how to accurately find the voltage sensor gains. Same procedure can be followed to find the current sensors gains.

Using the BK Precision DC power supply, low voltage tests were performed to check the performance of the serial port acquisition using MATLAB program (see Appendix 10.9). At low voltages, the data acquired had a significant gain error. This is because, the LEM sensors give precise readings while it operates around its designed operating point i.e. when 10mA is flowing through the secondary windings of the sensor. The power resistor on the sensor board is $40k\Omega$, which gives precise readings when the DC voltage to be sensed is above 75 V. The control algorithm requires a headroom on the DC link voltage so that accurate readings can be obtained around 370V point as well.

Table 8.1: DC link voltage data acquisition using the sensor board

Input Voltage (V)	Output Voltage from Sensor (V)	Data received from Serial Port
50	0.310	51.6
100	0.623	100.9
150	0.930	149.7
200	1.230	198.4
250	1.548	246.5
300	1.856	299.8
350	2.165	349.5
400	2.470	399.1
450	2.780	449.4

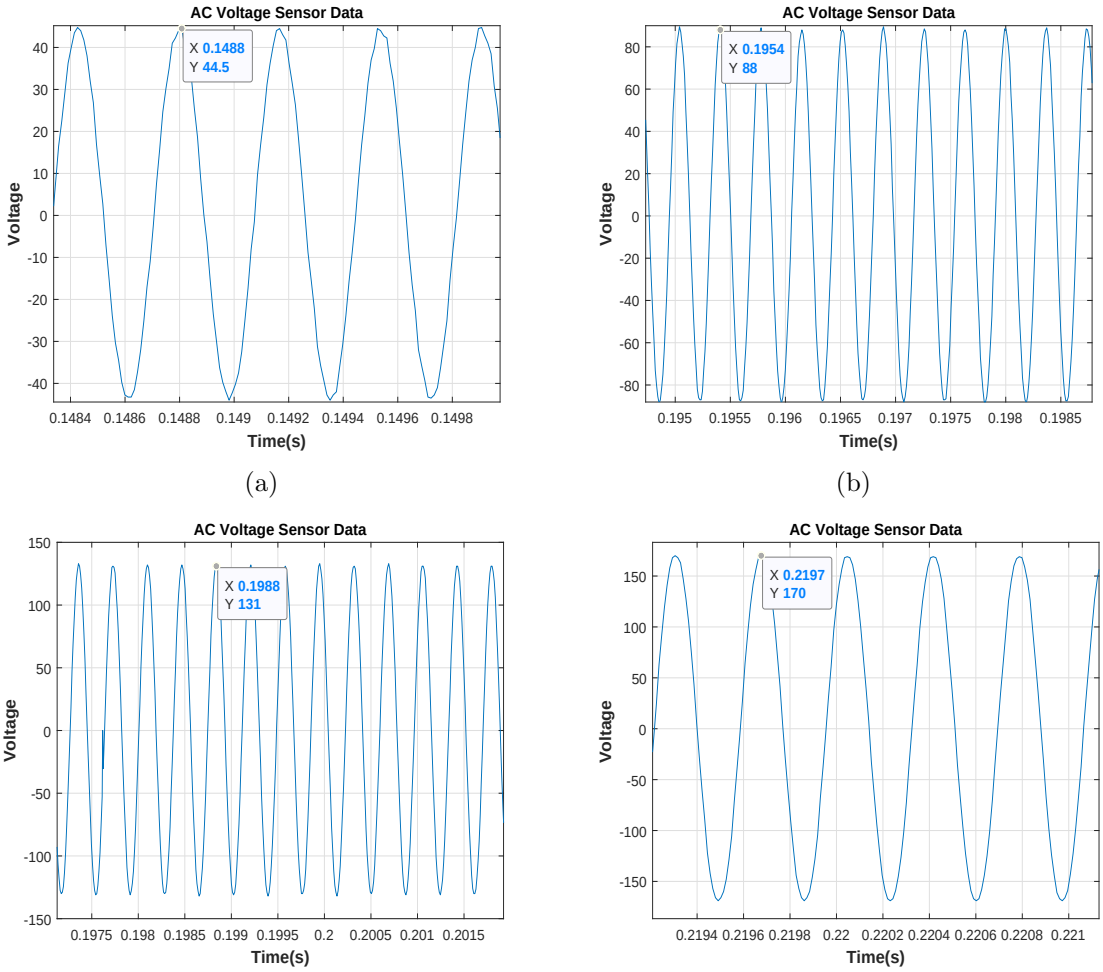


Figure 8.12: (a) Voltage sensor readings with an input voltage of $30V$ RMS, (b) Voltage sensor readings with an input voltage of $60V$ RMS, (c) Voltage sensor readings with an input voltage of $90V$ RMS and (d) Voltage sensor readings with an input voltage of $120V$ RMS.

By increasing the DC voltage using Sorensen DC power supply, the following readings are taken and tabulated in Table 8.1.

(a) (b)

Figure 8.13: (a) Bus bridge node before reconfiguration and (b) Bus bridge node after reconfiguration.

From Table 8.1 it is observed that gain adjustment has been correctly performed. The same procedure is carried out for sinusoidal input voltage. The output results from the serial port acquisition program are shown in Fig.8.12. From these results, it is concluded that the gain adjustment of sensors has been correctly performed and that the serial communication is able to capture the data packet as received and perform necessary operations on the incoming data stream. These operations include converting the data type from the 32 bit single data format to 32 bit floating point.

8.1.9 Bus bridge reconfiguration

The 3 pole, 4 wire bus bridge node in the lab is a point where the local distributed generations, inverters and storage devices can be segregated into 2 areas. The idea behind this design is basically to protect one region of the lab, where DG sources and storage devices are being used in experiments from the other region where these resources are not powered up. This bus bridge node provides an ideal location for placing the designed back-to-back converter by making use of one of the phases in this bus bridge. The advantage of using this node is to add protection and isolation between the phases

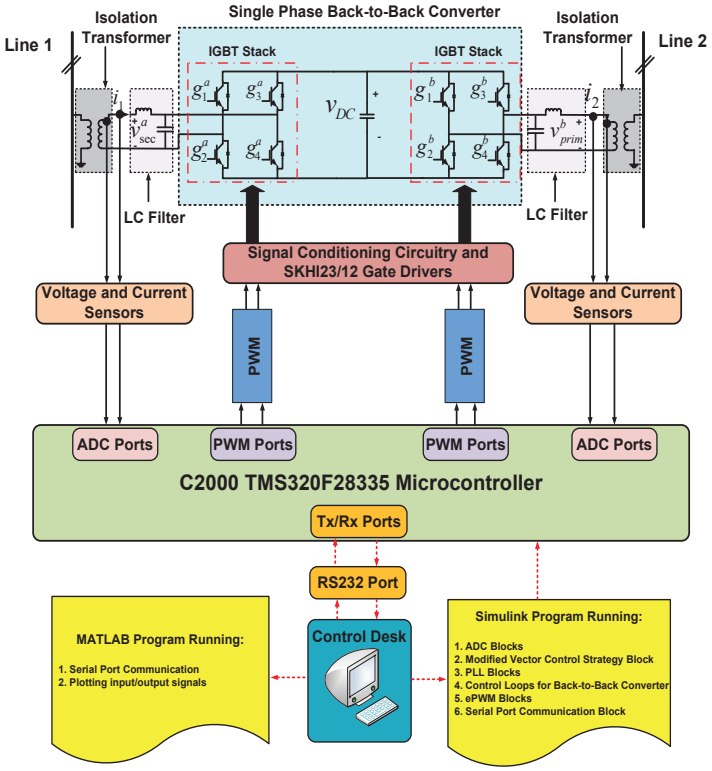


Figure 8.14: Overall hardware-in-the-loop architecture for the developed back-to-back converter.

while testing a prototype equipment. The initial state and wiring inside this bus bridge node is shown in Fig.8.13(a). The wiring inside in this node is subsequently altered to incorporate the back-to-back converter as shown in Fig.8.13(b).

Based on the detailed explanation of the elements required for the development of the back-to-back converter, the overall hardware-in-the-loop setup is setup as shown in Fig.8.14.

8.2 Test of Single-phase Isolation Transformers

The isolation transformers used between the sources for each phase are a crucial part of the experimental setup, as they provide the over-current protection with inbuilt circuit breakers and fuse assemblies. In this case, toroidal isolation transformers have been used for the experiments. Before any major experiments can be performed with the setup, it is necessary to first check the operation of these transformers under no load conditions.

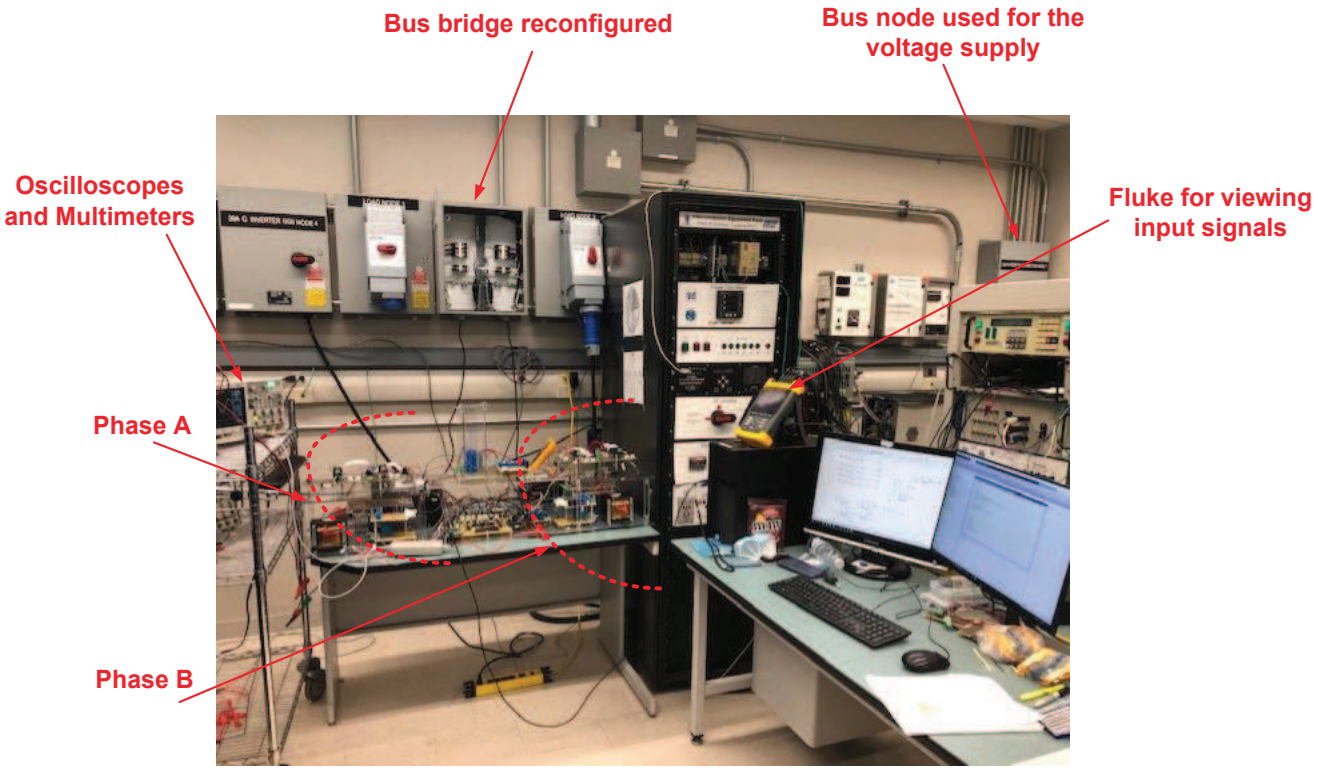
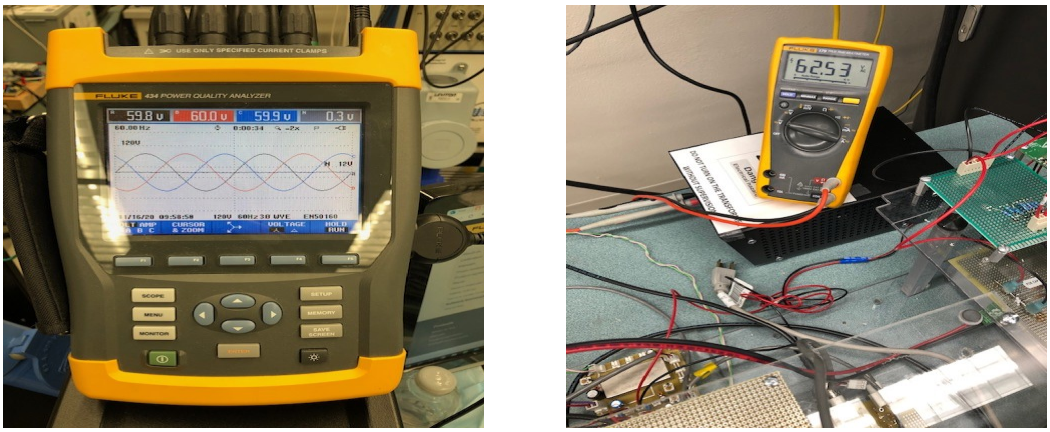


Figure 8.15: Setup for test of the isolation transformers.

Figure 8.16: AC voltage source.

The setup used for this experiment is shown in Fig.8.15. For this experiment, the AC source is connected on one end of the bus bridge by making use of the reconfiguration



(a) (b)

Figure 8.17: (a) Fluke scope view of low voltage input AC voltage and (b) Voltage RMS measurement for the input AC voltage.

as shown in Fig.8.13(b) and is labeled in Fig.8.15. This experiment is divided into two stages. The preliminary test checks the transformer at low voltage below the rated $120V$ conditions while the second at the rated voltage of $120V$. The AC voltage source is programmed for the low voltage test with 60.5V RMS voltage per phase as shown in Fig.8.16. The resulting sinusoidal input voltage is observed on the fluke power quality analyzer as shown in Fig.8.17(a). This is confirmed with the multi-meter measurement as well as shown in Fig.8.17(b). The sinusoidal output is then observed using high voltage differential probes on the oscilloscope. This is shown in Fig.8.18. From the oscilloscope measurements, it is concluded that the secondary side of the isolation transformer is free of any harmonics that could affect the operation of these transformers under loaded conditions.

The second experiment deals with the rated voltage of these isolation transformers. The AC voltage source is programmed to supply 120V RMS, which is observed on the Fluke meter. The sinusoidal output is then observed using high voltage differential probes on the oscilloscope. This is shown in Fig.8.19. From the oscilloscope measurements, it is concluded that the secondary side of the isolation transformer is free of any harmonics at the rated voltage under no load conditions.

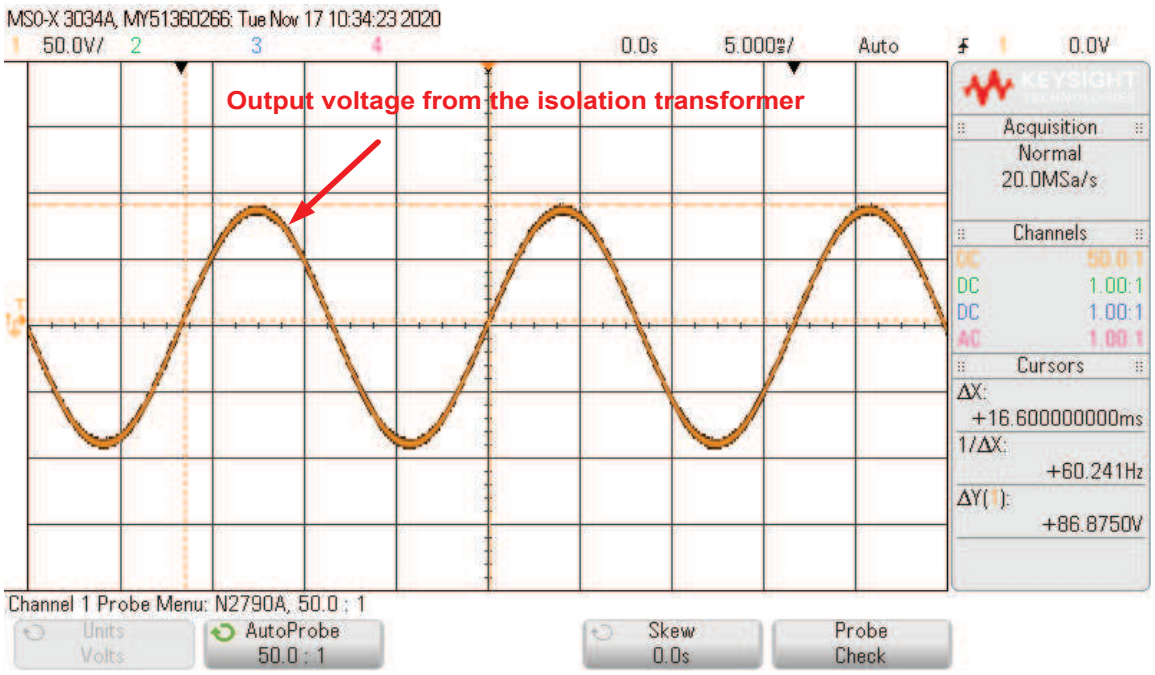


Figure 8.18: Low voltage oscilloscope measurement for the input AC voltage.

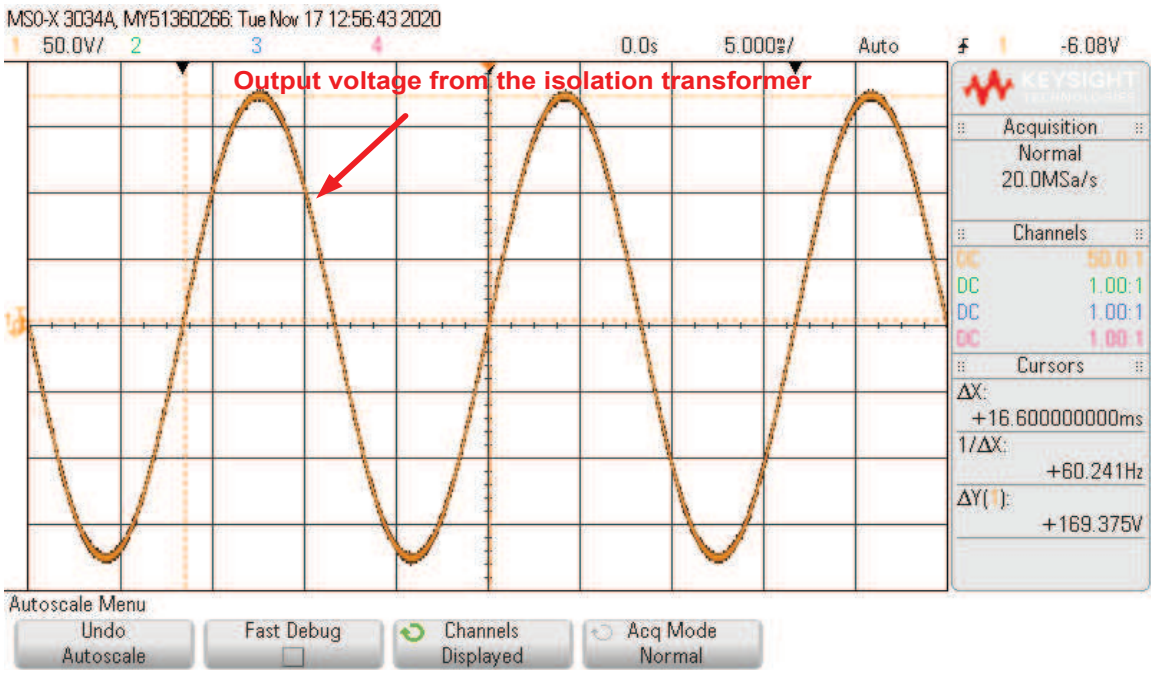


Figure 8.19: High voltage oscilloscope measurement for the input AC voltage.

8.3 Preliminary AC-DC Rectification Test

The purpose of conducting this experiment is to ascertain the proper operation of various elements that have been installed in the AC-DC side of the back-to-back converter. The

block diagram for this experiment is shown in Fig.8.20 while the overall setup for this experiment is shown in Fig.8.21. A closeup of the AC-DC side of the back-to-back converter is shown in Fig.8.22, where therein the interconnection of various elements such as the isolation transformer, SKHI23/12 driver board, the signal conditioning board, the voltage and current sensors, filter capacitor and inductor with the DC link are visible.

For this experiment, the control desk runs a MATLAB/Simulink based program, which covers the analog-to-digital conversion of various signals, data acquisition, the modified vector control scheme, phase locked loop, the voltage and current control loops that generate the gating signals for the SEMIKRON SK25GH063 IGBT module (see Appendix section 10.2). A screenshot of the Simulink program is shown in Fig.8.23, while the voltage and current loops are shown in Fig.8.24. The AC input is set at $50V$ on the programmable AC source. The Simulink program makes use of serial communication by making use of the RS232 protocol to communicate with the voltage and current sensors. Access to various variables on the serial port is made available through MATLAB program that converts the incoming data packet (identified by the start and end ASCII characters that are placed for each packet) from single precious format to floating point. The DC link voltage is the plotted and is shown in Fig.8.26. A reference voltage of $29V$ is given to the system. At $t = t_1$ the isolation transformer is turned on. The system reaches the voltage reference at $t = t_2$. At $t = t_2$, the system is turned off. It is observed that the DC link voltage decreases as it bleeds through the bleeding resistor, which is connected in parallel to the DC link capacitor. This experiment also verifies the effectiveness of modified vector strategy for single-phase systems.

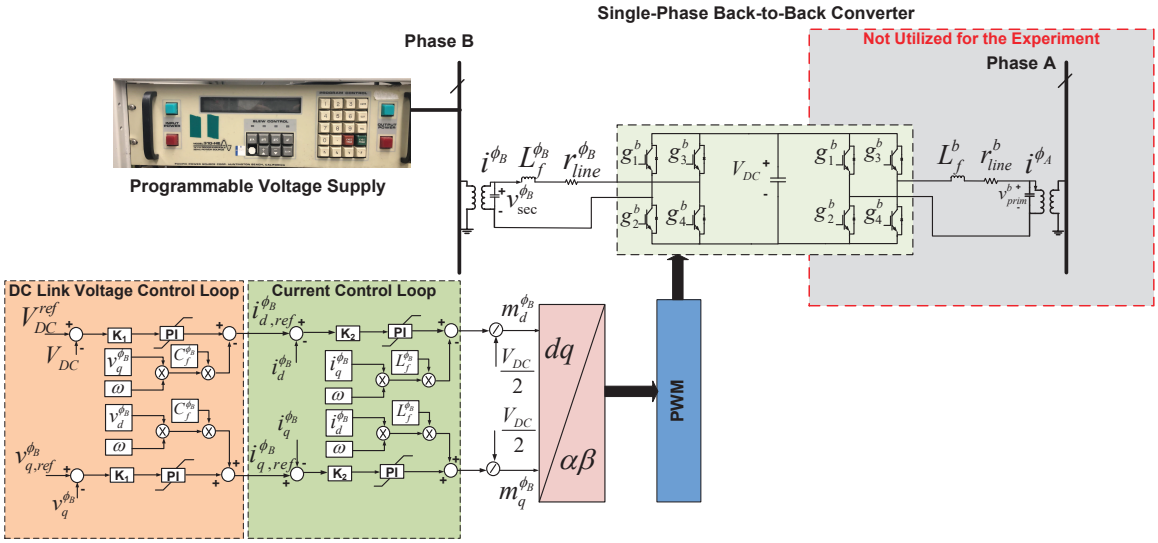


Figure 8.20: Block diagram for the preliminary AC-DC rectification test.

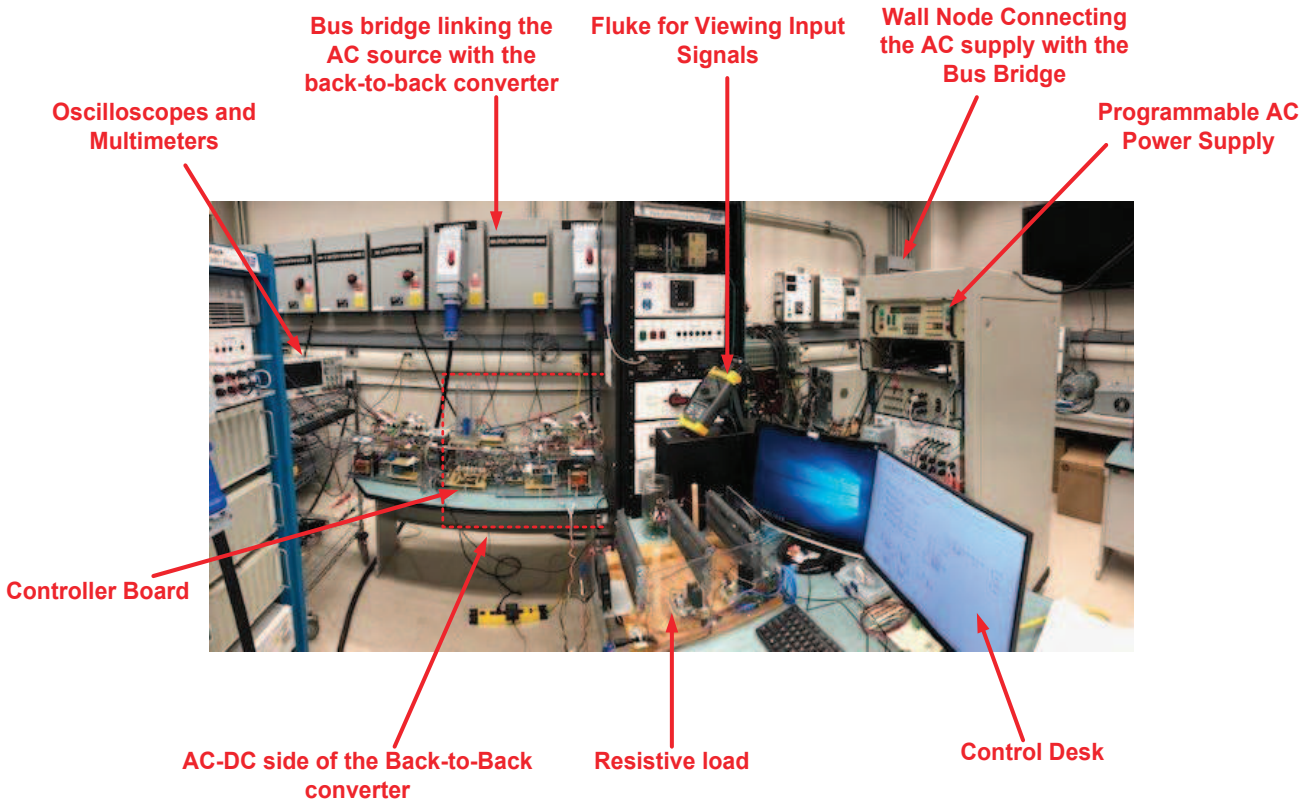


Figure 8.21: Overall experimental setup for the preliminary test.

8.4 Actual AC-DC Rectification Test

The actual AC-DC rectification test is next performed after the successful running of the preliminary test. For this experiment, the input AC voltage is set at $120V$ RMS

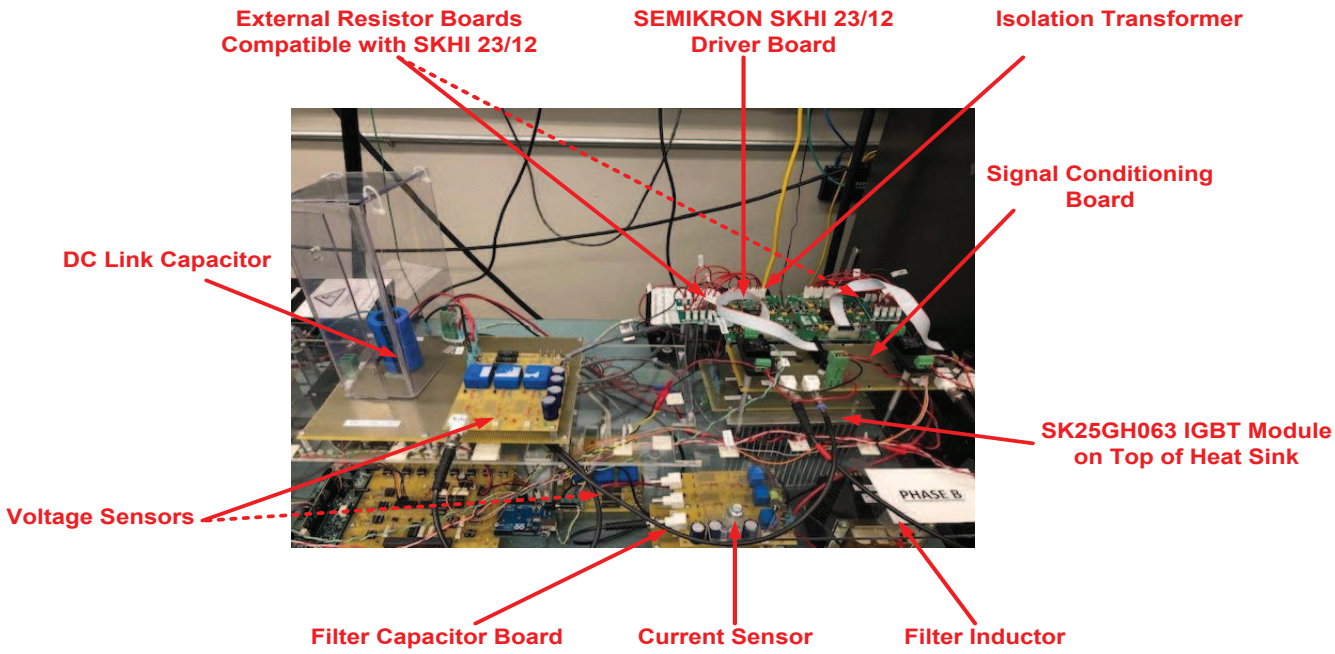


Figure 8.22: AC-DC side of the back-to-back converter used for the preliminary test.

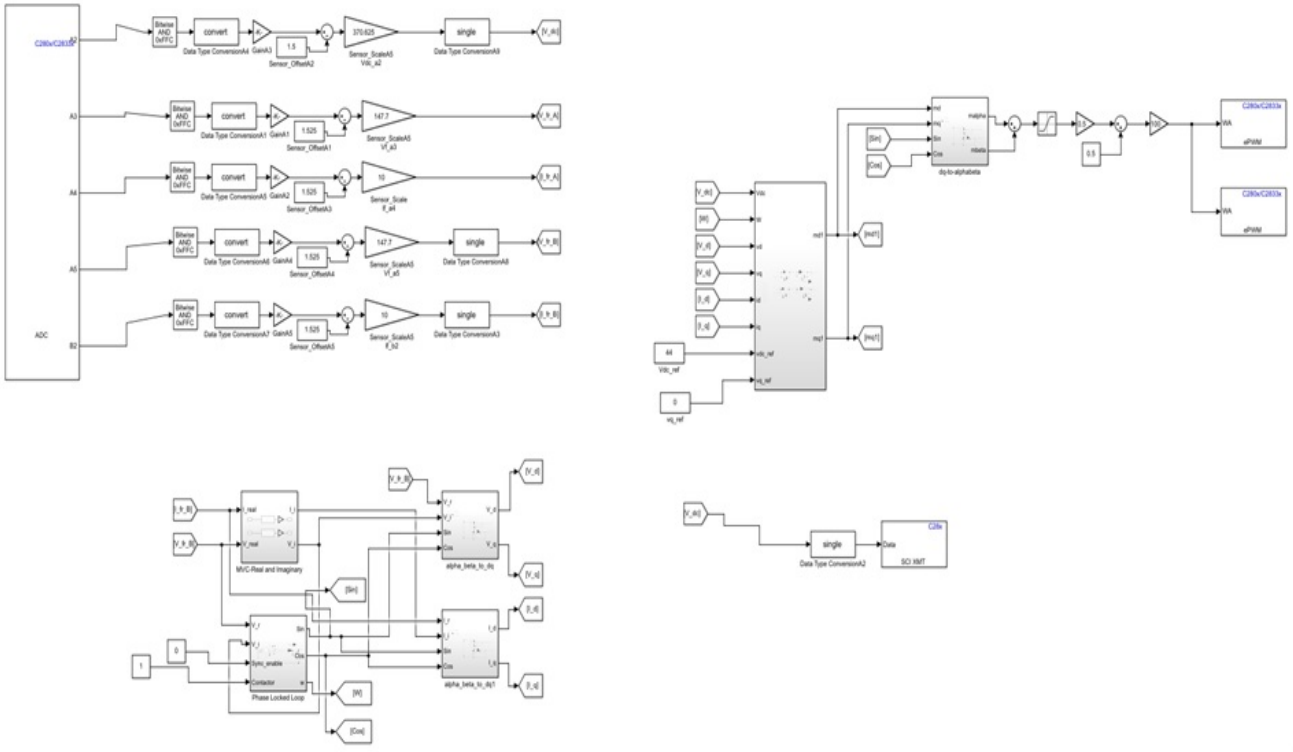


Figure 8.23: Simulink control program used for the preliminary test.

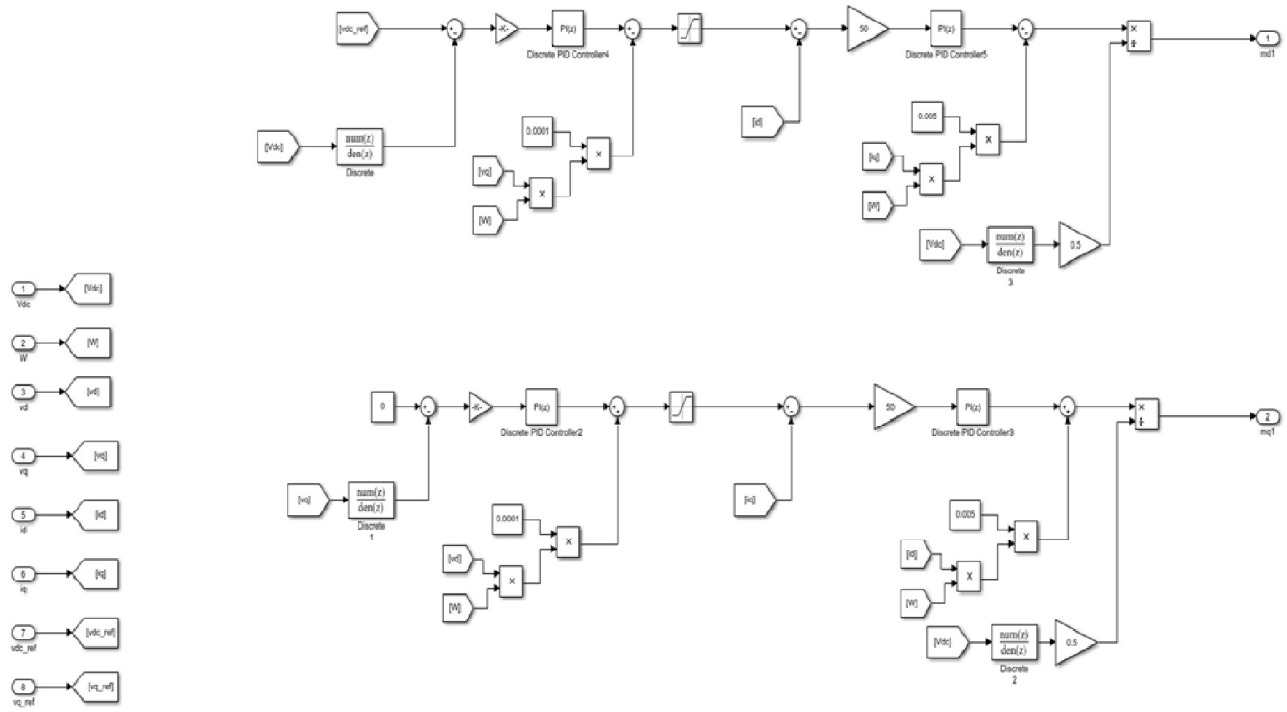


Figure 8.24: Voltage and current loops used for the preliminary test.

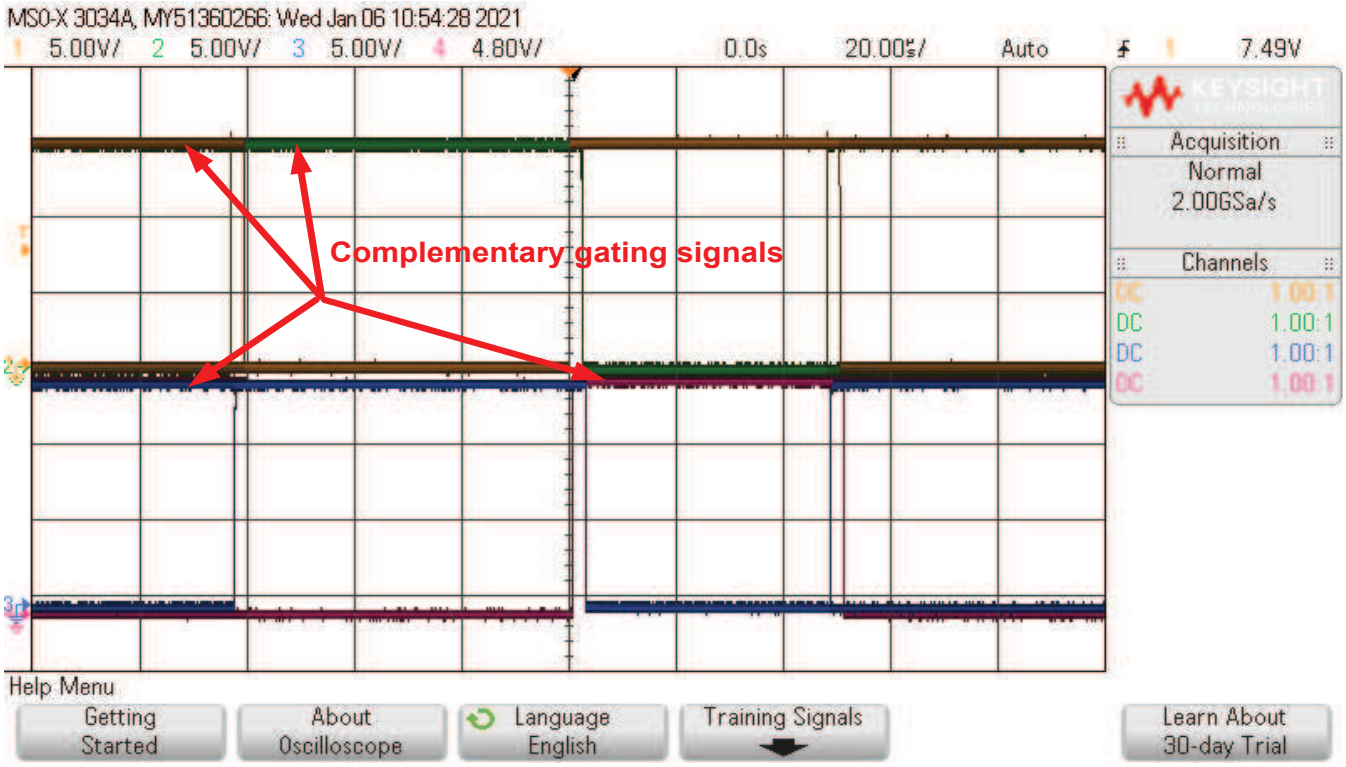


Figure 8.25: Gating signals as observed on the oscilloscope for the preliminary test.

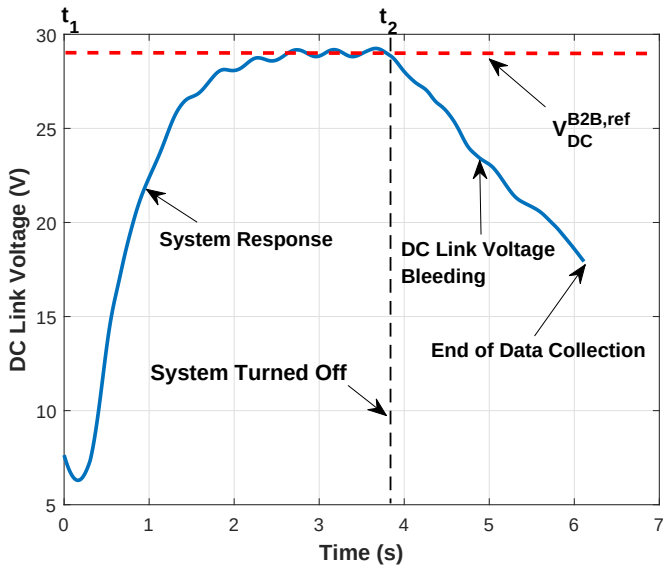
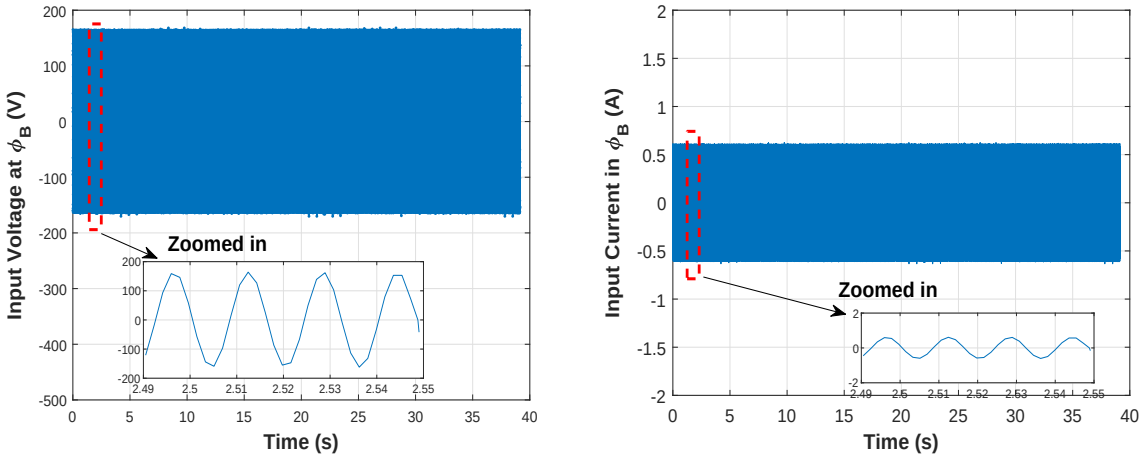


Figure 8.26: Result of the low voltage test, with the system turned on and then turned off.



(a) (b)

Figure 8.27: (a) Input voltage on ϕ_B and (b) DC Link voltage of the back-to-back converter.

with a current limit of $4.7A$ on the programmable AC source. The DC link voltage reference is set at $350V$. The input voltage on ϕ_B with a zoomed in version is plotted in Fig.8.27(a), while the current in ϕ_B is shown in Fig.8.27(b). DC link voltage is shown in Fig.8.28. At $t = 0$ the serial port communication is enabled and the data collection starts. Between $t = 0$ and $t = t_1$, is the system response as it tries to maintain $350V$ across the DC link capacitor. The system reaches the voltage reference at $t = t_2$ and stabilizes. The respective $d - q$ components for both the input voltage and current are

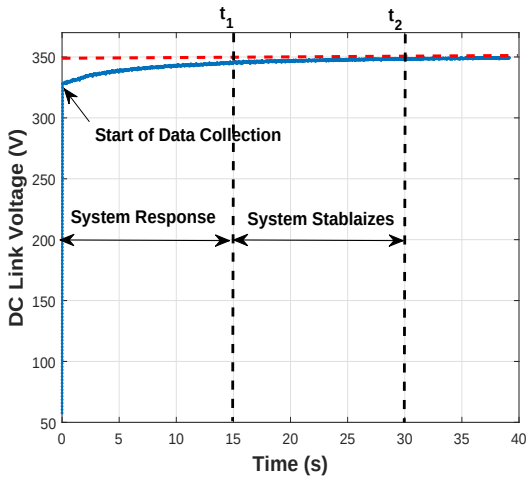
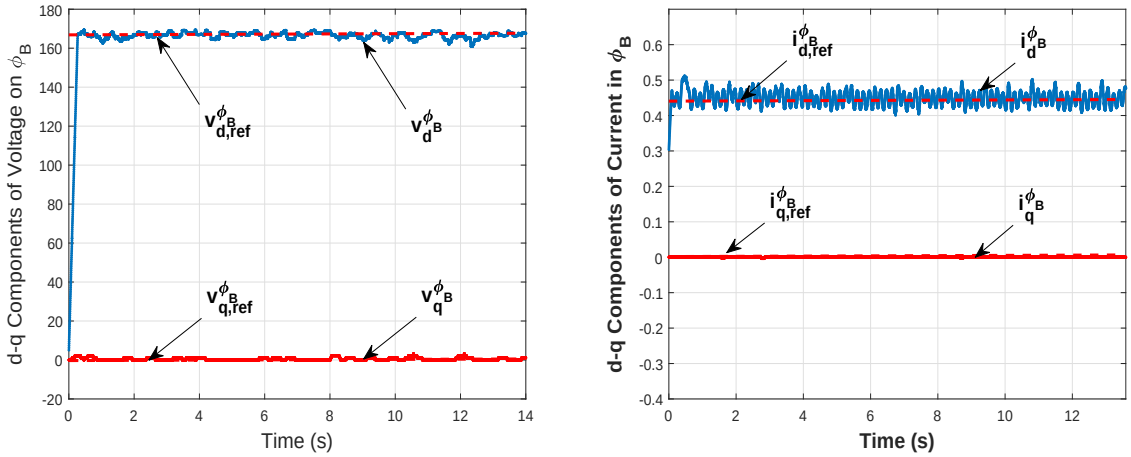


Figure 8.28: DC Link voltage of the back-to-back converter.



(a) (b)

Figure 8.29: (a) $d-q$ components of the input voltage and (b) $d-q$ components of the input current in ϕ_B of the back-to-back converter along with their specified references.

shown in Fig.8.29. It can be observed that system is able to set the desired references for individual signals very well and also verifies the effectiveness of modified vector strategy for single-phase systems in high voltage scenario. This experiment also shows that the voltage and current loops have been correctly configured for consequent experiments on the same equipment.

8.5 DC-AC Side of the Back-to-Back Converter

The next phase in the development of the back-to-back converter is the DC-AC side. In this respect, the same procedure is followed as in the case of the AC-DC side. The signal

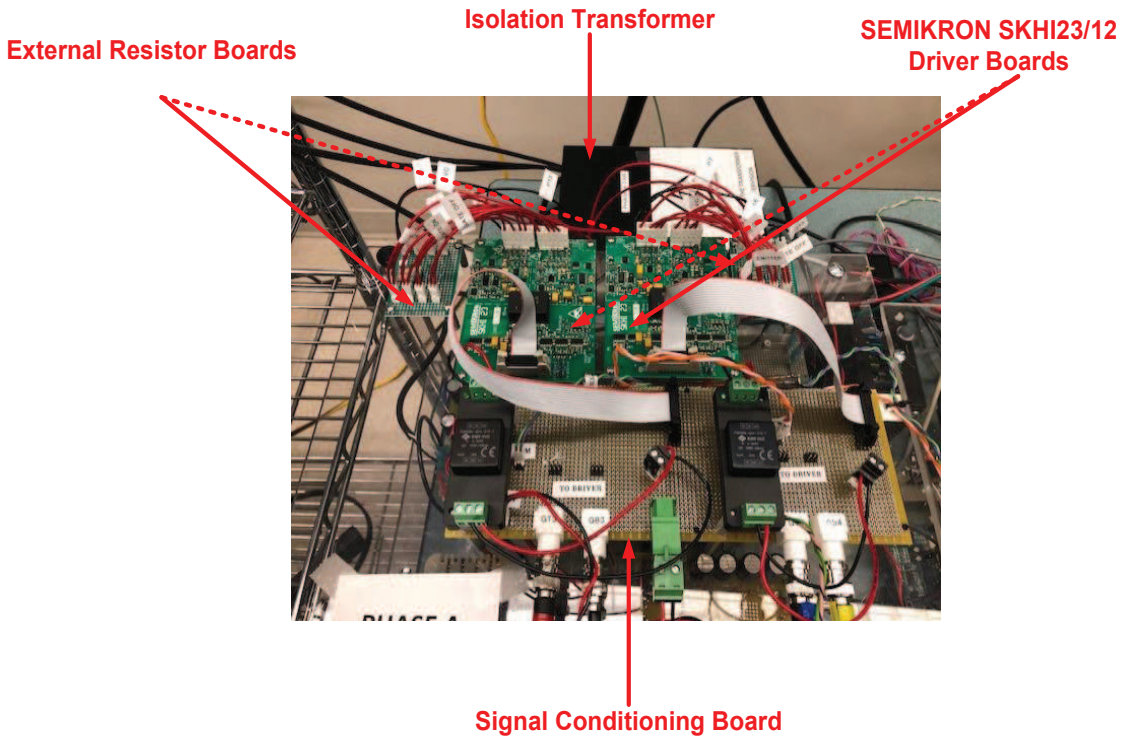


Figure 8.30: Signal conditioning board connected with SEMIKRON SKHI23/12 driver boards.

conditioning boards and the SEMIKRON gate drivers SKHI23/12 are utilized along with external resistor boards to be connected with the IGBT module as shown in Fig.8.30. The power circuit includes the filter inductor and capacitor along with the current and voltage sensors as shown in Fig.8.31. The overall setup for DC-AC side of the back-to-back converter is shown in Fig.8.32. Once the interconnections are complete, basic serial communication tests are performed, to make sure that the data from each sensor is collected correctly by the Simulink program. Furthermore, these tests also verify whether the sensor gains have been correctly calibrated or not.

8.6 Preliminary Unloaded Test

The purpose of this experiment is to ascertain the overall satisfactory operation of the back-to-back converter. The block diagram for this experiment is shown in Fig.8.33 while the overall setup for this experiment is shown in Fig.8.21. A closeup of the back-to-back

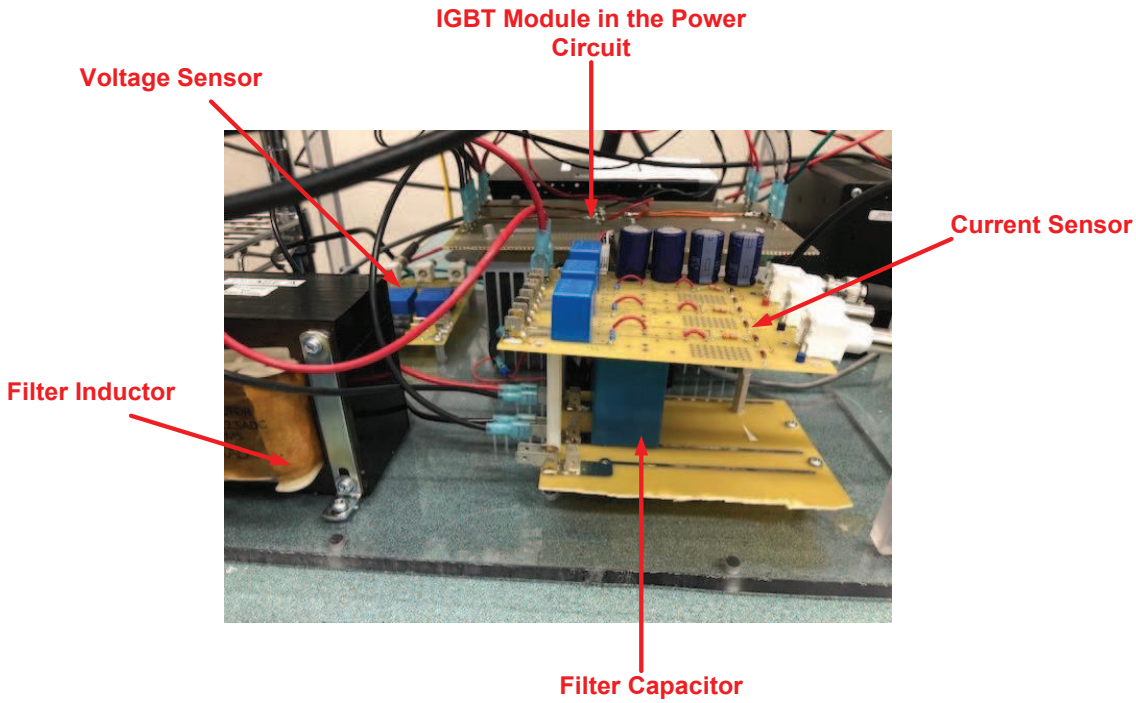


Figure 8.31: Power circuit board for DC-AC side of the back-to-back converter.

converter is shown in Fig.8.34, where therein the interconnection of various elements like the isolation transformer, SKHI23/12 driver board, the signal conditioning board, the voltage and current sensors, filter capacitor and inductor with the DC link is visible.

For this experiment, the control desk runs a MATLAB/Simulink based program, which covers the analog-to-digital conversion of various signals, data acquisition, the modified vector control scheme, phased locked loop, the voltage and current control loops that generate the gating signals for the SEMIKRON SK25GH063 IGBT module, as well as the control blocks for the AC-DC side and DC-AC side of the back-to-back converter. A screenshot of the Simulink program is shown in Fig.8.35, while the voltage and current loops for the AC-DC side of the back-to-back converter is shown in Fig.8.36. The AC input is set at $30V$ RMS on the programmable AC source, while a reference voltage of $11V$ RMS is set for the inverter side of the back-to-back converter. For this experiment, the back-to-back converter is operating under no load conditions. This experiment is conducted to check the response of the system as well the operation of the LC filters in

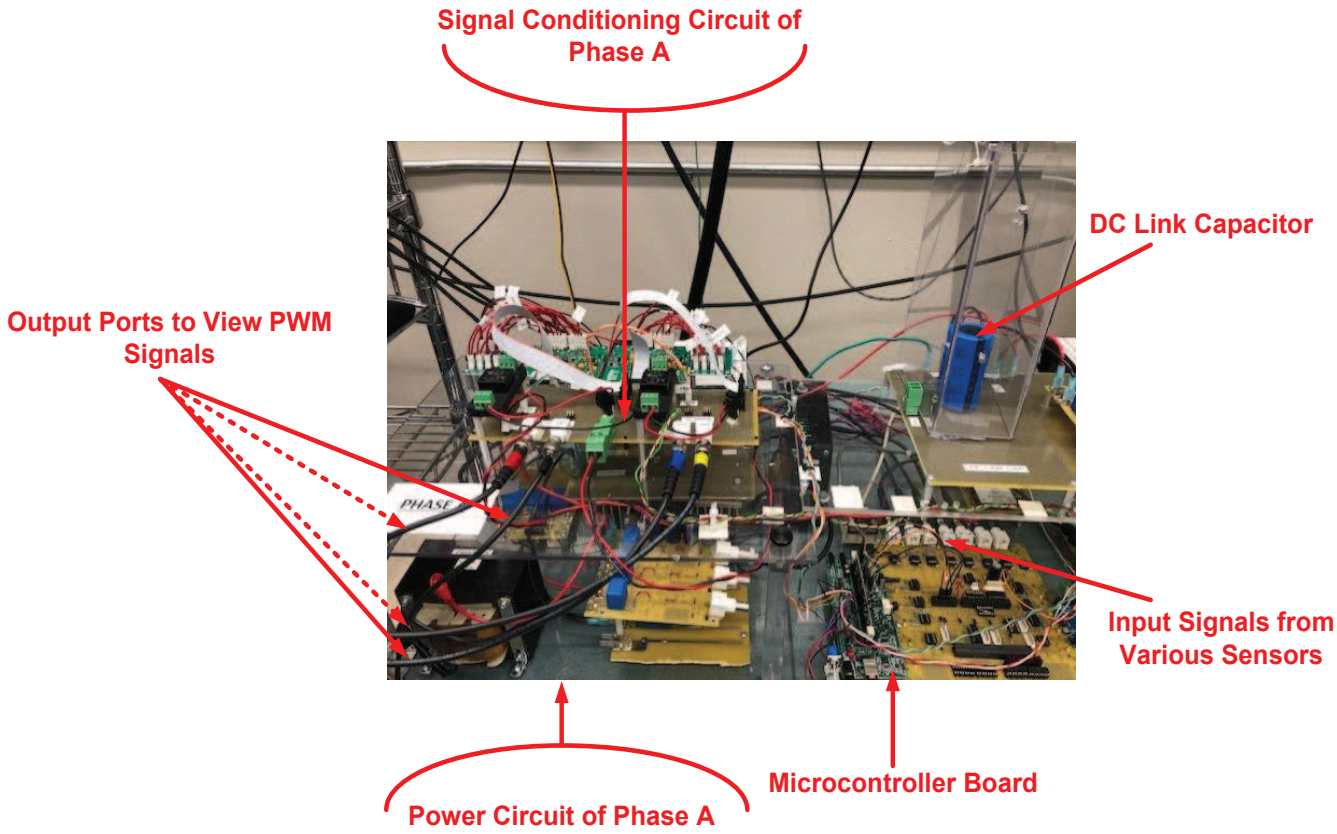


Figure 8.32: Overall setup of DC-AC side of the back-to-back converter.

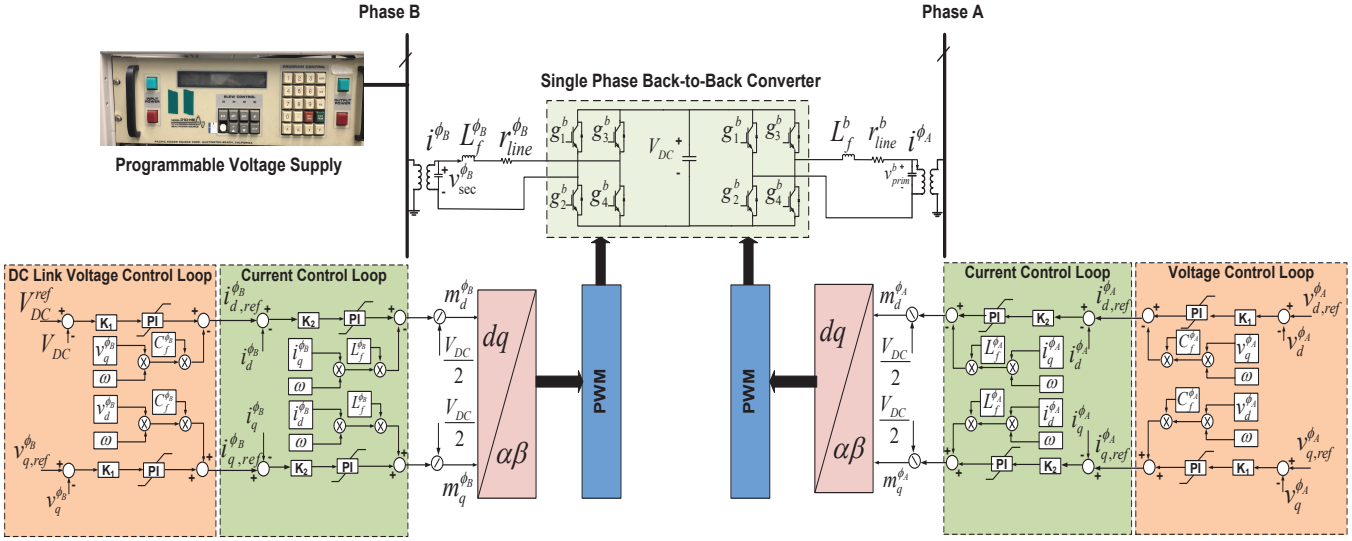


Figure 8.33: Block diagram for the unloaded preliminary test.

the circuits. The gating signals for both sides of the back-to-back converter are shown in Figures 8.39 and 8.40.

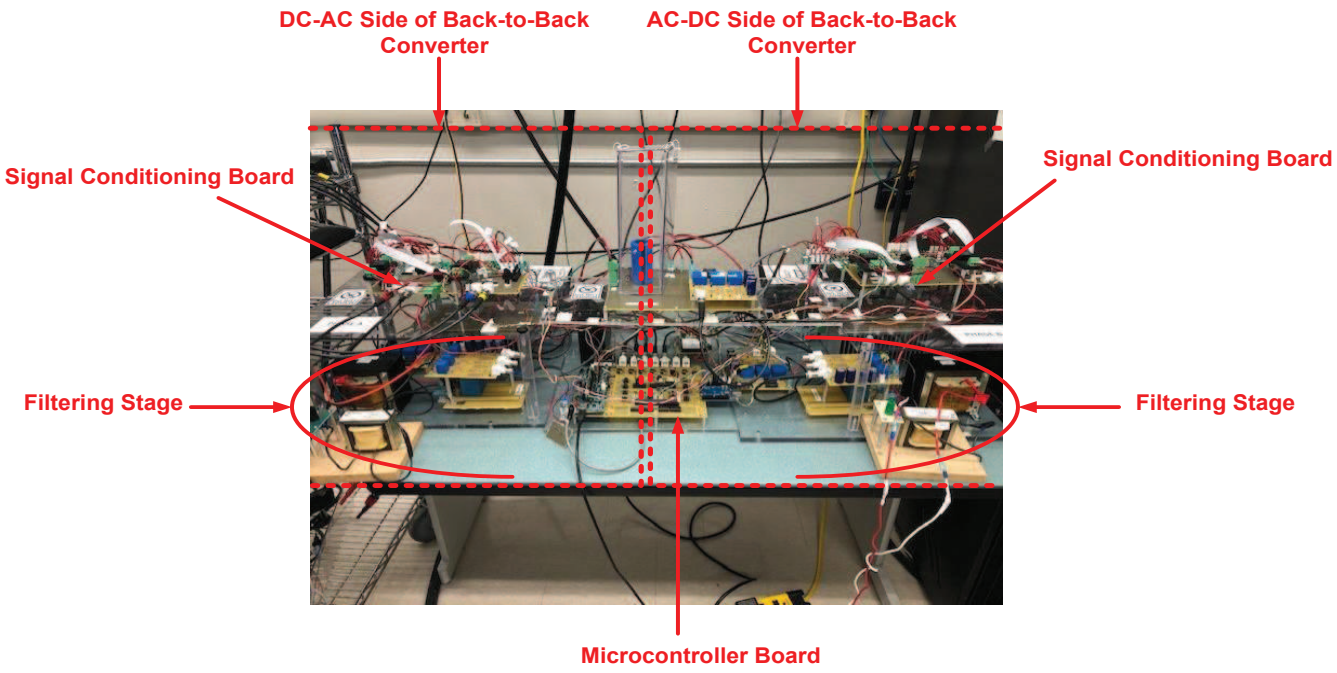


Figure 8.34: Back-to-back converter used for the preliminary test.

The signals as received over the serial port are also observed. In this respect, the input and output voltages and currents at both phases are shown in Figures 8.41 and 8.42. The output voltage is stable at the given references and with minimal harmonics. The internal variables of the system i.e. the $d-q$ components of voltages and currents for each phase are shown in Figures 8.43 and 8.44. The $d-q$ components are also controlled at their given references, which verifies the effectiveness of modified vector strategy for single-phase systems.

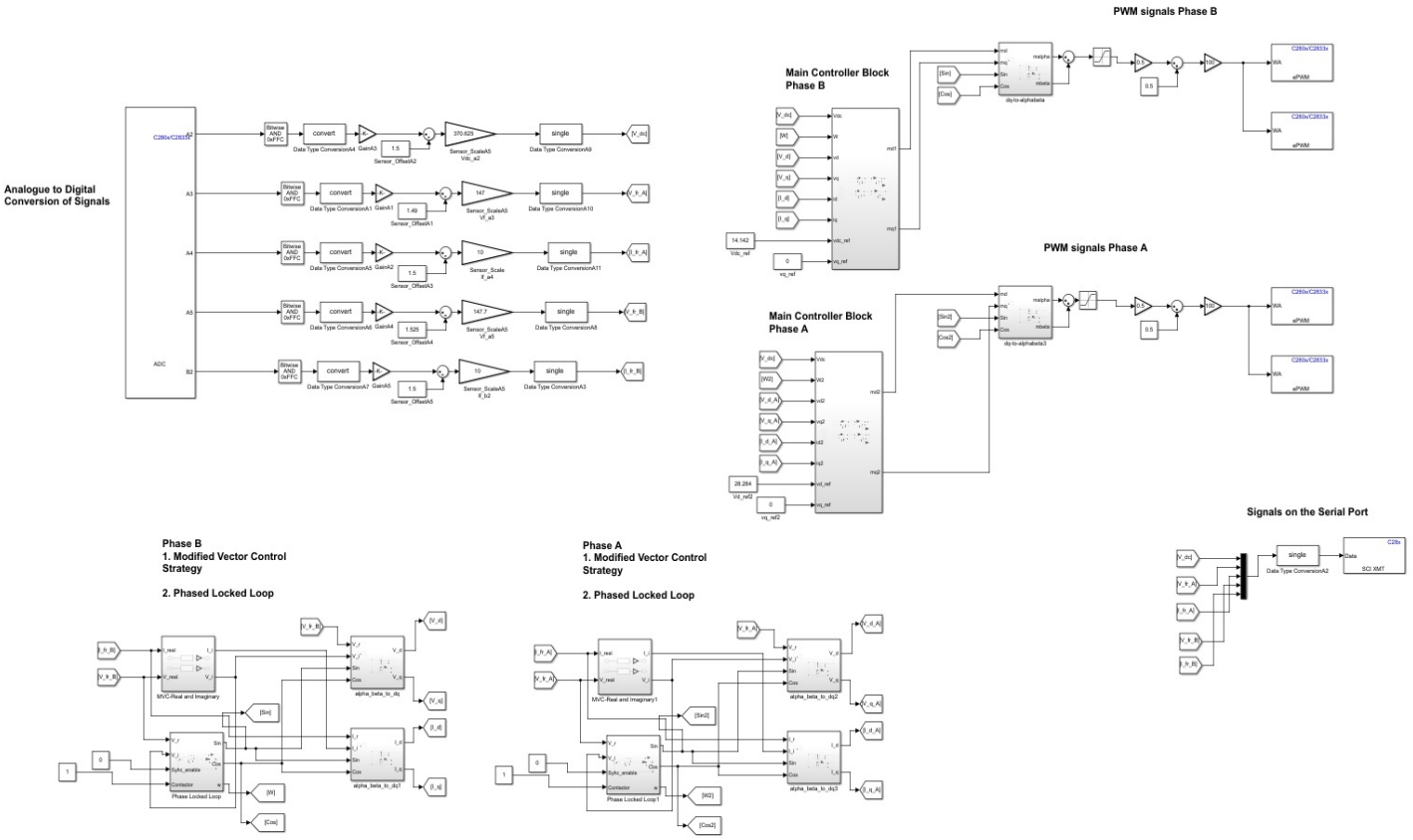


Figure 8.35: Simulink control program used for the preliminary test for the entire system.

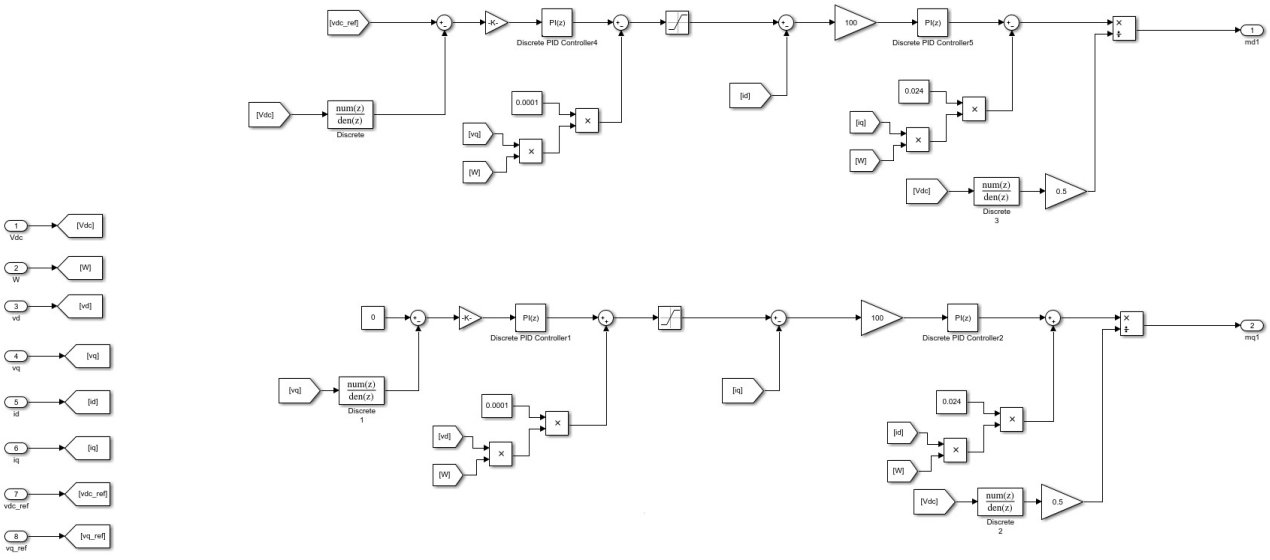


Figure 8.36: Simulink control program for AC-DC side of the back-to-back converter used for the preliminary test.

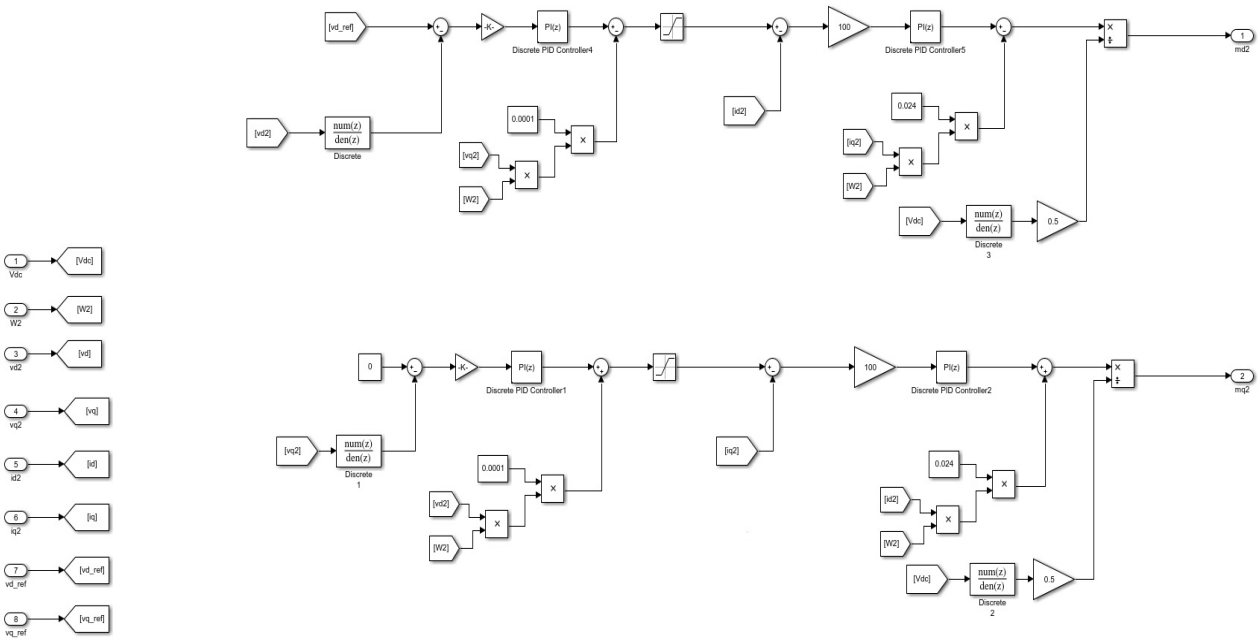


Figure 8.37: Simulink control program for DC-AC side of the back-to-back converter used for the preliminary test.

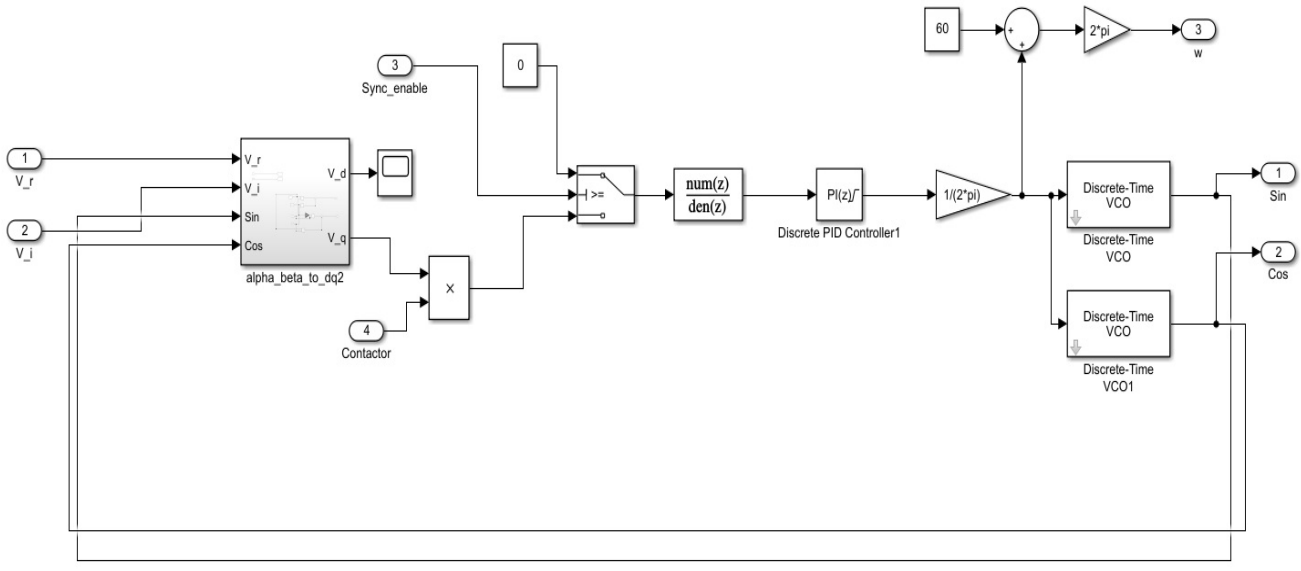


Figure 8.38: Designed PLL block for the back-to-back converter that is used for the preliminary test.

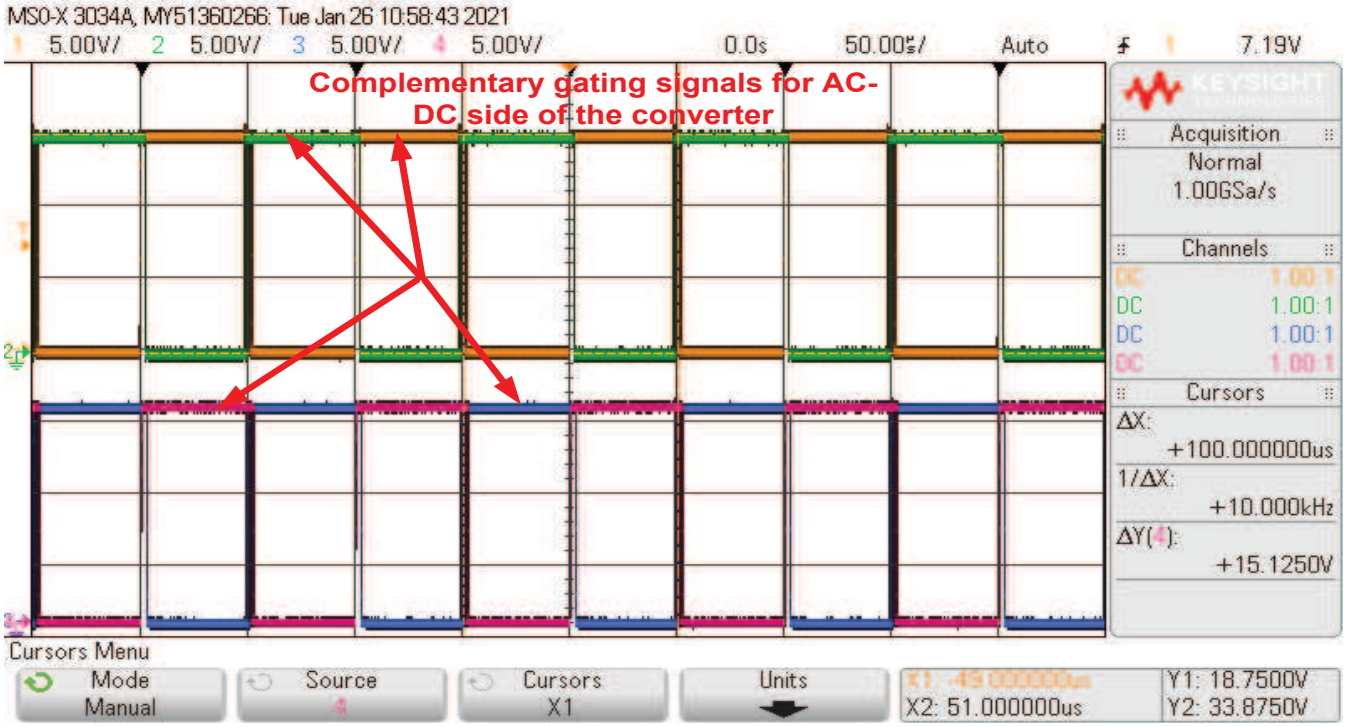


Figure 8.39: Gating signals as observed on the oscilloscope for the AC-DC side of the back-to-back converter.

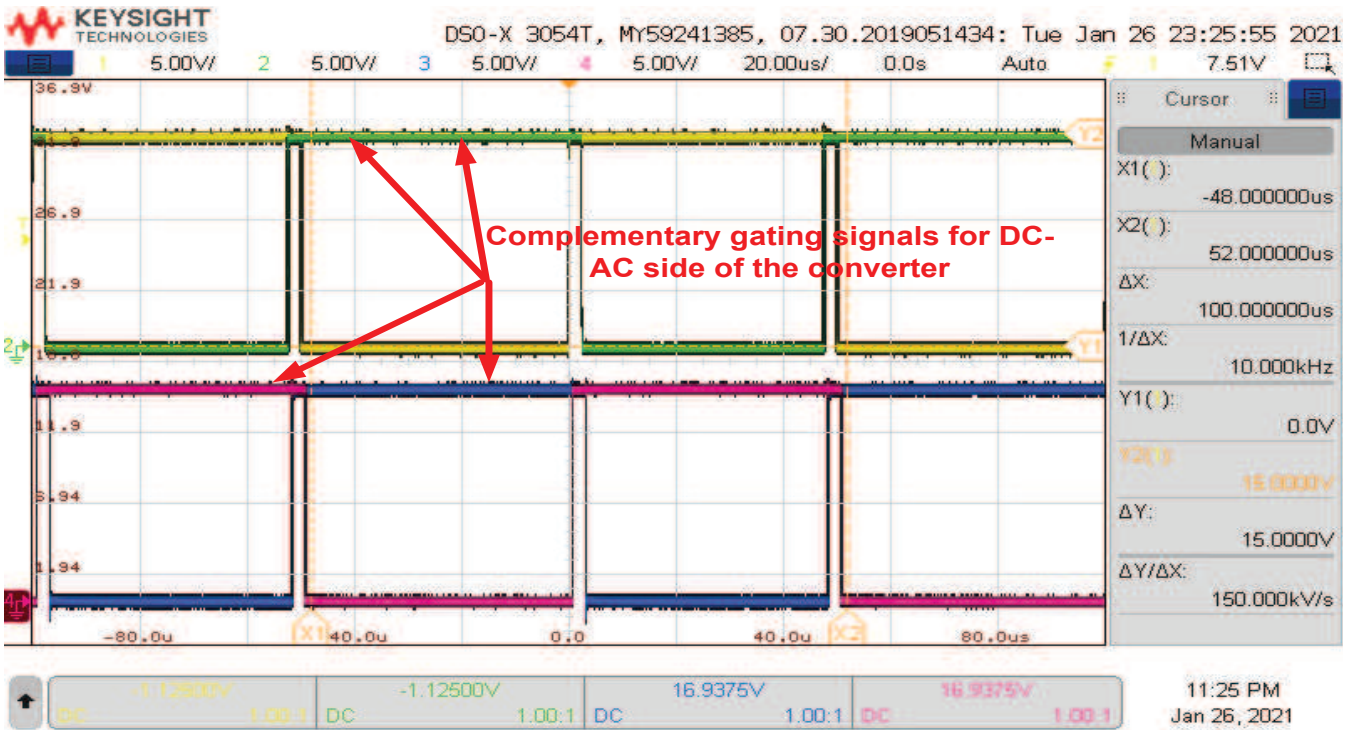
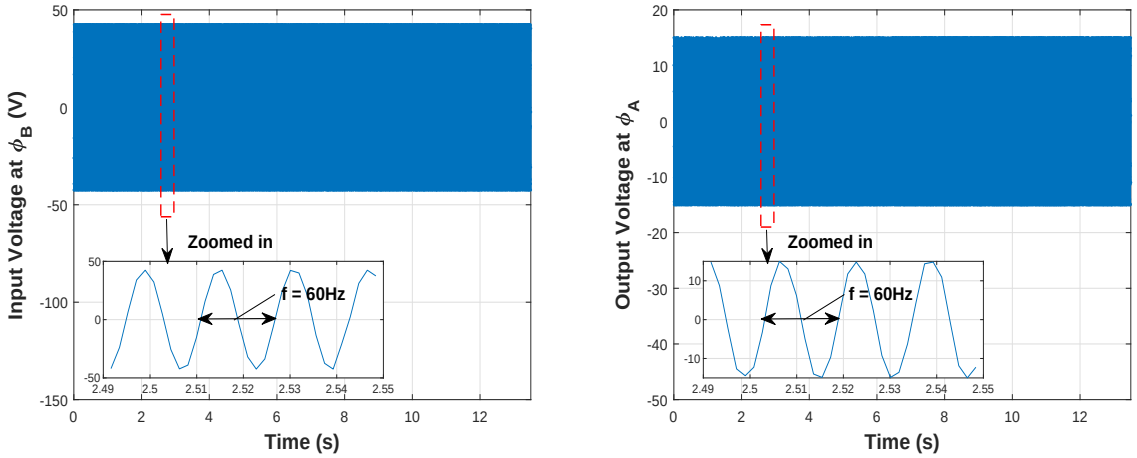
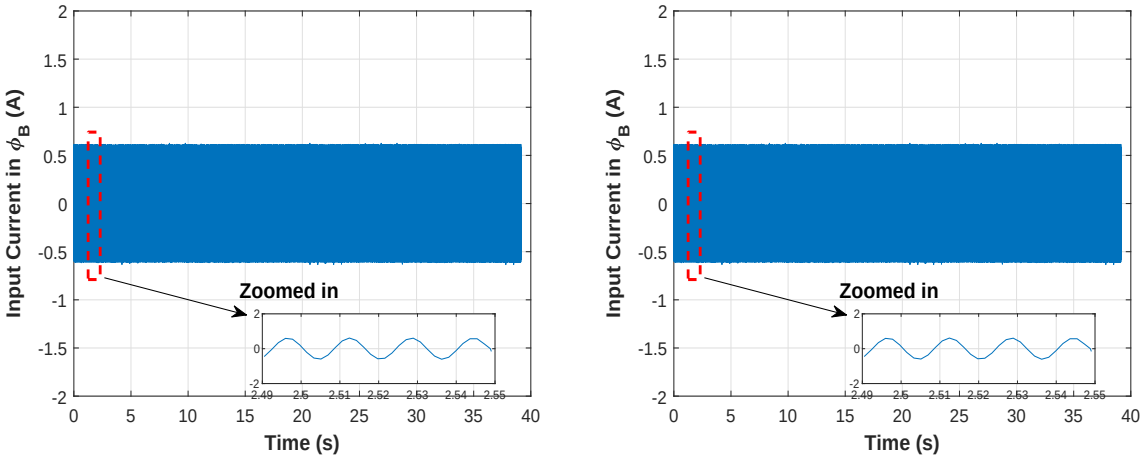


Figure 8.40: Gating signals as observed on the oscilloscope for the DC-AC side of the back-to-back converter.



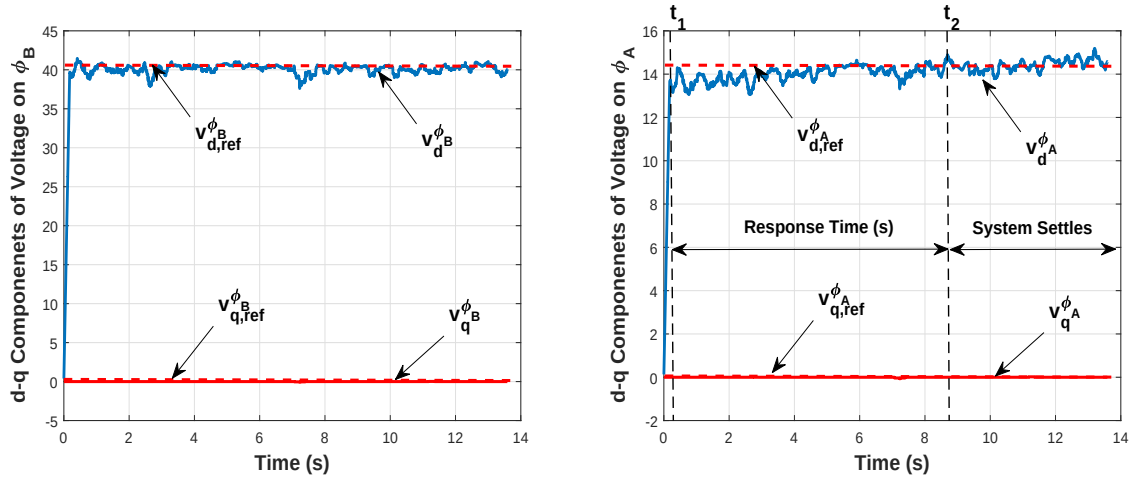
(a) (b)

Figure 8.41: (a) Input voltage and (b) Output voltage of the back-to-back converter.



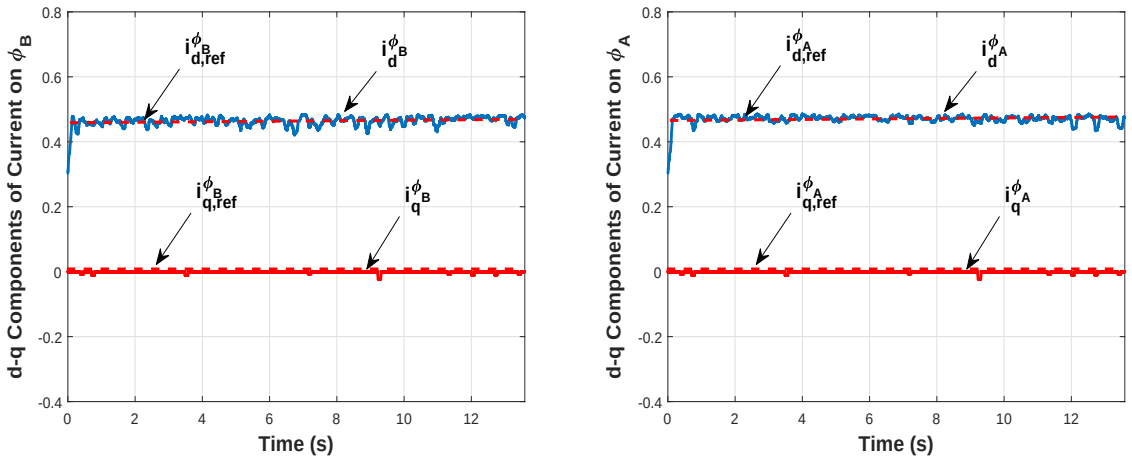
(a) (b)

Figure 8.42: (a) Input current and (b) Output current of the back-to-back converter.



(a) (b)

Figure 8.43: (a) $d-q$ components of the input voltage and (b) $d-q$ components of the output voltage of the back-to-back converter along with their specified references.



(a) (b)

Figure 8.44: (a) $d-q$ components of the input current and (b) $d-q$ components of the output current of the back-to-back converter along with their specified references.

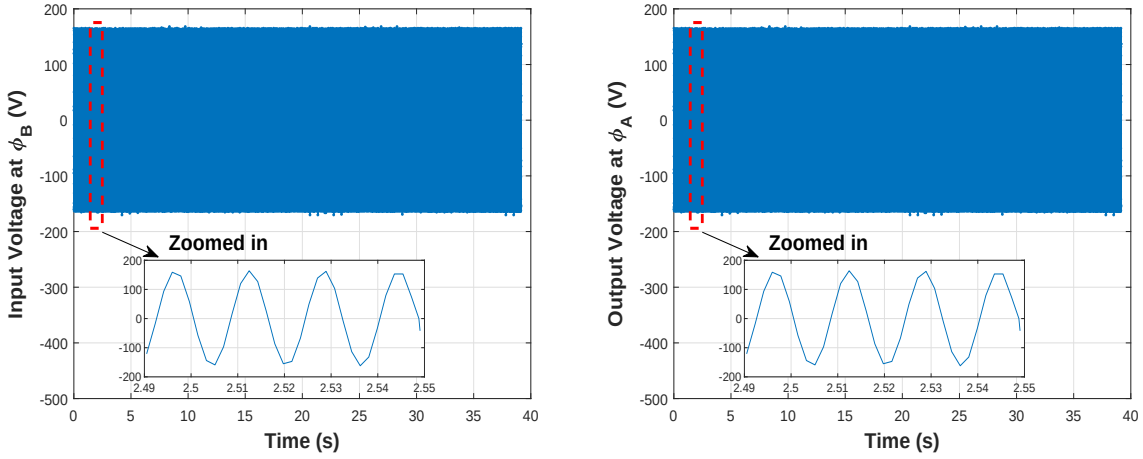
8.7 Actual Unloaded Test

The purpose of conducting this experiment is to ascertain the overall satisfactory operation of the back-to-back converter at rated voltage. The block diagram for this experiment is shown in Fig.8.33.

In this experiment, the control desk runs a MATLAB/Simulink based program similar to the preliminary test, which is previously described. A screenshot of the Simulink program is shown in Fig.8.35, while the voltage and current loops for the AC-DC side of the back-to-back converter is shown in Fig.8.36. The AC input is set at $120V$ RMS on the programmable AC source, while a reference voltage of $120V$ RMS is set for the inverter side of the back-to-back converter. The DC link voltage is set at $370V$. For this experiment, the back-to-back converter is operating under no load conditions. This experiment is conducted to check the response of the system as well the operation of the LC filters in the circuits.

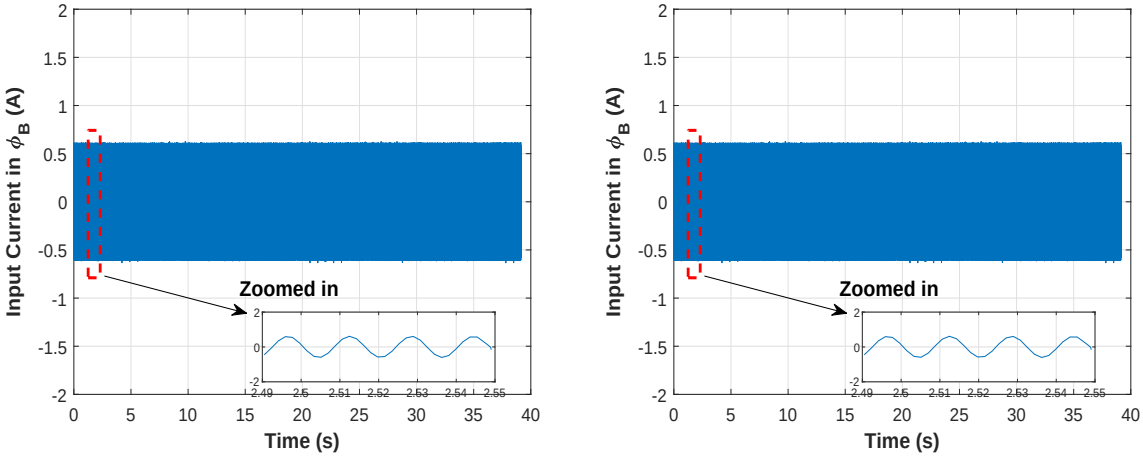
The signals as received over the serial port are also observed. In this respect, the input and output voltages at both phases is shown in Fig.8.45. The output voltage is stable at the given references and with minimal harmonics. The internal variables of the system i.e. the $d-q$ components of voltages is shown in Fig.8.47. The $d-q$ components

are also controlled at their given references, which verifies the effectiveness of modified vector strategy for single-phase systems. The DC link voltage is shown in Fig.8.48, which demonstrates the overall effectiveness of the control strategy to maintain the DC link, while the setting the correct references at the output of the back-to-back converter.



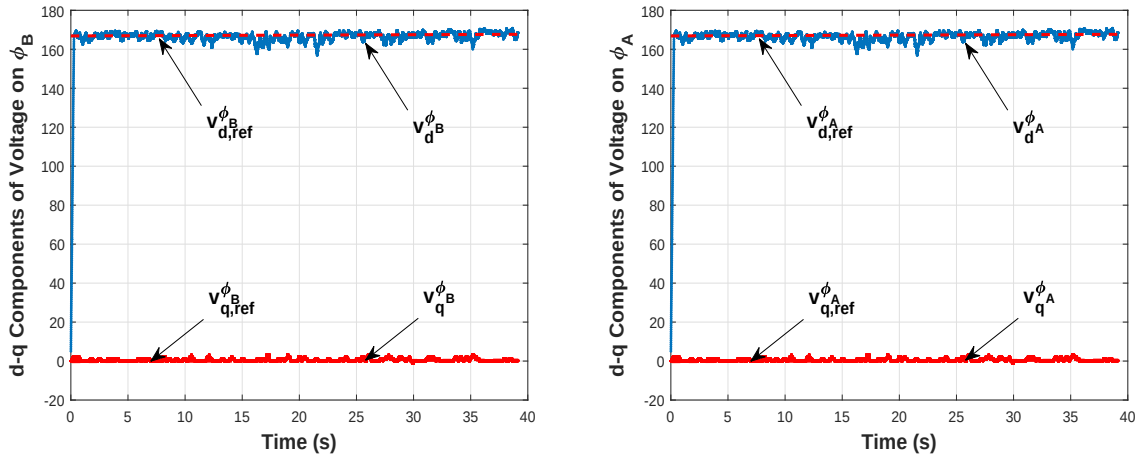
(a) (b)

Figure 8.45: (a) Input voltage on ϕ_B and (b) Output voltage on ϕ_A.



(a) (b)

Figure 8.46: (a) Input current and (b) Output current of the back-to-back converter.



(a) (b)

Figure 8.47: (a) $d-q$ components of the input voltage and (b) $d-q$ components of the input current in ϕ_B of the back-to-back converter along with their specified references.

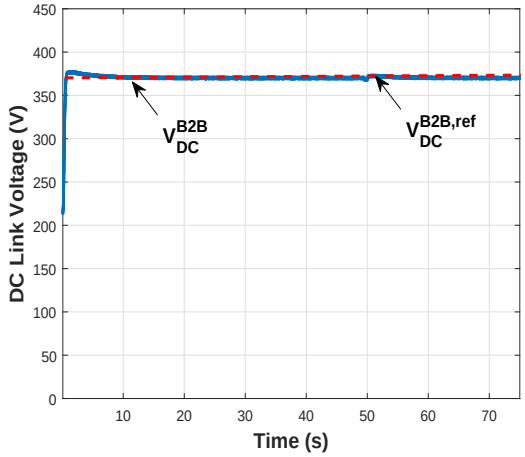


Figure 8.48: (a) DC link voltage of the back-to-back converter along with its specified reference.

8.8 System Test

The system test, which comprises of a programmable AC source, AC loads on other phases and Chroma single-phase load on phase A to demonstrate the phase imbalance. This experiment is decomposed into two stages; (1) preliminary and (2) actual test.

8.8.1 Overall experimental setup

The back-to-back converter developed needs to be interfaced with an AC source and loads to run the system test for the validity of the proposed idea. The overall setup is shown in Fig.8.49. On Phase A of the system, the back-to-back converter is connected to Chroma

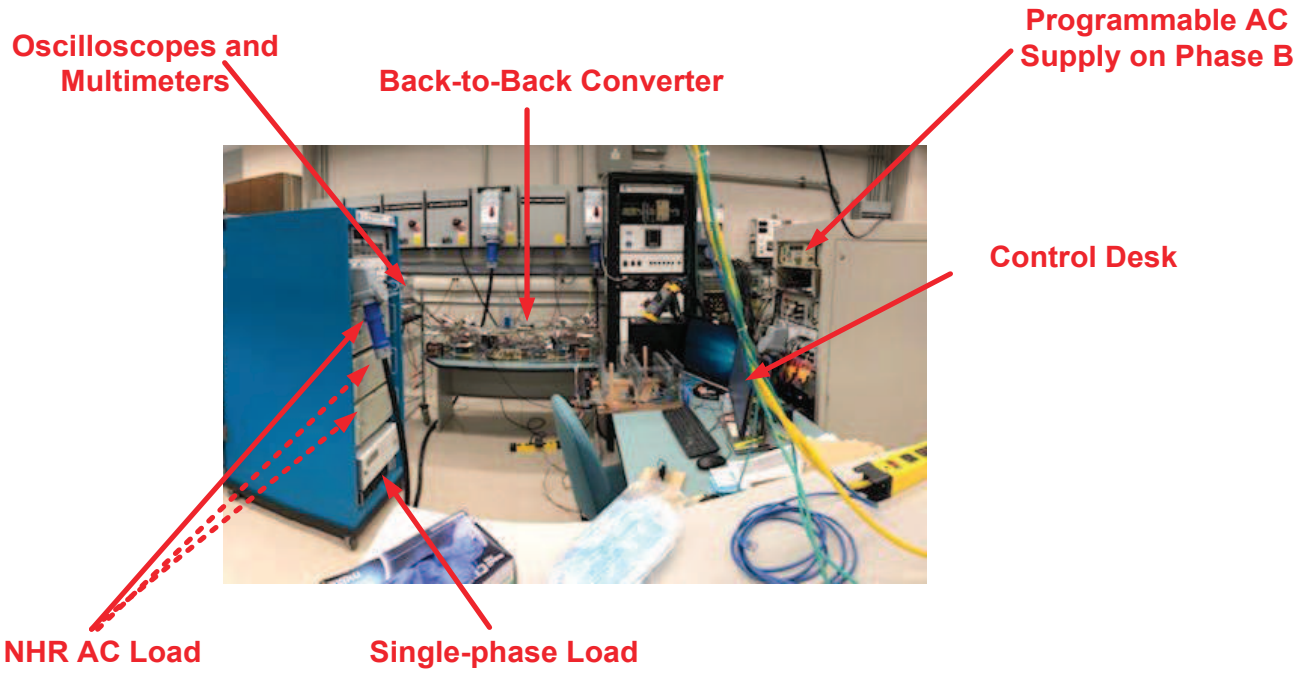


Figure 8.49: Overall setup for conducting the system test.

single-phase load and a programmable NHR AC load. On Phase B, the back-to-back converter is connected to a programmable AC source. Phase C is also balanced with NHR AC load. The back-to-back converter is controlled by control desk, as shown in Fig.8.49. Various instrumentations including Agilent oscilloscopes and multi-meters are available to measure different signals in the system.

8.8.2 Preliminary test

As is the case with all the preliminary experiments that have been performed in this chapter, the prime purpose is to observe if the system is capable of handling constant resistance loads to transfer power from one phase to the other. The programmable AC voltage supply is connected to the system, while the Chroma programmable single-phase load is connected on Phase A. AC loads are connected to the other phases. In order to perform this experiment, there is a need to use the 3 pole-4 wire bus bridge which divides the main AC line of the Distributed Generation lab into two sections. For this experiment, the ground wire has been left untouched from the previous configuration

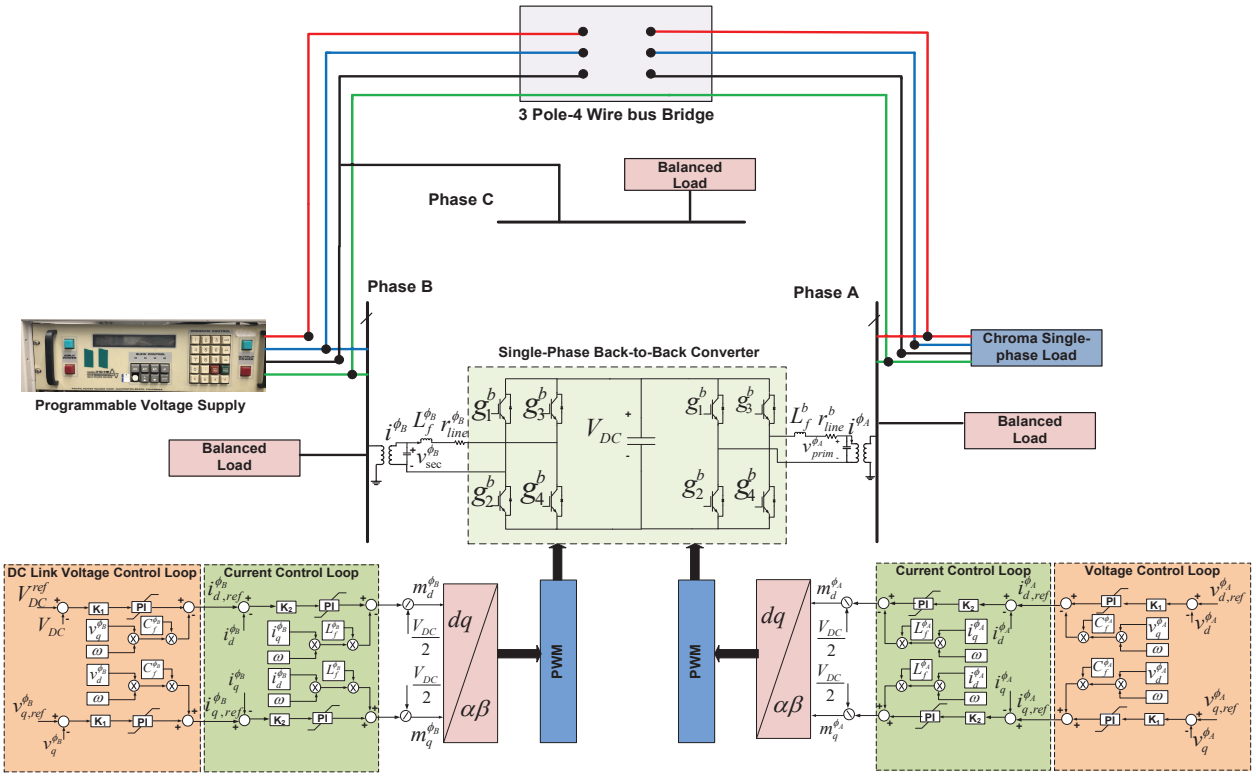
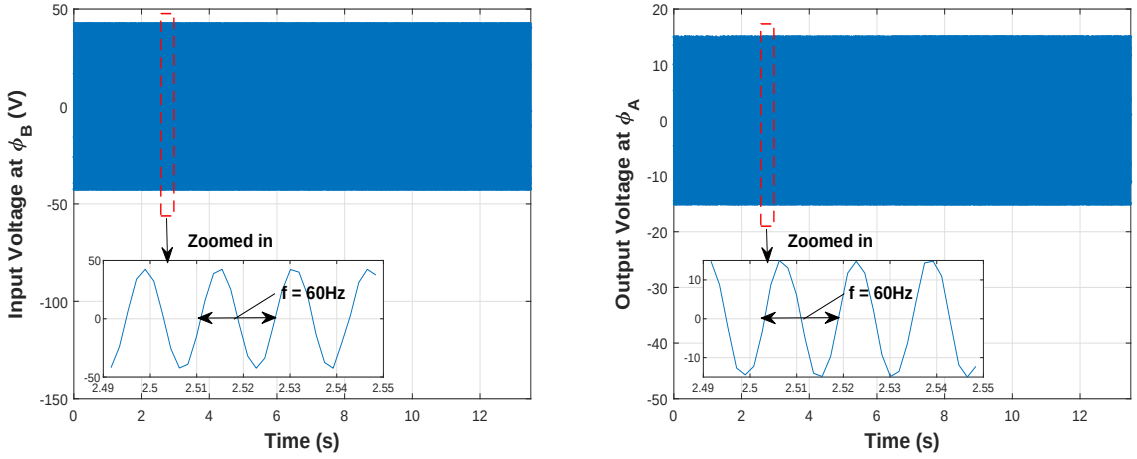


Figure 8.50: Block diagram for system test with programmable voltage supply as a source in phase B and single-phase unbalanced loads in phase A.

while the isolation transformers on each of the phases are connected to their respected phases along with the neutral wire. The block diagram for this experiment is shown in Fig.8.50. The basic control strategy remain the same as discussed in the previous tests. The input voltage is set at $30V$ RMS, while the output voltage across the filter capacitor is set at $11V$ RMS. The Chroma programmable single-phase load is set at resistive load with a value of 200Ω. Since this is a preliminary test, it is expected that $0.5W$ of power is going to flow between the phases under ideal conditions. With a relatively high DC link voltage and output voltage settings, higher power flow is expected.

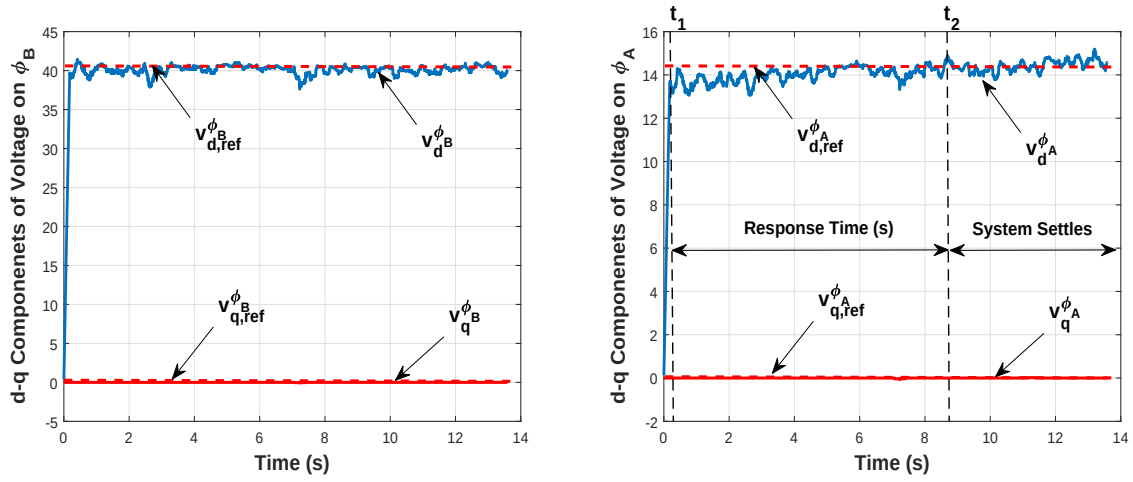
The results for this experiment are shown in Figures 8.51-8.53, which essentially show that system is controllable even under loaded conditions for low voltages. The power flow between the phases is around $0.45W$, as compared to the simulation results of $0.5W$. From this, it is evident that there are power losses in the system; primarily due to high frequency switching, isolation transformer, line losses and due to the rectifying capacitor

in the system. These are discussed in more detail in section 8.8.3. The losses are higher at low voltages but these are expected to reduce significantly in the actual test. Finally, the working of the back-to-back converter under loaded conditions is proven through this test along with the efficacy of the control strategies that have been implemented.



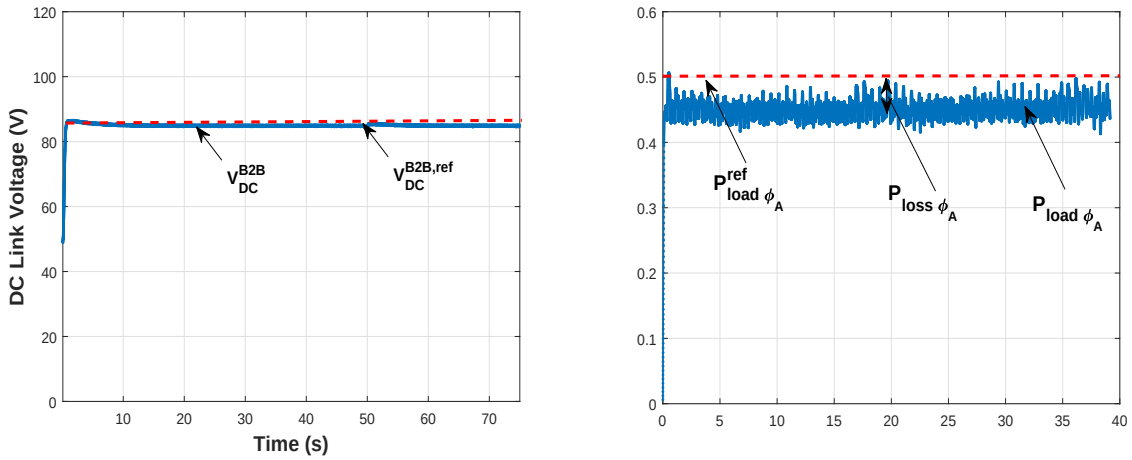
(a) (b)

Figure 8.51: (a) Input voltage and (b) Output voltage of the back-to-back converter.



(a) (b)

Figure 8.52: (a) $d-q$ components of the input voltage and (b) $d-q$ components of the output voltage of the back-to-back converter along with their specified references.



(a) (b)

Figure 8.53: (a) DC link voltage of the back-to-back converter and (b) Power delivered to a resistive load along with their specified references.

8.8.3 Actual test

The actual system test is next performed after the successful running of the preliminary test. For this experiment, the input AC voltage is set at $120V$ RMS with a current limit of $4.7A$ on the programmable AC source, with balanced AC loads in all of the three phases. The Chroma single-phase is added to phase A as an imbalance factor for the system. The DC link voltage reference is set at $370V$.

General observations

The input voltage on ϕ_B with a zoomed in version is plotted in Fig.8.54(a), while the DC link voltage is shown in Fig.8.54(b). At $t = 0$ the serial port communication is enabled and the data collection starts. Between $t = 0$ and $t = t_1$, the system tries to maintain $370V$ across the DC link capacitor. The respective $d - q$ components for both the input voltage and current are shown in Fig.8.55. It can be observed that system is able to set the desired references for individual signals very well and also verifies the effectiveness of modified vector strategy for single-phase systems in high voltage scenario.

The Chroma single-phase load on phase A is then increased in steps to determine, if the back-to-back converter is capable of transferring the required power to this phase to balance the system. The instantaneous power delivered to phase A is shown in

Fig.8.56(a). It is observed that the system is unable to exactly match the reference power for the deficit phase. This is because, there are power losses in the system; primarily due to high frequency switching, isolation transformer, line losses and due to the rectifying capacitor in the system. Solving for η, the power loss factor, introduced in Chapter 4, comes out to be 0.15 on average. The variation of DC link capacitor voltage in response to the load change in phase A is shown in Fig.8.56. It is observed that there are slight dips in the voltage as it tries to push more power into phase A, but eventually the back-to-back converter's controller is able to stabilize it again around the reference value.

Detailed observations for Figures 8.56(a) and (b) follows next to discuss in detail the response time, dynamic behavior, system losses and the total harmonic distortion in these figures.

Response time

In response to the step load changes for this experiment, the details of system's response time for power transfer from surplus phase to deficit phase are plotted. Two regions of interest are observed in detail, which are highlighted in Fig.8.56(a). For region 1, a zoomed in version is plotted in Fig.8.57(a).

From Chapter 6, the plant equation for the system is derived and is given by,

$$G_{cl}(s) = K_v \cdot \frac{k_p s + k_i}{s} \cdot \frac{K_c}{LC^2 s^2 + rC^2 s^2 + K_c C s} \tag{8.2}$$

where, $G_{cl} = \frac{P(s)}{R(s)}$, $P(s)$ is the plant's transfer function and $R(s)$ is the input to the system. Given that $R(s)$, for this experiment is a step input of $45W$ for region 1, the steady state error is written as,

$$e(\infty) = \frac{s.45/s}{1 + \lim_{s \to 0} G_{cl}(s)} \tag{8.3}$$

By inserting the limit in (8.2), $G_{cl}(s) = \infty$, which makes $e(\infty)$ in (8.3) equal to zero. This result shows that under ideal conditions, the step response for the system, in Fig.8.56(a), should result in zero steady state error. It should be noted here that in Figures 8.56(a) and 8.57(a), instantaneous transferred power is plotted against time and not the RMS power, hence the periodic oscillations are observed in these figures. The response of power flow from the back-to-back converter during a step change remains well within the stability envelope as shown in Fig.8.57(a). It is also observed that response of the DC link capacitor voltage is also stable owing to the overall stability of the system, as shown in Fig.8.57(b).

Dynamic behaviour

The dynamic behaviour of the system's response, as shown in for Fig.8.57(a), includes the rise, peak and settling times. From the definition, rise time, T_r, is defined as the time between 0.1 and 0.9 times of the final value. The rise time from Fig.8.57(a) comes out to be $0.18s$. The rise time is calculated to be approximately $0.03s$ from the step response of the converter's controller, as in Chapter 6, Fig.6.7. The deviation in rise time is because of additional damping due to series resistive load in the experimental setup.

Similarly, the peak time, T_p, is the time required to reach the first maximum peak. The peak time from Fig.8.57(a) is observed to be equal to be $0.38s$. The peak time is calculated to be approximately $0.035s$ from Fig.6.7. The deviation in two response times is referred back to the damping effect in the experimental apparatus.

The settling time, T_s, is the time require for the transient's damped oscillations to reach and stay within 2% of the steady state value. Since, the plots in Figures 8.56(a) and 8.57(a) are instantaneous power plots, the settling time in this case is the time required to reach sustained instantaneous power oscillations. Hence, T_s, from Fig.8.57(a) is observed to be $1.01s$. The settling time is calculated to be approximately $0.2s$ from Fig.6.7.

Besides the above calculations for the dynamic behaviour of the system, overshoots

and undershoots are an important criteria for measuring the performance of the designed controller for the back-to-back converter. The region 1, as shown in Fig.8.56(a), observes a percentage overshoot of around 3% from the base value as highlighted in Fig.8.57(a). In comparison to the significant overshoots, as observed in Fig.6.7 for $K_v = 3$, the overshoots in the system response of experimental results are significantly low. The reason being, the presence of line resistance and the inserted resistive load in series with source. This has resulted in significant damping to the system; hence reducing the overshoots.

Following the same procedure, the T_r for the response of DC link voltage is found out to be $0.15s$, $T_p = 0.5s$ and $T_s = 6s$, from Fig.8.57(b). The percentage overshoot and undershoot for the DC link voltage are calculated to be 1.62% and 1.9% respectively. The rise, peak and settling time calculations from Figures 8.57(a) and (b), show that the experimental results obtained for the high voltage system test are in direct correlation with the design of the back-to-back converter as discussed in Chapter 6.

System losses

As highlighted in the general observations, the system losses are identified to be primarily due to high frequency switching, isolation transformer, line losses and due to the rectifying capacitor in the system. From Chapter 4, the power supplied from the surplus phase to the deficient phase is written as,

$$\begin{aligned} P^{sup}|_{\phi_x} = P^{req}|_{\phi_y} + \left[\left(I^2 R_x\right)|_{\phi_x} + P_{loss}^{B2B}|_{\phi_x} + Tfr_{loss} \right] \\ + \left[\left(I^2 R_y\right)|_{\phi_y} + P_{loss}^{B2B}|_{\phi_y} + Tfr_{loss} \right] \end{aligned} \tag{8.4}$$

whereby, the terms in brackets account for the actual loss in the power transfer between the two phases. In the experimental setup, the I^2R_x losses will occur due to the long line cables connecting the programmable AC supply with the bus bridge and finally due to the isolation transformer. In a laboratory setup, the I^2R_x losses, are not significant due to the close proximity of the source and back-to-back converter to the phase loads. In

practical scenarios, e.g. in the benchmark distribution system model in Chapter 3, these losses will become significant, mainly because of the service drop cables that connect long distance participating customers with the back-to-back converter. These losses can be reduced by introducing reactive power control in the system, which inherently can reduce the voltage difference between the pole transformer and the customer at a phase. The term P_{loss}^{B2B} in (8.4) is composed of two components, as listed in Chapter 4. These include,

$$P_{loss}^{B2B}|_{\phi_x} = P_{loss}^{cap} + 2P_{con} \tag{8.5}$$

where,P_{loss}^{cap}, is the loss across the DC link of the back-to-back converter and is dependent upon its equivalent series resistance (ESR), while P_{con} is the conduction losses due to switching of gates in the dc-to-dc converters. For the $1200\mu F$ capacitor, as used in the experimental setup in this chapter, the ESR is around $2.5m\Omega$. The power loss across the capacitor is then written as,

$$P_{loss}^{cap} = ESR \times I_{RMS}^2 \tag{8.6}$$

where, I_{RMS}, is the RMS current supplied by the source to maintain the DC link voltage. For the high voltage system test, the source is supplying around $4.5A$ for the AC-DC side of the back-to-back converter. Using (8.6), the power loss across the capacitor for this experiment comes out to be $0.01W$. Again, under practical implementation of the system and large power flow between phases, this loss can be significant, because of a large source current to maintain the DC link voltage.

The high frequency switching losses of IGBT stack are another major component of the loss equation in (8.5). The turn-on and off switching losses in, (mJ), according to SEMIKRON's specifications can be calculated as,

$$\begin{aligned} E_{on} &= \int_{t1}^{t2} v_{CE}(t) \times i_C(t)dt \\ E_{off} &= \int_{t3}^{t4} v_{CE}(t) \times i_C(t)dt \end{aligned} \tag{8.7}$$

The integration limits for the turn-on losses are between 10% of V_{G-on} and 2% of VCC, where V_{G-on} is the turn on gate voltage and VCC is the maximum collector voltage. On the other hand, limits for turn-off losses are between 90% of $+V_{G-on}$ and 2% of I_C, where, I_C is the collector current. At the rated voltage of the IGBT stack, it is found that turn-on and off energy losses are $27mJ$ and $39mJ$ respectively.

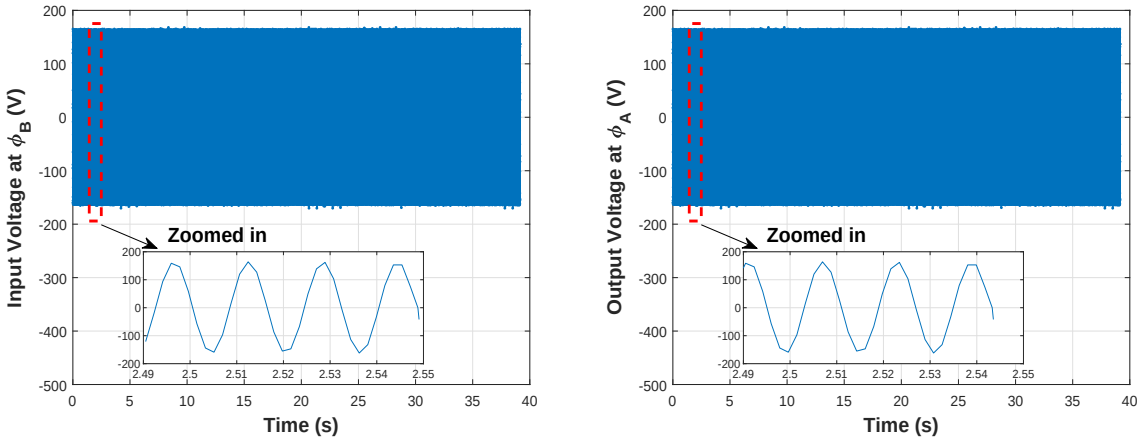
Furthermore, the isolation transformers used for the experiments are not ideal. These transformers with their toroidal core have an average power loss in the range of $5-20\%$, depending upon the quality and rating of these transformers. For the experimental setup as explained in this chapter, a 500VA transformer is utilized, which is significantly lower in rating from typical kVA ratings for isolation transformers that will be required in practical scenarios. It is believed that the core losses in isolation transformers, used in an actual setup for residential microgrids, will account for significant portion of the overall system losses.

From the experimental results, it is found out that the average power loss per step change in unbalanced load on ϕ_A is approximately $4W$, which is 8% of the required deficit power. This is an accumulative power loss of all the factors that have been discussed in this section. For high power applications, these losses will be higher from the quoted results.

Total harmonic distortion

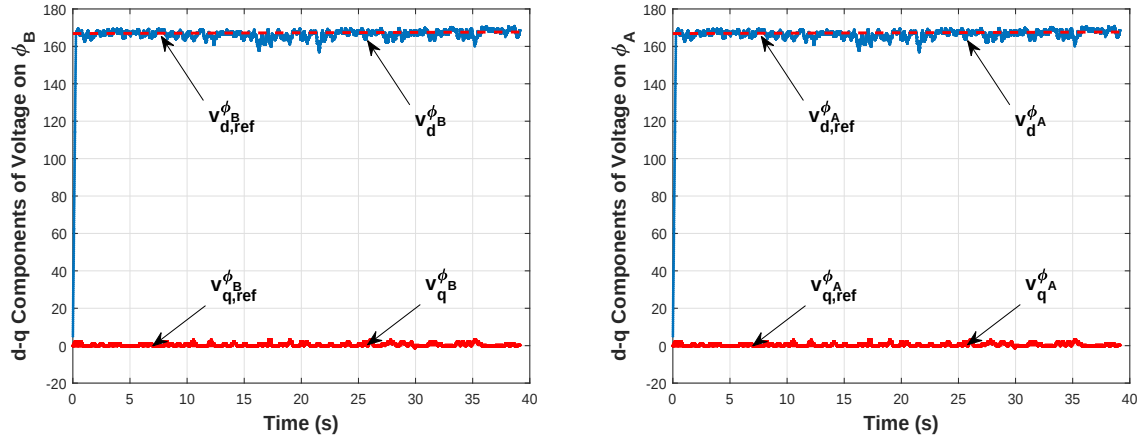
After observing the dynamic behaviour and system losses, the next most important criteria of gauging the response of the system is by studying the total harmonic distortion in the power transfer between the two phases. The most important region of interest to study this phenomenon is to look more closely at region 2 as identified in Fig.8.56(a) due to high harmonic content during this stage. Using Fast Fourier transform (FFT) on Fig.8.56(a), the total harmonics distortion is calculated to be $-7.63dB$ and the harmonic contributions are shown in Fig.8.58(a). It is observed that there is presence of

odd harmonics during power transformer; most importantly the $3rd$ and $5th$ harmonics. Usually, these harmonics need to be suppressed to avoid further system losses. The percentage levels of these harmonics is represented in Fig.8.58(b). This also shows that the modified vector control strategy used for single-phase back-to-back converter works well in suppressing these harmonics.



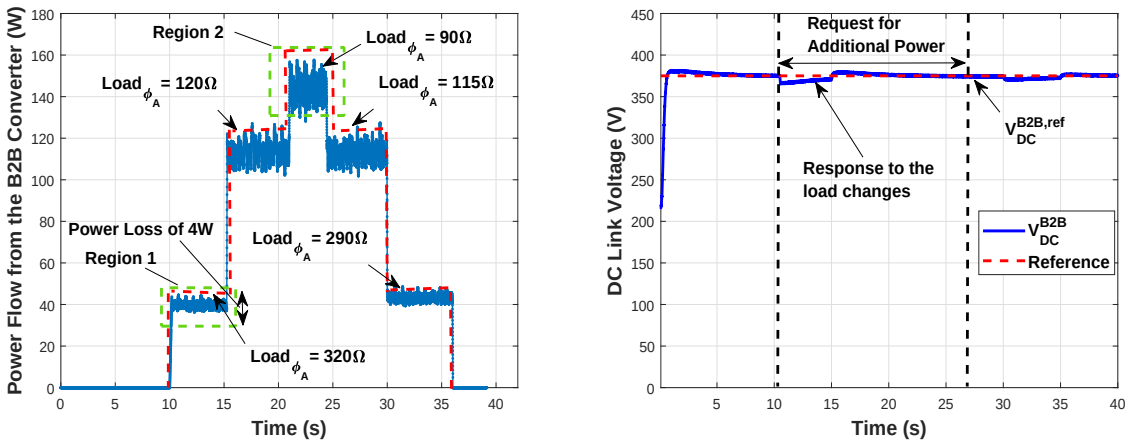
(a) (b)

Figure 8.54: (a) Input voltage on ϕ_B and (b) Output voltage on ϕ_A.



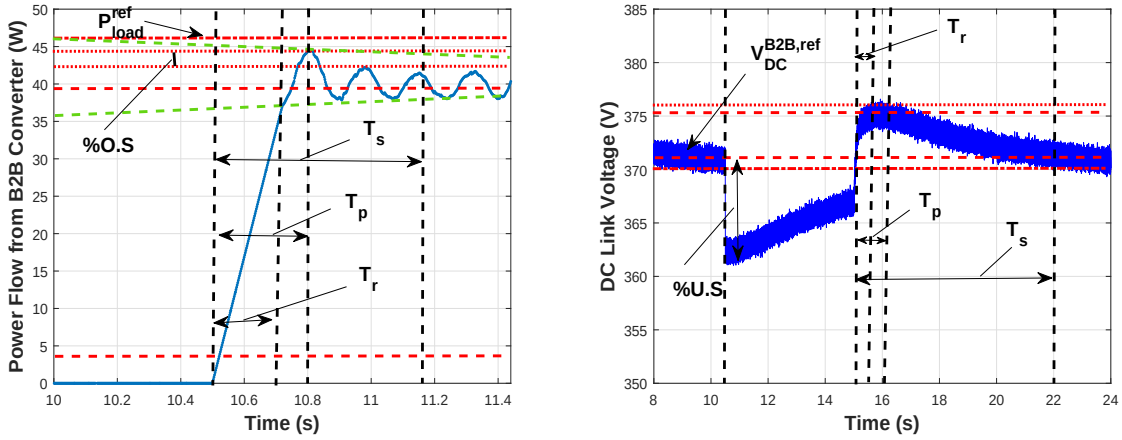
(a) (b)

Figure 8.55: (a) $d-q$ components of the input voltage and (b) $d-q$ components of the output voltage on ϕ_A of the back-to-back converter along with their specified references.



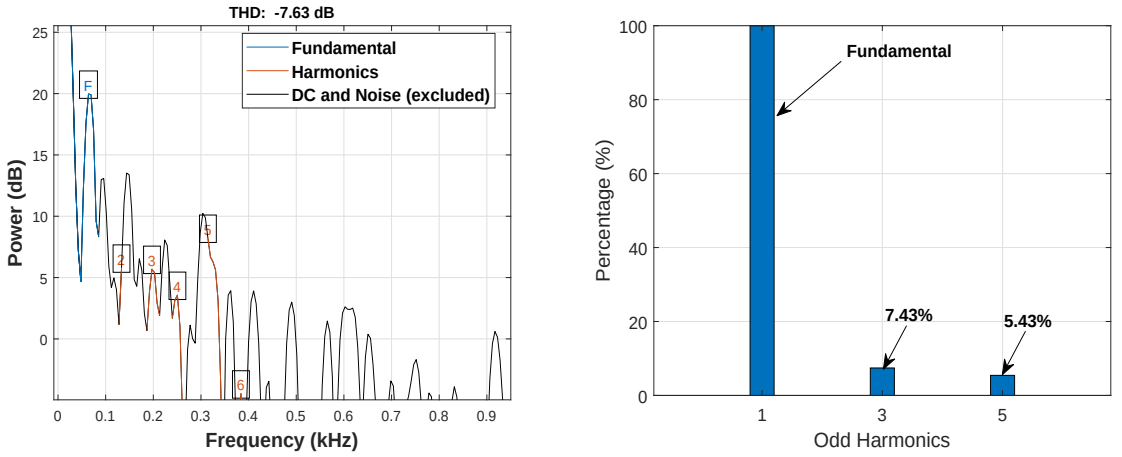
(a) (b)

Figure 8.56: (a) Power transferred to ϕ_A from ϕ_B (b) DC link voltage variation with respect to load change in ϕ_A of the back-to-back converter along with their specified references.



(a) (b)

Figure 8.57: (a) Transient response of the power flow from ϕ_B to ϕ_A during a step change in load (b) Transient response of DC link voltage with respect to load change in ϕ_A of the back-to-back converter along with their specified references.



(a) (b)

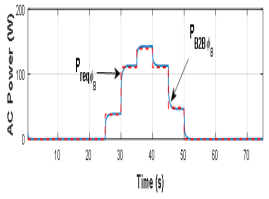
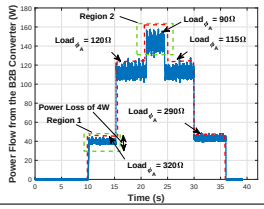
Figure 8.58: (a) Total harmonic distortion for the power transfer stage from ϕ_B to ϕ_A with key harmonics indicated, and (b) Individual harmonics with their percentages.

8.9 Comparison of simulations with experimental results

At this stage, it is important to compare the various aspects of simulation studies, performed in Chapters 4-7 and the experimental test results in this chapter. For this purpose, the proposed management strategies and their properties in this thesis are compared with the execution and test results of this chapter and are tabulated in Table 8.2. A '✓', indicates the completion of a task, while '×' denotes that a task is not implemented.

Since, a single back-to-back converter is developed in this chapter to prove the concept of power flow between the phases, some of the experiments are not performed. These include power transfer between multiple phases i.e. one phase is in power surplus while other phases are power deficit and two phases are in power surplus and the other phase is in power deficit. All these limitations are listed in Table 8.2.

Table 8.2: Qualitative and quantitative comparison of simulations with experimental results

System Property	Simulations Results	Experimental Validation	Comments
I. **Intra-phase power management with tasks of:** (a) Coordination of DG units (b) Maintaining the DC link Voltage for B2B converter	Tasks: (a) ✓ (b) ✓	Tasks: (a) × (b) ✓	(a)For experimental setup DG sources are not connected to individual phases. (b) Experiment 8.7 shows that no power transfer occurs unless there is phase imbalance.
II. **Inter-phase power management for Power Transfer between:** (a) Two phases (b) Multiple Phases	Tasks: (a) ✓ (b) ✓	Tasks: (a) ✓ (b) ×	(a)Due to limitations of experimental setup, power transfer between two phases is not tested. (b) Sections 8.7 and 8.8 detail the complete experimental analysis for power transfer between a power surplus phase and a deficit phase.
III. **Modified Vector Control Strategy with tasks of:** (a) To generate orthogonal signals (b) Control of single-phase inverter (c) Control of back-to-back converter	Tasks: (a) ✓ (b) ✓ (c) ✓	Tasks: (a) ✓ (b) ✓ (c) ✓	This strategy is validated both in simulations and experiments.
IV. **Improved Multi-Segment Droop Strategy with tasks of:** (a) Power coordination between sources (b) Activate B2B converter when required	Tasks: (a) ✓ (b) ✓	Tasks: (a) × (b) ✓	This strategy is only used when activating the back-to-back converter
V. **Dynamic Phase Balancing**	✓	Partial	Due to experimental limitations, dynamic phase balancing in one phase is only studied.
VI. **Comparison of Key Result of Power Transfer between Phases**			Both simulation and experimental results show that power can be transferred between phases to mitigate phase imbalance. Due to power rating limitation of the B2B converter, further imbalance cannot be mitigated.
VI. **B2B Converter's Controller Response for Power Transfer:** (a) Stability (b) Rise Time (s) (c) Peak Time (s) (d) Settling Time (s) (e) % Overshoot (f) System Losses	Response of Controller: (a) Stable (b) $0.03s$ (c) $0.04s$ (d) $0.2s$ (e) 25% (f) 2%	Response of Controller: (a) Stable (b) $0.18s$ (c) $0.38s$ (d) $1.01s$ (e) 3% (f) 8%	Dynamic response of the developed B2B converter is comparative with the simulation results.

8.10 Summary

This chapter has demonstrated and validated the results for inter-phase power management that has been proposed in this thesis. A hardware-in-the-loop based system is developed at the laboratory scale to test the efficacy of modified vector control strategy and the control of back-to-back converter to transfer power from the power surplus phase to the deficit phase. In this respect, a set of experiments (both preliminary and actual tests) have been performed and the experimental results have been presented. Since, a single back-to-back converter is developed, the experiments have validated that power transfer between two phases can take place under unbalanced conditions. Based on this rationale, it is concluded that with the development of another two back-to-back converters between phases, the remaining cases pertaining to inter-phase power management strategy can be validated. The results show that adequate control of back-to-back converter can be achieved through the proposed control strategies, correct power references can be setup for the deficit phase when required and that the deficit power can be delivered to it from the surplus phase, all while maintaining system stability.

Chapter 9

Conclusion and Future Work

9.1 Conclusions

This work has covered an overview of the existing distribution networks. It is determined that with high penetration of DG units at the distribution level, residential microgrids at the customer level can be formed. The formation of these microgrids with different capacities of DG units, is a major source of imbalance for the distribution network. This imbalance, ultimately is a cause of further stressing the distribution transformer connecting these residential microgrids.

The investigation has led to developing a benchmark distribution network model to support residential microgrid studies. A unique feature of this model is that it allows for integration of multiple single-phase DG sources to be located in a particular phase, yet, it also supports coordination of these units within their respective phases or across different phases. In this respect, two schemes are proposed namely, '*intra- and inter-power management strategies*', which are analyzed both analytically and through simulations to test their validity in balancing phases with respect to the distribution transformer.

For intra-phase power management strategy within a phase, a modified vector control is adopted with a multi-segment (P/f) droop based load-sharing, while for inter-phase

power management strategy control of back-to-back converters is proposed to transfer power from the power surplus phase(s) to power deficit phase(s). Seven scenarios have been considered to cover all conceivable operating conditions and are simulated in PSCAD/EMTDC. The results have shown that the developed schemes can provide effective control and power management for intra-and inter-phase scenarios in residential distribution microgrids with renewable energy resources and storage devices.

The inter-phase power management strategy is demonstrated and validated by developing a hardware-in-the-loop based system at the laboratory-scale to test the efficacy of modified vector control strategy and the control of back-to-back converter to transfer power from the power surplus phase to the power deficit phase. In this respect, a set of experiments (both preliminary and actual tests) have been performed and the experimental results are presented. The results show that adequate control of back-to-back converter can be achieved through the proposed control strategies, correct power references can be setup for the deficit phase when required and that the deficit power can be delivered to it from the surplus phase, all while maintaining desired system behaviours.

9.2 Future Work

The proposed architecture and control strategies in this thesis are validated against a certain type of residential microgrids. The control strategies can be evaluated with different combinations of distributed generation resources and storage units to identify any shortcomings in the proposed techniques. Furthermore, the architecture used for experimental validation can be improved further to investigate the potential issues in the overall system. Based on this, the potential future work is suggested as follows:

1. The thesis presented control strategies by which the back-to-back converter(s) is capable of transferring the required real power requirement from one phase to another. The same concept can be extended further by sharing the reactive power

amongst the residential microgrids if necessary.

2. With the growing use of renewable energy resources at the residential level, the interaction of other sources including electric cars, super capacitors, micro-turbines, solar panels on recreational vehicles etc. can be considered as future work in the domain of system level control and stability. Furthermore, the concept of working with these different power resources under the improved multi-segment droop control strategy can be investigated in the future.

3. The idea of residential single-phase microgrids can be extended further by investigating scenarios where multi-microgrids, both single-phase and three-phase systems, are interconnected with back-to-back converters. The conditions under which these converters need to operate and transfer the deficit power between multi-microgrids to achieve overall system balance is definitely an area which requires further research. This architecture will involve significantly complex decision criteria for the secondary and tertiary control layers, making the overall system and its control much closer to microgrids, which are envisioned for the future.

4. The back-to-back converter is developed to validate the concepts presented in this thesis. In the proposed experimental architecture, a single converter is developed. In order to further prove the viability and stability of system, it is important to look into the possibility of developing another similar converter and observe their operation, when both the converters are enabled to transfer the required power from the surplus phases to the deficient phase. This will require another generation source, which is available in the distributed generation lab, and an improvement over the original Simulink program that is developed to control the system. The motivation is to develop a fully working residential microgrid at the laboratory scale.

5. In this thesis, the entire focus has been on the management of real power flow in

the single-phase residential microgrids. For future work, the voltage balance within these microgrids using reactive power flow can be investigated. The combined real and reactive power management strategies will provide a complete picture of the complexity required in the control structures to achieve this task.

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Chapter 10

Appendices

10.1 Data Sheet for Isolation Transformer

HAMMOND MANUFACTURING

Quality Products. Service Excellence.

TOROIDAL Isolation (120VAC to 120VAC) *178 Series*

Plug-In

Features

- Primary 120VAC, 50/60 Hz., Secondary 120VAC.
- Provides circuit isolation.
- Toroidal transformer for high isolation, low noise, light weight, cool operation and low profile.
- World wide applications, 50 or 60 Hz. operation, step down (120VAC to 120 VAC).
- Standard 3-wire, grounded plug (for use with **adaptors** for proper grounding).
- Input (primary) connected to a 5 foot long cord & standard North American plug (NEMA 5 15P).
- Output (secondary) connected to two standard - 3 wire grounded receptacles (NEMA 5-15R).
- Features include ventilated black steel case, rocker lighted on-off switch & circuit breaker protected output.
- North American Mark of Safety - C UL & UL listed (File #E211544).
- Indoor use only.
- **Remember** - These units do NOT convert line frequency.
- **Note about Inrush Current:**
  Due to the superior magnetic properties of Toroidal transformers they will be susceptible to high magnetizing current when initially energized, only limited by the low DC resistance of the primary winding. Depending on where you are in the AC cycle when the transformer is energized dictates the chances of overloading the supply circuit. This is why the transformer may sometimes energize without a problem and other times it will blow the fuse or trip the circuit breaker. The duration of this overload is rarely longer than a half of a cycle. Therefore, you should consider using a slow-blow fuse, time delayed circuit breaker or other form of soft start circuitry for the supply line when using these high efficient Toroidal transformers.

Accessories

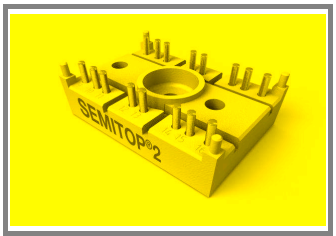
- International Grounded Adaptor Plugs

	Capacity	Outlet	Overall Dimensions		
Part No.	VA	Qty	Length	Width	Height
178CT	250	2	8.25	6.00	4.00
178DT	500	2	9.00	6.00	4.00
178ET	750	2	10.25	7.50	5.00
178FT	1000	2	10.25	7.50	5.00
178GT	1500	2.00	12.50	9.00	5.00

Data subject to change without notice

10.2 Data Sheet for SK25GH063

SK25GH063



SEMITOP® 2

IGBT Module

SK25GH063

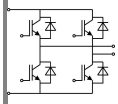
Preliminary Data

Features

- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminium oxide ceramic (DCB)
- N channel, homogeneous Silicon structure (NPT-Non punchtrough IGBT)
- High short circuit capability
- Low tail current with low temperature dependence
- UL recognized, file no. E63532

Typical Applications*

- Switching (not for linear use)
- Inverter
- Switched mode power supplies
- UPS

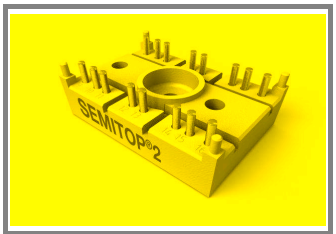


GH

Absolute Maximum Ratings			T_s = 25 °C, unless otherwise specified	
Symbol	**Conditions**		**Values**	**Units**
IGBT				
V_{CES}	T_j = 25 °C		600	V
I_C	T_j = 125 °C	T_s = 25 °C	30	A
		T_s = 80 °C	21	A
I_{CRM}	I_{CRM}= 2 x I_{Cnom}		60	A
V_{GES}			± 20	V
t_{psc}	V_{CC} = 300 V; $V_{GE} \leq$ 20 V; V_{CES} < 600 V	T_j = 125 °C	10	µs
Inverse Diode				
I_F	T_j = 150 °C	T_s = 25 °C	36	A
		T_s = 80 °C	24	A
I_{FRM}	I_{FRM}= 2 x I_{Fnom}			A
I_{FSM}	t_p = 10 ms; half sine wave	T_j = 150 °C	200	A
Module				
$I_{t(RMS)}$				A
T_{vj}			-40 ... +150	°C
T_{stg}			-40 ... +125	°C
V_{isol}	AC, 1 min.		2500	V

Characteristics			T_s = 25 °C, unless otherwise specified			
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Units**
IGBT						
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 0,7 mA		4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0 V, V_{CE} = V_{CES}	T_j = 25 °C			0,1	mA
		T_j = 125 °C				mA
I_{GES}	V_{CE} = 0 V, V_{GE} = 30 V	T_j = 25 °C			120	nA
		T_j = 125 °C				nA
V_{CE0}		T_j = 25 °C		1		V
		T_j = 125 °C		1,1		V
r_{CE}	V_{GE} = 15 V	T_j = 25°C		37		mΩ
		T_j = 125°C		30		mΩ
$V_{CE(sat)}$	I_{Cnom} = 30 A, V_{GE} = 15 V	T_j = 25°$C_{chiplev.}$		2,1	2,5	V
		T_j = 125°$C_{chiplev.}$		2	2,3	V
C_{ies}	V_{CE} = 25, V_{GE} = 0 V	f = 1 MHz		1,3		nF
C_{oes}				0,15		nF
C_{res}				0,1		nF
$t_{d(on)}$	R_{Gon} = 33 Ω	V_{CC} = 300V		37		ns
t_r		I_C= 25A		40		ns
E_{on}		T_j = 125 °C		1,1		mJ
$t_{d(off)}$	R_{Goff} = 33 Ω	V_{GE}=±15V		200		ns
t_f				30		ns
E_{off}				0,8		mJ
$R_{th(j-s)}$	per IGBT				1,4	K/W

SK25GH063



SEMITOP® 2

IGBT Module

SK25GH063

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Typical Applications*

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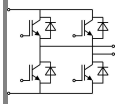


GH

Characteristics

Symbol	Conditions		min.	typ.	max.	Units
Inverse Diode						
$V_F = V_{EC}$	I_{Fnom} = 25 A; V_{GE} = 0 V	T_j = 25 °$C_{chiplev.}$		1,45	1,7	V
		T_j = 125 °$C_{chiplev.}$		1,4	1,75	V
V_{F0}		T_j = 125 °C		0,85	0,9	V
r_F		T_j = 125 °C		22	32	mΩ
I_{RRM}	I_F = 25 A	T_j = 125 °C		16		A
Q_{rr}	di/dt = -500 A/µs			2		µC
E_{rr}	V_{CC}= 300V			0,25		mJ
$R_{th(j-s)D}$	per diode				1,7	K/W
M_s	to heat sink M1				2	Nm
w				21		g

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX.

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliances and systems is subject to prior specification and written approval by SEMIKRON. We therefore strongly recommend prior consultation of our personal.

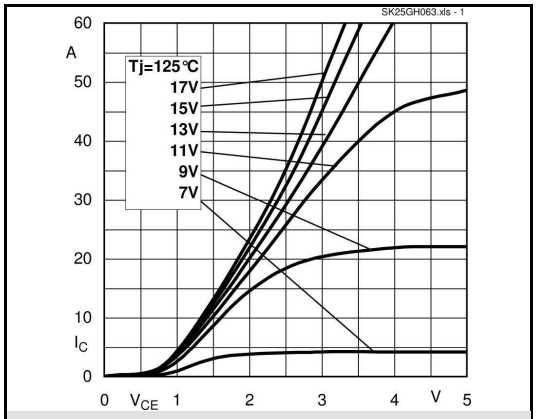


Fig. 1 Typ. output characteristic, inclusive $R_{CC'+EE'}$

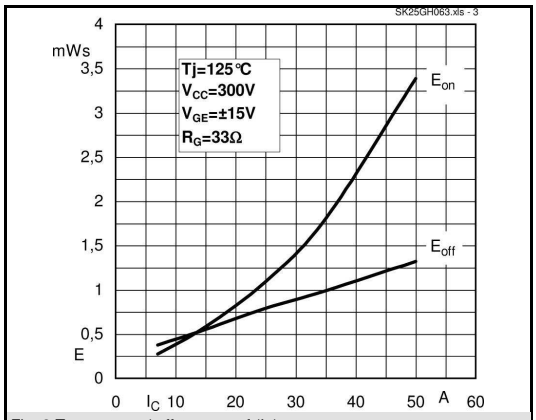


Fig. 3 Typ. turn-on /-off energy = f (I_C)

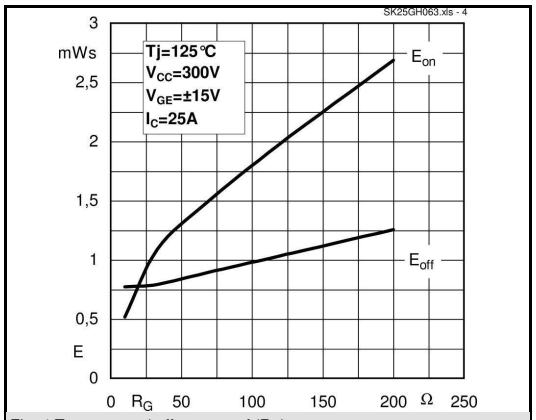


Fig. 4 Typ. turn-on /-off energy = f (R_G)

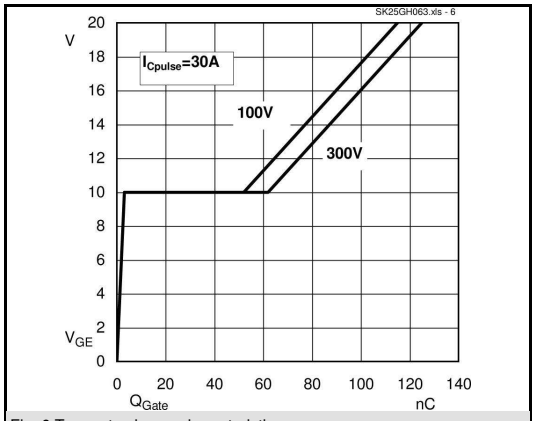


Fig. 6 Typ. gate charge characteristic

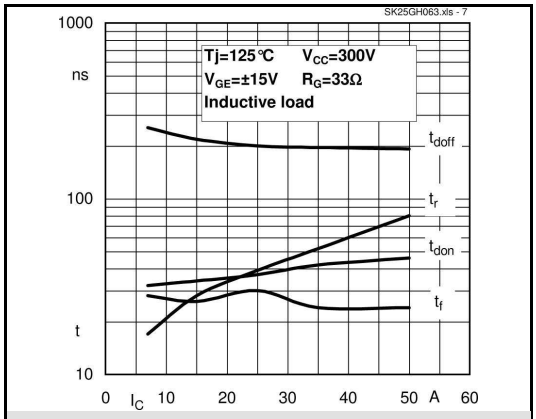


Fig. 7 Typ. switching times vs. I_C

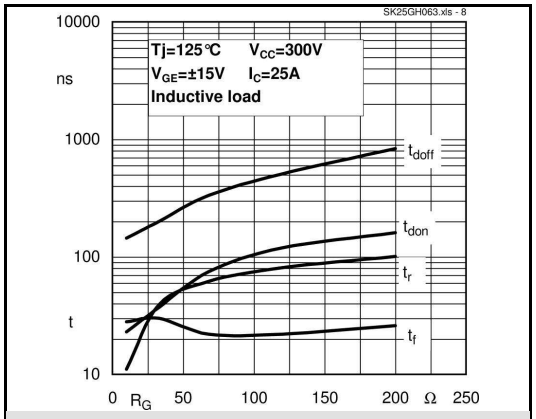


Fig. 8 Typ. switching times vs. gate resistor R_G

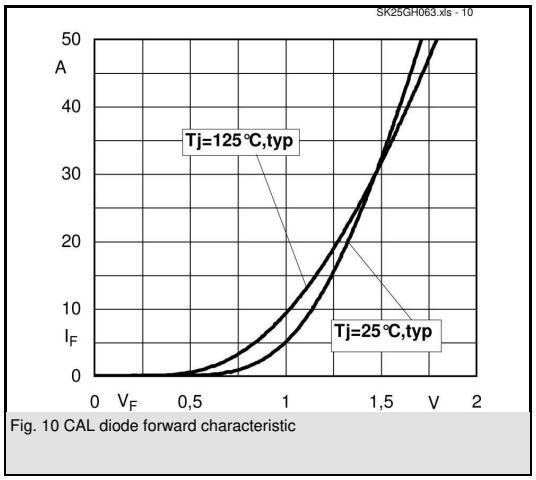
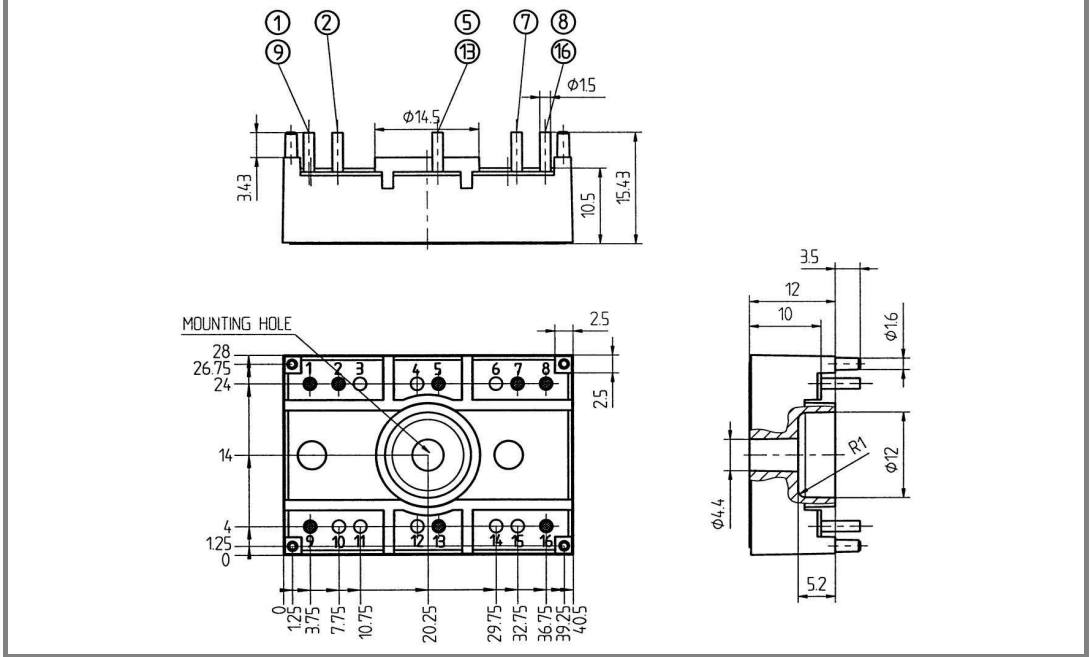


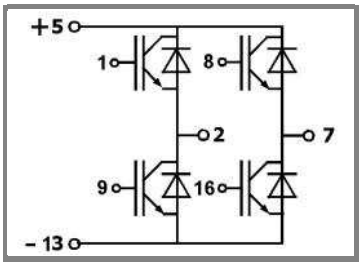
Fig. 10 CAL diode forward characteristic

SK25GH063

UL recognized file no. E 63 532



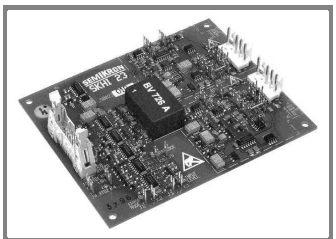
Case T5 (Suggested hole diemater, in the PCB, for solder pins and plastic mounting pins:2mm)



Case T 5 GH

10.3 Data Sheet for SKHI23/12

SKHI 23/12 (R) ...



SEMIDRIVER™

Medium Power Double IGBT Driver

SKHI 23/12 (R)

Features

- SKHI 23/12 drives all SEMIKRON IGBTs with V_{CES} up to 1200 V (VCE-monitoring adjusted from factory for 1200 V-IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drivers
- CMOS / TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / ouput signal (LOW or HIGH logic)
- Driver interlock top / bottom
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Half and Full bridges
- Three phase motor inverters
- High power UPS

1) This current value is a function of the output load condition
2) Operating fsw = 0 Hz
3) This value does not consider t_{on} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}; see also fig. 14
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 4
5) With R_{CE} = 18 kΩ, C_{CE} = 330 pF; see fig. 6
6) Factory adjusted; other values see table 3

Absolute Maximum Ratings		T_a = 25 °C, unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
V_S	Supply voltage primary	18	V
V_{iH}	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AV}$	Output average current	± 50	mA
V_{CE}	Collector emitter voltage sense	1200	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (2 sec. AC)	2500	V
$R_{Gon\ min}$	minimal R_{Gon}	2,7	Ω
$R_{Goff\ min}$	minimal R_{Goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	4,8	µC
T_{op}	Operating temperature	- 25 ... + 85	°C
T_{stg}	Storage temperature	- 25 ... + 85	°C

Characteristics		T_a = 25 °C, unless otherwise specified			
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,32[1]		A
I_{SO}[2]	Supply current primary side (standby)		0,12		A
V_{iT+}	Input threshold voltage (HIGH) min.				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) max.				
	for 15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4		µs
$t_{d(err)}$	Error input-output propagation time		1,0[3]		µs
t_{TD}	Dead time		10[6]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		5,2[5]		V
R_{Gon}	Internal gate resistor for ON signal		22[4]		Ω
R_{Goff}	Internal gate resistor for OFF signal		22[4]		Ω
C_{ps}	Primary to secondary capacitance		12		pF

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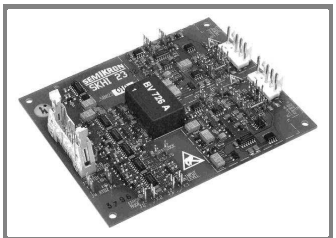
SKHI 23/17 (R) ...



SEMIDRIVER™

Medium Power Double IGBT Driver

SKHI 23/17 (R)

Features

- SKHI 23/17 drives all SEMIKRON IGBTs with V_{CES} up to 1700 V (VCE-monitoring adjusted from factory for 1700 V-IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drivers
- CMOS / TTL (HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers (no opto couplers)
- Supply undervoltage monitoring (< 13 V)
- Error memory / ouput signal (LOW or HIGH logic)
- Driver interlock top / bottom
- Internal isolated power supply

Typical Applications

- High frequency SMPS
- Half and Full bridges
- Three phase motor inverters
- High power UPS

1) This current value is a function of the output load condition
2) Operating fsw = 0 Hz
3) This value does not consider t_{on} of IGBT and t_{MIN} adjusted by R_{CE} and C_{CE}; see also fig. 14
4) Matched to be used with IGBTs < 100 A; for higher currents, see table 4
5) With R_{CE} = 36 kΩ, C_{CE} = 470 pF; see fig. 6
6) Factory adjusted; other values see table 3

Absolute Maximum Ratings		T_a = 25 °C, unless otherwise specified	
Symbol	**Conditions**	**Values**	**Units**
V_S	Supply voltage primary	18	V
V_{iH}	Input signal voltage (HIGH) (for 15 V and 5 V input level)	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	± 8	A
$Iout_{AV}$	Output average current	± 50	mA
V_{CE}	Collector emitter voltage sense	1700	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
$V_{isol\ IO}$	Isolation test volt. IN-OUT (2 sec. AC)	4000	V
$R_{Gon\ min}$	minimal R_{Gon}	2,7	Ω
$R_{Goff\ min}$	minimal R_{Goff}	2,7	Ω
$Q_{out/pulse}$	charge per pulse	4,8	µC
T_{op}	Operating temperature	- 25 ... + 85	°C
T_{stg}	Storage temperature	- 25 ... + 85	°C

Characteristics		T_a = 25 °C, unless otherwise specified			
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Units**
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_S	Supply current (max.)		0,32[1]		A
I_{SO}[2]	Supply current primary side (standby)		0,12		A
V_{iT+}	Input threshold voltage (HIGH) min.				
	15 V input level	12,5			V
	for 5 V input level	2,4			V
V_{iT-}	Input threshold voltage (LOW) max.				
	for 15 V input level			3,6	V
	for 5 V input level			0,50	V
$V_{G(on)}$	Turn-on output gate voltage		+ 15		V
$V_{G(off)}$	Turn-off output gate voltage		- 8		V
f	Maximum operating frequency		see fig. 15		
$td(on)_{IO}$	Input-output turn-on propagation time		1,4		µs
$td(off)_{IO}$	Input-output turn-off propagation time		1,4		µs
$t_{d(err)}$	Error input-output propagation time		1,0[3]		µs
t_{TD}	Dead time		10[6]		µs
V_{CEstat}	Reference voltage for V_{CE} monitoring		6,3[5]		V
R_{Gon}	Internal gate resistor for ON signal		22[4]		Ω
R_{Goff}	Internal gate resistor for OFF signal		22[4]		Ω
C_{ps}	Primary to secondary capacitance		12		pF

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Block diagramm SKHI 23

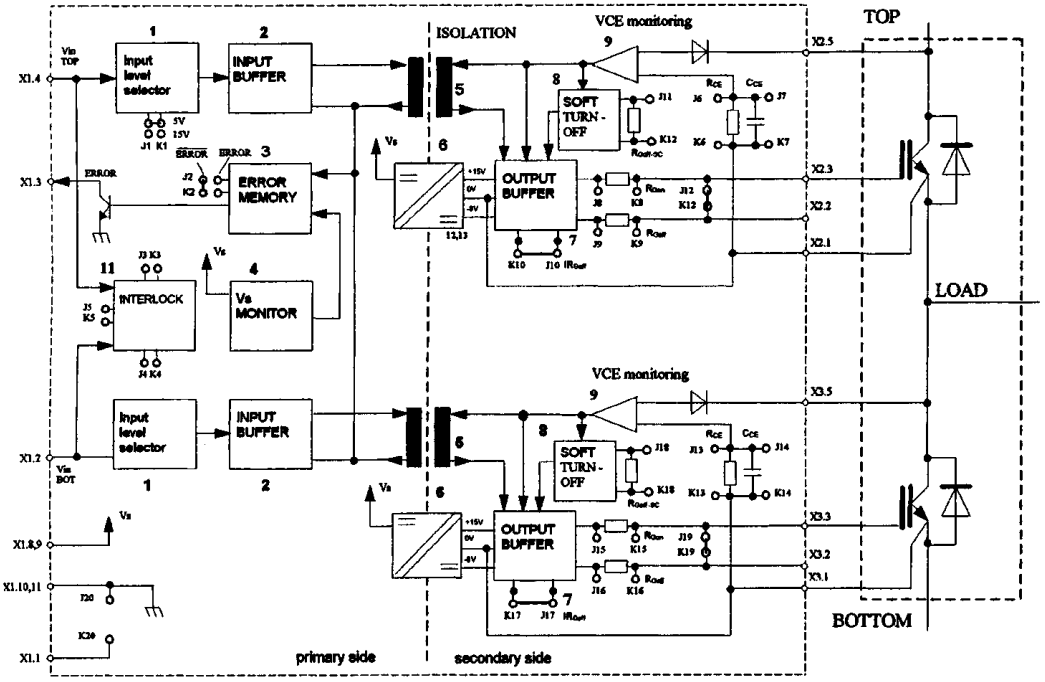
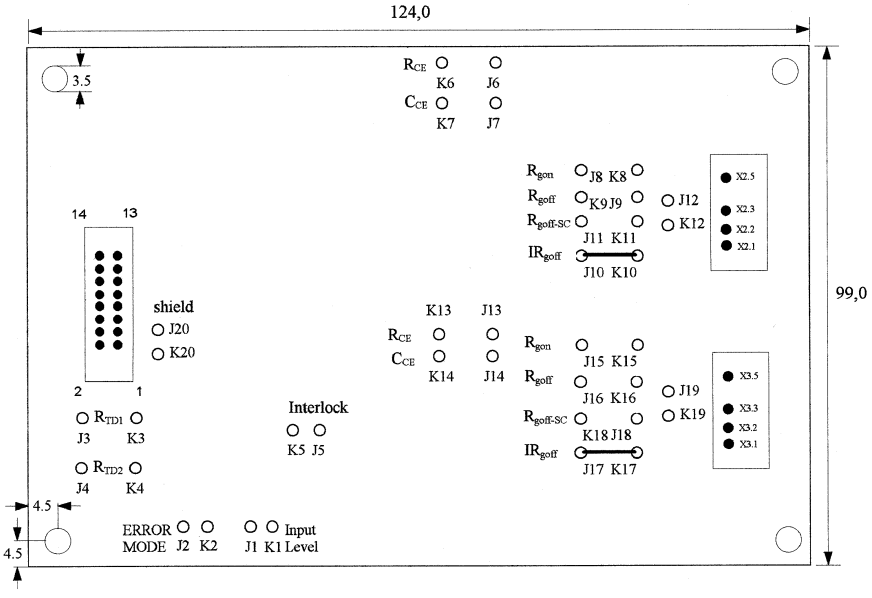


Fig. 1 The numbers refer to the description on page B14 – 45, section B.



Input connector = 14 pin flat cable according to DIN 41651
Output connector = MOLEX 41791 Series (mates with 41695 crimp terminals 7258)

Fig. 2 Dimensions (in mm) and connections of the SKHI 23

SEMIDRIVER™ SKHI 23/12
SEMIDRIVER™ SKHI 23/17

Medium Power Double IGBT Driver

Overview

The new intelligent double IGBT driver, SKHI 23 respectively SKHI 23/17 is a standard driver for all power IGBTs in the market.

SKHI 23/12 drives all IGBTs with V_{CE} up to 1200 V. SKHI 23/17 drives all IGBTs with V_{CE} up to 1700 V. To protect the driver against moisture and dust it is coated with varnish. The adaption of the drivers to the application has been improved by using pins to changing several parameters and functions. The connections to the IGBTs can be made by using only one MOLEX connector with 12 pins or by using 2 separate connectors with 5 pins for each IGBT.

The high power outputs capability was designed to switch high current double or single modules (or paralleled IGBTs). The output buffers have been improved to make it possible to switch up to 200 A IGBT modules at frequencies up to 20 kHz.

A new function has been added to the short circuit protection circuitry (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages. This means an increase in the final output power.

Integrated DC/DC converters with high galvanic isolation (4 kV) ensures that the user is protected from the high voltage (secondary side).

The power supply for the driver may be the same as used in the control board (0/+15 V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75 kV/µs).

The driver input stages are connected directly to the control board output and due to different control board operating voltages, the input circuit includes a user voltage level selector (+15 V or +5 V). In the following only the designation SKHI 23 is used. This is valid for both driver versions. Any unique features will be marked as SKHI 23/12 (V_{CE} = 1200 V) or SKHI 23/17 (V_{CE} = 1700 V) respectively.

A. Features and Configuration of the Driver

a) A short description is given below. For detailed information, please refer to section B. The following is valid for both channels (TOP and BOTTOM) unless specified.

b) The SKHI 23 has an INPUT LEVEL SELECTOR circuit for two different levels. It is preset for CMOS (15 V) level, but can be changed by the user to HCMOS (5 V) level by solder bridging between pins J1 and K1. For long input cables, we do not recommend the 5 V level due to possible disturbances emitted by the power side.

c) An INTERLOCK circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a "deadtime" can be adjusted by putting additional resistors between pins J3 and K3 (R_{TD1}) and pins J4 and K4 (R_{TD2}). Therefore it will be possible to reduce the deadtimet t_{TD} (see also table 3).
The interlocking may also be inhibit by solder bridging between pins J5 and K5 to obtain two independent drivers.

d) The ERROR MEMORY blocks the transmission of all turn-on signals to the IGBT if either a short circuit or malfunction of Vs is detected, a signal is sent to the external control board through an open collector transistor. It is preset to "high-logic" but can be set to "low-logic" (ERROR).

e) The V_s MONITOR ensures that V_s actual is not below 13 V.

f) With a FERRITE TRANSFORMER the information between primary and secondary may flow in both directions and high levels of dv/dt and isolation are obtained.

g) A high frequency DC/DC CONVERTER avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. An isolated ferrite transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT. With this feature, we can use the same power supply used in the external control circuit, even if we are using more than one SKHI 23, e.g. in three-phase configurations.

h) Short circuit protection is provided by measuring the collector-emitter voltage with a V_{CE} MONITORING circuit. An additional circuit detects the short circuit after a delay (adjusted with R_{CE} (this value can only be reduced) and C_{CE} (this value can only be increased) and decreases the turn off speed (adjusted by $R_{goff\text{-}SC}$) of the IGBT. SOFT TURN-OFF under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation.

i) The OUTPUT BUFFER is responsible for providing the correct current to the gate of the IGBT. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT) the equivalent value of R_{gon} and the R_{goff} must be matched to the optimum value. This can be done by putting additional parallel resistors R_{gon}, R_{goff} with those already on the board. If only one IGBT is to be used, (instead of paralleled IGBTs) only one cable could be connected between driver and gate by solder bridging between the pins J12 and K12 (TOP) as well as between J19 and K19 (Bottom).

j) Fig. 1 shows a simplified block diagram of the SKHI 23 driver. Some preliminary remarks will help the understanding:

- Stabilised +15 V must be present between pins X1.8,9 (V_s) and X1.10,11 (⊥); an input signal (ON or OFF command to the IGBTs) from the control system is supplied to pins X1.2 and X1.4 (V_{in}) where HIGH=ON and LOW=OFF. The pin X1.1 can be used as a shield for the input signals.
- Pin X2.5 on TOP (and X3.5 on BOT) at secondary side is normally connected to the collector of the IGBTs to monitor V_{CE}, but for initial tests without connecting the IGBT it must be connected to pin X2.1 on TOP (and X3.1 on BOT) to avoid ERROR signal and enable the output signals to be measured.
- The RESET is performed when both input V_{in} signals are zero (TOP = BOT = LOW).
- To monitor the ERROR signal in “high-logic”, a pull-up resistor must be provided between pin X1.3 and V_s.
- Table 1 (see page B 14–46) shows the factory adjustment and the different possible adjustments of the pins.

B. Description of the Circuit Block Diagram (Fig. 1)

The circuit in Fig. 1 shows the input on the left and output on the right (primary/secondary).

1. Input level circuit

This circuit was designed to accept two different CMOS logic voltage levels. The standard level is +15 V (factory adjusted) intended for noisy environments or when long connections (l > 50 cm) between the external control circuit and SKHI 23 are used, where noise immunity must be considerate. For lower power, and short connections between control and driver, the TTL-HCMOS level (+5 V) can be selected by solder bridging between J1 and K1, specially useful for signals coming from uP based controllers.

Fig.3 Selecting J1, K1 for 5 V level (TTL-HCMOS)

When connecting the SKHI 23 to a control board using short connections no special attention needs to be taken (Fig. 4a).

Otherwise, if the length is 50 cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL level should be avoided and CMOS/ 15 V is to be used instead; flat cable must have the pairs of conductors twisted or be shielded to reduce EMI/RFI susceptibility (Fig. 4b). If a shielded cable is used, it can be connected to pinX1.1 and coupled to 0 V through a capacitor, resistor or by solder bridging between pins J20 and K20.

As the input impedance of the INPUT LEVEL SELECTOR circuit is very high, an internal pull-down resistor keeps the IGBT in OFF state in case the V_{in} connection is interrupted or left non connected.

The following overview is showing the input treshold voltages

V_{IT+} (High)	min	typ	max
15 V	9,5 V	11,0 V	12,5 V
5 V	1,8 V	2,0 V	2,4 V

V_{IT-} (Low)	min	typ	max
15 V	3,6 V	4,2 V	4,8 V
5 V	1,8 V	0,65 V	0,8 V

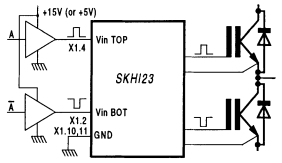


Fig. 4a Connecting the SKHI 23 with short cables

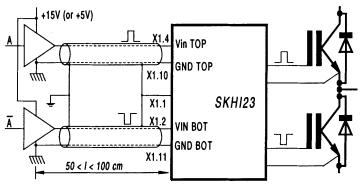


Fig. 4b Connecting the SKHI 23 with long cables

2. Input buffer

This circuit enables and improves the input signal V_{in} to be transferred to the pulse transformer and also prevents spurious signals being transmitted to the secondary side.

3. Error memory and RESET signal

The ERROR memory is triggered only by following events:

- short circuit of IGBTs
- V_s-undervoltage

In case of short circuit, the V_{CE} monitor sends a trigger signal (fault signal) through the pulse transformer to a FLIP-FLOP on the primary side giving the information to an open-collector transistor (pin X1.3), which may be connected to the external control circuit as ERROR message in “high-logic” (or “low-logic” if pins J2 and K2 are bridged). If V_s power supply falls below 13 V for more than 0,5 ms, the FLIP-FLOP is set and pin X1.3 is activated. For “high-logic” (factory preset), an external R_C must be connected, preferably in the control main board. In this way the connection between main board and driver is also monitored.

Function	pin description	adjustment by factory		possibilities of functions
input level selector	J1 / K1	not bridged ⇒15V CMOS		soldering bridged ⇒5V HCMOS
error - logic	J2 / K2	not bridged ⇒HIGH-aktiv		soldering bridged ⇒LOW-aktiv
interlock time	J3 / K3 (TOP R_{TD1}) J4 / K4 (BOT R_{TD2})	not equiped ⇒max. t_{TD} = 10 µs		adjustment according table 3
interlock of TOP and BOTTOM	J5 / K5	not bridged ⇒interlock activ		soldering bridged ⇒no interlock
$R_{CE\ TOP}$	J6 / K6	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ TOP}$	J7 / K7	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ TOP}$	J8 / K8	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ TOP}$	J9 / K9	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ TOP}$	J10 / K10	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ TOP}$	J11 / K11	equiped with ⇒R_{goffSC}= 22 Ω		
TOP: one IGBT/ paralleled IGBTs	J12 / K12	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
$R_{CE\ BOT}$	J13 / K13	**SKHI 23/12** not equiped ⇒ R_{CE}= 18 kΩ	**SKHI 23/17** not equiped ⇒ R_{CE}= 36 kΩ	adjustment according tab. 4a/b
$C_{CE\ BOT}$	J14 / K14	**SKHI 23/12** not equiped ⇒ C_{CE}= 330 pF	**SKHI 23/17** not equiped ⇒ C_{CE}= 470 pF	adjustment according tab. 4a/b
$R_{gon\ BOT}$	J15 / K15	**SKHI 23/12** not equiped ⇒ R_{gon}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{gon}= 22 Ω	adjustment according tab. 4a/b
$R_{goff\ BOT}$	J16 / K16	**SKHI 23/12** not equiped ⇒ R_{goff}= 22 Ω	**SKHI 23/17** not equiped ⇒ R_{goff}= 22 Ω	adjustment according tab. 4a/b
$IR_{goff\ BOT}$	J17 / K17	equiped with IR_{goff}= 0 Ω		adjustment according tab. 4a/b
$R_{goffSC\ BOT}$	J18 / K18	equiped with ⇒R_{goffSC}= 22 Ω		
BOT: one IGBT/ paralleled IGBTs	J19 / K19	not bridged ⇒2 cables to gates		soldering bridged ⇒1 cable to gate
shield	J20 / K20	not bridged ⇒no screening		soldering bridged ⇒screening to GND

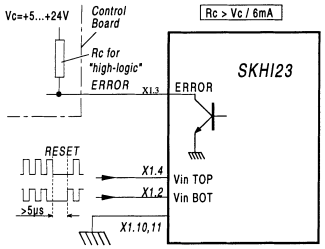


Fig. 5 Driver status information ERROR, and RESET

If “low-logic” version ERROR is used (pins J2 and K2 are bridged), an internal pull-up resistor (internally connected to V_S) is provided, and the ERROR signal from more SKHI23s can be connected together to perform an wired-or-circuit.

The ERROR signal may be disabled either by delivering zero to both signal inputs (RESET = active = $V_{in\text{-}TOP}$ = $V_{in\text{-}BOT}$ = 0) or by switching the power supply (V_S) off. The “RESET” signal width must be more than 5 µs long (see Fig. 5).

FAULT	RESET	ERROR[1)]	switching on of IGBT
no	no active	0	possible
no	active	0	not possible
yes	no active	1	not possible
yes	active	0	not possible

1) default logic (HIGH); for LOW logic the signals are complementary

Table 2 ERROR signal truth table

The open-collector transistor (pin X1.3) may be connected through a pull-up resistor to an extemal (internal V_S for the “low-logic” version) voltage supply +5 V...+24 V, limiting the current to I_{sink} 6 mA.

4. Power supply (V_s) monitor

The supply voltage V_S is monitored. If it falls below 13 V an ERROR signal is generated and the turn-on pulses for the IGBTs gate are blocked.

5. Pulse transformer

It transmits the turn-on and turn-off signals to the driver’s secondary side. In the reverse direction the ERROR signal from the V_{CE} monitoring is transmitted via the same transformer. The isolation is 4 kV_{AC}.

6. DC/DC converter

In the primary side of the converter, a half-bridge inverter transfers the necessary energy from V_S to the secondary of a ferrite transformer. In the secondary side, a full bridge and filters convert the high frequency signal coming from the primary to DC levels (+15V/- 8V) that are stabilised by a voltage regulator circuit.

7. Output buffer

The output buffer is supplied by the +15V/- 8V from the DC/DC converter and amplifies the control signal received from the pulse transformer. If the operation proceeds normally (no fault), the signal is transmitted to the gate of an IGBT through R_{gon} and R_{goff}. The output stage has a MOSFET pair which is able to source/sink up to 8 A peak current to/from the gate improving the turn-on/off time of the IGBT. Additionally, we can select I_{Rgoff} (see Fig. 2) either to discharge the gate capacitance with a voltage source (standard) or with a current source, specially design for the 1700 V IGBT series (it speeds up the turn-off time of the IGBT). The present factory setting is voltage source (I_{Rgoff} = 0Ω). and to change to current source I_{Rgoff}, must be adjusted, while R_{goff} = 0.

8. Soft turn-off

In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with R_{goff} and turns-off the IGBT at a lower speed. This produces a smaller voltage spike (due LSTRAY ’ di/dt) above the DC link by reducing the di/dt value. Because in short-circuit conditions the Homogeneous IGBT’s peak current increases up to 8 times the nominal current (up to 10 times with Epitaxial IGBT structures), and some stray inductance is ever present in power circuits, it must fall to zero in a longer time than at normal operation. This “soft turn-off time” can be reduced by connecting a parallel resistor R_{goff}-SC (see Fig. 2) with those already on the printed circuit board.

9. V_{CE} monitoring

This circuit is responsible for short-circuit sensing. Due to the direct measurement of V_{CEstat} on the IGBT’s collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side. The recognition of which V_{CE} level must be considered as a short circuit event, is adjusted by R_{CE} and C_{CE} (see Fig. 2), and it depends of the IGBT used. For the drivers SKHI23/12 typical values R_{CE} =18 kΩ and C_{CE} =330 pF for SKHI 10 are delivered from factory (Fig. 6, curve 2). Using SKHI 10/17 the driver will be delivered with R_{CE} = 36 kΩ and C_{CE} = 470 pF from factory.

The V_{CEref} is not static but a dynamic reference which has an exponential shape starting at about 15 V and decreases to V_{CEstat} (determinated by R_{CE}), with a time constant τ (controlled by C_{CE}).

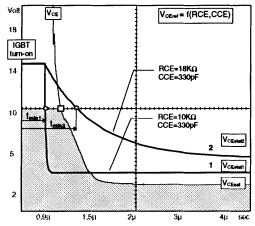


Fig. 6 V_{CEref} waveform with parameters R_{CE}, C_{CE}

Adjustements for SKHI 23/12

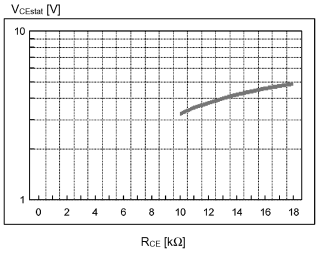


Fig. 7a V_{CEstat} as function of R_{CE}

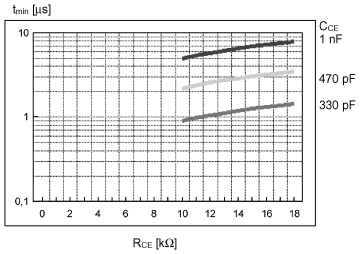


Fig. 7b t_{min} as function of R_{CE} and C_{CE}

Adjustements for SKHI 23/17

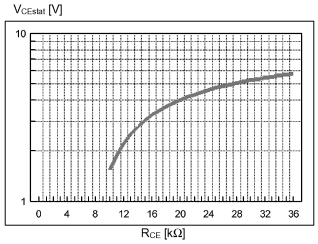


Fig. 7c V_{CEstat} as function of R_{CE}

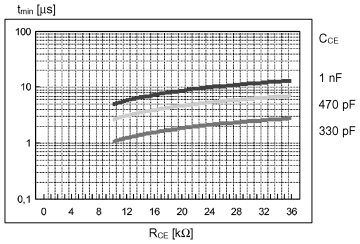


Fig. 7d t_{min} as function of R_{CE} and C_{CE}

The V_{CEstat} must be adjusted to remain above V_{CEsat} in normal operation (the IGBT is already in full saturation).

To avoid a false failure indication when the IGBT just starts to conduct (V_{CEsat} value is still too high) some decay time must be provided for the V_{CEref}. As the V_{CE} signal is internally limited at 10 V, the decay time of V_{CEref} must reach this level after V_{CE} or a failure indication will occur (see Fig.6, curve 1). A t_{min} is defined as function of V_{CEstat} and τ to find out the best choice for R_{CE} and V_{CE} (see Fig.6, curve 2). The time the IGBT come to the 10 V (represented by a "□" in Fig. 6) depends on the IGBT itself and R_{gon} used.

The R_{CE} and C_{CE} values can be found from Fig. 7a and 7b for SKHI 23/12 and from Fig. 7c and 7d for SKHI 23/17 by taking the V_{CEstat} and t_{min} as input values with following remarks:

- R_{CE} > 10KΩ
- C_{CE} < 2,7nF

Attention!: If this function is not used, for example during the experimental phase, the V_{CE} MONITORING must be connected with the EMITTER output to avoid possible fault indication and consequent gate signal blocking.

10. R_{gon}, R_{goff}

These two resistors are responsible for the switching speed of each IGBT. As an IGBT has input capacitance (varying during the switching time) which must be charged and discharged, both resistors will dictate what time must be taken to do this. The final value of resistance is difficult to predict, because it depends on many parameters, as follows:

- DC-link voltage
- stray inductance of the circuit
- switching frequency
- type of IGBT

The driver is delivered with two R_g resistors (22 Ω) on the board. This value can be reduced to use the driver with bigger modules or higher frequencies, by putting additional resistors in parallel.

The outputs G_{on} and G_{off} were previewed to connect the driver with more than one IGBT (paralleling). In that case we need both signals ON/OFF separately to connect additional extremal resistors R_{gon} and R_{goff} for each IGBT. If only one IGBT is to be used, we suggest connecting both outputs together by solder bridging between pins J12 and K12 and respectiveley pins J19 and K19 to save on external connection. We also suggest using two restistors for R_{gon} and two resistors for R_{goff} when using low values of resistance, due the high current peak (up to 8 A) which could damage a single resistor.

11. Interlock

The interlock circuit prevents the IGBT turning on before the gate charge of the other IGBT is completely discharged. It should be set to delay time longer than the turn-off time of the IGBT. From the factory: t_{TD} = 10 µs. By putting additional resistors onto the pins J3/K3 ($R_{TD\ TOP}$) and onto the pins J4/K4 ($R_{TD\ BOT}$) the interlock time t_{TD} can be reduced (see table 3).

$R_{TD1} = R_{TD2}$	interlock time t_{TD}
10 kΩ	0,9 µs
22 kΩ	1,8 µs
33 kΩ	2,5 µs
47 kΩ	3,2 µs
68 kΩ	4,0 µs
100 kΩ	5,0 µs
330 kΩ	7,7 µs
not equiped (adjustement by factory)	10 µs

It have to be considered: $R_{TD1} = R_{TD2}$ 10 kΩ
Table 3 adjustement of interlock time

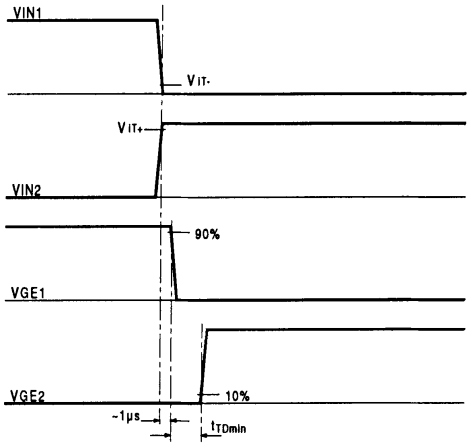


Fig. 8 Interlock function time diagram

C. Operating Procedure

1. One dual IGBT connection

To realize the correct switching and short-circuit monitoring of one IGBT-module some additional components must be used (Fig. 9).

Typical component values: *)

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0

Table 4a 1200V IGBT@ DC-link< 700V

SK-IGBT-Module	R_{Gon} Ω	R_{Goff} Ω	C_{CE} pF	R_{CE} kW	I_{rgoff} Ω
SKM 75GB123D	15	15	470	36	0
SKM 100GB123D	12	12	470	36	0
SKM 150GB123D	10	10	470	36	0
SKM 200GB123D	8,2	8,2	470	36	0
SKM 300GB123D	6,8	6,8	470	36	0

Table 4b 1700V IGBT@ DC-link< 1000V

*) Only starting values, for final optimization.

The adjustment of R_{goffSC} (factory adjusted R_{goffSC} = 22 Ω) should be done observing the overvoltages at the module in case of short circuit. When having a low inductive DC-link the module can be switched off faster.

The shown values should be considered as standard values for a mechanical/electrical assembly, with acceptable stray inductance level, using only one IGBT per SKHI 23 driver. The final optimised value can be found only by measuring.

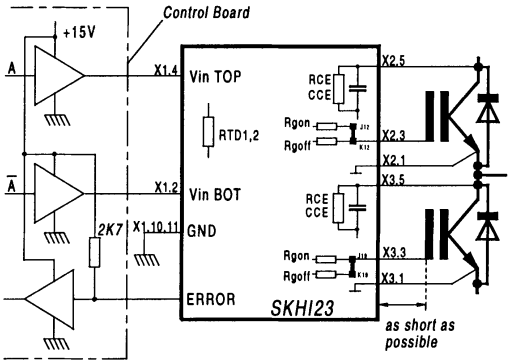


Fig. 9 Preferred dual IGBT-module standard circuit

2. Paralleling IGBTs

The parallel connection is recommended only by using IGBTs with homogeneous structure (IGHT), that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element. Care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT (Fig. 10). The IGBTs must have independent values of R_{gon} and R_{goff}, and an auxiliary emitter resistor R_e as well as an auxiliary collector resistor R_c must also be used. The external resistors R_{gonx}, R_{goffx}, R_{ex} and R_{cx} should be mounted on an additional circuit board near the paralleled modules, and the R_{gon}/R_{goff} should be changed to zero ohms.

The R_{ex} has a value of 0,5 Ω and its function is to avoid the main current to circulate by the auxiliary ermitter what could make the ermitter voltage against ground unbalanced.

The R_{cx} assumes a value of 47 Ω and its function is to create an average of V_{CEsat} in case of short circuit for V_{CE}-monitoring.

The mechanical assembly of the power circuit must be symmetrical and low inductive.

The maximum recommended gate charge is 4,8 µC.

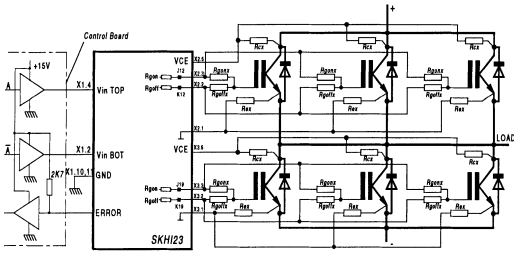


Fig. 10 Preferred circuit for paralleld dual IGBT-modules

D. Signal Waveforms

The following signal waveforms were measured under the conditions below:

- V_S = 15 V
- T_{amb} = 25 °C
- load = SKM75GB120D
- R_{CE} = 18 kΩ
- C_{CE} = 330 pF
- U_{DC} = 600 V
- I_C = 100 A

All results are typical values if not otherwise specified.

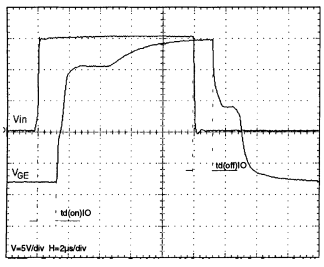


Fig. 11 Input and output voltage propagation time

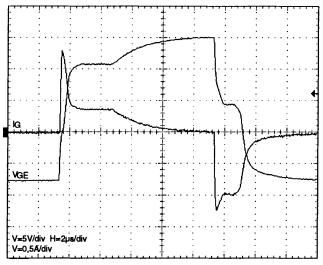


Fig. 12 Output voltage V_{GE} and output current (I_G)

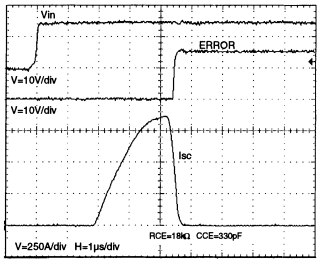


Fig.13 Short circuit and ERROR propagation time worste case (V_{IN} with SC already present)

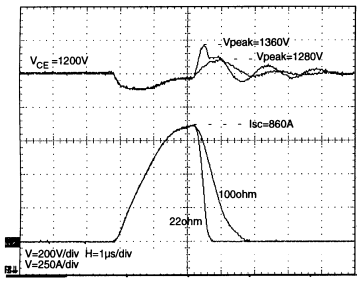


Fig.14 Effect of $R_{goff\text{-}SC}$ in short - circuit

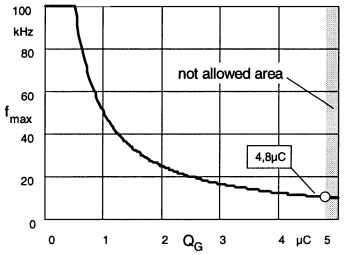


Fig. 15 Maximum operating frequency x gate charge

The limit frequency of SKHI 23 depends on the gate charge connected in its output pins.

If small IGBT modules are used, the frequency could theoretically reach 100 kHz. For bigger modules or even paralleled modules, the maximum frequency must be determinate (Fig. 15). Q_G is the total equivalent gate charge connected to the output of the driver. The maximum allowed value is limited (about 4,8 µC).

E. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than (V_S + 0,3 V) or under - 0,3 V may destroy these inputs.

Therefore the following safety requirements are to be observed:

- To make sure that the control signals do not see overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the hybrid driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded. The same safety requirements apply to the IGBTs.

2. The connecting leads between the driver and the power module must be as short as possible, and should be twisted.

3. Any parasitic inductance should be minimized. Overvoltages may be damped by C or RCD snubber networks between the main terminals [3] = C1 (+) and [2] = E2 (-) of the power module.

4. When first operating a newly developed circuit, low collector voltage and load current should be used in the beginning. These values should be increased gradually, observing the turn-off behavior of the free-wheeling diodes and the turn-off voltage spikes across the IGBT by means of an oscilloscope. Also the case temperature of the power module should be monitored. When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.

For further details ask SEMIKRON

10.4 Data Sheet for AD820

ANALOG DEVICES

Single Supply, Rail to Rail Low Power FET-Input Op Amp

AD820

FEATURES

True Single Supply Operation
- Output Swings Rail-to-Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V
- Dual Supply Capability from ±1.5 V to ±18 V

Excellent Load Drive
- Capacitive Load Drive Up to 350 pF
- Minimum Output Current of 15 mA

Excellent AC Performance for Low Power
- 800 μA Max Quiescent Current
- Unity Gain Bandwidth: 1.8 MHz
- Slew Rate of 3.0 V/μs

Excellent DC Performance
- 800 μV Max Input Offset Voltage
- 1 μV/°C Typ Offset Voltage Drift
- 25 pA Max Input Bias Current

Low Noise
- 13 nV/$\sqrt{\text{Hz}}$ @ 10 kHz

APPLICATIONS

Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

PRODUCT DESCRIPTION

The AD820 is a precision, low power FET input op amp that can operate from a single supply of +3.0 V to 36 V, or dual supplies of ±1.5 V to ±18 V. It has true single supply capability with an input voltage range extending below the negative rail,

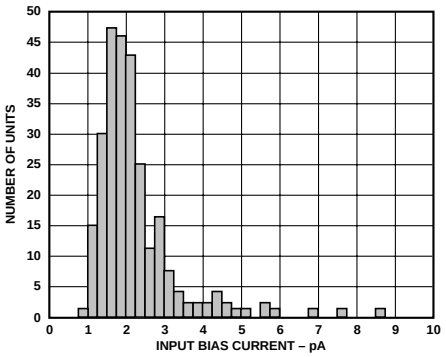
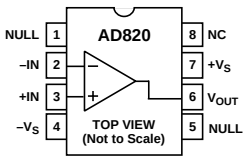


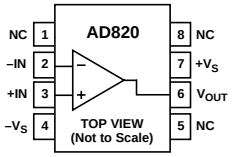
Figure 1. Typical Distribution of Input Bias Current

CONNECTION DIAGRAMS

8-Lead Plastic Mini-DIP



8-Lead SOIC



NC = NO CONNECT

allowing the AD820 to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

Offset voltage of 800 μV max, offset voltage drift of 1 μV/°C, typ input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/μs slew rate are provided for a low supply current of 800 μA. The AD820 drives up to 350 pF of direct capacitive load and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD820 is available in three performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C. There is 3 V grade—the AD820A-3V, rated over the industrial temperature range.

The AD820 is offered in two varieties of 8-lead package: plastic DIP, and surface mount (SOIC).

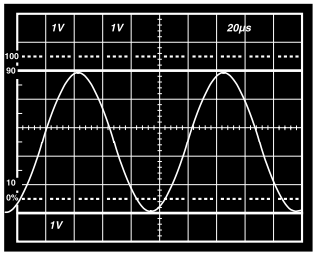


Figure 2. Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD820—SPECIFICATIONS (V_S = 0, 5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_O = 0 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V							
	R_L = 100k	400	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k to 2.5 V							
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–0.2		4	–0.2		4	V
T_{MIN} to T_{MAX}		–0.2		4	–0.2		4	V
CMRR	V_{CM} = 0 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|\|0.5$			$10^{13}\|\|0.5$		Ω‖pF
Common Mode			$10^{13}\|\|2.8$			$10^{13}\|\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		620	800		620	800	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		dB
T_{MIN} to T_{MAX}		70			66			dB

(V_S = +5 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.3	0.4	mV
Max Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = –5 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 4 V to –4 V							
	R_L = 100k	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±4.5 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.8		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–5.2		4	–5.2		4	V
T_{MIN} to T_{MAX}		–5.2		4	–5.2		4	V
CMRR	V_{CM} = –5 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω‖pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			30			30		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		650	800		620	800	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

AD820–SPECIFICATIONS (V_S = ±15 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.0	mV
Max Offset over Temperature			0.5	3		0.5	2	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	10	pA
	V_{CM} = –10 V		40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = +10 V to –10 V							
	R_L = 100k	500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500			V/mV
	R_L = 10k	100	500		100	500		V/mV
T_{MIN} to T_{MAX}		100			100			V/mV
	R_L = 1k	30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		nV/√Hz
f = 100 Hz			21			21		nV/√Hz
f = 1 kHz			16			16		nV/√Hz
f = 10 kHz			13			13		nV/√Hz
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±10 V		–85			–85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1		µs
to 0.01%			4.5			4.5		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–15.2		14	–15.2		14	V
T_{MIN} to T_{MAX}		–15.2		14	–15.2		14	V
CMRR	V_{CM} = –15 V to 12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}		70			74			dB
Input Impedance								
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω‖pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Short Circuit Current			45			45		mA
Capacitive Load Drive			350			350		
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		700	900		700	900	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

(V_S = 0, 3 volts @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A-3V Min	Typ	Max	Units
DC PERFORMANCE					
Initial Offset			0.2	1	mV
Max Offset over Temperature			0.5	1.5	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V to +2 V		2	25	pA
at T_{MAX}			0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V				
	R_L = 100k	300	1000		V/mV
T_{MIN} to T_{MAX}		400			V/mV
	R_L = 10k	60	150		V/mV
T_{MIN} to T_{MAX}		80			V/mV
	R_L = 1k	10	30		V/mV
T_{MIN} to T_{MAX}		8			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise					
0.1 Hz to 10 Hz			2		µV p-p
f = 10 Hz			25		nV/√Hz
f = 100 Hz			21		nV/√Hz
f = 1 kHz			16		nV/√Hz
f = 10 kHz			13		nV/√Hz
Input Current Noise					
0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k to 1.5 V				
f = 10 kHz	V_O = ±1.25 V		–92		dB
DYNAMIC PERFORMANCE					
Unity Gain Frequency			1.5		MHz
Full Power Response	V_O p-p = 2.5 V		240		kHz
Slew Rate			3		V/µs
Settling Time					
to 0.1%	V_O = 0.2 V to 2.5 V		1		µs
to 0.01%			1.4		µs
INPUT CHARACTERISTICS					
Common-Mode Voltage Range[1]		–0.2		2	V
T_{MIN} to T_{MAX}		–0.2		2	V
CMRR	V_{CM} = 0 V to +1 V	60	74		dB
T_{MIN} to T_{MAX}		60			dB
Input Impedance					
Differential			$10^{13}\|\|0.5$		Ω||pF
Common Mode			$10^{13}\|\|2.8$		Ω||pF
OUTPUT CHARACTERISTICS					
Output Saturation Voltage[2]					
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7	mV
T_{MIN} to T_{MAX}				10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14	mV
T_{MIN} to T_{MAX}				20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55	mV
T_{MIN} to T_{MAX}				80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110	mV
T_{MIN} to T_{MAX}				160	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA		200	400	mV
T_{MIN} to T_{MAX}				400	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA		500	1000	mV
T_{MIN} to T_{MAX}				1000	mV
Operating Output Current		15			mA
T_{MIN} to T_{MAX}		12			mA
Short Circuit Current		18	25		mA
T_{MIN} to T_{MAX}		15			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current	T_{MIN} to T_{MAX}		620	800	µA
Power Supply Rejection	V_S+ = 3 V to 15 V	70	80		dB
T_{MIN} to T_{MAX}		70			dB

AD820–SPECIFICATIONS

NOTES
[1]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range (+ V_S – 1 V) to +V_S. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.
[2]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}). V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic DIP (N) . . . . . 1.6 Watts
  SOIC (R) . . . . . 1.0 Watts
Input Voltage . . . . . (+V_S + 0.2 V) to – (20 V + V_S)
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±30 V
Storage Temperature Range (N) . . . . . –65°C to +125°C
Storage Temperature Range (R) . . . . . –65°C to +150°C
Operating Temperature Range
  AD820A/B . . . . . –40°C to +85°C
Lead Temperature Range
  (Soldering 60 sec) . . . . . +260°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Lead Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Lead SOIC Package: θ_{JA} = 160°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD820AN	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820BN	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8
AD820AR	–40°C to +85°C	8-Lead SOIC	R-8
AD820BR	–40°C to +85°C	8-Lead SOIC	R-8
AD820AR-3V	–40°C to +85°C	8-Lead SOIC	R-8
AD820AN-3V	–40°C to +85°C	8-Lead Plastic Mini-DIP	N-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Characteristics–AD820

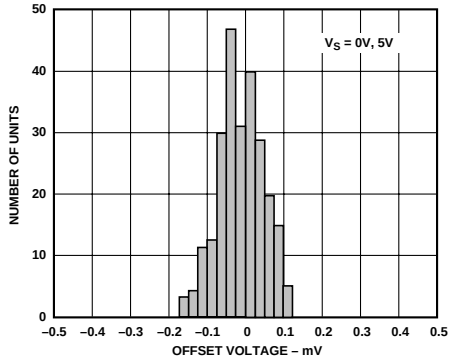


Figure 3. Typical Distribution of Offset Voltage (248 Units)

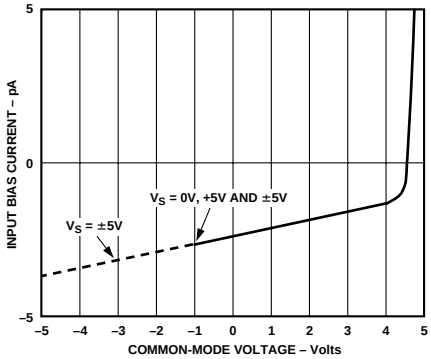


Figure 6. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

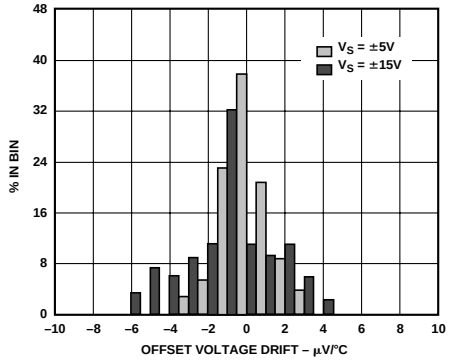


Figure 4. Typical Distribution of Offset Voltage Drift (120 Units)

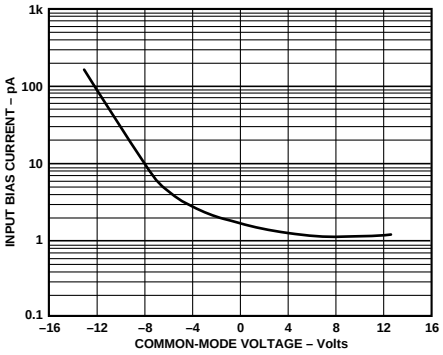


Figure 7. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

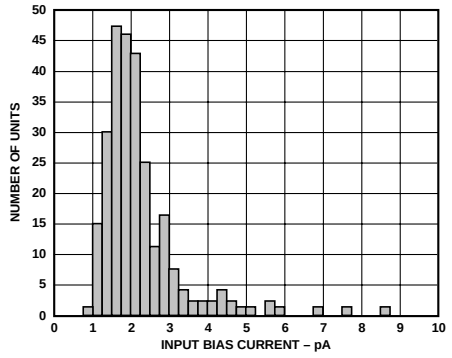


Figure 5. Typical Distribution of Input Bias Current (213 Units)

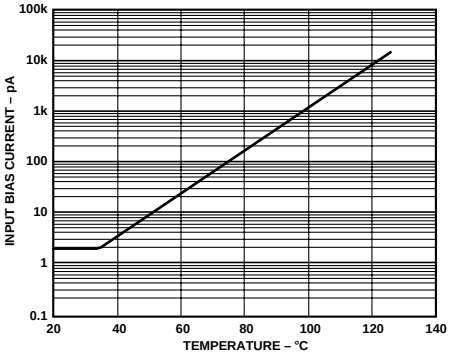


Figure 8. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0

AD820–Typical Characteristics

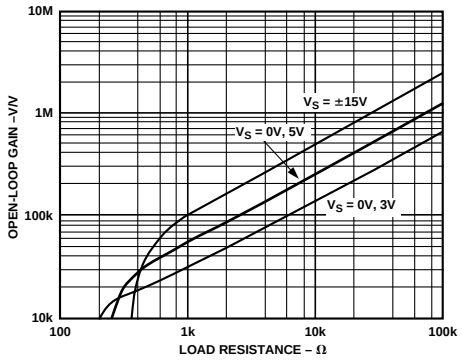


Figure 9. Open-Loop Gain vs. Load Resistance

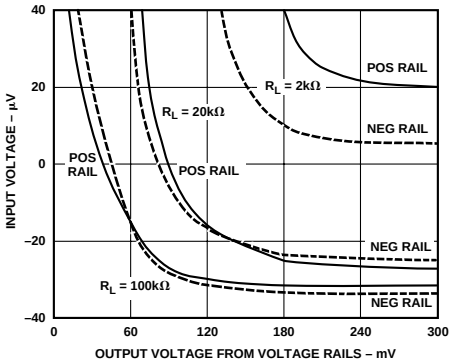


Figure 12. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; V_S = ±5 V

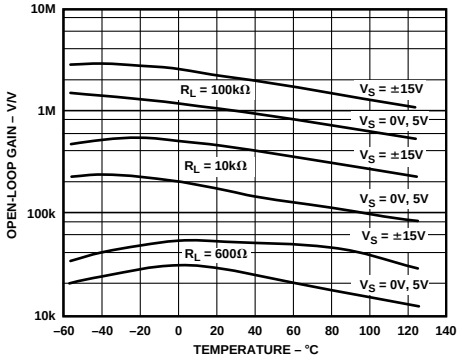


Figure 10. Open-Loop Gain vs. Temperature

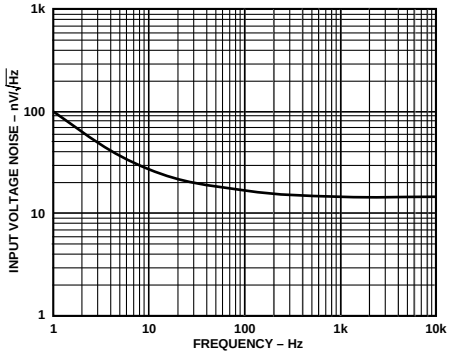


Figure 13. Input Voltage Noise vs. Frequency

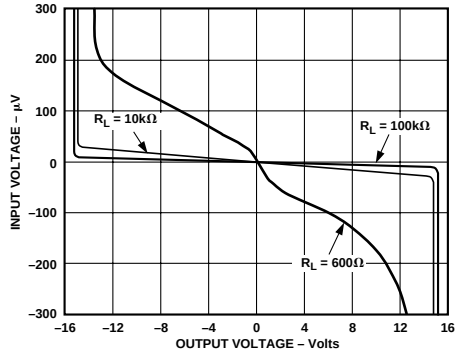


Figure 11. Input Error Voltage vs. Output Voltage for Resistive Loads

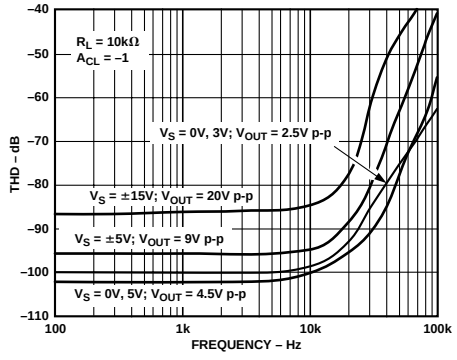


Figure 14. Total Harmonic Distortion vs. Frequency

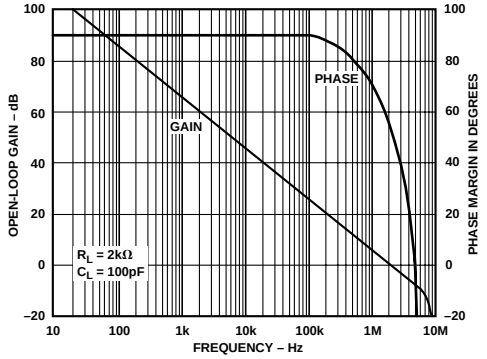


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

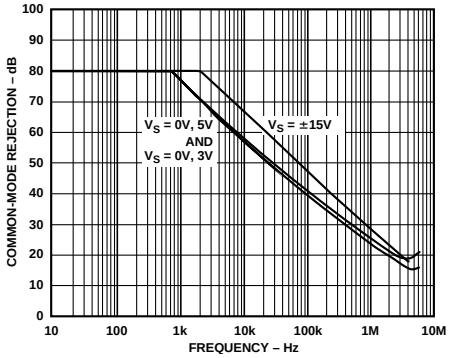


Figure 18. Common-Mode Rejection vs. Frequency

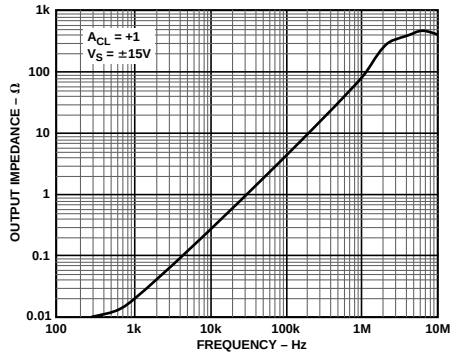


Figure 16. Output Impedance vs. Frequency

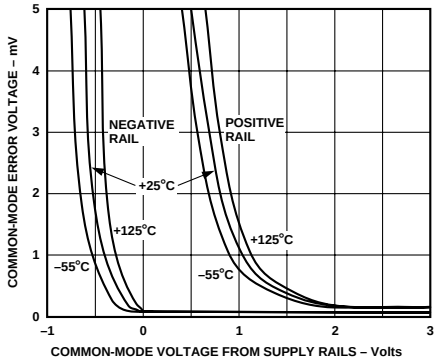


Figure 19. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails (V_S – V_{CM})

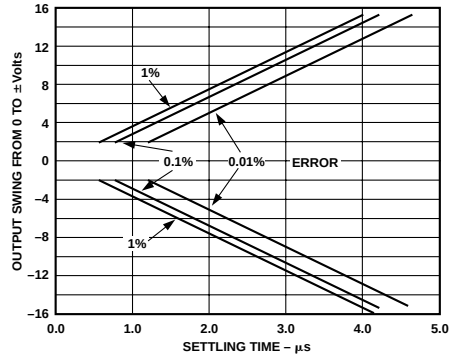


Figure 17. Output Swing and Error vs. Settling Time

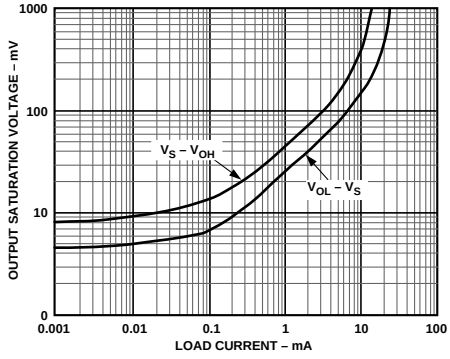


Figure 20. Output Saturation Voltage vs Load Current

AD820–Typical Characteristics

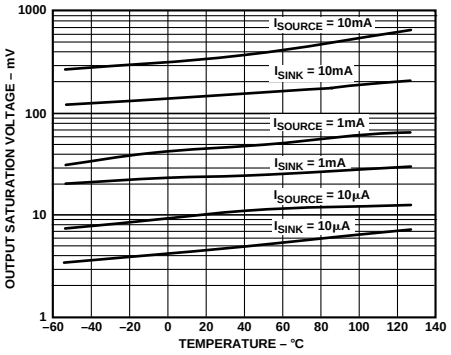


Figure 21. Output Saturation Voltage vs. Temperature

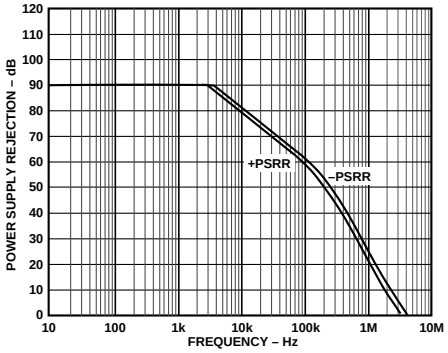


Figure 24. Power Supply Rejection vs. Frequency

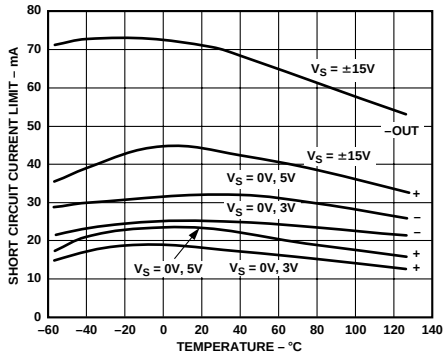


Figure 22. Short Circuit Current Limit vs. Temperature

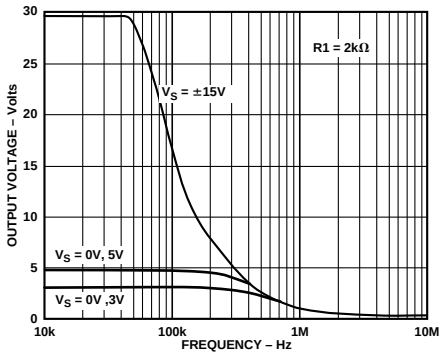


Figure 25. Large Signal Frequency Response

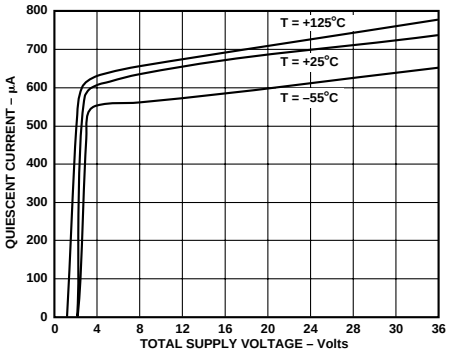


Figure 23. Quiescent Current vs. Supply Voltage vs. Temperature

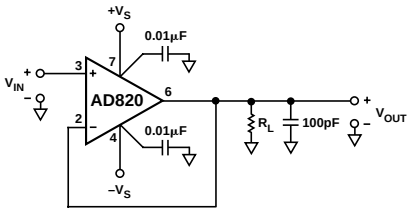


Figure 26. Unity-Gain Follower

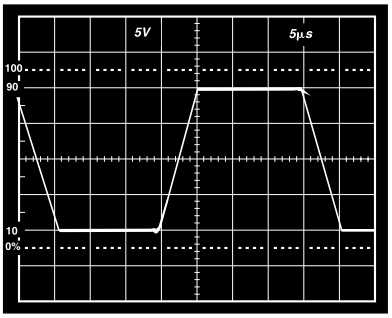


Figure 29. Large Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

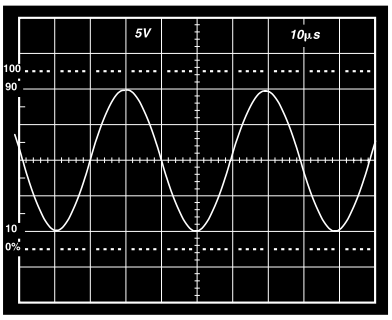


Figure 27. 20 V, 25 kHz Sine Input; Unity Gain Follower; $R_L = 600\ \Omega$, $V_S = \pm 15$ V

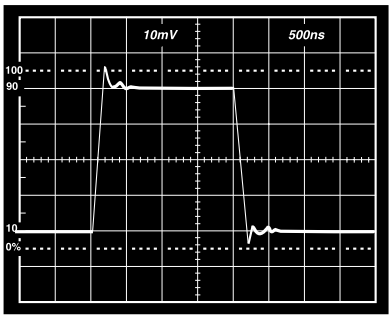


Figure 30. Small Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

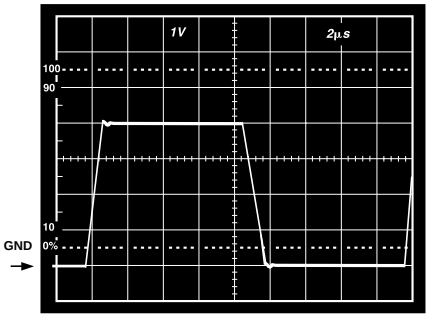


Figure 28. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

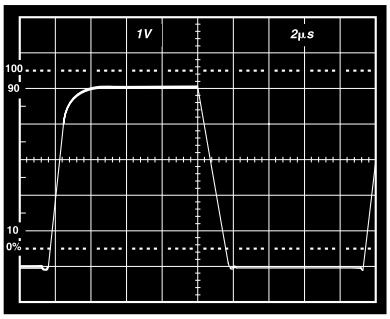


Figure 31. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

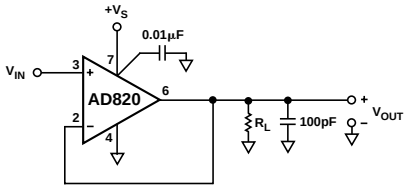


Figure 32. Unity-Gain Follower

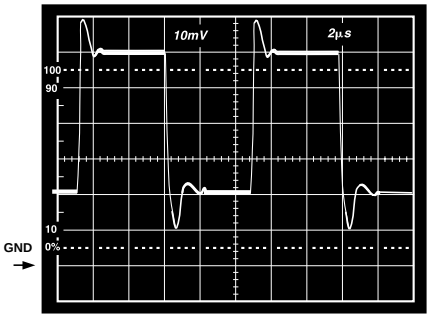


Figure 35. V_S = +5 V, 0 V; Unity Gain Follower Response to 40 mV Step Centered 40 mV Above Ground

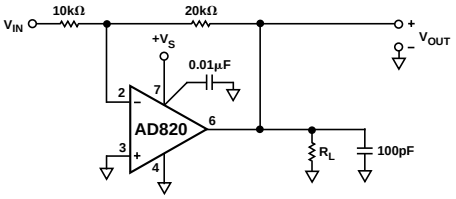


Figure 33. Gain of Two Inverter

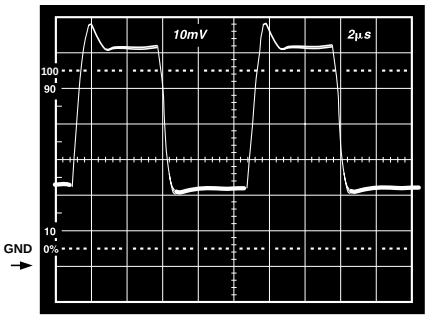


Figure 36. V_S = +5 V, 0 V; Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground

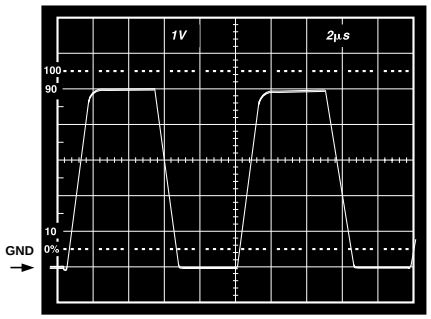


Figure 34. V_S = +5 V, 0 V; Gain of Two Inverter Response to 2.5 V Step Centered –1.25 V Below Ground

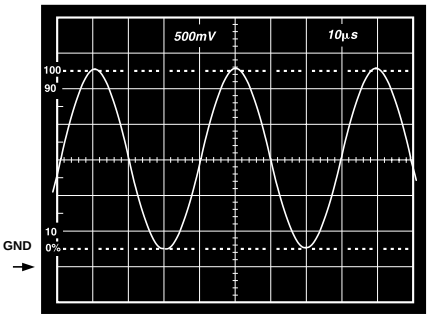


Figure 37. V_S = 3 V, 0 V; Gain of Two Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at –0.75 V, R_L = 600 Ω

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD820, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 28 and 31) and increased common-mode voltage error as illustrated in Figure 19.

The AD820 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 38a shows the response of an AD820 voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$—no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD820's plus input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 38b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 6.

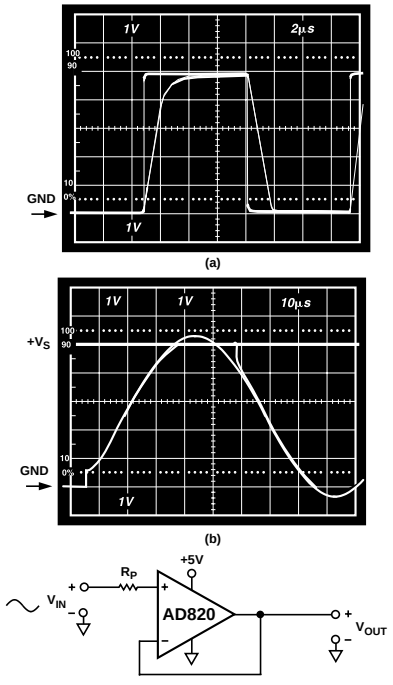


Figure 38. (a) Response with R_P = 0; V_{IN} from 0 to $+V_S$
(b) V_{IN} = 0 to $+V_S$ + 200 mV
V_{OUT} = 0 to $+V_S$
R_P = 49.9 kΩ

A current limiting resistor should be used in series with the input of the AD820 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD820 when $\pm V_S$ = 0. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD820 is designed for 13 nV/$\sqrt{\text{Hz}}$ wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 13). This noise performance, along with the AD820's low input current and current noise means that the AD820 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 39.

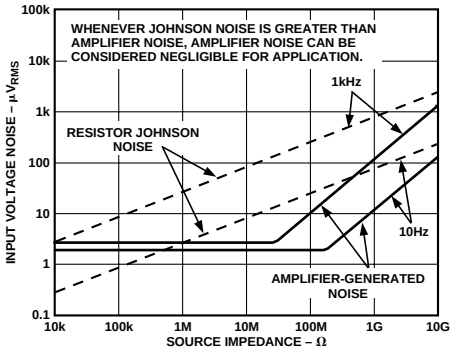


Figure 39. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD820's unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The AD820's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will he 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in Figures 9 through 12. For load resistances over 20 kΩ, the AD820's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820's output is driven hard against the output saturation voltage, it will recover within 2 µs of the input returning to the amplifier's linear operating region.

Direct capacitive load will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 40 shows the AD820's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 41 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD820. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

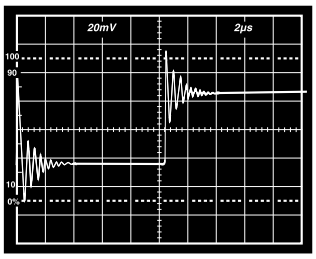


Figure 40. Small Signal Response of AD820 as Unity Gain Follower Driving 350 pF Capacitive Load

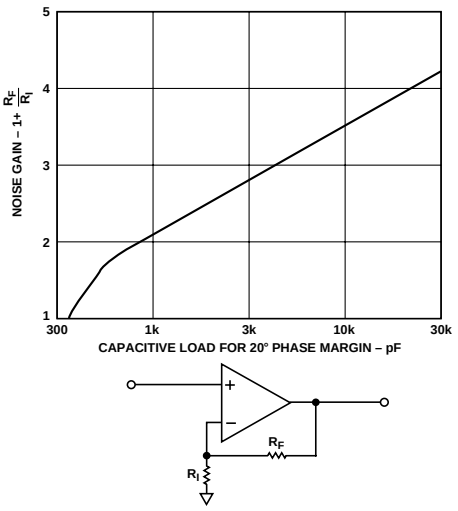


Figure 41. Capacitive Load Tolerance vs. Noise Gain

Figure 42 shows a possible configuration for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

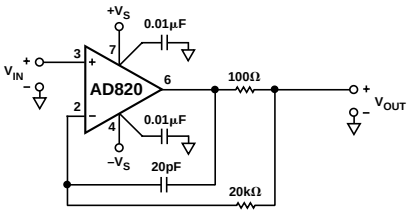


Figure 42. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

OFFSET VOLTAGE ADJUSTMENT

The AD820's offset voltage is low, so external offset voltage nulling is not usually required. Figure 43 shows the recommended technique for AD820's packaged in plastic DIPs. Adjusting offset voltage in this manner will change the offset voltage temperature drift by 4 µV/°C for every millivolt of induced offset. The null pins are not functional for AD820s in the SO-8 "R" package.

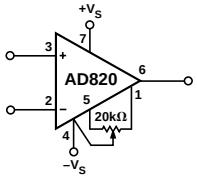


Figure 43. Offset Null

APPLICATIONS

Single Supply Half-Wave and Full-Wave Rectifiers

An AD820 configured as a unity gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820's inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over 10^{11} Ω for input voltages from 1 volt from the positive supply to 20 volts below the negative supply.

The full and half-wave rectifier shown in Figure 44 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity gain follower A1 and the loop of amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of amplifier A2 sees the ground level output of A1, therefore A2 operates as a unity gain inverter. The output at node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 volts can be rectified, depending on the voltage supply used.

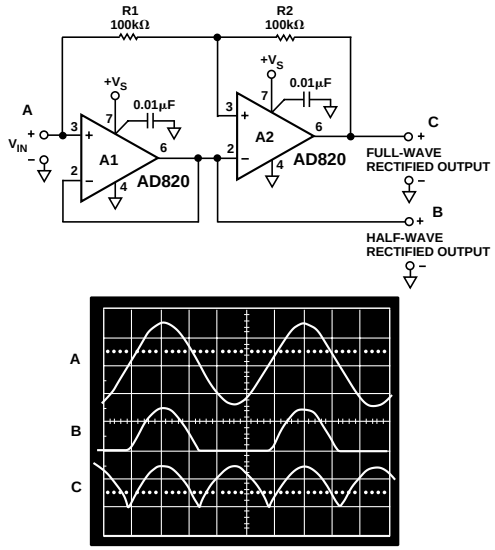


Figure 44. Single Supply Half- and Full-Wave Rectifier

4.5 Volt Low Dropout, Low Power Reference

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 45 shows a 4.5 volt reference using the AD820 and the AD680, a low power 2.5 volt bandgap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 volt output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

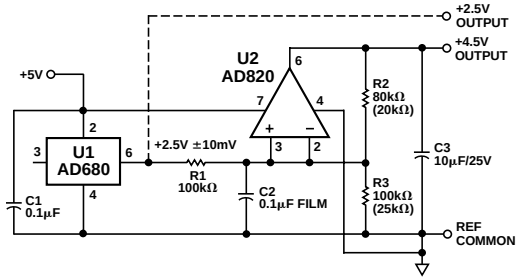


Figure 45. Single Supply 4.5 Volt Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 volt output with a supply voltage down to 4.7 volts. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 µV rms in a 25 kHz noise bandwidth.

Low Power Three-Pole Sallen Key Low-Pass Filter

The AD820's high input impedance makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 µF. The AD820's picoamp level input currents contribute minimal dc errors.

Figure 46 shows an example, a 10 Hz three-pole Sallen Key Filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of resistors R1, R2, and R3, thus minimizing the inherent output voltage noise of the filter.

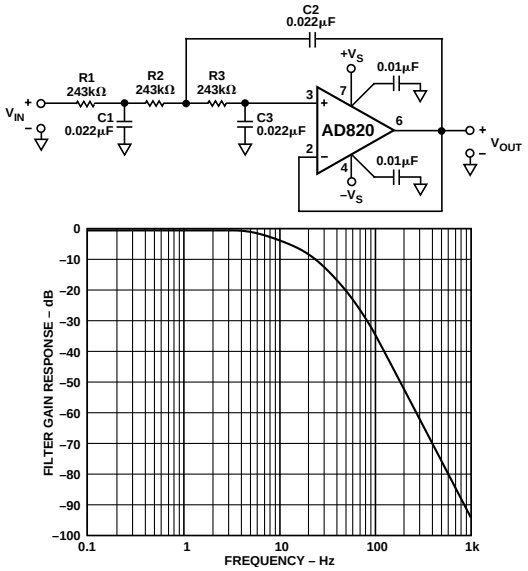
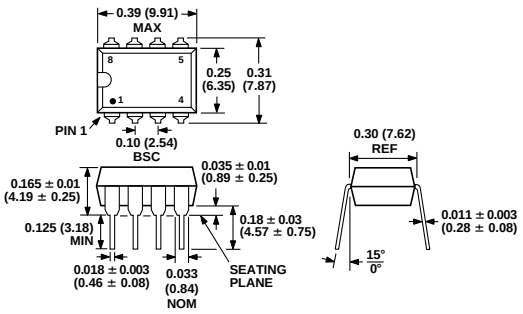


Figure 46. 10 Hz Sallen Key Low-Pass Filter

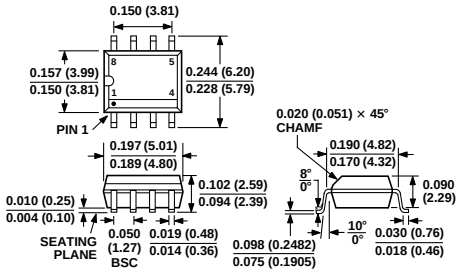
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Mini-DIP Package
(N-8)



SOIC Package
(R-8)



C1792b–0–8/99

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10.5 Data Sheet for CD40109B

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS099B – Revised January 2003

CD40109B Types

CMOS Quad Low-to-High Voltage Level Shifter

High-Voltage Types (20-Volt Rating)

■ CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a higher-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS}.

The CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD}, V_{CC}, or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between V_{SS} and at least 0.7 V_{CC}; V_{CC} may exceed V_{DD}, and input signals may exceed V_{CC} and V_{DD}. When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

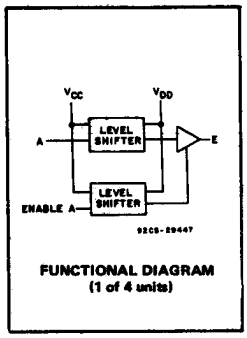
The CD40109B-Series types are supplied in 16-lead ceramic dual-in-line packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

- High-or-low level-shifting with three-state outputs for unidirectional or bidirectional bussing
- Isolation of logic subsystems using separate power supplies from supply sequencing, supply loss and supply regulation considerations

Features:

- Independence of power supply sequence considerations—V_{CC} can exceed V_{DD}, input signals can exceed both V_{CC} and V_{DD}
- Up and down level-shifting capability
- Three-state outputs with separate enable controls
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range)
  = 1 V at V_{CC} = 5 V, V_{DD} = 10 V
  = 2 V at V_{CC} = 10 V, V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM
(1 of 4 units)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... −0.5V to +20V
OUTPUT VOLTAGE RANGE, ALL OUTPUTS ..... −0.5 V to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

TRUTH TABLE

INPUTS		OUTPUTS
A, B, C, D	ENABLE A, B, C, D	E, F, G, H
0	1	0
1	1	1
X	0	Z

LOGIC 0 = LOW(V_{SS}) X = DON'T CARE Z = HIGH IMPEDANCE
LOGIC 1 = V_{CC} at INPUTS and V_{DD} at OUTPUTS

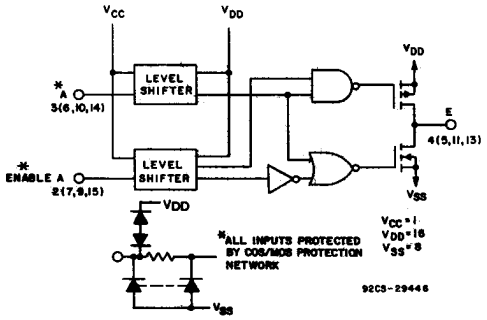


Fig.1 – CD40109B logic diagram (1 of 4 units).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.		0,18	18	±0.4	±0.4	±12	±12	–	$±10^{-4}$	±0.4	μA
	V_O (V)	V_{CC} (V)	V_{DD} (V)								
Input Low Voltage, V_{IL} Max.	1,9	5	10	1.5				—	—	1.5	V
	1.5, 13.5	10	15	3				—	—	3	
Input High Voltage, V_{IH} Min.	1,9	5	10	3.5				3.5	—	—	
	1.5,13.5	10	15	7				7	—	—	

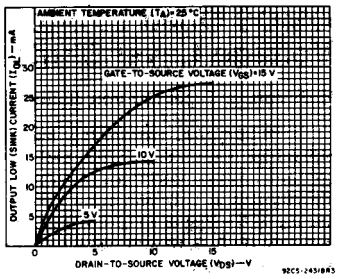


Fig.2 – Typical output low (sink) current characteristics.

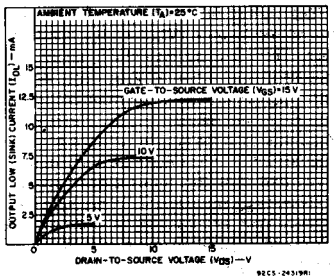


Fig.3 – Minimum output low (sink) current characteristics.

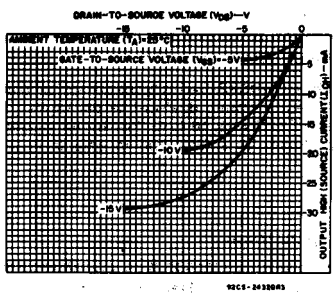


Fig.4 – Typical output high (source).

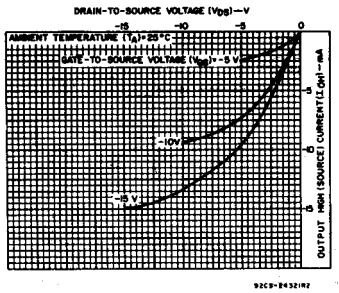


Fig.5 – Minimum output high (source) current characteristics.

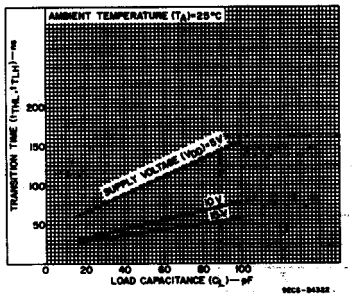


Fig.6 – Typical transition time as a function of load capacitance.

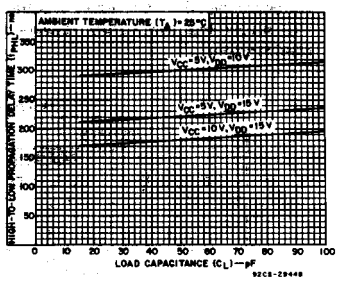


Fig.7 – Typical high-to-low propagation delay time as a function of load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ unless otherwise specified

CHARACTERISTIC	SHIFTING MODE	V_{CC} (V)	V_{DD} (V)	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay – Data Input to Output: High-to-Low Level, t_{PHL}	L–H	5	10	300	600	ns
		5	15	220	440	
		10	15	180	360	
	H–L	10	5	250	500	
		15	5	250	500	
		15	10	120	240	
Low-to-High Level, t_{PLH}	L–H	5	10	130	260	ns
		5	15	120	240	
		10	15	70	140	
	H–L	10	5	230	460	
		15	5	230	460	
		15	10	80	160	
3-State Disable Delay: R_L = 1 kΩ Output High to High Impedance, t_{PHZ}	L–H	5	10	60	120	ns
		5	15	75	150	
		10	15	35	70	
	H–L	10	5	200	400	
		15	5	200	400	
		15	10	40	80	
Output Low to High Impedance, t_{PLZ}	L–H	5	10	370	740	ns
		5	15	300	600	
		10	15	250	500	
	H–L	10	5	250	500	
		15	5	250	500	
		15	10	130	260	
High Impedance to Output High, t_{PZH}	L–H	5	10	320	640	ns
		5	15	230	460	
		10	15	180	360	
	H–L	10	5	300	600	
		15	5	300	600	
		15	10	130	260	
High Impedance to Output Low, t_{PZL}	L–H	5	10	100	200	ns
		5	15	80	160	
		10	15	40	80	
	H–L	10	5	200	400	
		15	5	200	400	
		15	10	40	80	
Transition Time, t_{THL}, t_{TLH}	L–H	5	10	50	100	ns
		5	15	40	80	
		10	15	40	80	
	H–L	10	5	100	200	
		15	5	100	200	
		15	10	50	100	
Input Capacitance, C_I		Any Input		5	7.5	pF

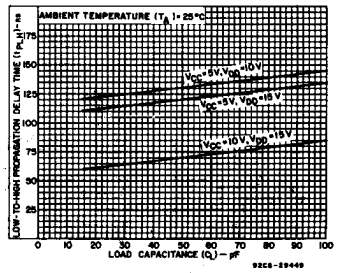


Fig.8 – Typical low-to-high propagation delay time as a function of load capacitance.

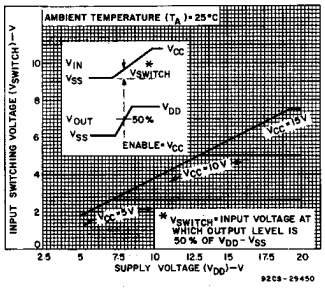


Fig.9 – Typical input switching as a function of high-level supply voltage.

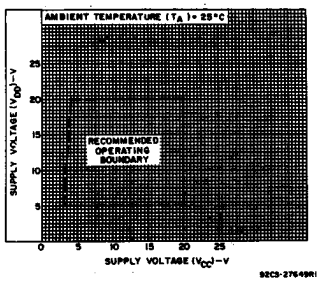


Fig.10 – High-level supply voltage vs. low-level supply voltage.

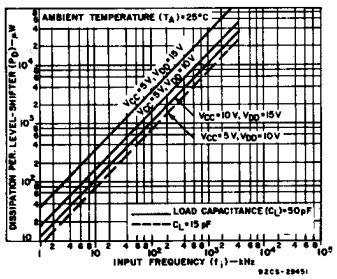


Fig.11 – Typical dynamic power dissipation as a function of input frequency.

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

TEST CIRCUITS

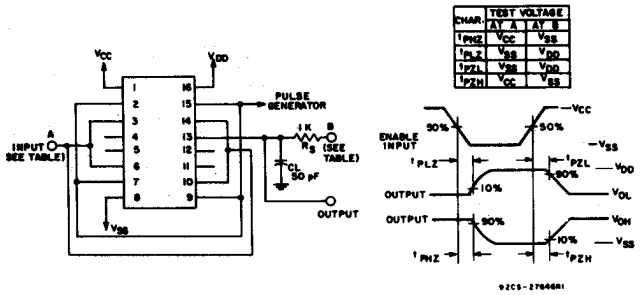


Fig. 12 – Output enable delay times test circuit and waveforms.

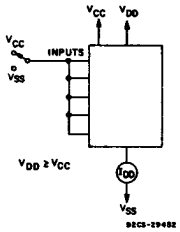


Fig. 13 – Quiescent device current.

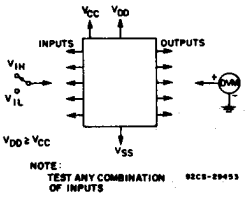


Fig. 14 – Input voltage.

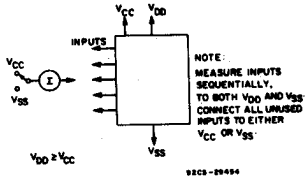


Fig. 15 – input current.

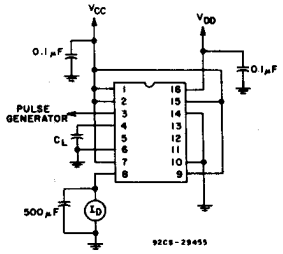
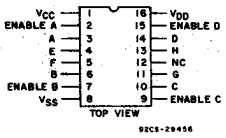
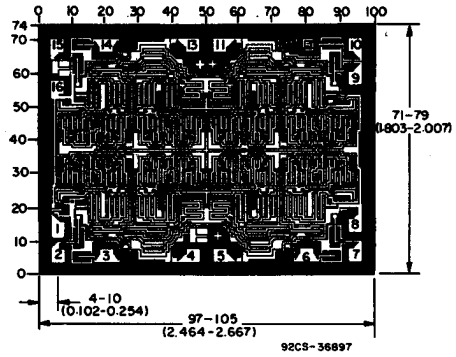


Fig. 16 – Dynamic power dissipation test circuit.



CD40109B
TERMINAL ASSIGNMENT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and pad layout for CD40109BH.

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	D
CD40109BE	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD401
CD40109BF	ACTIVE	CDIP	J	16	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD401
CD40109BF3A	ACTIVE	CDIP	J	16	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	CD401
CD40109BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD401
CD40109BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD401
CD40109BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010
CD40109BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010
CD40109BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010
CD40109BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010
CD40109BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM010

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processe reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony triox flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a co of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may w lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on i provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40109B, CD40109B-MIL :

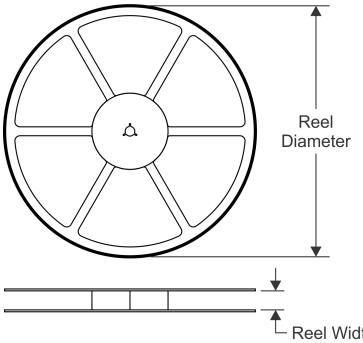
- Catalog: CD40109B
- Automotive: CD40109B-Q1, CD40109B-Q1
- Military: CD40109B-MIL

NOTE: Qualified Version Definitions:

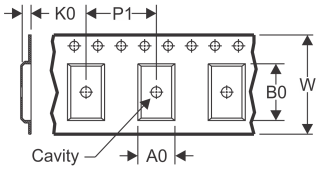
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

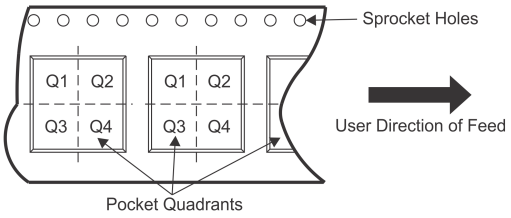


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

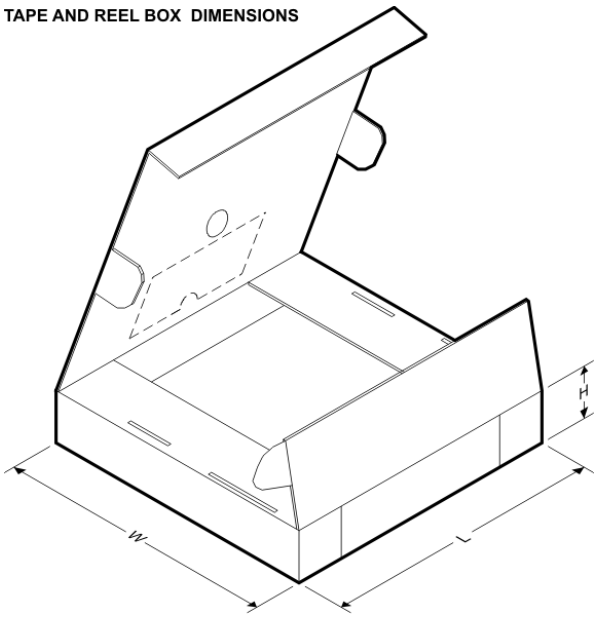
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

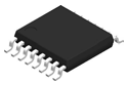
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40109BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40109BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

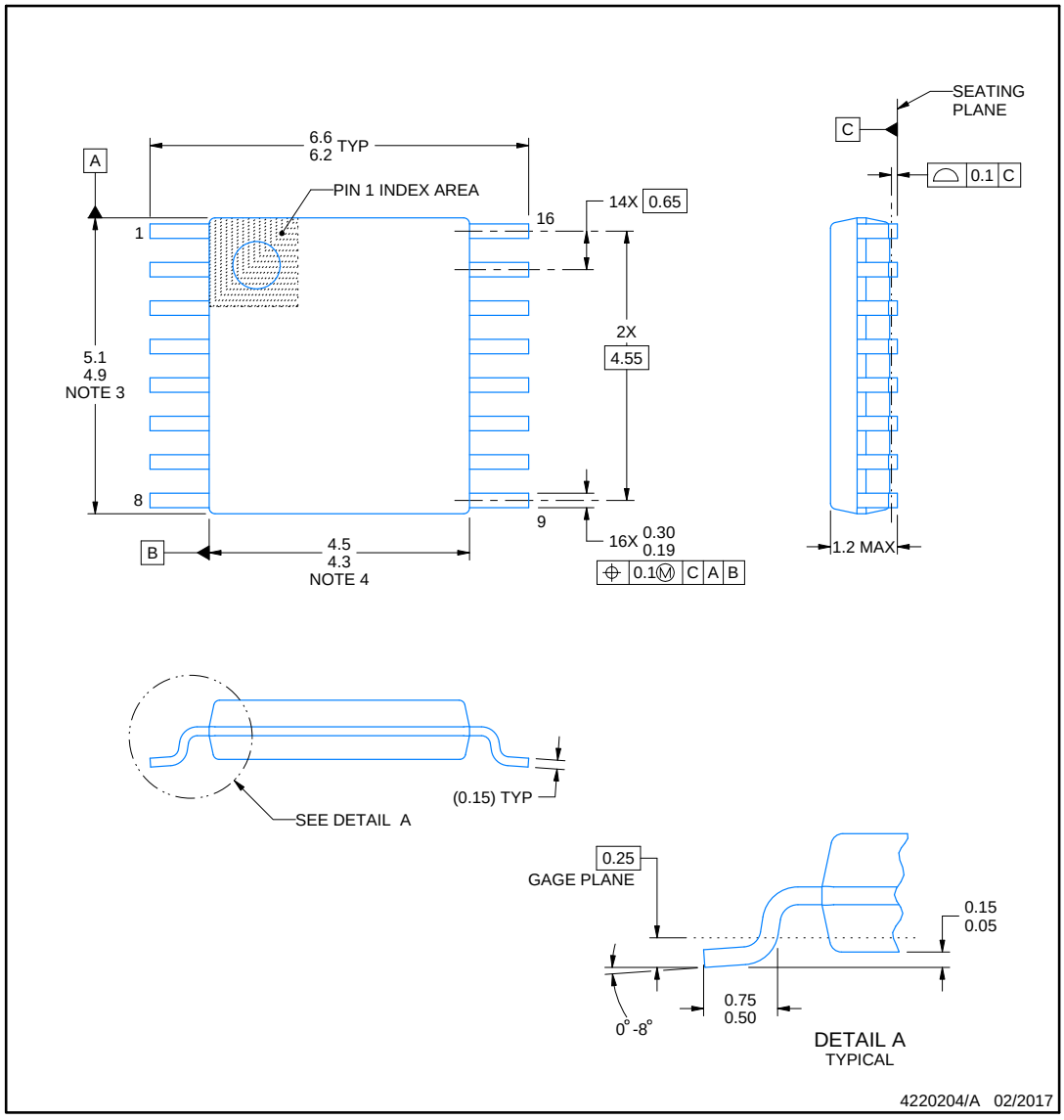


PACKAGE OUTLINE

PW0016A

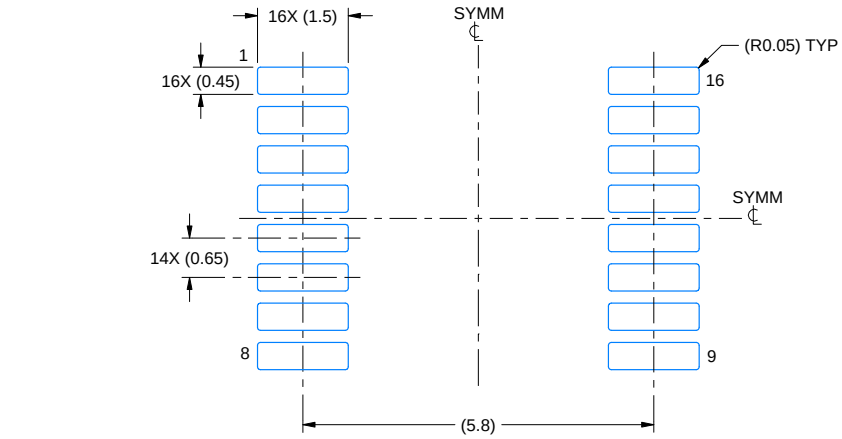
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

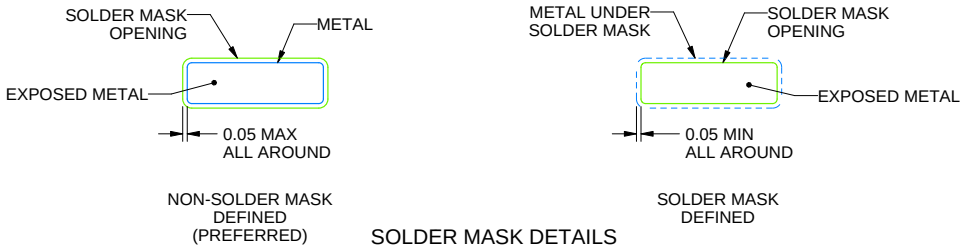


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

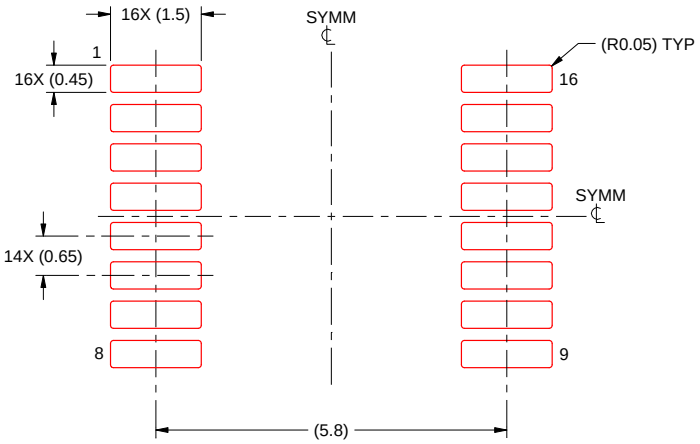


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

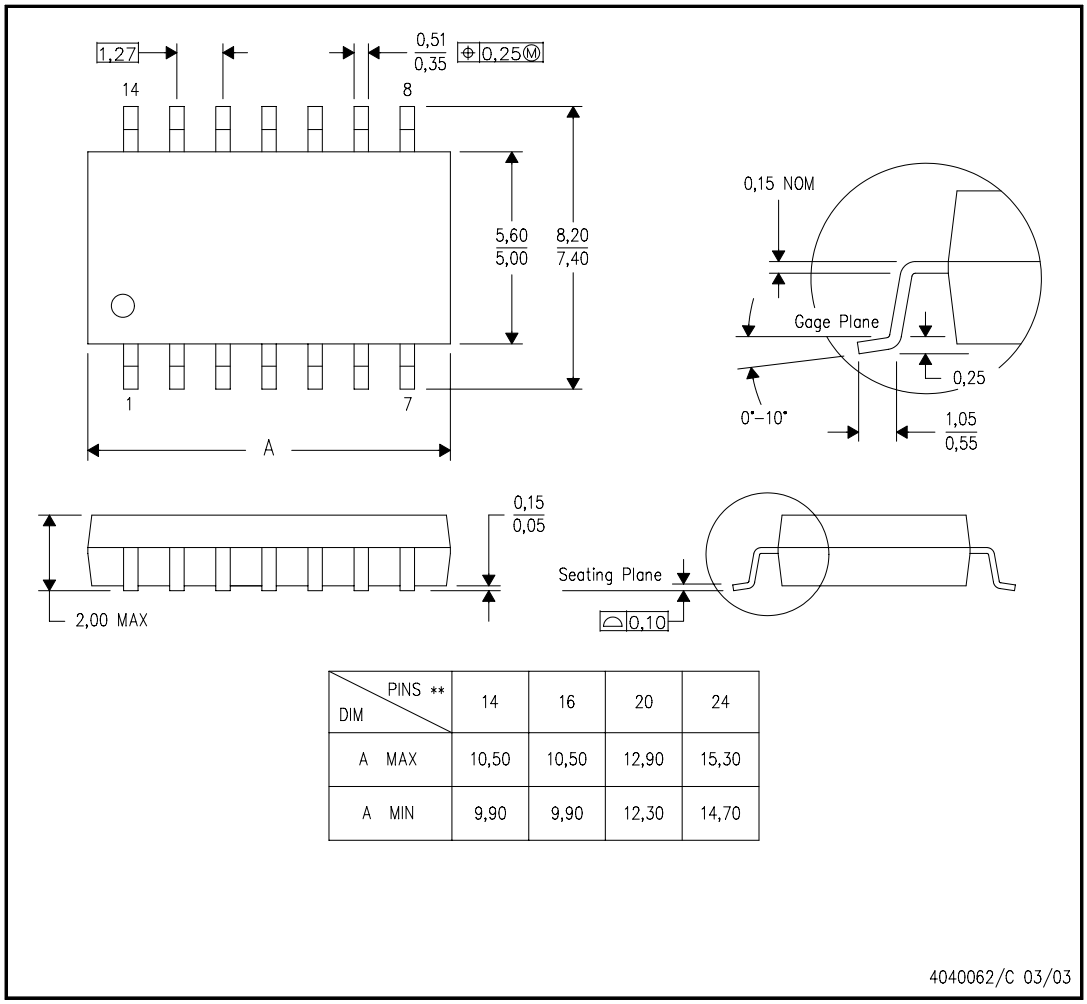
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

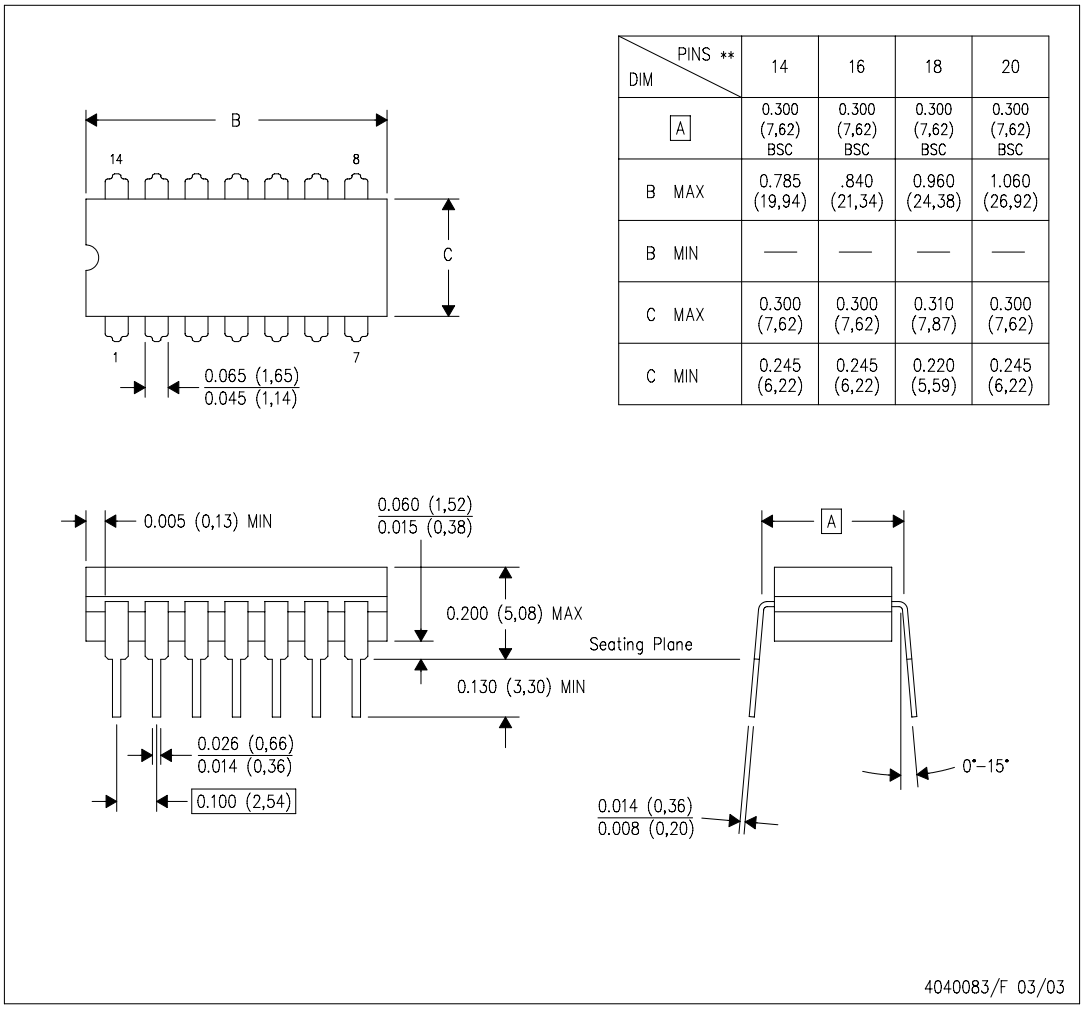


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



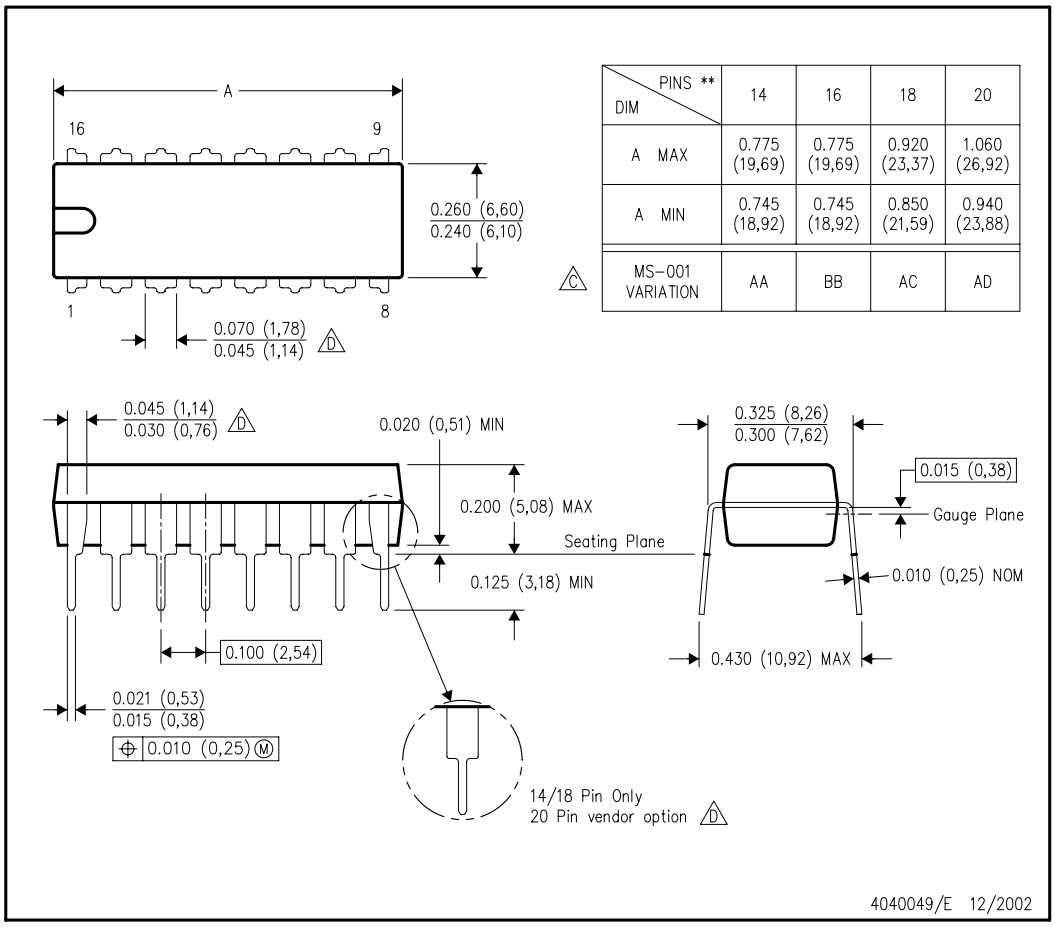
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

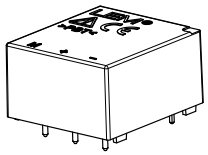
10.6 Data Sheet for LEM LV 25-P

Voltage Transducer LV 25-P

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic separation between the primary circuit and the secondary circuit.

I_{PN} = 10 mA

V_{PN} = 10 .. 500 V



Electrical data

I_{PN}	Primary nominal rms current			10	mA
I_{PM}	Primary current, measuring range			0 .. ± 14	mA
R_M	Measuring resistance			$R_{M\,min}$ $R_{M\,max}$	
	with ± 12 V	@ ± 10 mA $_{max}$		30 190	Ω
		@ ± 14 mA $_{max}$		30 100	Ω
	with ± 15 V	@ ± 10 mA $_{max}$		100 350	Ω
		@ ± 14 mA $_{max}$		100 190	Ω
I_{SN}	Secondary nominal rms current			25	mA
K_N	Conversion ratio			2500 : 1000	
U_C	Supply voltage (± 5 %)			± 12 .. 15	V
I_C	Current consumption			10 (@ ± 15 V) + I_S	mA

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN}, T_A = 25 °C	@ ± 12 .. 15 V		± 0.9	%
		@ ± 15 V (± 5 %)		± 0.8	%
ε_L	Linearity error			< 0.2	%
				Typ Max	
I_O	Offset current @ I_P = 0, T_A = 25 °C			± 0.15	mA
I_{OT}	Temperature variation of I_O	0 °C .. + 25 °C		± 0.06 ± 0.25	mA
		+ 25 °C .. + 70 °C		± 0.10 ± 0.35	mA
t_r	Step response time [1] to 90 % of I_{PN}			40	µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Resistance of primary winding	@ T_A = 70 °C	250	Ω
R_S	Resistance of secondary winding	@ T_A = 70 °C	110	Ω
m	Mass		22	g
	Standards		EN 50178: 1997	
			UL 508: 2010	

Note: [1] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit).

Features

- Closed loop (compensated) current transducer using the Hall effect
- Insulating plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Voltage Transducer LV 25-P

Insulation coordination

U_d	Rms voltage for AC insulation test, 50 Hz, 1 min	2.5 [1]	kV
$\hat{U}_W$	Impulse withstand voltage 1.2/50 µs	16	kV
		Min	
d_{Cp}	Creepage distance	19.5	mm
d_{Cl}	Clearance	19.5	mm
CTI	Comparative tracking index (group IIIa)	175	

Note: [1] Between primary and secondary.

Applications examples

According to EN 50178 and IEC 61010-1 standards and following conditions:

- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

	EN 50178	IEC 61010-1
d_{Cp}, d_{Cl}, $\hat{U}_W$	Rated insulation voltage	Nominal voltage
Basic insulation	1600 V	1600 V
Reinforced insulation	800 V	800 V

Safety

This transducer must be used in limited-energy secondary circuits according to IEC 61010-1.

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply).
Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a build-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

UL 508:Ratings and assumptions of certification

File # E189713 Volume: 2 Section: 1

Standards

- CSA C22.2 NO. 14 - 10 INDUSTRIAL CONTROL EQUIPMENT - Edition 11 - Revision Date 2011/08/01
- UL 508 STANDARD FOR INDUSTRIAL CONTROL EQUIPMENT - Edition 17 - Revision Date 2010/04/15.

Parameter	Symbol	Unit	Value
Primary involved potential		V AC/DC	600
Max surrounding air temperature	T_A	°C	85
Primary current	I_P	mA	0 to 10
Secondary supply voltage	U_C	V DC	± 12 to ±15
Secondary nominal rms current	I_{SN}	mA	25

Conditions of acceptability

When installed in the end-use equiment, consideration shall be given to the following:

1 - These devices must be mounted in a suitable end-use enclosure.

2 - The terminals have not been evaluated for field wiring.

3 - The LV 25-P series are intended to be mounted on the printed wiring board of the end-use equipment (with a minimum CTI of 100).

4 - The LV 25-P series shall be used in a pollution degree 2 environment when the Printed Wiring Board has not been coated.

5 - The LV 25-P series shall be mounted on the load side of line filters.

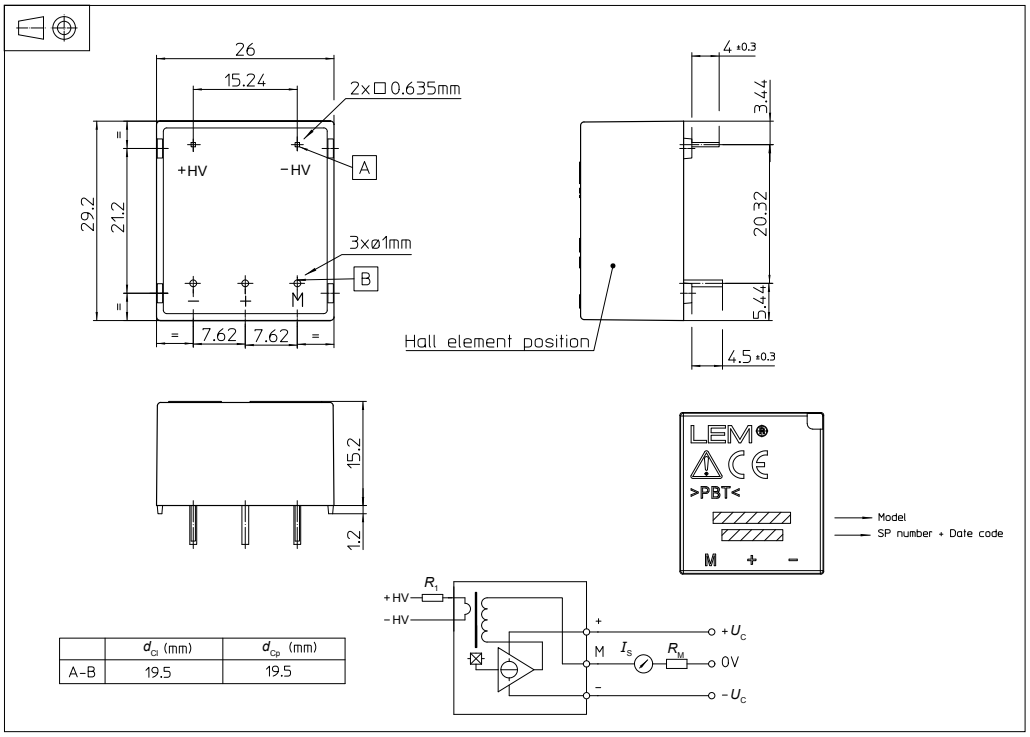
6 - Low voltage circuits are intended to be powered by a circuit derived from an isolating source (such as a transformer,optical isolator,limiting impedance or electro-mechanical relay) and having no direct connection back to the primary circuit (other than through the grounding means).

7 - Base on results of temperature tests, int he end use application, a maximum of 100 °C cannot be exceeded at soldering point between primary coil pin and soldering point of on the primary bus bar (corrected to the appropriate evaludated max. surrounding air).

Marking

Only those products bearing the UL or UR Mark should be considered to be Listed or Recognized and covered under UL's Follow-Up Service.Always look for the Mark on the product.

Dimensions LV 25-P (in mm)



	d_{Cl} (mm)	d_{Cp} (mm)
A-B	19.5	19.5

Mechanical characteristics

- General tolerance ± 0.2 mm
- Fastening & connection of primary 2 pins
  0.635 × 0.635 mm
- Fastening & connection of secondary 3 pins Ø 1 mm
- Recommended PCB hole Ø 1.2 mm

Remarks

- I_S is positive when V_P is applied on terminal + HV.
- Installation of the transducer must be done unless otherwise specified on the datasheet, according to LEM Transducer Generic Mounting Rules. Please refer to LEM document N°ANE120504 available on our Web site: **Products/Product Documentation**.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Instructions for use of the voltage transducer model LV 25-P

Primary resistor R_1: the transducer's optimum accuracy is obtained at the nominal primary current. As far as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Example: Voltage to be measured V_{PN} = 250 V a) R_1 = 25 kΩ / 2.5 W, I_P = 10 mA Accuracy = ± 0.9 % of V_{PN} (@ T_A= + 25 °C)
b) R_1 = 50 kΩ / 1.25 W, I_P = 5 mA Accuracy = ± 1.5 % of V_{PN} (@ T_A= + 25 °C)

Operating range (recommended): taking into account the resistance of the primary windings (which must remain low compared to R_1, in order to keep thermal deviation as low as possible) and the insulation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

10.7 Data Sheet for Hint Sink

wakefield-vette

Standard Catalog P/N[5] Milled Base[1]	Nonmilled Base[2]	Base Width in. (mm)	Length in. (mm)	Height Milled Base[1] ("M Series") in. (mm)	Height Nonmilled Base[2] ("U" Series) in. (mm)	Thermal Resistance[5] (Øsa) at Typical Load Natural Convection[3] (°C/W)	Thermal Resistance[5] (Øsa) at Typical Load Forced Convection[4] (°C/W @ 100 CFM)
510-3M	510-3U	7.380 (187.452)	3.000 (76.2)	3.106 (78.9)	3.136 (79.7)	0.56	0.088
510-6M	510-6U	7.380 (187.452)	6.000 (152.4)	3.106 (78.9)	3.136 (79.7)	0.38	0.070
510-9M	510-9U	7.380 (187.452)	9.000 (228.6)	3.106 (78.9)	3.136 (79.7)	0.29	0.066
510-12M	510-12U	7.380 (187.452)	12.000 (304.8)	3.106 (78.9)	3.136 (79.7)	0.24	0.062
510-14M	510-14U	7.380 (187.452)	14.000 (355.6)	3.106 (78.9)	3.136 (79.7)	0.21	0.059
511-3M	511-3U	5.210 (132.33)	3.000 (76.2)	2.350 (59.7)	2.410 (61.2)	0.90	0.120
511-6M	511-6U	5.210 (132.33)	6.000 (152.4)	2.350 (59.7)	2.410 (61.2)	0.65	0.068
511-9M	511-9U	5.210 (132.33)	9.000 (228.6)	2.350 (59.7)	2.410 (61.2)	0.56	0.060
511-12M	511-12U	5.210 (132.33)	12.000 (304.8)	2.350 (59.7)	2.410 (61.2)	0.45	0.045
512-3M	512-3U	7.200 (182.88)	3.000 (76.2)	2.350 (59.7)	2.410 (61.2)	0.90	0.120
512-6M	512-6U	7.200 (182.88)	6.000 (152.4)	2.350 (59.7)	2.410 (61.2)	0.65	0.068
512-9M	512-9U	7.200 (182.88)	9.000 (228.6)	2.350 (59.7)	2.410 (61.2)	0.56	0.060
512-12M	512-12U	7.200 (182.88)	12.000 (304.8)	2.350 (59.7)	2.410 (61.2)	0.45	0.045

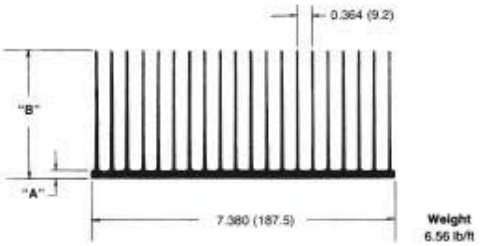
MECHANICAL DIMENSIONS

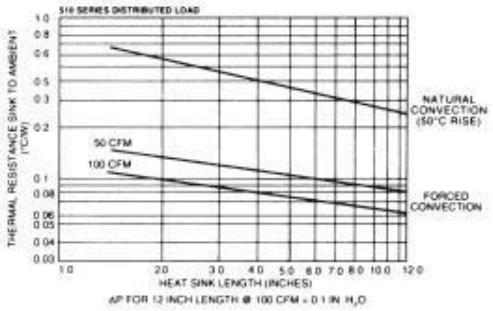
NATURAL AND FORCED CONVECTION CHARACTERISTICS

510 SERIES

510 Series (Extrusion Profile 5113)

Series	A (MIN)	B	Flatness
510-U	0.216 (5.5)	3.136 (79.7)	0.006 in./in. (0.15 mm/mm)
510-M	0.165 (4.2)	3.106 (78.9)	0.002 in./in. (0.05 mm/mm)

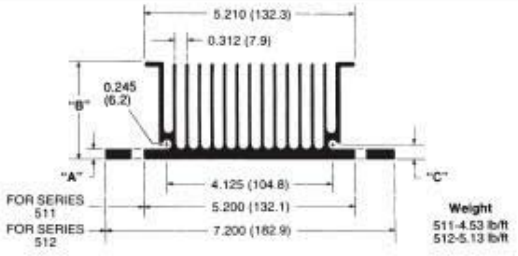


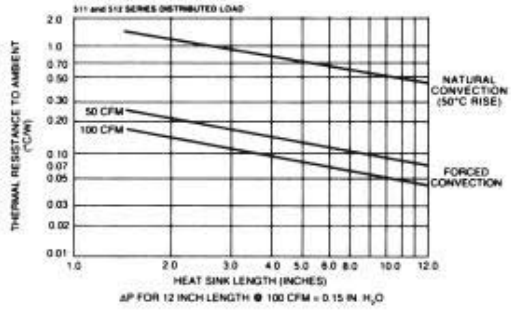


511 AND 512 SERIES

511 Series (Extrusion Profile 6438-1)
512 Series (Extrusion Profile 6438-2)

Series	A	B	C	Flatness
511-U 512-U	0.250 (6.4)	2.410 (61.2)	0.372 (9.4)	0.006 in./in. (0.15 mm/mm)
511-M 512-M	0.220 (5.6)	2.350 (59.7	0.342 (8.7)	0.002 in./in. (0.05 mm/mm)





10.8 Mounting Instructions for IGBT Modules

SEMIKRON
innovation + service

SEMITOP® Mounting instructions

ESD protection

IGBT and MOS circuits in SEMITOP® modules are sensitive to electrostatic charges. All SEMITOP® modules are ESD protected during transport, storage and mounting process with an ESD cover.
During the handling and assembly of the modules use a conductive grounded wristlet and working place.

Heat sink specification

The mounting area on the heatsink must be clean and free of grease and particles.
The mechanical specifications for the heat sink are (See Figure 1):

- Flatness: 50 µm per 100 mm
- Roughness Rz : 6,3 µm
- Machined without overlaps

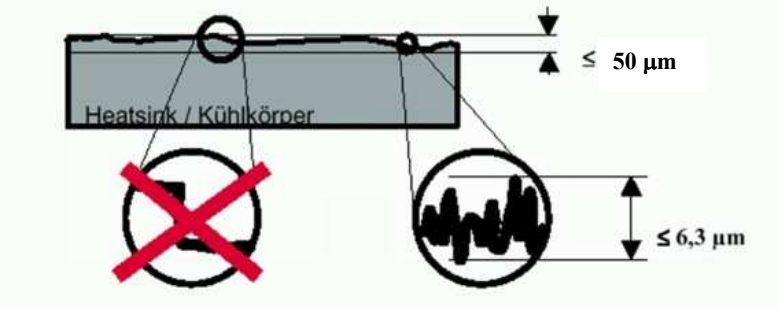


Figure 1 – Heatsink specifications

Mounting surface

- The mounting surface of SEMITOP module must be free from grease and particles.
- Fingerprints or on the bottom side do not affect the thermal behaviour.
- Due to the manufacturing process, the bottom side of the SEMITOP may exhibit scratches, holes or similar marks.
- Discoloration on the bottom side do not affect the thermal behaviour
- The following figures (Figure 2 and Figure 3) define surface characteristics, which do not affect the thermal behaviour.

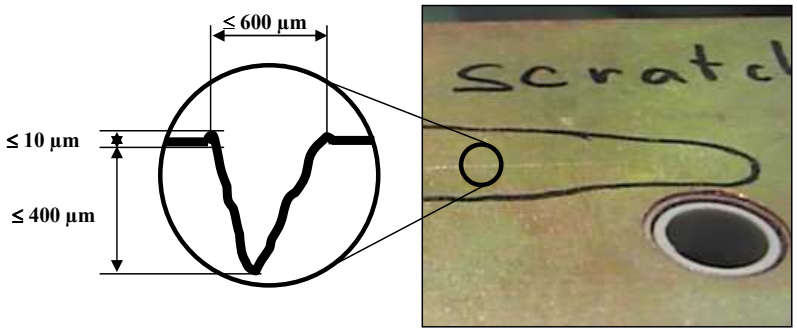


Figure 2 - Scratches on the SEMITOP bottom surface

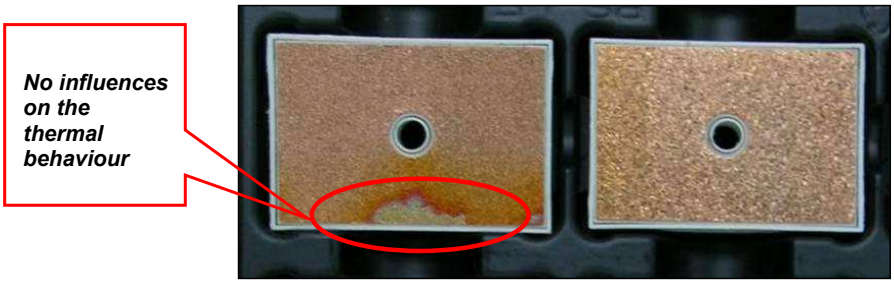


Figure 3 – Discoloration on SEMITOP bottom surface

Assembling Steps

SEMITOP® modules could be assembled by either starting soldering the modules to the PCB (Figure 4) and then fix the subsystem PCB+SEMITOP® to heat sink, or fixing SEMITOP® to the heat sink (Figure 5) and then solder to the PCB.

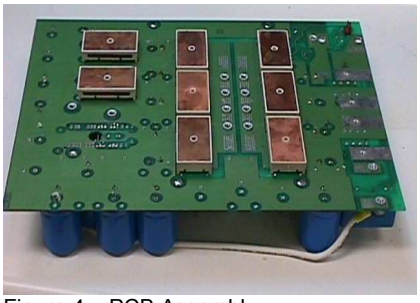


Figure 4 – PCB Assembly

Figure 5 – Heatsink assembly

To avoid any damage to the SEMITOP® modules, it is important to respect important operative conditions during the main assembling steps such as the application of thermal grease, the soldering process and the assembly to the heat sink.

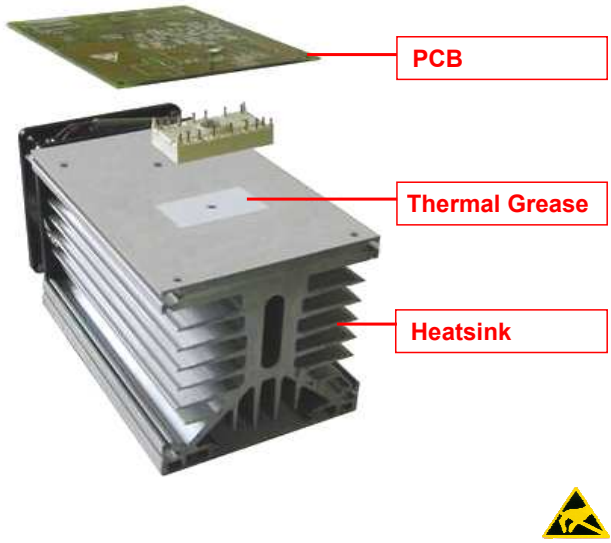


Figure 6 – Assembling steps

Thermal grease application

To avoid air gaps at the interface between the module and the heat sink a thermal grease must be applied.
The function of the grease is to flow according to the shape of the interface, allowing a metal-to-metal contact where it is possible, and filling the remaining gaps.
Recommended thermal grease material is Wacker-Chemie P 12.

SEMIKRON recommends a hard rubber roller or a screen print for an even distribution of the grease.

The thickness of the applied grease layer should be:

Module	Thermal Grease Thickness
SEMITOP® 1	20 – 25 µm (Wacker P12)
SEMITOP® 2	30 – 35 µm (Wacker P12)
SEMITOP® 3	50 – 55 µm (Wacker P12)
SEMITOP® 4	40 – 45 µm (Wacker P12)

The thickness of the applied grease can be checked by a measuring gauge (e.g. Fa. ELCOMETER Instruments GmbH, Himmlingstr. 18, 73434 Aalen, Tel. +49-7366-919283: Sechseck-Kamm 5 - 150 µm).

Assembly on heat sink
After applying the recommended thickness of thermal grease on the heat sink, tighten the screw with the corresponding mounting torque:

Module	Screw	Washer	Maximum Mounting Torque
SEMITOP® 1	ISO 4762-M4x16	former DIN 6798-A + ISO 7089	1,5 Nm +0/-10%
SEMITOP® 2	ISO 4762-M4x16	former DIN 6798-A + ISO 7089	2,0 Nm +0/-10%
SEMITOP® 3	ISO 4762-M4x16	former DIN 6798-A + ISO 7089	2,5 Nm +0/-10%
SEMITOP® 4	ISO 4762-M4x16	former DIN 6798-A + DIN 7349	2,6 Nm +/- 5%

SEMIKRON recommends:

- a torque wrench with automatic control;
- the above recommended screws and washers;
- tighten the screws only once. After the mounting do not re-tighten the screws to the nominal mounting torque value.
  Due to relaxation of the housing and flow of thermal paste, the loosening torque is lower than the mounting torque. However, the construction of the housing, the washers and the adhesion of the thermal paste still ensure sufficient thermal coupling of the module to the heat sink.
- Do not exceed the mounting torque because a further increase of the maximum mounting torque will not improve the thermal contact but could only damage the module.

Connecting SEMITOP® – PCB

Use plastic anchor pins in each corner on the top of the SEMITOP® for mechanical connection between PCB and SEMITOP®.
To avoid mechanical stress to the soldering pins, the PCB has to be additionally supported (e.g. using spacers).
Suggested hole diameter for the soldering pins and the mounting pins in the PCB is 2mm.

Soldering on PCB

SEMITOP® modules could be soldered to the PCB using the most common soldering process:

- Hand iron;
- Wave soldering process.

Independent of the soldering process used to solder SEMITOP® modules to the PCB, SEMIKRON recommends a thorough evaluation of the solder joints to ensure an optimal connection between SEMITOP® and the PCB.
Figure 7 shows a profile of a good soldered joint. Notice that the solder forms a concave meniscus between pin and pad. This is an example of a properly formed meniscus and it is a result of good wetting during the soldering process.

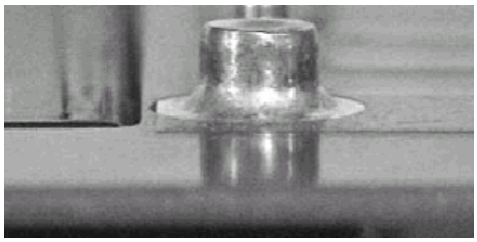


Figure 7 - Good soldered joint profile

In both Figure 7 and Figure 8 it can also be seen that the soldering covers a good deal of the surface area of the pin and of the pad. This is also evidence of good wetting. Notice that the soldering joint has a smooth surface with a silver colour. This is the result of good immobilization of the joint during cooling as well as good cleaning of the board prior to soldering. All soldering connections should exhibit similar characteristics regardless whether they are soldered by hand iron or wave soldering process.

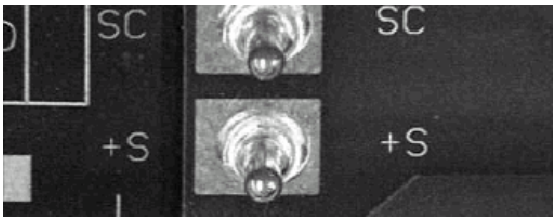


Figure 8 - Details

The time required to create a robust connection depend on several parameters:

a) PCB thickness: When increasing the PCB thickness, the heat dissipation capability of the PCB itself will be the higher, and thus it will require a longer soldering time.

b) Copper wire area: Pins require large copper wire to minimize resistive power losses during the current flowing.
Since copper has a good heat transmission coefficient, the size of these copper wires directly affects the soldering time necessary to heat the PCB pad.

c) Hand iron power: power, tip size and working temperature of the hand iron affect the soldering time. These parameters have to be adjusted in order to keep the maximum temperature within the specified limit.

SEMIKRON recommends that the soldering joints should be thoroughly checked to ensure a high quality soldering joint. If necessary, different parameters should be adjusted in order to optimise the process.

Hand Soldering
SEMIKRON recommends to not exceed the maximum temperature of 260°C for a soldering time of 10seconds.

Wave Soldering Profile
SEMIKRON recommends:

- do not exceed the maximum wave soldering profile of figure 9;
- the maximum preheating temperature has to be kept under or equal to the maximum storage temperature (125°C);
- do not exceed the maximum preheating time of 100seconds;
- during the soldering phase, do not exceed the maximum soldering time of 10 seconds at the maximum temperature of 260°.

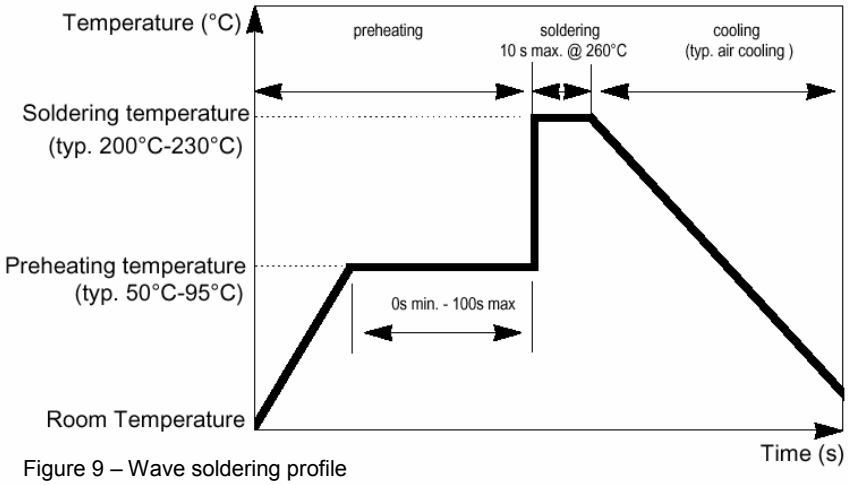


Figure 9 – Wave soldering profile

10.9 MATLAB Program for Serial Communication

MATLAB Code for Serial Communication:

```
%%Clear all variables
clc
clear all;
SerialPort='com1'; %serial port
MaxDeviation = 3;%Maximum Allowable Change from one value to next
TimeInterval=0.00000000434;%time interval between each input.
loop=620;%count values
%%Set up the serial port object

s = serial(SerialPort);
get(s,{'InputBufferSize','BytesAvailable'});
s.BaudRate=115200;
fopen(s);
%


time1 =now;
time2=now;
voltage = 0;
voltage2=0;
data_for_plot=0;
counter=1;
row_count=1;
%% Initializing variables

A=0;
B=0;
C=0;
D=0;
time1(1)=0;
time2(1)=0;
count =1;
k=1;
n=1;
array=0;
jj=0;
[rows,cols]=size(array);

fid = fopen('capture.txt','w');
while ~isequal(count,loop)
    %%Serial data accessing
      [A1,varcount,msg]=fread(s);
      fwrite(fid,A1);
      count = count +1;
end
fclose(fid);
fclose(s);
delete(s);
clear s;
```

```
fid = fopen('capture.txt');
A = fread(fid);
fclose(fid);
[rows2,cols2]=size(A);
for i=1:1:rows2
     row_count=counter;
      if A(row_count,1)==83
             for jj=3:1:4
                if jj+row_count>=rows2 && A(end,1)~=69
                    break
                else
                    B(jj)=A(jj+row_count);
                    data_dc_voltage(jj-2,1)=B(jj);        % This channel is
dedicated to DC link voltage
                end
             end

             for kk=7:1:8
                if kk+row_count>=rows2 && A(end,1)~=69
                    break
                else
                    C(kk)=A(kk+row_count);
                    data_ac_voltage_A(kk-6,1)=C(kk);          % This channel
is dedicated to AC voltage on Phase A
                end
             end

             for ll=11:1:12
                if ll+row_count>=rows2 && A(end,1)~=69
                    break
                else
                    D(ll)=A(ll+row_count);
                    data_ac_current_A(ll-10,1)=D(ll);        % This channel
is dedicated to Phase A filter current
                end
             end

             for mm=15:1:16
                if mm+row_count>=rows2 && A(end,1)~=69
                    break
                else
                    E(mm)=A(mm+row_count);
                    data_ac_voltage_B(mm-14,1)=E(mm);       % This channel is
dedicated to AC voltage on Phase B
                end
             end


             for nn=19:1:20
                if nn+row_count>=rows2 && A(end,1)~=69
                    break
                else
                    F(nn)=A(nn+row_count);
                    data_ac_current_B(nn-18,1)=F(nn);       % This channel is
dedicated to AC voltage on Phase B
```

```
   end
end

        bin1=dec2bin(data_dc_voltage(2,1),8);
        bin1_ac_A=dec2bin(data_ac_voltage_A(2,1),8);
        bin1_cc_A=dec2bin(data_ac_current_A(2,1),8);
        bin1_ac_B=dec2bin(data_ac_voltage_B(2,1),8);
        bin1_cc_B=dec2bin(data_ac_current_B(2,1),8);

        bin2=dec2bin(data_dc_voltage(1,1),8);
        bin2_ac_A=dec2bin(data_ac_voltage_A(1,1),8);
        bin2_cc_A=dec2bin(data_ac_current_A(1,1),8);
        bin2_ac_B=dec2bin(data_ac_voltage_B(1,1),8);
        bin2_cc_B=dec2bin(data_ac_current_B(1,1),8);

        bin3=dec2bin(0,8);
        DC_voltage=[bin1 bin2 bin3 bin3];
        AC_voltage_A=[bin1_ac_A bin2_ac_A bin3 bin3];
        AC_current_A=[bin1_cc_A bin2_cc_A bin3 bin3];
        AC_voltage_B=[bin1_ac_B bin2_ac_B bin3 bin3];
        AC_current_B=[bin1_cc_A bin2_cc_A bin3 bin3];

        V_DC = DC_voltage-'0'; % convert to numeric
        V_ac_A = AC_voltage_A-'0'; % convert to numeric
        C_ac_A = AC_current_A-'0'; % convert to numeric
        V_ac_B = AC_voltage_B-'0'; % convert to numeric
        C_ac_B = AC_current_B-'0'; % convert to numeric

        frc = 1+sum(V_DC(10:32).*2.^(-1:-1:-23));
        frc_2 = 1+sum(V_ac_A(10:32).*2.^(-1:-1:-23));
        frc_3 = 1+sum(C_ac_A(10:32).*2.^(-1:-1:-23));
        frc_4 = 1+sum(V_ac_B(10:32).*2.^(-1:-1:-23));
        frc_5 = 1+sum(C_ac_B(10:32).*2.^(-1:-1:-23));

        pow = sum(V_DC(2:9).*2.^(7:-1:0))-127;
        pow_2 = sum(V_ac_A(2:9).*2.^(7:-1:0))-127;
        pow_3 = sum(C_ac_A(2:9).*2.^(7:-1:0))-127;
        pow_4 = sum(V_ac_B(2:9).*2.^(7:-1:0))-127;
        pow_5 = sum(C_ac_B(2:9).*2.^(7:-1:0))-127;

        sgn = (-1)^V_DC(1);
        sgn_2 = (-1)^V_ac_A(1);
        sgn_3 = (-1)^C_ac_A(1);
        sgn_4 = (-1)^V_ac_B(1);
        sgn_5 = (-1)^C_ac_B(1);

        val = sgn * frc * 2^pow;
        val_2 = sgn_2 * frc_2 * 2^pow_2;
        val_3 = sgn_3 * frc_3 * 2^pow_3;
        val_4 = sgn_4 * frc_4 * 2^pow_4;
        val_5 = sgn_5 * frc_5 * 2^pow_5;

        data_for_plot_DC(1,row_count)=(val);
        data_for_plot_sine_VA(1,row_count)=(val_2);
        data_for_plot_sine_CA(1,row_count)=(val_3);
```

```
                    data_for_plot_sine_VB(1,row_count)=(val_4);
                    data_for_plot_sine_CB(1,row_count)=(val_5);

                    data_DC(row_count,1)=data_for_plot_DC(1,row_count);

data_ac_VA(row_count,1)=data_for_plot_sine_VA(1,row_count);

data_ac_CA(row_count,1)=data_for_plot_sine_CA(1,row_count);

data_ac_VB(row_count,1)=data_for_plot_sine_VB(1,row_count);

data_ac_CB(row_count,1)=data_for_plot_sine_CB(1,row_count);

                    if data_for_plot_DC(1,row_count)>450 ||
data_for_plot_DC(1,row_count)<0  % Change this to 450 when connected to DC
sensor
                        data_for_plot_DC(1,row_count)=0;
                    end

                    if data_for_plot_sine_VA(1,row_count)>200 ||
data_for_plot_sine_VA(1,row_count)<-200
                        data_for_plot_sine_VA(1,row_count)=0;
                    end

                    if data_for_plot_sine_CA(1,row_count)>20 ||
data_for_plot_sine_CA(1,row_count)<-20
                        data_for_plot_sine_CA(1,row_count)=0;
                    end

                    if data_for_plot_sine_VB(1,row_count)>200 ||
data_for_plot_sine_VB(1,row_count)<-200
                        data_for_plot_sine_VB(1,row_count)=0;
                    end

                    if data_for_plot_sine_CB(1,row_count)>20 ||
data_for_plot_sine_CB(1,row_count)<-20
                        data_for_plot_sine_CB(1,row_count)=0;
                    end

        else
              data_for_plot_DC(1,row_count)=0;
               data_for_plot_sine_VA(1,row_count)=0;
               data_for_plot_sine_CA(1,row_count)=0;
               data_for_plot_sine_VB(1,row_count)=0;
               data_for_plot_sine_CB(1,row_count)=0;
        end


        time1(counter) = counter/115200/4.5;
        time2(counter) = counter/115200/4.5;
    pause(TimeInterval);
    counter=counter+1;
    row_count=row_count+1;

end
```

```
%% Plotting

figure
subplot(5,1,1)
isNZ=(~data_for_plot_DC==0);           % addressing logical array of nonzero
elements
plot(time1(isNZ).*51.5873,data_DC(isNZ),'Marker','.','Linewidth',1);
xlabel('Time(s)');
ylabel('Voltage (V)');
title('DC Voltage Sensor Data');
grid on

subplot(5,1,2)
isNZ=(~data_for_plot_sine_VA==0);           % addressing logical array of
nonzero elements
plot(time1(isNZ).*51.5873,data_for_plot_sine_VA(isNZ),'Marker','.','Linewidth
',1);
xlabel('Time(s)');
ylabel('Voltage (V)');
title('AC Voltage Sensor Data');
grid on

subplot(5,1,3)
isNZ=(~data_for_plot_sine_CA==0);           % addressing logical array of
nonzero elements
plot(time1(isNZ).*51.5873,data_for_plot_sine_CA(isNZ),'Marker','.','Linewidth
',1);
xlabel('Time(s)');
ylabel('Current (A)');
title('Current Sensor Data');
grid on

subplot(5,1,4)
isNZ=(~data_for_plot_sine_VB==0);           % addressing logical array of
nonzero elements
plot(time1(isNZ).*51.5873,data_for_plot_sine_VB(isNZ),'Marker','.','Linewidth
',1);
xlabel('Time(s)');
ylabel('Voltage (V)');
title('AC Voltage Sensor Data');
grid on

subplot(5,1,5)
isNZ=(~data_for_plot_sine_CB==0);           % addressing logical array of
nonzero elements
plot(time1(isNZ).*51.5873,data_for_plot_sine_CB(isNZ),'Marker','.','Linewidth
',1);
xlabel('Time(s)');
ylabel('Current (A)');
title('Current Sensor Data');
grid on
```

```
windowSize = 5;
b = (1/windowSize)*ones(1,windowSize);
a = 1;
y = (filter(b,a,data_for_plot_DC(isNZ)));
y2 = (filter(b,a,data_for_plot_sine_VA(isNZ)));

figure
plot(time1(isNZ),data_for_plot_DC(isNZ))
% hold on
% plot(time1(isNZ),y)
% legend('Input Data','Filtered Data')
xlabel('Time(s)');
ylabel('Voltage');
title('DC Link Voltage Sensor Data');
grid on

figure
isNZ=(~data_for_plot_sine_VA==0);
plot(time1(isNZ),data_for_plot_sine_VA(isNZ))
% hold on
% plot(time1(isNZ),y2)
%legend('Input Data','Filtered Data')
xlabel('Time(s)');
ylabel('Voltage');
title('AC Voltage Sensor Data');
grid on


figure
isNZ=(~data_for_plot_sine_CA==0);
plot(time1(isNZ),data_for_plot_sine_CA(isNZ))
% hold on
% plot(time1(isNZ),y2)
%legend('Input Data','Filtered Data')
xlabel('Time(s)');
ylabel('Current(A)');
title('Current Sensor Data');
grid on

figure
isNZ=(~data_for_plot_sine_VB==0);
plot(time1(isNZ),data_for_plot_sine_VB(isNZ))
% hold on
% plot(time1(isNZ),y2)
%legend('Input Data','Filtered Data')
xlabel('Time(s)');
ylabel('Voltage (V)');
title('Voltage Sensor Data');
grid on

figure
isNZ=(~data_for_plot_sine_CB==0);
plot(time1(isNZ),data_for_plot_sine_CB(isNZ))
% hold on
% plot(time1(isNZ),y2)
%legend('Input Data','Filtered Data')
```

```
xlabel('Time(s)');
ylabel('Current(A)');
title('Current Sensor Data');
grid on

% subplot(2,1,2)
% plot(time2.*87126.98,voltage2,'Marker','.','Linewidth',1);
% xlabel('Time(s)');
% ylabel('vd');
% title('MVC-Data');
% grid on
```

10.10 Connecting TMS320F28335 Microcontroller with Simulink

The versions of MATLAB/Simulink that are 2014 and above, are already compatible with this microcontroller and there is no need for a separate target block to be placed in the Simulink file as it used to happen in the previous versions. The desired algorithm is built in Simulink using the available blocks. The C-code file that is built after building this program is then used in the code composer to link the computer with the microcontroller and the .HEX file is downloaded on the DSP. The startup procedure of loading the Simulink file to TMS320F28335 microcontroller is summarized below:

1. Open MATLAB and write the following command in the command line: xmakefilesetup
2. Uncheck the "Display operational configurations only".
3. Now choose ticcs c2000 ccs5.
4. Make sure that the compiler and linker paths are correctly chosen.
5. Press "New".
6. Make a clone of ticcs c2000 ccs5, it should say: ticcs c2000 ccs5 clone and check "Display operational configurations only".
7. In the command window write: Simulink
8. Open a blank model.
9. Go the "Build Configurations".
10. Go to "Code Generation".
11. In the System target file choose "idelink ert.tlc".

12. In the Coder Targets go to “Target Hardware Resources”.

13. Select the code composer version and target hardware.

14. Press apply. The target configuration is complete.

15. Build your program in Simulink and press “Build” option.

16. If there are no errors, a command window will open.

17. Once built, load the .out file in the code composer and press “Run”.

18. Check the output of the program.

Curriculum Vitae

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Conference Publication:

1. **S.A. Raza** and J. Jiang, *"Cooperative Control and Power Management for Islanded Residential Microgrids with Local Phase-wise Generation and Storage Units"*, in 7th

International Conference on Renewable Energy Research and Applications (ICRERA), Oct. 2018.

Journal Publications:

1. **S.A. Raza** and J. Jiang, *"Intra- and Inter-Phase Power Management and Control of a Residential Microgrid at the Distribution Level"*, IEEE Transactions of Smart Grid, Vol.10, No.6, April 2019,

2. **S.A. Raza** and J. Jiang, *"A Benchmark Distribution System for Investigation of Residential Microgrids with Multiple Local Generation and Storage devices"*, IEEE Open Access Journal of Power and Energy, Vol.7, pp. 41-50, November 2019.

3. **S.A. Raza** and J. Jiang, *" Mathematical Foundations for Balancing Single-Phase Residential Microgrids Connected to Three-Phase Distribution System"*, under review for IET Generation, Transmission and Distribution Journal.

4. **S.A. Raza** and J. Jiang, *"Balancing Three Single-Phase Residential Microgrids in Distribution Networks through Phase-wise Power Exchange"*, under review for IEEE Transactions on Smart Grid.

5. **S.A. Raza** and J. Jiang, *"Experimental Investigation of Inter-phase Power Management in Residential Microgrids"*, under review for IEEE Open Access Journal of Power and Energy.

Other Publications:

1. **S.A. Raza** and A.H.M.A. Rahim, *"An Adaptive Pitch Control Strategy for Doubly Fed Wind Generation System"*, Summer Simulation Conference, Toronto, Canada, 2013, pp. 714-719.

2. **S.A. Raza** and S.A.R. Naqvi, *"Design of a Power System Stabilizer for a Synchronous Generator using Hybrid Intelligent Controller"*, 7th IEEE GCC conference, Doha, Qatar, November 2013, pp. 468-473.

3. **S.A. Raza** and R.K. Varma, *"Coordinated Control of STATCOM and PSS for Damping Generator Electromechanical Oscillations"*, in IEEE EPEC London, Ontario, November 2015.

Patent:

1. Patent in USPTO, titled *"Adaptive Pitch Control System for Wind Generators"*, file US 13/862327. Publication No: US20140306451 A1.