

Electronic Thesis and Dissertation Repository

5-29-2015 12:00 AM

Control System Design, Analysis, and Simulation of a Photovoltaic Inverter for Unbalanced Load Compensation in a Microgrid

Elizabeth K. Tomaszewski, *The University of Western Ontario*

Supervisor: Dr. Jin Jiang, *The University of Western Ontario*

A thesis submitted in partial fulfillment of the requirements for the Master of Engineering Science degree in Electrical and Computer Engineering

© Elizabeth K. Tomaszewski 2015

Follow this and additional works at: <https://ir.lib.uwo.ca/etd>



Part of the [Power and Energy Commons](#)

Recommended Citation

Tomaszewski, Elizabeth K., "Control System Design, Analysis, and Simulation of a Photovoltaic Inverter for Unbalanced Load Compensation in a Microgrid" (2015). *Electronic Thesis and Dissertation Repository*. 2882.

<https://ir.lib.uwo.ca/etd/2882>

This Dissertation/Thesis is brought to you for free and open access by Scholarship@Western. It has been accepted for inclusion in Electronic Thesis and Dissertation Repository by an authorized administrator of Scholarship@Western. For more information, please contact wlsadmin@uwo.ca.

CONTROL SYSTEM DESIGN, ANALYSIS, AND SIMULATION OF A
PHOTOVOLTAIC INVERTER FOR UNBALANCED LOAD COMPENSATION IN A
MICROGRID

(Thesis format: Monograph)

by

Elizabeth Klara-Marie Tomaszewski

Graduate Program in Electrical and Computer Engineering

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Engineering Science

The School of Graduate and Postdoctoral Studies
The University of Western Ontario
London, Ontario, Canada

© Elizabeth Tomaszewski 2015

Abstract

This thesis presents a control scheme for a single-stage three-phase Photovoltaic (PV) converter with negative sequence load current compensation.

In this thesis a dual virtual impedance active damping technique for an LCL filter is proposed to address the issue of LCL filter resonance. Both inverter-side current and the capacitor current are used in the feedback loop. Using both signals provides higher DC rejection than using capacitor current alone. The proposed active damping scheme results in a faster transient response and higher damping ratio than can be obtained using inverter-side current alone. The feedback gains can be calculated to achieve a specified damping level.

A method of determining the gains of the Proportional and Resonant current controller based on frequency response characteristics is presented. For a specified set of gain and phase margins, the controller gains can be calculated explicitly. Furthermore, a modification is proposed to prevent windup in the resonator.

A numerically compensated Half-Cycle Discrete Fourier Transform (HCDFT) method is developed to calculate the negative sequence component of the load current. The numerical compensation allows the HCDFT to accurately estimate the fundamental component of the load current under off-nominal frequency conditions. The proposed HCDFT method is shown to have a quick settling time that is comparable to that obtained with conventional sequence compensation techniques as well as immunity to harmonics in the input signal.

The effect of unbalance compensation on the PV power output depending on the irradiance and the operational region on the power-voltage curve is examined. Analysis of the DC link voltage ripple shows the region of operation on the P-V curve affects the amplitude of the DC link voltage ripple during negative sequence compensation.

The proposed control scheme is validated by simulation in the Matlab/Simulink® environment. The proposed control scheme is tested in the presence of excessive current imbalance, unbalanced feeder impedances, and non-linear loads. The results have shown that the proposed control scheme can improve power quality in a hybrid PV-diesel microgrid by reducing both voltage and current imbalance while simultaneously converting real power from a PV array.

Keywords: Photovoltaic (PV), LCL, Active Damping, Proportional Resonant Controller, Anti-Windup, Active Power Filter, Discrete Fourier Transform (DFT), Negative sequence, Load Compensation, Microgrid, Inverter control.

Dedication

To my family, JMJ

Acknowledgements

I would like to express my gratitude and appreciation for all those who made this work possible. First and foremost on this list is my supervisor Dr. Jin Jiang, for the guidance, support, and inspiration he has provided. I would also like to thank Dr. Xinhong Huang for her invaluable support in managing the final stages of this work in particular. Without her assistance this work would never have reached this stage.

I am very grateful to Dr. Gerry Moschopoulos, Dr. Rajiv K. Varma, and Dr. Mehrdad Kermani for their valuable courses and Dr. Mohammad Dadash Zadeh for his advice.

I am grateful to my colleagues at the UWO CIES lab: Andrew T. Moore for giving generously of his time to offer his advice and expertise; Devbratta Thakur, Syed A. Raza, and Mike Gverzdys for all the coffee trips; and Hisham Mahmood, Denis Michaelson, and Drew Rankin for the many conversations, technical and non-technical.

I would like to thank Johnathan Houghtan for his work editing this thesis. I would also like to also thank my “chemical” friends Isabela Reiniati and Reyna Gomez. Their patience in helping me rehearse presentations and words of wisdom were a source of hope when I needed it most.

Without the friendship, encouragement, and prayers from my family I could not have completed this work. Particular praise is due to my first teacher, my mom Kathy Tomaszewski, for passing on her own love of learning, for all the Thursday night phone calls, the time spent reviewing this thesis, and for encouraging me to pursue graduate studies in the first place.

Above all I owe the successful completion of this work to God, the author of truth.

Table of Contents

Abstract	ii
Dedication	iii
Acknowledgements	iv
Table of Contents	v
List of Tables	x
List of Figures	xi
List of Appendices	xviii
List of Abbreviations	xix
Symbols and Nomenclature	xxi
Chapter 1	1
1 Introduction	1
1.1 'Unbalance in Three-Phase Grids	2
1.2 Control of PV Systems	4
1.3 Research Objectives and Scope	5
1.3.1 Motivations and Problem Statement	5
1.3.2 Scope and Objectives	6
1.4 Organization of the Thesis	7
1.5 References	8
Chapter 2	12
2 Background and Literature Review	12

2.1	Review of Symmetrical Components.....	12
2.2	Calculation of Symmetrical Components for Control Applications	15
2.3	Review of Compensating Devices	20
2.4	Review of Dual Purpose PV Systems	24
2.5	LCL Filter Resonance Damping	26
2.6	Summary	30
2.7	References	30
Chapter 3.....		38
3	Design and Analysis of the Control Strategy.....	38
3.1	Inverter Modeling.....	40
3.2	Virtual Impedance Active Damping Scheme.....	43
3.2.1	Damping Coefficient Calculation	45
3.2.2	Effects of Grid Inductance Variation.....	48
3.3	Calculation of the Current Controller Gains	50
3.4	Anti-Windup Scheme for a PR Controller	56
3.4.1	Discrete Implementation of a PR Controller.	56
3.4.2	Windup in PR Controllers.....	57
3.4.3	Proposed Anti-windup Scheme.....	61
3.4.4	Anti-windup Gain Selection	65
3.4.5	Extension to Three-Phase, Three-Wire Inverters.....	67

3.4.6	Performance Comparison of the Proposed Anti-Windup Scheme	71
3.5	DC Link Voltage Control.....	73
3.6	Frequency Estimation.....	76
3.7	Maximum Power Point Tracking	78
3.8	Conclusion.....	80
3.9	References	81
Chapter 4	84
4	Calculation of the Negative Sequence Current Component	84
4.1	Negative Sequence Calculation.....	84
4.1.1	The Half-Cycle DFT	86
4.1.2	Negative Sequence Calculation in the Phasor Domain.....	88
4.1.3	Numerical Compensation for Off-Nominal Frequency	89
4.1.4	Estimated Error of the Fundamental Phasor due to Off-Nominal Frequency ..	91
4.2	Verification of the Compensation Algorithm.....	96
4.2.1	Performance of the Compensated HCDFT	96
4.3	Comparison with Conventional Techniques	99
4.3.1	Settling Time.....	99
4.3.2	Unbalanced Harmonics	100
4.3.3	Balanced Harmonics	101
4.4	Calculation of the Compensation Reference Current.....	102

4.5	Conclusion.....	103
4.6	References	103
Chapter 5.....		105
5	Compensation of Unbalanced Load for Different Operating Conditions of a PV Array 105	
5.1	Case 1: PV Curve Region of Operation and Effect of Unbalance Compensation .	106
5.1.1	Analysis of DC Link Voltage Ripple in APF Mode	112
5.1.2	Analysis of the DC Link Voltage Ripple in the Constant Voltage Region	114
5.2	Case 2: Negative Sequence Compensation Under Different Irradiance Levels.....	116
5.3	Conclusion.....	121
5.4	References	122
Chapter 6.....		123
6	Control of a PV Inverter for Negative Sequence Current Compensation in a Microgrid 123	
6.1	Case Study Test Network.....	123
6.2	Case Study 1: Compensation Current Scaling	124
6.2.1	Magnitude Scaling for Limiting Negative Sequence Current.....	124
6.2.2	Simulation Results	126
6.3	Case Study 2: Unbalanced Grid Impedance.....	129
6.4	Case Study 3: Non-Linear Loads	133
6.5	Case Study 4: Transient Unbalanced Loads.....	139

6.6	Case Study 5: Phase Balancing in a Hybrid Diesel-PV Microgrid	143
6.6.1	System Performance without Negative Sequence Compensation	144
6.6.2	System Performance with Negative Sequence Current Compensation	147
6.7	Conclusions	151
Chapter 7.....		152
7	Summary and Conclusions	152
7.1	Summary of Major Contributions	153
7.2	Suggestions for Future Work	154
Curriculum Vitae		163

List of Tables

Table 3.1: LCL filter parameter values	42
Table 3.2: Current Controller Parameters	55
Table 3.3: Current THDs before and after saturation	68
Table 4.1: HCDFT Filter length.....	94
Table 4.2: Coefficients of approximate gain equation.....	95
Table 5.1: Array parameters for Case 1	108
Table 6.1: Feeder impedances for case study 2	130
Table 6.2: Current and voltage THDs for case study 3.....	138
Table A.1: PV Panel/array parameters [1].....	157
Table B.1: Diesel engine parameters	159
Table B.2: Excitation system parameters.....	160

List of Figures

Figure 2.1: Symmetrical Sequence Components	12
Figure 2.2: Frequency response of a 1 st order AP filter	16
Figure 2.3: Symmetrical component calculation using AP filters [5]	17
Figure 2.4: Second order generalized integrator block diagram [8]	17
Figure 2.5: Positive sequence calculation in the $\alpha\beta$ frame	18
Figure 2.6: Passive balancing network [17].....	21
Figure 2.7: (a) Three-wire and (b) four-wire voltage source converters	22
Figure 2.8: A DVR with line-side Harmonic filter [14]	24
Figure 2.9: Single line diagram of a VSC with an LCL filter.....	26
Figure 2.10: Passive damping of an LCL filter.....	27
Figure 2.11: Weighted-average current control active damping	28
Figure 2.12: Virtual impedance damping	29
Figure 3.1: Overall block diagram of the inverter control scheme	39
Figure 3.2: A single stage PV inverter with an LCL filter.....	40
Figure 3.3: Poles of the inverter with the LCL Filter	41
Figure 3.4: LCL filter frequency response.....	43
Figure 3.5: Proposed active damping scheme for an LCL filter	44
Figure 3.6: Equivalent Filter with virtual impedance active damping.....	45

Figure 3.7: Frequency Response of the damped filter as ζ is increased from 0.1 to 1	47
Figure 3.8: Frequency response of the LCL filter with and without AD.....	47
Figure 3.9: Filter response for filters with low, medium, and high natural resonance frequencies	48
Figure 3.10: (a) Impact of a ten-fold increase and (b) decrease in L_g on open loop poles	49
Figure 3.11: Frequency response of the LCL filter.....	50
Figure 3.12: The current control loop.....	50
Figure 3.13: Block diagram of a proportional + resonant controller	51
Figure 3.14: PR controller frequency response.....	52
Figure 3.15: Bode plot of the loop transfer function for PI and PR controllers	55
Figure 3.16: Step response of current control loop when a PR controller is used for a 100% increase in current reference magnitude at $t = 0.25$ s	56
Figure 3.17: Discrete-time Proportional Resonator	57
Figure 3.18: Amplitude integrator for a sinusoidal signal	57
Figure 3.19: Controller output u for constant error input signal $i_{g,ref} - i_g$	58
Figure 3.20: Anti-windup scheme using back-calculation [10].....	59
Figure 3.21: PR output for a constant error signal when a back-calculation anti-windup scheme is used.....	60
Figure 3.22: Proposed Anti-Windup scheme for PR based current controller with an AD loop	62
Figure 3.23: Equivalent block diagram of Modified PR controller	63

Figure 3.24: Frequency response of the gain of the back calculation signal for normalized value of $K_2 = 0$ and $K_2 = 500$	64
Figure 3.25: Modulation index for phase A with maximum error input and $K_2 = 0$	66
Figure 3.26: dq axis inverter current for $K_2 = 1000$	66
Figure 3.27: Modulation index for phase A with $K_2 = 1000$	67
Figure 3.28: (a) Inverter current, (b) PR controller output (d) modulation index, and (c) summation of the three phase controller outputs	68
Figure 3.29: Zero sequence elimination loop	69
Figure 3.30: (a) Inverter current, (b) PR controller output (d) modulation index, and (c) summation of the three phase controller outputs when zero sequence feedback loop is employed.....	70
Figure 3.31: (a) Inverter current and (b) modulation index when only two PR controllers are used	71
Figure 3.32: Inverter current (a) and modulation index (b) without anti-windup, inverter current (c), modulation index (e) and dq frame current (g) with the proposed AW scheme, and with the AW scheme from [10](d)(f)(h)	73
Figure 3.33: Bus voltage control loop.....	74
Figure 3.34: Frequency response of the compensated and non-compensated forward loop gains at maximum and minimum output power	75
Figure 3.35: Sinusoidal reference current generation.....	76
Figure 3.36: Frequency Locked Loop.....	77
Figure 3.37: Output of the FLL.....	77
Figure 3.38: Effect of irradiance on P-V curve (a) and effect of temperature variation (b) ..	78

Figure 3.39: P&O MPPT algorithm.....	80
Figure 4.1: (a) Input signal and DFT magnitude and (b) phase.....	86
Figure 4.2: Settling time of the Full and Half cycle DFT.....	87
Figure 4.3: (a) Magnitude and (b) phase of the discrete-time frequency response of the HCDFD 88	88
Figure 4.4: (a) Three-phase load current, and (b) the magnitude of the –ve sequence calculated by the HCDFD	89
Figure 4.5: (a) Negative sequence magnitude and (b) phase error under off nominal frequency conditions, with $f_g = 60.9\text{Hz}$	90
Figure 4.6: Case 1, Compensated negative sequence (a) phasor magnitude and (b) phase for $f_g = 61\text{ Hz}$	96
Figure 4.7 Case 2, (a) Negative sequence output with $f_g = 58.2\text{ Hz}$ and (b) input signals containing 5 th , 7 th , and 11 th harmonics with THD of 11.2%	97
Figure 4.8: Case 2, (a) Negative sequence for $f_g = 61.0\text{ Hz}$ and (b) input signals containing 5 th , 7 th , and 11 th harmonics with THD of 11.2%	98
Figure 4.9: (a) Settling time of HC-DFT, SOGI, $dq0$, and APF method of sequence calculation (b) to 50% decrease in the negative sequence	100
Figure 4.10: (a) Negative sequence calculated by HC-DFT, APF, and SOGI techniques and (b) unbalanced harmonic input with $f_g = 60.5\text{ Hz}$	101
Figure 4.11: (a) Output of negative sequence calculation algorithms, and (b) balanced, highly distorted input with $f_g = 59.8\text{ Hz}$	102
Figure 4.12: Compensating current reference calculation	103
Figure 5.1: Distribution network simulated in Chapter 5	106
Figure 5.2: Power relationship with DC link connections of the PV system	107

Figure 5.3: Regions of the I-V curve for a PV array	107
Figure 5.4: Three PV characteristic curves used in Case 1.....	108
Figure 5.5: Steady state DC bus voltage waveforms during negative sequence compensation for Active Power Filter (APF), Constant Current (CC), Constant Voltage (CV), and Maximum Power Point (MPP) operation	109
Figure 5.6: Total DC link power, P_{dc} during negative sequence compensation for (a) MPP region, (b) CC region, and (c) CV region	110
Figure 5.7: Capacitor power during negative sequence compensation P_{cap} for (a) MPP region (b) CC region, and (c) CV region	111
Figure 5.8: PV array power during negative sequence compensation, P_{pv} in (a) MPP region, (b) CC region, and (c) CV region in the CV region.....	112
Figure 5.9: PV curves for irradiance from 200-800 W/m ²	117
Figure 5.10: Load current for case 2.....	117
Figure 5.11: Grid current when irradiance is (a) 200, (b) 400, (c) 600, and (d) 800 W/m ² ..	118
Figure 5.12: Inverter current when irradiance is (a) 200, (b) 400, (c) 600, and (d) 800 W/m ²	118
Figure 5.13: DC link voltage for irradiance of (a) 200, (b) 400, (c) 600, and (d) 800 W/m ²	119
Figure 5.14: Average PV array power before and during negative sequence current compensation	120
Figure 6.1: Single line diagram of the test system used in cases 1-4.....	124
Figure 6.2: Negative sequence reference current limiting	125
Figure 6.3: PV curves for case study 1	127
Figure 6.4: Irradiance of the PV array for case study 1	127

Figure 6.5: Moving- average of the power of the PV array	128
Figure 6.6: Scaling factor limiting the negative sequence inverter current I_{comp}	128
Figure 6.7: Grid power for case study 1	128
Figure 6.8: DC link voltage	128
Figure 6.9: (a) Positive and (b) negative sequence voltage at bus B1	129
Figure 6.10: (a) Three-phase load power, (b) +ve sequence voltage (c), -ve sequence voltage, (d)-(e) -ve sequence current, (f) grid power, (g) DC link voltage, and (h) average PV power for case study 2	133
Figure 6.11: (a) Voltage at the inverter bus and (b) load current, and (c) grid current when the HCDFT is used for case study 3	135
Figure 6.12: Negative sequence amplitude calculated by the HCDFT when a three-phase rectifier load is connected	135
Figure 6.13: (a) Current injected by the PV inverter when the HCDFT method is used to calculate the compensation current and (b) inverter current when the compensation loop is disabled	136
Figure 6.14: (a) Amplitude of the negative sequence reference current and (b) inverter current when AP filters are used to calculate the compensation current	137
Figure 6.15: (a) Amplitude of the negative sequence current reference and (b) inverter current when SOGI filters are used to calculate the compensation current	138
Figure 6.16: (a) Load current, (b) grid current, and (c) inverter current for case study 4	140
Figure 6.17: (a) Grid current and (b) inverter current transient following connection of the unbalanced load	141
Figure 6.18: Moving-window average of PV power during Case 4	142
Figure 6.19: DC link voltage during case study 4	142

Figure 6.20: Single line diagram of the remote grid simulated in case study 5.....	144
Figure 6.21:Unbalanced loading without phase balancing, (a)positive sequence voltage at bus 1 , (b) negative sequence voltage at bus 1, (c) frequency, (d) real and reactive power supplied by the generator, (e) load current, (f) generator current, (g) inverter current, (h) DC link voltage, and (i) average PV array power	147
Figure 6.22: System variables when the PV inverter compensates load unbalance, (a) positive and (b) negative sequence voltages at bus 1, (c) generator real and reactive power, (d) grid frequency , (e) measured negative sequence load current , (f) load current, (g) generator current, and (h) inverter current. (i) DC link voltage, and (j) average PV power	150
Figure A.1: Single diode model of a PV cell [1]	155
Figure B.1: Diesel engine model	159
Figure B.2: Voltage regulator and excitation system for the generator	160

List of Appendices

Appendix A: PV Modeling.....	155
Appendix B: Diesel Generator Parameters.....	158
Appendix C: Derivations for Section 3.3.....	161

List of Abbreviations

AD	Active Damping
ANF	Adaptive Notch Filter
AP	All Pass
APF	Active Power Filter
AVR	Automatic Voltage Regulator
AW	Anti-Windup
BW	BandWidth
CC	Constant Current
CSC	Current Source Converter
CV	Constant Voltage
DFT	Discrete Fourier Transform
DSOGI	Dual-Second Order Generalized Integrator
DSRF	Dual Synchronous Reference Frame
DVR	Dynamic Voltage Restorer
FC	Fuel Cell
FLL	Frequency-Locked Loop
GM	Gain Margin
HCDFT	Half-Cycle Discrete Fourier Transform
IGBT	Insulated Gate Bi-polar Transistor
INC	Incremental Conductance
IR	Irradiance
ISC	Instantaneous Symmetrical Components
MOSFET	Metal Oxide Semi-conductor Field Effect Transistor

MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
P&O	Perturb and Observe
PI	Proportional Integral
PLL	Phase-Locked Loop
PM	Phase Margin
PR	Proportional Resonant
pu	Per Unit
PV	Photovoltaic
PWM	Pulse Width Modulation
SOGI	Second Order Generalized Integrator
SPWM	Sinusoidal Pulse Width Modulation
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

Symbols and Nomenclature

C_{DC}	DC link capacitor
S_1 - S_6	VSC bridge switches 1 through 6
ABC	Three-phase
a	Complex gain with 120° phase shift
V	Voltage
I	Current
p	Instantaneous power
ω_0	Nominal frequency, rad/s
Hz	Hertz, 1/sec
v_α	Alpha-axis voltage
v_β	Beta-axis voltage
L_c	Inverter-side filter inductor
r_c	Inverter-side filter parasitic resistance
C_f	VSC filter capacitor
L_g	Grid-side filter inductor
r_g	Grid-side filter parasitic resistance
i_g	Current injected into the grid by the PV system
i_c	Current in filter capacitor
i	Current at inverter terminals
v_g	Voltage at the point of common coupling
v_{inv}	Voltage at the inverter terminals
v_c	Voltage across filter capacitor
L_{gr}	Equivalent grid inductance
r_{gr}	Equivalent grid resistance

x_{damp}	Virtual impedance active damping feedback variable
V_{DC}	DC link voltage
M	Modulating index
k_{dl}	Active damping inverter-side current feedback gain
k_{dc}	Active damping capacitor current feedback gain
R_{eq}	Equivalent series resistance
Z_{eq}	Equivalent impedance in parallel with the filter capacitor
u	Output of PR current controller
ζ	Damping ratio
m	Relative distance of the real pole
$i_{g,ref}$	Inverter current reference
k_p	Proportional gain of PR controller
k_i	Resonator gain of PR controller
ω_r	LCL filter resonant frequency
ω_c	Cross-over frequency
u_r	Output of the resonator
K_1	Anti-windup gain 1
K_2	Anti-windup gain 2
$k_{dc,p}$	Proportional gain of the DC link voltage controller
$k_{dc,i}$	Integral gain of the DC link controller
f_g	Grid frequency
f_s	Sampling frequency
N	DFT filter length
X_N	DFT output phasor of signal x
M	Half-Cycle DFT filter length

X_{Ng}	Compensated phasor
k_1, k_2	HCDFT Complex error coefficients
X_{Ng}^-	Compensated negative sequence phasor
X_{Ng}^+	Compensated positive sequence phasor
R_{lg}^-	Compensated real filtered negative sequence load current
I_{lg}^-	Compensated imaginary filtered negative sequence load current
i_l	Load current
V_{pv}	Voltage across PV array terminals
P_{pv}	Output power of the PV array
P_{cap}	Power from the DC link capacitor
I-V	Current vs. Voltage
P-V	Power vs. Voltage
rms	Root mean square
X	Reactance
R	Resistance
SF	Scaling factor for the compensation current reference
Z_{gr}	Grid impedance

Chapter 1

1 Introduction

In recent years, the concept of a microgrid has gained significant attention in academia and practical applications and is at the forefront of power system research and development. By definition, a microgrid is a small scale power system including at least two generation sources and a collection of loads [1], [2]. Most microgrids are low voltage distribution scale systems [2]. A microgrid can be electrically connected to a larger grid or operated in stand-alone mode (termed ‘islanded mode’). Renewable or alternative energy resources, such as wind, solar Photovoltaic (PV) or hydrogen Fuel Cell (FC) can be integrated into microgrids relatively easily. Most of these resources do not produce electricity in a form that is directly compatible with the AC grid. Thus interfacing power electronic converters are required for grid integration purposes.

Because of their possibility for flexibility, microgrids can offer potential advantages over the conventional grid. By operating in islanded mode a microgrid can continue to supply power to critical loads during a grid blackout. Industrial users in particular can benefit from on-site combined heat and power generation in the form of a microgrid. Microgrids also offer an alternative to electrification of remote locations without the high capital cost of transmission line construction. Because loads and generators are close together, transmission losses can be reduced. The closer tie between generation and consumption means that demand response and load shedding can be used more effectively. Moreover, microgrids potentially offer a way of utilizing the capabilities of converter interfaced generation sources to deal with power quality issues [3]. The potential military applications for microgrids have motivated much research as well [4]-[8].

Small, stand-alone distribution systems ranging in capacity from a few kW’s to tens of MW’s have long been used to supply electricity to many remote communities scattered throughout northern Canada [9]. According to a 2011 report by CANMET Energy, of the 292 remote residential communities in Canada, 249 have diesel power plants or gasoline gen-sets [9]. The total installed capacity is 453.3 MW of fossil fuel driven generators and 153.1 MW of hydro-electric generators. Synchronous generators driven by diesel engines are used for

electrification of remote communities in much of the world. As an established technology they have the advantage of reliability, and availability of maintenance technicians. Diesel gen-sets are also being used in conjunction with renewable resources to provide a backup source of electricity. The main drawbacks of diesel generating units are the high cost of diesel fuel and the difficulty of transporting the fuel to ultra-remote locations. Some communities in Nunavut and Ontario, for example, must have diesel fuel flown in. This has caused electricity prices to reach \$1.3/kWh CAD in some locations [10] creating a financial incentive to investigate alternative energy possibilities. Incorporating renewable energy resources in remote communities could be an improvement from both a financial and environmental perspective [9]. Since the 1970s many solutions have been proposed [10]-[14], nearly all of which involve adding renewable generation in the form of solar Photovoltaic (PV) or wind to the supply mix. Pilot projects have produced some promising results but system capacity is often under-utilized due to improper sizing, low load conditions, and seasonal variation in daily solar Irradiance (IR) [10].

During times of lower power production, the under-utilized PV inverter can be used for ancillary functions like power quality improvement and voltage regulation. In the literature PV inverters have been reported to be used for voltage control in low voltage grids [15], [16] increasing transmission line capacity [17], and active power filtering [18]. Unbalance in three-phase microgrids is another power quality issue which has the potential to be addressed by PV inverters.

1.1 'Unbalance in Three-Phase Grids

An ideal power grid is assumed to be balanced, but in practice factors such as single phase loads, untransposed lines, asymmetrical faults, open conductors, and single phase distributed generation can all contribute to grid unbalance. There are several factors which can cause microgrids and remote grids to be susceptible to unbalance. Distribution level microgrids may have a high portion of single phase loads which can cause unbalanced feeder loading. Unequal feeder lengths in rural microgrids can cause voltage unbalance. Distributed generation units with single phase connections can cause unbalanced voltage swells. In the islanded mode of operation microgrids cannot rely on support from the utility grid to maintain balanced voltages in the presence of unbalanced loads [19].

Unbalanced voltages can have a severe impact on three-phase loads, especially machine loads which require de-rating when the voltage unbalance exceeds a certain level [20]. Unbalance can occur in either the load current, voltage, or both. Unbalanced load current will cause a double line frequency ripple in the three-phase power, and can cause torque pulsation in three-phase generators [21]. Serious overheating of the rotor can occur in a synchronous generator producing negative sequence current [22]. Unbalanced voltages have long been known to have a negative impact on polyphase induction motors. In [23] it was reported that the negative sequence current induced by voltage imbalance increases losses in the rotor and stator and decreases the net torque produced on the shaft. The losses in the machine produce higher levels of heating. Other effects include higher noise levels and increased mechanical vibrations.

An unbalanced three phase power system can be represented by the superposition of three balanced systems, known as the positive sequence circuit, negative sequence circuit, and zero sequence circuit [24]. Several definitions for quantifying voltage unbalance have been proposed [20]. The National Electrical Manufacturers Association measures the degree of unbalance by the ratio of the maximum deviation from the average voltage over the average of the phase to phase voltages, while European standards use the ratio of negative to positive sequence voltage [20]. The European standard definition has been widely accepted in the literature [20], [22] and is adopted in this thesis.

For a voltage unbalance of 2%, a 5% derating of three-phase induction motors is required [20]. For 5% unbalance, 25% derating is recommended according to NEMA Standard MG 1-1993 [20]. For synchronous generators the limit on negative sequence current depends on the type of machine. The suggested negative sequence continuous current limitation for turbo-generators is 10-15% of the maximum current depending on the cooling system used [22]. Hydro turbines on the other hand can typically supply continuous negative sequence current of up to 40% of the rated stator current without sustaining damage. The strong damper windings in salient pole hydro generators provide a path for the double line frequency current induced during unbalanced operation, which prevents excessive heating of the rotor.

Power electronic interfaced loads and energy sources can also be affected by voltage unbalance [25], [26]. Under unbalanced voltage conditions a double line frequency ripple is induced in the voltage of the DC link of Voltage Source Converters (VSCs). Increased harmonics in the output current are also observed when the voltage is unbalanced [25]. Unlike machine loads and generators, the impact of unbalanced voltages on static converters can be mitigated through proper control techniques. A control scheme is reported in [27] which suppresses ripples in the DC link voltage in a grid interfacing converter for a renewable source under unbalanced voltage conditions.

The potentially adverse effects associated with grid unbalance have motivated researchers to find innovative ways to deal with unbalanced systems. Transmission line transposition, load switching, and adequate system planning are among the ways of preventing unbalance. In situations where unbalance cannot be prevented a number of devices can be used to mitigate the voltage and/or current unbalance. These devices include passive compensators, Active Power Filters (APFs), Static Synchronous Compensators (STATCOMs), and Dynamic Voltage Restorers (DVRs). All these devices, with the exception of passive compensators, are based on the VSC architecture. Many PV inverters use the same basic topology as STATCOMs and APFs. With an appropriate control strategy, a PV converter can also provide negative sequence compensation.

1.2 Control of PV Systems

Sinusoidal current injection is accomplished by controlling the VSC. A typical PV inverter control scheme consists of several nested loops. The outer loop tracks the Maximum Power Point (MPP) and generates the voltage reference for the DC link voltage controller. The DC link voltage controller generates the power reference. The inner current controller regulates the current and generates the terminal voltage reference for the inverter. Pulse Width Modulation (PWM) or another switching scheme is used to determine the instantaneous state of each of the six switches to produce the desired voltage at the VSC terminals.

To simplify design and implementation, conventional VSC control schemes often utilize the rotating reference frame [28], [29]. The transformation from the stationary ABC frame to the rotating dq frame converts AC signals into DC quantities. This allows Proportional Integral (PI) controllers to be used for current control. However, PI controllers are ineffective in

controlling the ripples caused by the synchronous reference frame transformation of unbalanced quantities. Standard dq frame control schemes cannot inject the necessary negative sequence compensating current.

For negative sequence compensation, the current control loop should be able to control the grid-injected current directly and must be able to control unbalanced signals. The DC link voltage control loop needs to be immune to double-line frequency oscillations in the measured DC link voltage. The control scheme must also include a method of generating the reference compensation current.

1.3 Research Objectives and Scope

1.3.1 Motivations and Problem Statement

Solid-state converters can tolerate unbalanced conditions as long as the control strategy is capable of dealing with unbalanced quantities. This is in contrast with rotating machines which can be damaged by unbalanced voltage and current. PV interfacing VSCs normally have under-utilized power rating capacity at times because of the intermittency of solar energy. Unbalanced load compensation can be achieved without installing additional devices by using available capacity of the converter of a PV generator to inject an unbalanced three-phase current. This results in only a balanced current being drawn from the generator. Although the physical hardware of the inverter is capable of handling unbalanced quantities, synchronous reference frame control techniques cannot. Most of the control strategies for three-phase PV inverters proposed in the literature are based on synchronous reference frame theory.

Since the primary purpose of the PV system is for real power conversion there may be scenarios where total compensation of the load unbalance in addition to power conversion would exceed the ratings of the converter. In these situations it should be possible to prioritize power conversion by reducing the compensating current reference. This requires explicit calculation of the fundamental negative sequence current. An accurate, robust method of calculating the compensating current is needed. To be suitable for deployment in a remote grid it should have tolerance for frequency deviation and harmonic loads.

In a single stage PV converter not only does negative sequence current compensation affect the control requirements, it can also impact the production of real power from the PV generator. It is important to verify the performance of the whole system under different irradiance and temperature conditions. The effect of double line frequency DC link voltage oscillations is considered for single phase PV inverters in [30]. The interaction between APF operation and PV system performance is investigated in [31]. However, only two-stage converter configurations are considered in [31]. There is a need to further investigate the limitations and effects of the PV array on phase compensation for single stage converters.

1.3.2 Scope and Objectives

Power system planning to estimate loads on each phase is an essential step in preventing and reducing network unbalance. However, not all causes of load and voltage unbalance can be foreseen. In this thesis the focus is on compensating existing load unbalance rather than preventing it. New converter topologies are also outside the scope of this investigation since the goal is to make use of existing converter systems for phase balancing purposes. Maximum power point tracking for PV systems is a well-studied topic and is also outside the focus of this work. The Perturb-and-Observe (P&O) method which has been previously reported in many other works is adopted in this thesis. This also allows the effect of negative sequence compensation on a conventional MPPT scheme to be verified.

The focus of this thesis is on development of control strategies for a PV interfacing VSC which has the secondary objective of compensating negative sequence load current. A three-phase PV system connected to a three wire grid has been considered. With the goal of making use of existing under-utilized converters, a conventional three leg VSC distribution scale converter is examined.

The main objectives of this research are:

1. To design a control scheme for a single-stage three-phase VSC with an LCL filter configuration to compensate negative sequence load current.
 - This requires the current controller to be able to track unbalanced current references.

- In order to effectively compensate the negative sequence load current, the grid-side current of the inverter must be controlled. An active damping scheme is proposed for the VSC AC filter to allow control of the grid-side current.
 - Single-stage PV converters must operate over a relatively wide range of DC-link voltages. The current controller should be able to function without saturating the switching function even under low DC link voltage conditions. An anti-windup scheme is proposed for stationary frame proportional resonant controllers to improve robustness under both low voltage and high voltage conditions.
2. To design a negative sequence load current estimator to generate the compensation current reference.
 - The negative sequence load current is calculated using the Half-Cycle Discrete Fourier Transform (HCDFT). The HCDFT reaches its output in one-half of a cycle of the fundamental regardless of harmonic or noise distortion in the input signal, and is able to reject harmonics in the input signal.
 - During off-nominal frequency conditions however, the standard HCDFT will not accurately calculate the fundamental component of the load current. A numerical compensation method is proposed to accurately calculate the negative sequence load current during frequency variation.
 3. To investigate the interaction between PV power production and unbalanced load compensation in a single-stage voltage source converter.
 - The ability of the system to compensate negative sequence load current under various operating conditions of the PV is examined. The oscillating power injected by the converter during unbalance compensation affects the DC link voltage differently depending on the region of operation on the P-V curve. From the analysis and simulations conducted, recommendations for real power curtailment are drawn.

1.4 Organization of the Thesis

Chapter 2 provides further background on compensating devices and their control. The first section of Chapter 2 contains a brief introduction to the theory of symmetrical components

and a literature review of unbalance compensating devices. Previously proposed dual-purpose PV systems are discussed in Section 2.5. An overview of techniques for damping resonance in higher order VSC filters is presented. Control issues for single stage PV interfacing VSCs with 3rd order filters are presented along with previous solutions found in the literature. The proposed control scheme is developed and discussed in Chapter 3. A dual-feedback active damping technique is presented. Design of the Proportional Resonant (PR) controller gains based on frequency response for a VSC with the proposed active damping scheme is shown. A modification to the PR control to prevent resonator windup is proposed. Chapter 4 presents a numerically compensated half-cycle DFT algorithm for calculation of symmetrical components. The compensating current reference is calculated using the proposed HCDFT of the load current. The performance of the proposed technique is demonstrated and compared with conventional symmetrical sequence calculation methods. In Chapter 5 the effect of load compensation on a PV generator is investigated. The case studies in Chapter 6 verify the performance of the proposed control scheme in a microgrid containing diesel gen-sets. Chapter 7 summarizes the contributions of the thesis and provides some suggestions for future work.

1.5 References

- [1] R.H. Lasseter and P. Paigi, "Microgrid: a conceptual solution," in *IEEE Power Electronics Specialists Conf. 35th Annual*, 2004, pp. 4285-4290.
- [2] J.A. Peas Lopes, C.L. Moreira and A.G. Madureira, "Defining control strategies for MicroGrids islanded operation," *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 916-924, May 2006.
- [3] IEEE Guide for Design, Operation, and Integration of Distributed Resource Island Systems with Electric Power Systems," *IEEE Std 1547.4-2011*, pp. 1-54, Jul. 2011.
- [4] T. Ersal, Changsun Ahn, I.A. Hiskens, Huei Peng, A. Stefanopoulou and J.L. Stein, "On the effect of DC source voltage on inverter-based frequency and voltage regulation in a military microgrid," in *American Control Conf. (ACC)*, 2012, pp. 2965-2971.
- [5] T. Ersal, Changsun Ahn, I.A. Hiskens, Huei Peng and J.L. Stein, "Impact of controlled plug-in EVs on microgrids: A military microgrid example," in *IEEE Power and Energy Soc. Gen. Meet.*, 2011, pp. 1-7.

- [6] T. Eرسال, C. Ahn, D.L. Peters, J.W. Whitefoot, A.R. Mechtenberg, I.A. Hiskens, H. Peng, A.G. Stefanopoulou, P.Y. Papalambros and J.L. Stein, "Coupling between component sizing and regulation capability in microgrids," *IEEE Trans. Smart Grid*, vol. 4, no. 3, pp. 1576-1585, Sep. 2013.
- [7] J. Mitra and M.R. Vallem, "Determination of storage required to meet reliability guarantees on island-capable microgrids with intermittent sources," *IEEE Trans. Power Syst.*, vol. 27, no. 4, pp. 2360-2367, Nov. 2012.
- [8] T.A. Nguyen, Xin Qiu, J.D. Guggenberger, M.L. Crow and A.C. Elmore, "Performance characterization for photovoltaic-vanadium redox battery microgrid systems," *IEEE Trans. Sustain. Energy*, vol. 5, no. 4, pp. 1379-1388, Oct. 2014.
- [9] J. Royer. (2013, June 18). *Status of Remote/Off-Grid Communities in Canada*. [online]. Available: <http://www.nrcan.gc.ca/energy/publications/sciences-technology/renewable/smart-grid/11916>.
- [10] M. Arriaga, C.A. Canizares, M. Kazerani, "Renewable Energy Alternatives for Remote Communities in Northern Ontario, Canada," *IEEE Trans. Sustain. Energy*, vol.4, no.3, pp.661-670, Jul. 2013.
- [11] W.A. Adams, C.L. Gardner, E.J. Casey, "Electrochemical energy storage systems: A small scale Application to isolated communities in the Canadian Arctic," *Canadian Elect. Eng. J.*, vol.4, no.3, pp.4-10, Jul. 1979.
- [12] D. Thevenard, L. Dignard-Bailey, S. Martel and D. Turcotte, "Performance monitoring of a northern 3.2 kWp grid-connected photovoltaic system," in *Proc. IEEE Photovoltaic Spec. Conf.*, 2000, pp.1711-1714.
- [13] S. Pelland, D. Turcotte, G. Colgate and A. Swingler, "Nemiah Valley Photovoltaic-Diesel Mini-Grid: System Performance and Fuel Saving Based on One Year of Monitored Data," *IEEE Trans. Sustain. Energy*, vol.3, no.1, pp.167-175, Jan. 2012.
- [14] J. Clavier, G. Joos and S. Wong, "Economic assessment of the remote community microgrid: PV-ESS-diesel study case," in *Proc. IEEE 26th Annu. Canadian Conf. on Elect. and Comput. Eng. (CCECE)*, 2013, pp. 5-8.
- [15] E. Demirok, P. Casado González, K.H.B. Frederiksen, D. Sera, P. Rodriguez and R. Teodorescu, "Local Reactive Power Control Methods for Overvoltage Prevention of Distributed Solar Inverters in Low-Voltage Grids," *IEEE J. Photovolt.*, vol.1, no.2, pp.174-182, Oct. 2011.
- [16] M. Fazeli, J.B. Ekanayake, P.M. Holland and P. Iqic, "Exploiting PV Inverters to Support Local Voltage—A Small-Signal Model," *IEEE Trans. Energy Convers.*, vol.29, no.2, pp.453-462, Jun. 2014.

- [17] R.K. Varma, S.A. Rahman, and T. Vanderheide, "New Control of PV Solar Farm as STATCOM (PV-STATCOM) for Increasing Grid Power Transmission Limits During Night and Day," *IEEE Trans. Power Del.*, vol.30, no.2, pp.755-763, Apr. 2015.
- [18] T. Wu, H. Nien, C. Shen and T. Chen, "A single-phase inverter system for PV power injection and active power filtering with nonlinear inductor consideration," *IEEE Trans. Ind. Appl.*, vol.41, no.4, pp.1075-1083, Jul.-Aug. 2005.
- [19] Q. Liu, Y. Tao, X. Liu, Y. Deng and X. He, "Voltage unbalance and harmonics compensation for islanded microgrid inverters," *IET Power Electron.*, vol.7, no.5, pp.1055-1063, May 2014.
- [20] A. von Jouanne and B. Banerjee, "Assessment of voltage unbalance," *IEEE Trans. Power Del.*, vol. 16, no. 4, pp. 782-790 Oct. 2001.
- [21] A. Elmitwally and M. Rashed, "Flexible Operation Strategy for an Isolated PV-Diesel Microgrid without Energy Storage," *IEEE Trans. Energy Convers.*, vol.26, no.1, pp.235-244, Mar. 2011.
- [22] (2010, Oct.). *Distribution Automation Handbook*. ABB. Vassa, Finland. [online]. Available: [http://www08.abb.com/global/scot/scot229.nsf/veritydisplay/238f74ed168c818ec125795f004342e7/\\$file/DAHHandbook_Section_08p12_Generator_Protection_757292_ENa.pdf](http://www08.abb.com/global/scot/scot229.nsf/veritydisplay/238f74ed168c818ec125795f004342e7/$file/DAHHandbook_Section_08p12_Generator_Protection_757292_ENa.pdf).
- [23] B.N. Gafford, W.C. Duesterhoeft and C.C. Mosher, "Heating of induction motors on unbalanced voltages," *Trans. Amer. Inst. of Elect. Eng. Power App. and Syst., Part III.*, vol. 78, no. 3, pp. 282-286, Apr. 1959.
- [24] J.D. Glover, M.S. Sarma and T.J. Overbye, *Power system analysis and design*, 4th ed. Toronto, Ont., Thomson: 2008.
- [25] A.I. Maswood, G. Joos, P.D. Ziogas and J.F. Lindsey, "Problems and solutions associated with the operation of phase-controlled rectifiers under unbalanced input voltage conditions," *IEEE Trans. Ind. Applicat.*, vol. 27, no. 4, pp. 765-772, Jul.-Aug. 1991.
- [26] L. Xiao, S. Huang and K. Lu, "DC-bus voltage control of grid-connected voltage source converter by using space vector modulated direct power control under unbalanced network conditions," *IET Power Electron.*, vol. 6, no. 5, pp. 925-934, May 2013.
- [27] A. Junyent-Ferré, O. Gomis-Bellmunt, T.C. Green and D.E. Soto-Sanchez, "Current control reference calculation issues for the operation of renewable source grid interface VSCs under unbalanced voltage sags," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3744-3753, Dec. 2011.

- [28] C.K. Sao and P.W. Lehn, "Control and Power Management of Converter Fed Microgrids," *IEEE Trans. Power Syst.*, vol.23, no.3, pp.1088-1098, Aug. 2008.
- [29] J. Dannehl, F.W. Fuchs, S. Hansen, and P.B. Thøgersen, "Investigation of Active Damping Approaches for PI-Based Current Control of Grid-Connected Pulse Width Modulation Converters With LCL Filters," *IEEE Trans. Ind. Applicat.*, vol.46, no.4, pp.1509-1517, Jul.-Aug. 2010.
- [30] T. Wu, C. Chang, L. Lin and C. Kuo, "Power Loss Comparison of Single- and Two-Stage Grid-Connected Photovoltaic Systems," *IEEE Trans. Energy Convers.*, vol.26, no.2, pp.707-715, Jun. 2011.
- [31] H. Patel and V. Agarwal, "Investigations into the performance of photovoltaics-based active filter configurations and their control schemes under uniform and non-uniform radiation conditions," *IET Renewable Power Generation*, vol.4, no.1, pp.12-22, Jan. 2010.

Chapter 2

2 Background and Literature Review

In this chapter more detail is given on the previous research done on phase balancing. Symmetrical components theory will be briefly reviewed. Previously reported methods of sequence component calculation will be discussed. In recent years, a number of power-electronic devices have been proposed which can compensate unbalanced networks. An overview of these devices is presented. Next, previously proposed dual-purpose PV systems are examined. The issue of VSC filter resonance is introduced and a review of resonance damping techniques is presented.

2.1 Review of Symmetrical Components

One of the most influential papers on the topic of power systems was written by Charles Fortescue in 1918 [1]. In this paper, a method of representing an unbalanced polyphase system by the summation of balanced polyphase systems was presented. The symmetrical components theory provides an analytical and consistent way to treat unbalanced three-phase systems. According to this theory, any three-phase system may be decomposed into three balanced systems with a positive, negative, and zero sequence [2]. The sequence components of a three-phase set of signals are depicted in the phasor diagram of Figure 2.1.

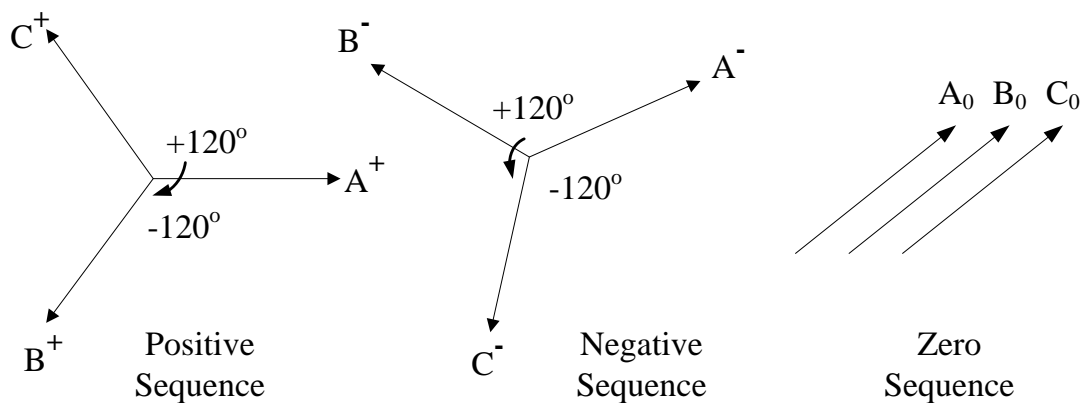


Figure 2.1: Symmetrical Sequence Components

For a set of three-phase sinusoidal signals f_{abc} defined in phasor form by (2.1).

$$f_{abc} = \begin{bmatrix} F_a \angle \theta_a \\ F_b \angle \theta_b \\ F_c \angle \theta_c \end{bmatrix} \quad (2.1)$$

The positive (f^+), negative (f^-), and zero (f^0) sequence phasor components for phase A are calculated by (2.2).

$$\begin{bmatrix} f_a^0 \\ f_a^+ \\ f_a^- \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} F_a \angle \theta_a \\ F_b \angle \theta_b \\ F_c \angle \theta_c \end{bmatrix}, \quad a = 1 \angle 120^\circ \quad (2.2)$$

The transformation matrix in (2.2) includes a complex number a which has magnitude of 1 and phase angle of 120° . The phase B and C values of the positive, negative, and zero sequence components have the same magnitude as their respective phase A quantities, and a phase shift defined according to Figure 2.1. The sum of the positive negative and zero sequence components is equal to the original three-phase quantities (2.3).

$$f_{abc} = f_{abc}^+ + f_{abc}^- + f_{abc}^0 \quad (2.3)$$

$$\begin{bmatrix} F_a \angle \theta_a \\ F_b \angle \theta_b \\ F_c \angle \theta_c \end{bmatrix} = \begin{bmatrix} F^+ \angle \theta^+ \\ F^+ \angle \theta^+ - 120^\circ \\ F^+ \angle \theta^+ + 120^\circ \end{bmatrix} + \begin{bmatrix} F^- \angle \theta^- \\ F^- \angle \theta^- + 120^\circ \\ F^- \angle \theta^- - 120^\circ \end{bmatrix} + \begin{bmatrix} F^0 \angle \theta^0 \\ F^0 \angle \theta^0 \\ F^0 \angle \theta^0 \end{bmatrix}$$

Under balanced conditions, a three-phase system will only contain a positive sequence component, and f_{abc}^- and f_{abc}^0 in (2.3) will be zero. Because the zero sequence component is defined as the sum of all three-phase values it is clear that there can be no zero sequence current in a three-phase, three-wire system. If a four-wire connected is used, then it is possible to have a non-zero zero sequence component. Equation (2.3) shows that the compensating current should be made to equal the negative sequence of the load current to achieve phase balancing. Although (2.2) gives the definition for the negative sequence current, all the terms are expressed as steady-state phasor representations. For a real-time control process, time domain quantities are required. Fortescue's method can also be applied to real-time transient signals when Instantaneous Symmetrical Components (ISC) theory is used to represent time-domain signals [3].

Symmetrical components theory is also a powerful tool for calculating power in unbalanced networks. For a three-phase, three-wire network, the instantaneous power can be calculated as the sum of the instantaneous line to ground voltages V multiplied by the line currents I , as in (2.4)

$$p(t) = VI, \quad (2.4)$$

$$V = [v_a(t) \quad v_b(t) \quad v_c(t)], \quad I = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$

Applying ISC theory, V and I can be represented by the positive and negative sequence components, and (2.4) can be rewritten as (2.5).

$$p(t) = (V^+ + V^-)(I^+ + I^-) \quad (2.5)$$

$$p(t) = (V^+I^+ + V^-I^-) + (V^-I^+ + V^+I^-)$$

In (2.5), V^+ and V^- are row vectors of the sinusoidal positive and sequence voltages with amplitude v^+ and v^- respectively, phase angles θ^+ and θ^- , and frequency ω . I^+ and I^- are column vectors of the positive and sequence currents respectively, with amplitudes i^+ and i^- , and phase angles θ_i^+ and θ_i^- . If θ^+ is taken as the reference, and hence it is equal to zero, the total three-phase instantaneous power can be expressed by (2.6).

$$p(t) = \frac{3}{2} \left(v^+ i^+ \cos(-\theta_i^+) + v^- i^- \cos(\theta^- - \theta_i^-) \right) + \quad (2.6)$$

$$\frac{3}{2} \left(v^+ i^- \cos(2\omega t + \theta_i^-) + v^- i^+ \cos(2\omega t + \theta^- + \theta_i^+) \right)$$

The instantaneous power $p(t)$ in (2.6) consists of a DC component, and an AC oscillating component. The frequency of the AC component is equal to twice that of the line frequency. Under balanced conditions, i.e. there are only positive sequence quantities, the instantaneous three-phase power is a DC quantity. If the voltage V is balanced, i.e. v^- is equal to zero, the instantaneous power in (2.6) becomes (2.7).

$$p(t) = \frac{3}{2} \left(v^+ i^+ \cos(-\theta^+) \right) + \frac{3}{2} \left(v^+ i^- \cos(2\omega t + \theta_i^-) \right) \quad (2.7)$$

From (2.7) it is clear that when the voltage is balanced, the negative sequence current contributes to the instantaneous power but with zero average component. Thus it does not contribute to the real power transfer. The magnitude of the ripple in the instantaneous power depends on the amplitude of the negative sequence current and positive sequence voltage. Because injecting negative sequence current component does not consume real power when the voltage is balanced, devices with no generation are able to provide negative sequence current compensation.

Since both voltage and current can be unbalanced in a three-phase system, there are two approaches to balancing a system: current balancing and voltage balancing. If the feeder impedance and the source voltages are balanced, then balancing the current will also lead to a balanced voltage. If the line impedance or source voltage is unbalanced, compensating the negative sequence load current may not eliminate the negative sequence load voltage. Likewise, balancing the load voltage will balance the current drawn from the source if the line impedance and source voltages are symmetrical. Compensating the negative sequence load voltage may not eliminate the negative sequence current supplied by the grid if the source voltage and impedance is unbalanced.

2.2 Calculation of Symmetrical Components for Control Applications

A well-known technique for generating the orthogonal components needed to calculate instantaneous symmetrical components is to use All Pass (AP) filters [4]-[6]. The transfer function of a first order AP filter is given in (2.8) where ω_0 is the fundamental grid frequency.

$$AP(s) = \frac{\omega_0 - s}{\omega_0 + s} \quad (2.8)$$

Equation (2.8) has a unity gain over the entire frequency spectrum, and introduces a -90° phase shift for signals at the frequency ω_0 . The frequency response when the filter is centered at 60 Hz is shown in Figure 2.2.

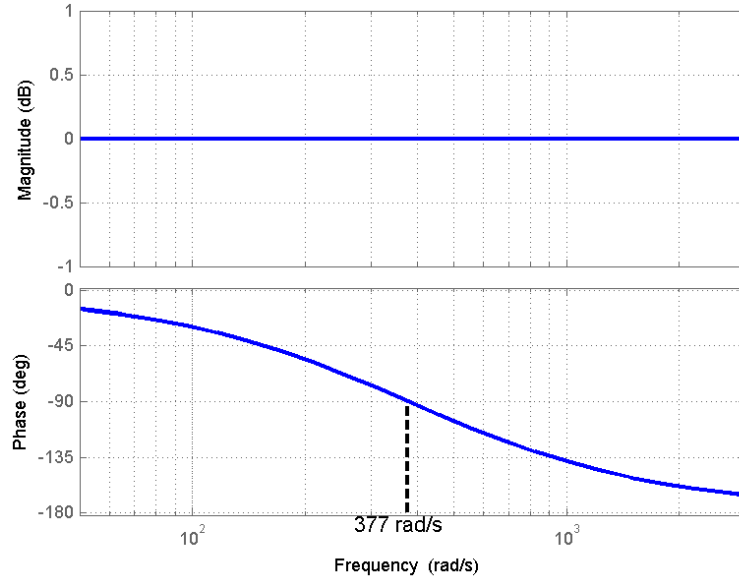


Figure 2.2: Frequency response of a 1st order AP filter

From the frequency response it is clear that an AP filter does not alter the amplitude of the input signal. If the frequency of the input signal varies, the time constants of the filter must be adjusted accordingly to ensure exact phase shift. This method however, has the advantage of being straightforward and computationally inexpensive [5].

In [6] the signals processed by the AP filters are used to compute the positive sequence quantities, although the same technique can be used to calculate the negative sequence. Figure 2.3 shows only the positive sequence case. This figure essentially shows implementation of the positive sequence portion of (2.2) using AP filters to create appropriate phase shifts.

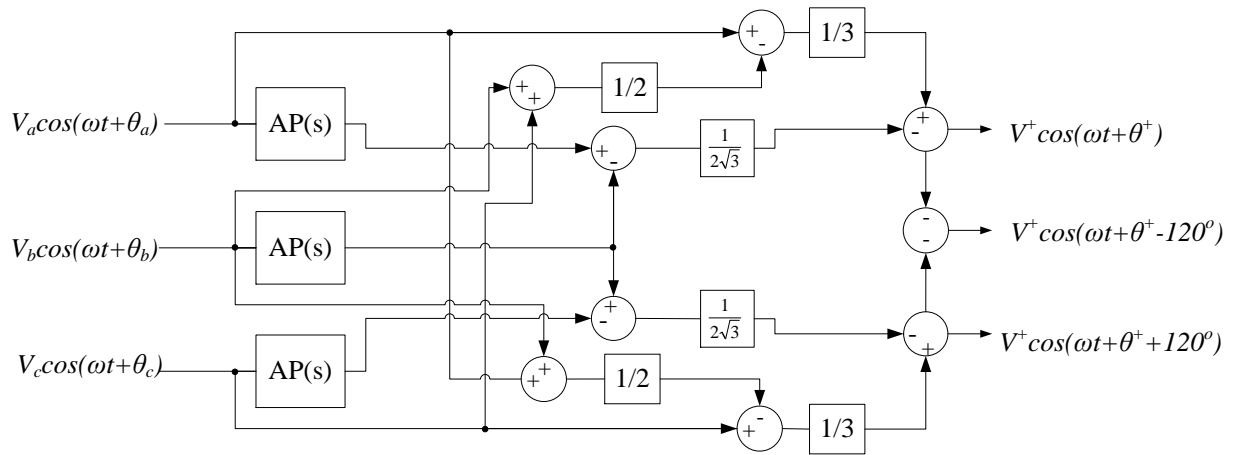


Figure 2.3: Symmetrical component calculation using AP filters [5]

The block diagram in Figure 2.3 computes the instantaneous positive sequence components with amplitude V^+ and phase angle of θ^+ from the three-phase sinusoidal input signals with amplitude V_{abc} and phase θ_{abc} .

Another technique to calculate the ISC is the Dual Second Order Generalized Integrator (DSOGI) method [7]. The building block of the DSOGI filter is a Second Order Generalized Integrator (SOGI) block, shown in figure 2.4.

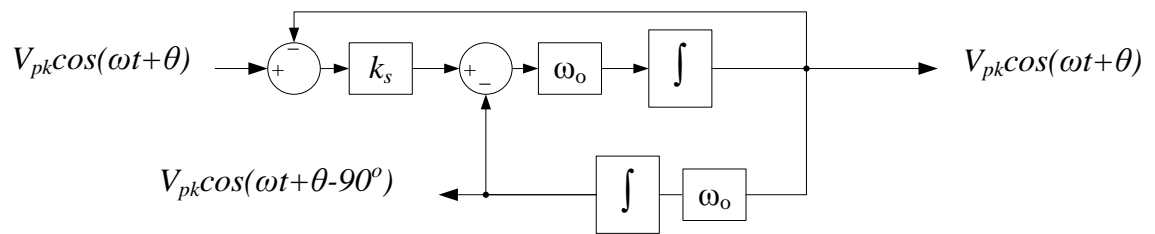


Figure 2.4: Second order generalized integrator block diagram [8]

The SOGI filter shown in Figure 2.4 has a unity gain and zero phase shift at the resonant frequency ω_0 , and less than unity gain at all other frequencies. The SOGI essentially acts as a resonant filter at the frequency ω_0 . This gives the DSOGI an advantage over AP filters due to superior harmonic filtering. When a sinusoidal input signal with frequency $\omega = \omega_0$ is passed through the SOGI block, the outputs are a sinusoid with the same amplitude and phase as the input, and a sinusoid with the same amplitude but with 90° phase lag compared to the input signal. In Figure 2.4 k_s is a constant which affects the transient response of the filter.

The symmetrical components can be calculated in the orthogonal (alpha-beta) reference frame as shown in Figure 2.5 [7]. First, three-phase sinusoidal input, $v_{abc}(t)$, is transformed into alpha-beta axis quantities $v_\alpha(t)$ and $v_\beta(t)$, respectively, via the Clarke transformation. Next, the $v_\alpha(t)$ and $v_\beta(t)$ quantities are processed by an SOGI block which provides the 90° phase shift to the input signal, denoted by the imaginary operator j . Finally, the positive sequence values $v_\alpha^+(t)$ and $v_\beta^+(t)$ are obtained as shown in Figure 2.5. The ABC frame positive sequence output can be obtained by applying the inverse Clarke transformation to the outputs of the DSOGI shown in Figure 2.5, $v_\alpha^+(t)$ and $v_\beta^+(t)$. The negative sequence α - β quantities can also be calculated using the same structure as shown in Figure 2.5 as long as the Clarke transformation follows the negative sequence direction.

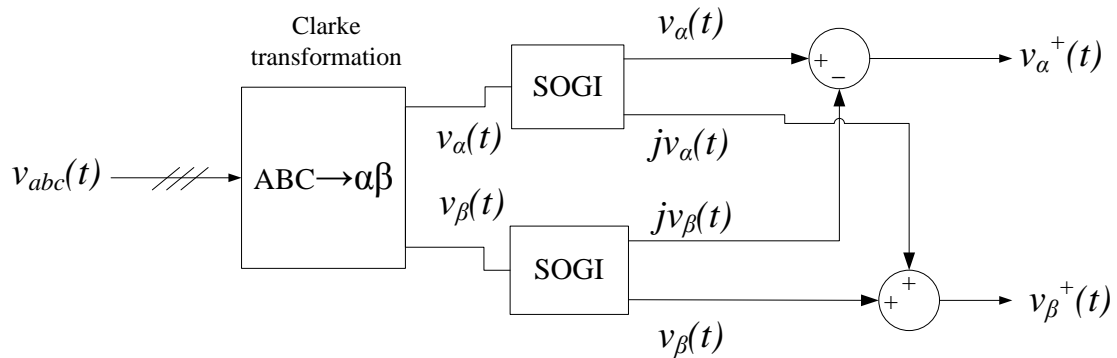


Figure 2.5: Positive sequence calculation in the $\alpha\beta$ frame

The DSOGI method offers improved harmonic rejection compared to the AP filter method but it requires designing the SOGI filter gain k_s to avoid either high oscillations in the output or unacceptably slow transient response. Adaptive Notch Filters (ANFs) are proposed in [9],[10] and have similar performance to the DSOGI method of [7]. The structure of an ANF is similar to that of the SOGI with an additional integral term used to estimate the frequency of the input signal and “adaptively” adjust the filter resonant frequency. Despite the frequency adaptive loop, ANF techniques have little advantage over the DSOGI in [7] for applications where the negative sequence current must be calculated. Improving the harmonic rejection can be obtained at the expense of increased settling time [9].

Synchronous Reference Frame (SRF) control dominates the academic literature on three-phase power electronic converters. Several authors have proposed methods of sequence extraction which take advantage of the properties of SRF quantities [8], [11]. A Dual

Synchronous Reference Frame (DSRF) structure for calculating sequence components in the rotating reference frame is presented in [11], [12]. The unbalanced signal is converted to the synchronous reference frame using both a positive and negative rotary angle. A decoupling network which combines the outputs of the two reference frames to remove the effect of cross-coupling between the positive and negative sequence components using a low pass filter is proposed in [12]. The dynamic response of the decoupling network is complicated to analyze and strongly depends on the cut-off frequency of the low-pass filters. A response time comparable to that of the SOGI based methods [7] can be obtained with the DSRF method. However, since there is no harmonic attenuation, band-pass filters must be used in conjunction with DSRF decoupling if the input signal is distorted. The need for additional filtering increases both the complexity of the DSRF and the transient response time.

A fast sequence component detector for SRF signals is proposed in [13]. This method uses differentiation of the d and q axis components along with some algebraic manipulation to remove the 2nd harmonic oscillation from the unbalanced dq components. Time derivation results in excessive noise so Savitzky-Golay filters are used for smoothing. Unlike the technique proposed in [12] only one synchronous reference transformation is required to calculate either the positive or negative sequence. Although a fast settling time can be obtained ($\sim 1/4$ cycle), the high level of noise at the output, renders this algorithm ill-suited for control applications.

Variations on the Least Error Squared (LES) method of phasor calculation combined with ISC have been proposed in [3] and [14] to determine the sequence components. A suitable frequency response with a short sampling window is obtained by sampling and computing the phasors at a very fast rate (10 kHz). The frequency response of a 50 sample LES filter sampling at 10 kHz shows, however, that there is still poor attenuation and amplification of harmonics [14]. Use of the Discrete Fourier Transform (DFT) has been reported in [15],[16] for calculating the positive sequence components of the fundamental and harmonic of the load currents. The control structure in [15] is shown to result in shorter computation time than a comparable synchronous reference frame controller, but the system frequency is assumed to be constant. In a microgrid, however, low system inertia can cause large frequency deviations compared with the main grid. Thus, the method of sequence extraction implemented in the control system of a DG unit must be resilient to frequency variations.

In all the methods of negative sequence calculation mentioned above there is a trade-off between the speed of response and the settling time/steady state oscillations. SRF sequence extraction techniques require computationally intensive variable transformations and are less attractive for control structures based in the stationary frame. For the control structure proposed in this thesis, the sequence calculation algorithm is required to be suitable for online calculation, have a short response time, and be robust against adverse grid conditions such as harmonic distortion and off-nominal frequencies. The numerically compensated, half-cycle DFT method proposed in this thesis is further discussed in Chapter 4.

2.3 Review of Compensating Devices

Although ideally all loads connected to a three-phase grid would be balanced, asymmetrical loading is inevitable in practical situations where different loads are connected to different phases. In cases where severe unbalance cannot be eliminated, some form of compensation may be required. Passive load balancing by means of passive inductive and capacitive elements was one of the earliest methods proposed [17]. The principle of passive load balancing is to connect a reactive admittance network in parallel with the load [17]. The combined admittance of the load and the reactive admittance network should be purely real and balanced [18]. Figure 2.6 illustrates this concept. The load is modelled as a resistor R_{ab} connected between phases A and B. The compensating network consists of a capacitor and an inductor connected between phases B and C, and phases C and A respectively, which yields an equivalent balanced wye connected load when the voltages are balanced. Because only reactive elements are used, no real power is consumed by the compensating network.

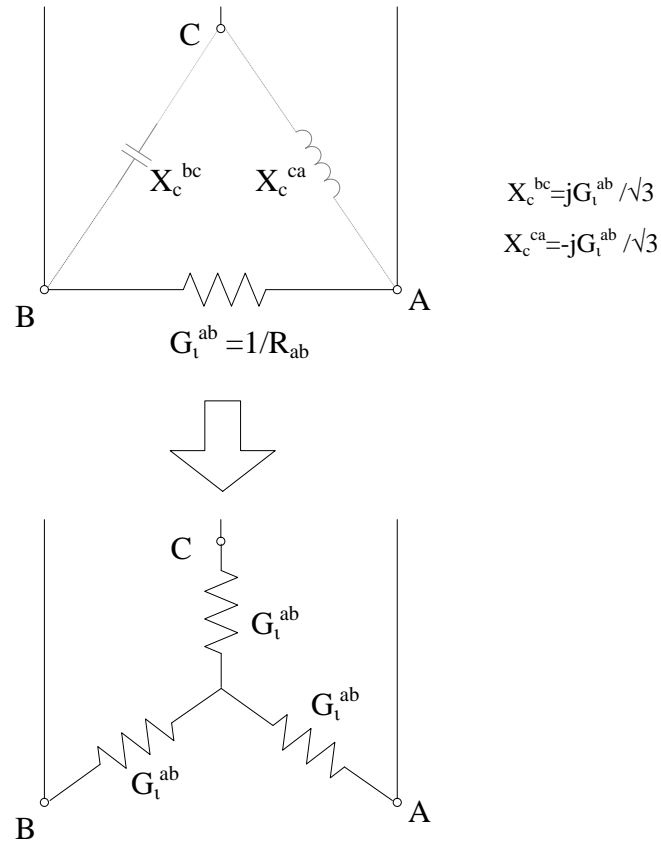


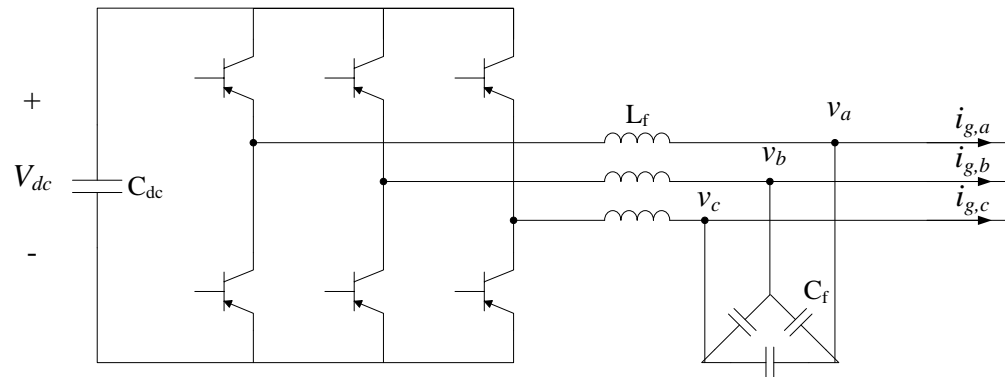
Figure 2.6: Passive balancing network [17]

Passive compensation techniques are limited to compensating fixed loads, and perform poorly in the presence of load variations. In addition to introducing unwanted resonance in the system, passive compensators can be overloaded during voltage transients due to their lack of inherent current limiting capabilities [19].

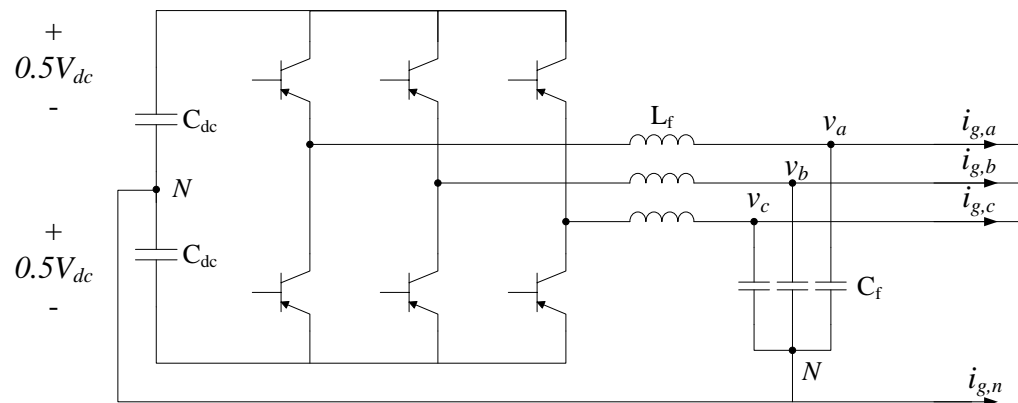
With the advent of solid-state power electronics, there has been great interest in voltage and current compensation devices based on the inverter topology. A great deal of literature is available on so-called Active Power Filters (APFs), which have been proposed to compensate varying unbalanced loads and harmonic distortion [19]-[27]. APFs compensate load unbalance and harmonics by injecting the negative sequence and harmonic currents consumed by the load. APFs can produce fast dynamics and can compensate rapidly varying loads. The three-phase shunt-connected Current Source Converter (CSC) is proposed in [20] to compensate negative sequence load currents.

Voltage Source Converters with either a three or four-wire configuration have been proposed as well [21]-[24]. The VSCs shown in Figure 2.7 can be connected either in series with the

load or in shunt. Series connected devices inject a voltage in the line to achieve the desired voltage at either the load or the grid side. Shunt connected devices inject current $i_{g,abc}$ into the network. The neutral point N is created in the four-wire converter in Figure 2.7(b) by splitting the DC link capacitor, C_{dc} , in two. L_f and C_f are passive filter elements used to reduce the harmonic content of the inverter voltage and current respectively.



(a)



(b)

Figure 2.7: (a) Three-wire and (b) four-wire voltage source converters

It should be noted that a three-wire VSC cannot compensate zero sequence current or voltage components for the reasons discussed in Section 2.1. In [27], to overcome this limitation, a zig-zag transformer is connected in parallel with a three-wire shunt APF. The zig-zag transformer provides a path for the zero sequence load current, while the APF is tasked with compensating negative sequence and harmonic currents.

A Static Synchronous Compensator (STATCOM) is a voltage control device based on the same VSC topologies shown in Figure 2.7, which provides dynamic reactive power support. A STATCOM injects/absorbs current by controlling the terminal voltage of the STATCOM to produce the needed phase shift and amplitude difference between the grid voltage and the terminal voltage of the STATCOM. In this way a STATCOM can inject/absorb reactive power without the need for large inductors or capacitors. The reactive elements in Figure 2.7 are used for filter purposes only. Although primarily for voltage support, STATCOMs have also been reported for load balancing applications [28]-[33].

A 30 kVA distribution level STATCOM is proposed in [28] to improve the operation of a Diesel generator set by balancing the load current. A relatively large 10,000 μF DC link capacitor is used to reduce the DC voltage ripple. An additional gain in the switching function is included in [29] to reduce the impact of DC link voltage ripple due to negative sequence compensation on current distortion, and to enable a smaller DC link capacitor to be used. Reference [30] presents a control strategy for combined balancing of either the load current or the voltage using a STATCOM. Voltage balancing rather than current compensation is described in [31],[32]. In [33] a 50 MVA STATCOM is presented along with coordinated control of positive and negative sequence voltage. The STATCOM is used to reduce wind turbine torque ripple during unbalanced faults. Priority, however, is given to positive sequence voltage control, rather than eliminating the negative sequence components.

Another class of power system compensation devices, Dynamic Voltage Restorers, can be used to improve voltage quality for sensitive loads by reducing voltage sags, swells, and harmonics [4], [14], [34]-[36]. A DVR topology is shown in Figure 2.8 which consists of a passive filter, a series connected VSC and a DC link capacitor, and a rectifier to provide power to the DC link capacitor [14].

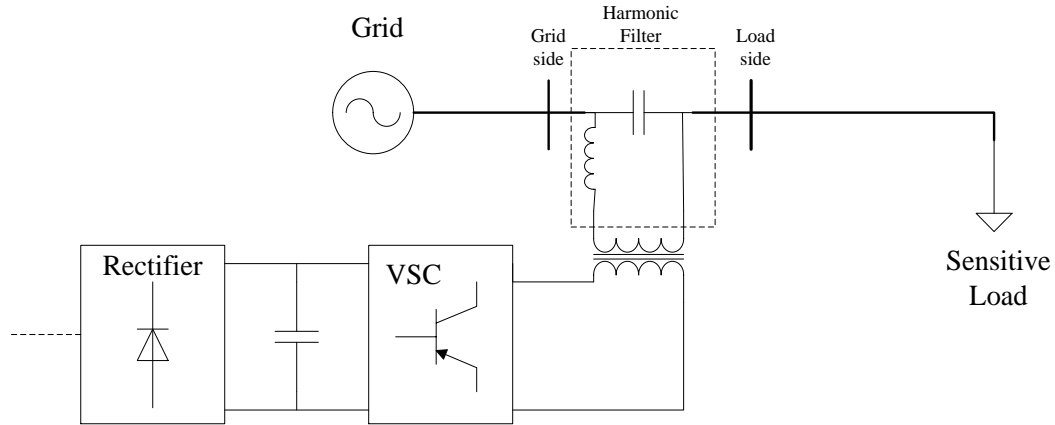


Figure 2.8: A DVR with line-side Harmonic filter [14]

With an appropriate control strategy the DVR depicted in Figure 2.8 can also compensate unbalanced voltage variations on the load side. In [14] the authors propose a control scheme based on LES filters to determine the amplitude and phase angles of the measured load and grid voltage. Phasor subtraction is used to determine the necessary voltage injected in the line. The presented results show that the DVR is able to compensate short term voltage unbalances even in the presence of distorted load currents.

The DVR structure presented in [35] uses two inverters connected in cascade through an open end winding transformer. Either an energy storage system or an auxiliary power supply is required at the DC link of each inverter to provide power to the DVR. In [34] a DVR topology is proposed which eliminates the DC link energy storage element. A shunt connected three-phase inverter is connected to the DC link of the DVR directly to provide power to the device, which is able to compensate unbalanced voltage swells and sags. Although they can provide voltage balancing, DVRs cannot provide current balancing, because they are connected in series with the load, unlike APFs and STATCOMs, which typically utilize a shunt connection.

2.4 Review of Dual Purpose PV Systems

Because PV power production fluctuates based on the time of day and weather conditions, it is almost guaranteed that the inverter's designed capacity for PV power conversion is under-utilized. In light of this, many authors have proposed using the excess converter capacity for various voltage/power quality improvement applications [37]-[50]. A novel converter

topology combining a PV generator with a DVR is presented in [43]. In [48], [49], PV inverters are operated as STATCOMs to support grid voltage.

In [38]-[40] single phase inverters have been used as active power filters for reducing current distortion and power factor correction. A method of reducing voltage unbalance in a distribution system with a high level of single phase PV generators has been discussed in [41] and [42]. If the system has a high R/X ratio it may require real power curtailment.

Shahnia *et al.* describe a compensating current reference calculation method for a 6 leg inverter in a microgrid [51]. A Fuel Cell is used as the source for the converter. The controller must switch between different modes to calculate the compensating current depending on whether the non-linear or unbalanced load is greater or less than rated output of the FC. Unbalanced load compensation using three-phase PV converters has been discussed in [37], [44]-[47], [50], [52]-[54]. Dual-stage topologies are considered in [37], [44], [46], [52], [53]. A dual-stage converter limits the impact that the DC link voltage oscillation has on the output of the PV array because the PV array is connected to the DC link by a DC-DC converter. A study of different PV converter configurations performing phase balancing and APF duties is reported in [46], but only dual-stage topologies are included for comparison.

Single-stage converter topologies for phase balancing are reported in [45], [47], [50], [54]. In [45] a notch filter is used to extract the fundamental in-phase component of the load current to be used as the grid current reference. Both [45] and [54] use the grid voltage to generate sinusoidal reference signals. However, unbalanced or distorted supply voltages will negatively impact the performance of the controller. The single-stage PV inverter control scheme proposed in [47] directly adds the measured load current to the current reference rather than just the negative sequence load current. In the presence of non-linear loads this approach can cause harmonic distortion in the inverter current. Neither [47] nor [45] discuss issues of resonance damping for the LCL filter used in the converter. In [50] a control scheme for a VSC fed by a renewable energy source is proposed to improve power quality in a distribution system. The grid current is controlled without the need for additional sensing of the inverter or load currents. The control scheme, however, is developed for a generic renewable source and the particular characteristics of a PV array have not been considered.

2.5 LCL Filter Resonance Damping

Current harmonics in power systems can cause interference with communications systems, increased losses and heating of electromagnetic equipment, and voltage distortion [55]. IEEE standard 519-2014 requires the total demand distortion of the current injected by all power generation equipment to be less than 5% [55]. The PWM switching scheme used by the inverter produces high order harmonics at the carrier and side-band frequencies which must be removed to comply with IEEE Std. 519-2014. LCL filters are used to remove the higher order switching harmonics in the inverter output voltage and to reduce current distortion. The LCL configuration, depicted in Figure 2.9, has an inverter-side filter inductor, L_c , a grid-side filter inductor L_g , and a filter capacitor, C_f . This configuration allows smaller values of inductance to be used compared to single order filter, which can improve the power factor and decrease power losses [56]. One design trade-off is, however, the presence of a resonance peak in the filter frequency response. If the resonance is not damped the control bandwidth must be limited to well below this resonance point. This imposes a severe restriction on the speed of the controller response. If the control bandwidth is not properly limited instability may occur. In Figure 2.9 i is the inverter-side current, i_c is the current flowing through the filter capacitor, and i_g is the current injected into the grid. The equivalent grid inductance and resistance is L_{gr} and r_{gr} respectively. v_{inv} is the voltage at the inverter terminals, and v_g is the voltage at the point of common coupling to the grid.

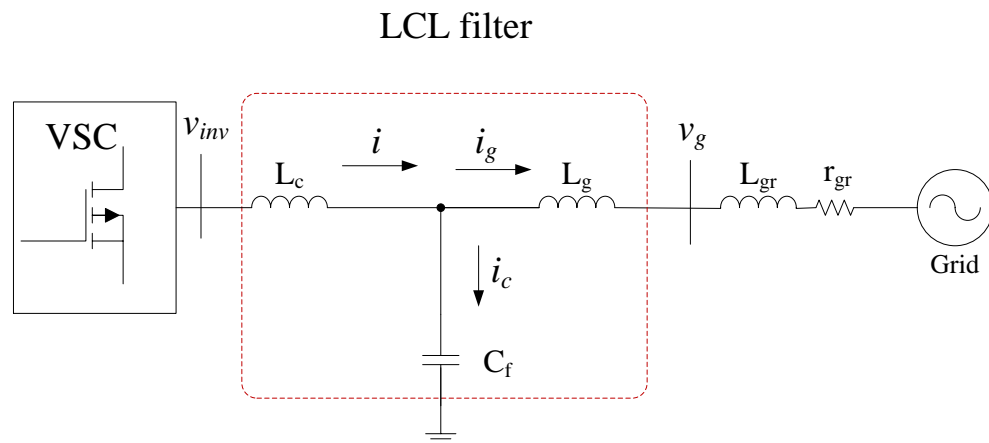


Figure 2.9: Single line diagram of a VSC with an LCL filter

The resonance issue has been examined in the literature and a number of solutions have been proposed [56]-[60]. These methods can be classified as either passive or active techniques, based on whether they involve additional physical components in the filter or alterations to the inverter control structure respectively. Passive damping methods require insertion of additional resistive elements in the filter [58], [61]. Figure 2.10 illustrates a passive damping approach. The resistive element R_{damp} is inserted in series with the AC filter capacitor C_f [58]. The advantages of passive damping include high reliability and lower control complexity [61]. However the damping elements consume real power which effectively decreases the inverter efficiency. Variations in the filter parameters can also lead to non-optimal damping which cannot be adaptively compensated.

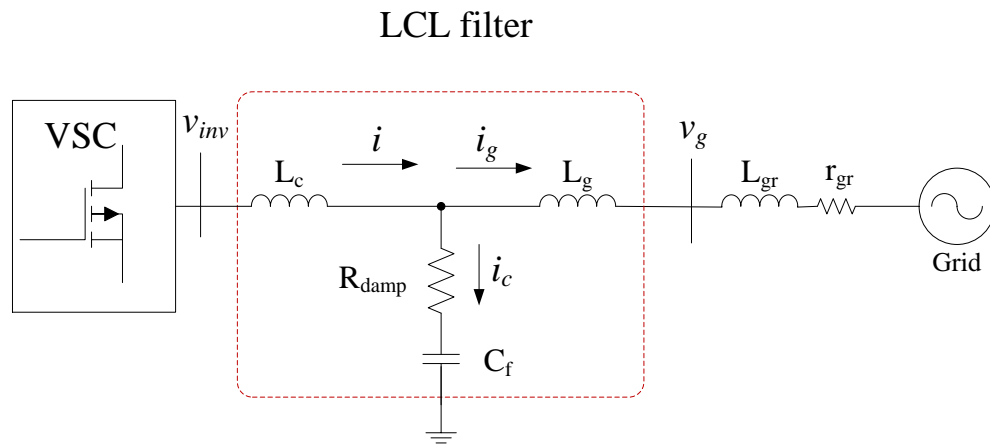


Figure 2.10: Passive damping of an LCL filter

Much of the literature is focused on active damping techniques which dampen the filter resonance without adding physical components to the filter. Although active damping requires additional sensors and a more complex control scheme, it offers a lossless solution to the resonance problem. An active damping method is proposed in [59] which avoids the resonance problem by controlling a weighted average of i_g and i rather than i_g . This scheme is depicted in Figure 2.11.

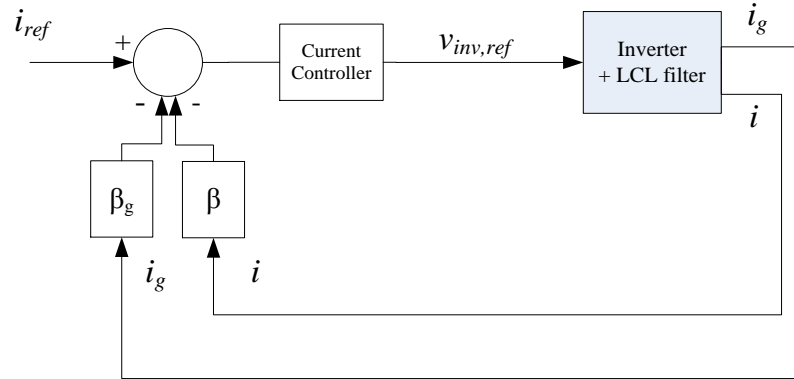


Figure 2.11: Weighted-average current control active damping

The current reference and inverter terminal voltage reference are denoted in Figure 2.11 by i_{ref} and $v_{inv,ref}$ respectively. By proper selection of the weighting gains, β_g and β , the equivalent LCL filter transfer function can be reduced from a third order to a first order function, which eliminates the resonance problem and simplifies the current controller gain design. However, using this method the current injected into the grid cannot be directly regulated.

Various digital filters have been proposed to dampen the resonant peak [62]-[64]. In [63] low-pass, lead-lag, and notch cascade filters are examined. A self-commissioning notch filter is proposed in [62] which is tuned based on the estimated resonant frequency. The performance of digital filter based active damping techniques can be highly sensitive to the accuracy of the filter parameters.

Virtual impedance is a multi-loop scheme which uses a proportional feedback loop to dampen the resonance [57], [60], [65]-[67]. The damping variable, x_{damp} , is multiplied by the gain K_d and subtracted from the output of the current controller, as shown in Figure 2.12. The feedback variable x_{damp} can either be the filter capacitor current, voltage, or the inverter-side current. The feedback variable may be physically measured [60] or mathematically estimated [68].

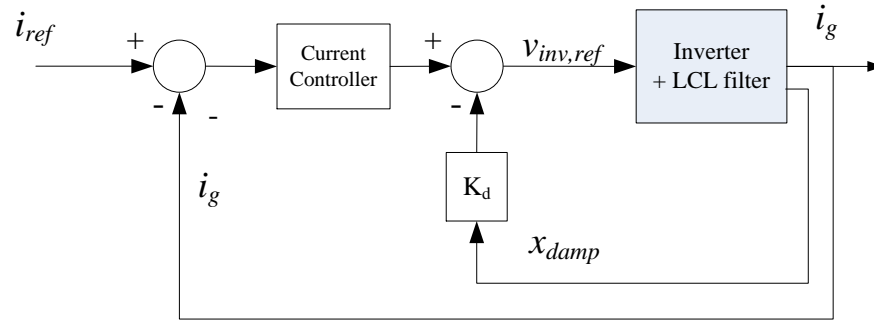


Figure 2.12: Virtual impedance damping

If the feedback variable is the inner inductor current, i , it is the equivalent of adding a resistor in series with the inner inductor. If the capacitor current is used, the virtual resistance is effectively in series with the filter capacitor [57]. A physical resistor damps resonance by dissipating energy to limit the oscillating energy transfer between the filter components whereas the virtual impedance absorbs “control energy” by reducing the control effort. The capacitor voltage is filtered by a lead-lag network and subtracted from the inverter voltage reference in [69],[70]. A hybrid method is proposed in [71] which incorporates both passive damping and capacitor current based active damping to provide robustness against component variations.

Of the possible feedback variables, capacitor current i_c is most commonly employed in the literature [57], [60], [65]-[67], [72]. The capacitor current can either be directly measured or can be calculated from the i_g and i . Wang *et. al* [72] investigate design considerations for an LCL filter as well as proper control parameter selection when an active damping scheme with capacitor current is employed. In [66] the authors use a combination of proportional and discretely implemented derivative capacitor current feedback. The authors of [66] derive an analytical discrete time open-loop optimization to calculate the required feedback gains as well as a numerical closed-loop solution which accounts for the closed-loop controller dynamics. A comparison of different two-loop damping variables has also been conducted in [65]. The results show that when the inverter-side current i is used as the damping variable, the control loop has better rejection of DC components in the controller output but at the cost of a slower transient response compared to using i_c for the damping feedback.

2.6 Summary

Many methods of calculating negative sequence components have been reported in the literature for both the ABC and rotating reference frame. Most have either high sensitivity to noise and harmonics or a slow transient response. The method which is used to calculate the compensating reference current can have a pronounced impact on the performance of the control scheme. In order to avoid deterioration of the system performance due to the negative sequence compensation loop, the sequence extraction algorithm must be impervious to harmonics, noise, and variations in the grid frequency.

Although dual-purpose PV systems have been previously reported, most of the control schemes are not suitable for a converter with an LCL filter. If a higher order filter is used an active damping scheme must be employed to enable control of the grid-side current. Virtual impedance active damping schemes have been shown to meet the requirement of good robustness to variations in the filter inductance without additional power loss in the filter. The choice of feedback variables for virtual impedance active damping schemes affects the performance. A fast transient response can be obtained when capacitor current is used. Using the inner inductor current results in better rejection of DC and low frequency harmonics in the controller output than when capacitor current feedback is used, but has a slower transient response.

Very little research has been reported on the effect of phase balancing on PV systems with single-stage configurations. For a single stage PV converter, variations in the DC link voltage will affect the efficiency of the power conversion. Hence, there is a need to examine the ability of the PV systems to compensate negative sequence load current under various conditions.

2.7 References

- [1] C.L. Fortescue, "Method of Symmetrical Co-Ordinates Applied to the Solution of Polyphase Networks," *Trans. Amer. Inst. of Elect. Eng.*, vol.37, no.2, pp.1027-1140, July 1918.
- [2] J.D. Glover, M.S. Sarma and T.J. Overbye, *Power system analysis and design*, 4th ed. Toronto, Ont., Thomson: 2008.

- [3] G. Chen, L. Zhang, R. Wang L. Zhang and X. Cai, "A Novel SPLL and Voltage Sag Detection Based on LES Filters and Improved Instantaneous Symmetrical Components Method," *IEEE Trans. Power Electron.*, vol.30, no.3, pp.1177-1188, Mar. 2015
- [4] A. O. Ibrahim, T. H. Nguyen, D. Lee and S. Kim, "A Fault Ride-Through Technique of DFIG Wind Turbine Systems Using Dynamic Voltage Restorers," *IEEE Trans. Energy Convers.*, vol. 26, pp. 871-882, Sept. 2011.
- [5] M. Karimi-Ghartemani, and M.R. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," *IEEE Trans. Power Syst.*, vol.19, no.3, pp.1263-1270, Aug. 2004.
- [6] S. Lee, J. Kang and S. Sul, "A new phase detecting method for power conversion systems considering distorted conditions in power system," in *Proc. 34th Annu. Meet. IAS Indus. Applicat. Conf.*, 1999, vol.4, pp.2167-2172.
- [7] N. Hoffmann, R. Lohde, M. Fischer, F.W. Fuchs, L. Asiminoaei and P.B. Thogersen, "A review on fundamental grid-voltage detection methods under highly distorted conditions in distributed power-generation networks," *Energy Convers. Congr. and Exposition, 2011*, pp.3045-3052.
- [8] F.J. Rodríguez, E. Bueno, M. Aredes, L.G.B. Rolim, F.A.S. Neves and M.C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," in *Proc. 34th Annu. Conf. Ind. Electron. Soc.(IECON)*, 2008, pp.176-181.
- [9] D. Yazdani, M. Mojiri, A. Bakhshai and G. Joos, "A Fast and Accurate Synchronization Technique for Extraction of Symmetrical Components," *IEEE Trans. Power Electron.*, vol.24, no.3, pp.674-684, Mar. 2009.
- [10] M. Mojiri, M. Karimi-Ghartemani and A. Bakhshai, "Estimation of Power System Frequency Using an Adaptive Notch Filter," *IEEE Trans. Instrum. Meas.*, vol.56, no.6, pp.2470-2477, Dec. 2007.
- [11] P. Xiao, K.A. Corzine and G.K. Venayagamoorthy, "Multiple Reference Frame-Based Control of Three-Phase PWM Boost Rectifiers under Unbalanced and Distorted Input Conditions," *IEEE Trans. Power Electron.*, vol.23, no.4, pp.2006-2017, July 2008.
- [12] P. Rodriguez, J. Pou, J. Bergas, J.I. Candela, R.P. Burgos and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *IEEE Trans. Power Electron.*, vol.22, no.2, pp.584-592, Mar. 2007.
- [13] J. Restrepo, J. Viola, F. Quizhpiand A. Ginart, "Fast detection of sequence components using Savitzky-Golay filters," in *Proc. 40th Annu. Conf. Ind. Electron. Soc.(IECON)*, 2014, pp.4453-4457.

- [14] F. Badrkhani Ajaei, S. Afsharnia, A. Kahrobaeian and S. Farhangi, "A Fast and Effective Control Scheme for the Dynamic Voltage Restorer," *IEEE Trans. Power Del.*, vol.26, no.4, pp.2398-2406, Oct. 2011.
- [15] S. Orts-Grau, F. J. Gimeno-Sales, A. Abellán-García, S. Seguí-Chilet and J. C. Alfonso-Gil, "Improved Shunt Active Power Compensator for IEEE Standard 1459 Compliance," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2692-2701, Oct. 2010.
- [16] S. Chandrasekaran and K. Ragavan, "Sliding DFT assisted instantaneous symmetrical components method for estimating reference current to active power filter," in *IEEE 55th Int. Midwest Symp. on Circuits and Syst. (MWSCAS)*, 2012, pp. 1168-1171.
- [17] T.J.E. Miller, "The Theory of Load Compensation," in *Reactive Power Control in Electric Systems*, Toronto, Canada: Wiley, 1982, ch. 1, sec. 1.9, pp. 34-35.
- [18] R. A. Otto, T. H. Putman and L. Gyugyi, "Principles and Applications of Static, Thyristor-Controlled Shunt Compensators," *IEEE Trans. Power App. Syst.*, vol.97, no. 5, pp. 1935-1945, Sept. 1978.
- [19] R. Panigrahi, B. Subudhi and P. C. Panda, "Model predictive-based shunt active power filter with a new reference current estimation strategy," *IET Power Electron.*, vol. 8, no. 2, pp. 221-233, Feb. 2015.
- [20] V. B. Bhavaraju and P. N. Enjeti, "Analysis and design of an active power filter for balancing unbalanced loads," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 640-647, Oct. 1993.
- [21] F.Z. Peng, G.W. Ott Jr. and D.J. Adams, "Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for three-phase four-wire systems," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1174-1181, Nov. 1998.
- [22] G.W. Chang and C.M. Yeh, "Optimisation-based strategy for shunt active power filter control under non-ideal supply voltages," *IEE Proc. Elect. Power Applicat.*, vol. 152, no. 2, pp. 182-190, Mar. 2005.
- [23] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Battle, P. Roncero-Sanchez and P. Garcia-Gonzalez, "Application of a Repetitive Controller for a Three-Phase Active Power Filter," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 237-246, Jan. 2007.
- [24] R.L. de Araujo Ribeiro, C.C. de Azevedo and R.M. de Sousa, "A Robust Adaptive Control Strategy of Active Power Filters for Power-Factor Correction, Harmonic Compensation, and Balancing of Nonlinear Loads," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 718-730, Feb. 2012.
- [25] R. L. A. Ribeiro, J. F. Moreira, R. M. Souza and C. C. Azevedo, "A robust control strategy for regulating dc-link voltage of active power filter without load current

- measurements," in *Proc. 38th Annu. Conf. Ind. Electron. Soc.(IECON)*, 2012, pp. 156-161.
- [26] P. Kanjiya, V. Khadkikar and H. H. Zeineldin, "Optimal Control of Shunt Active Power Filter to Meet IEEE Std. 519 Current Harmonic Constraints Under Nonideal Supply Condition," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 724-734, Feb. 2015.
- [27] H. Jou, K. Wu, J. Wu and W. Chiang, "A Three-Phase Four-Wire Power Filter Comprising a Three-Phase Three-Wire Active Power Filter and a Zig-Zag Transformer," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 252-259, Jan. 2008.
- [28] B. Singh and J. Solanki, "Load Compensation for Diesel Generator-Based Isolated Generation System Employing DSTATCOM," *IEEE Trans. Ind. Applicat.*, vol. 47, no. 1, pp. 238-244, Jan. 2011.
- [29] B. Blazic and I. Papic, "Improved D-StatCom control for operation with unbalanced currents and voltages," *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 225-233, Jan. 2006.
- [30] Y. Xu, L. M. Tolbert, J. D. Kueck and D. T. Rizy, "Voltage and current unbalance compensation using a static var compensator," *IET Power Electron.*, vol. 3, no. 6, pp. 977-988, Nov. 2010.
- [31] K. Li, J. Liu, Z. Wang and B. Wei, "Strategies and Operating Point Optimization of STATCOM Control for Voltage Unbalance Mitigation in Three-Phase Three-Wire Systems," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 413-422, Jan. 2007.
- [32] S. M. Fazeli, H. W. Ping, N. Bin Abd Rahim and B. T. Ooi, "Individual-phase control of 3-phase 4-wire voltage-source converter," *IET Power Electron.*, vol. 7, no. 9, pp. 2354-2364, Sept. 2014.
- [33] C. Wessels, N. Hoffmann, M. Molinas and F. W. Fuchs, "StatCom control at wind farms with fixed-speed induction generators under asymmetrical grid faults," *IEEE Trans. Indust. Electron.*, vol. 60, no. 7, pp. 2864-2873, July 2013.
- [34] E. Babaei and M. F. Kangarlu, "Voltage quality improvement by a dynamic voltage restorer based on a direct three-phase converter with fictitious DC link," *IET Gener. Transm. Distrib.*, vol. 5, no. 8, pp. 814-823, Aug. 2011.
- [35] G. Carlos, E. dos Santos, C. Jacobina and J. Mello, "Dynamic Voltage Restorer Based on Three-Phases Inverters Cascaded Through an Open-End Winding Transformer," *IEEE Trans. Power Electron.*, Feb. 2015.
- [36] G. Chen, M. Zhu and X. Cai, "Medium-voltage level dynamic voltage restorer compensation strategy by positive and negative sequence extractions in multiple reference frames," *IET Power Electron.*, vol.7, no.7, pp.1747-1758, July 2014.

- [37] X. Wang, F. Zhuo, J. Li, L. Wang and S. Ni, "Modeling and Control of Dual-Stage High-Power Multifunctional PV System in $d - Q -$ Coordinate," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1556-1570, Apr. 2013.
- [38] T.J. Liang, Y.C. Kuo and J.F. Chen, "Single-stage photovoltaic energy conversion system," *IEE Proc. Electric Power Applicat.*, vol. 148, no. 4, pp. 339-344, July 2001.
- [39] T. Wu, H. Nien, H. Hsieh and C. Shen, "PV Power Injection and Active Power Filtering With Amplitude-Clamping and Amplitude-Scaling Algorithms," *IEEE Trans. Ind. Applicat.*, vol. 43, no. 3, pp. 731-741, May 2007.
- [40] S. Munir and Y.W. Li, "Residential Distribution System Harmonic Compensation Using PV Interfacing Inverter," *IEEE Trans. Smart Grid*, vol.4, no.2, pp.816-827, June 2013.
- [41] X. Su, M.A.S. Masoum and P.J. Wolfs, "Optimal PV Inverter Reactive Power Control and Real Power Curtailment to Improve Performance of Unbalanced Four-Wire LV Distribution Networks," *IEEE Trans. Sustain. Energy*, vol. 5, no. 3, pp. 967-977, July 2014.
- [42] X. Su, M.A.S. Masoum and P. Wolfs, "Comprehensive optimal photovoltaic inverter control strategy in unbalanced three-phase four-wire low voltage distribution networks," *IET Gener. Transm. Distrib.*, vol. 8, no. 11, pp. 1848-1859, Nov. 2014.
- [43] A.M. Rauf and V. Khadkikar, "Integrated Photovoltaic and Dynamic Voltage Restorer System Configuration," *IEEE Trans. Sustain. Energy*, vol. 6, pp. 400-410, Apr. 2015.
- [44] B. Singh, D.T. Shahani and A.K. Verma, "Neural network controlled grid interfaced solar photovoltaic power generation," *IET Power Electron.*, vol. 7, no. 3, pp. 614-626, Mar. 2014.
- [45] B. Singh, C. Jain and S. Goel, "ILST Control Algorithm of Single-Stage Dual Purpose Grid Connected Solar PV System," *IEEE Trans. Power Electron.*, vol.29, no.10, pp.5347-5357, Oct. 2014.
- [46] H. Patel and V. Agarwal, "Investigations into the performance of photovoltaics-based active filter configurations and their control schemes under uniform and non-uniform radiation conditions," *IET Renew. Power Gener.*, vol. 4, no. 1, pp. 12-22, Jan. 2010.
- [47] A. Elmitwally and M. Rashed, "Flexible Operation Strategy for an Isolated PV-Diesel Microgrid Without Energy Storage," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 235-244, Mar. 2011.
- [48] R. K. Varma, S. A. Rahman and T. Vanderheide, "New Control of PV Solar Farm as STATCOM (PV-STATCOM) for Increasing Grid Power Transmission Limits During Night and Day," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 755-763, Apr. 2015.

- [49] R. K. Varma, V. Khadkikar and R. Seethapathy, "Nighttime Application of PV Solar Farm as STATCOM to Regulate Grid Voltage," *IEEE Trans. Energy Convers.*, vol. 24, no. 4, pp. 983-985, Dec. 2009.
- [50] M. Singh, V. Khadkikar, A. Chandra and R.K. Varma, "Grid Interconnection of Renewable Energy Sources at the Distribution Level With Power-Quality Improvement Features," *IEEE Trans. Power Del.*, vol.26, no.1, pp.307-315, Jan. 2011.
- [51] F. Shahnia, R. Majumder, A. Ghosh, G. Ledwich and F. Zare. "Operation and control of a hybrid microgrid containing unbalanced and nonlinear loads." *Electric Power Syst. Res.*, vol. 80, no. 8, pp. 954-965, Aug. 2010.
- [52] A. Hamadi, S. Rahmani, K. Al-Haddad and Y. A. Al-Turki, "A three-phase three wire grid-connect photovoltaic energy source with sepic converter to track the maximum power point," in *Proc. 37th Annu. Conf. Ind. Electron. Soc.(IECON)*, 2011, pp. 3087-3092.
- [53] R. Noroozian, and G.B. Gharehpetian, "An investigation on combined operation of active power filter with photovoltaic arrays." *Int. J. Elect. Power & Energy Syst.*, vol. 46, pp. 392-399, Mar. 2013.
- [54] R.N. Tripathi, A. Singh and T. Hanamoto. "Design and control of LCL filter interfaced grid connected solar photovoltaic (SPV) system using power balance theory" *Int. J. Elect. Power & Energy Syst.*, vol. 69, pp.264-272, July 2015.
- [55] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," IEEE Std 519-2014 (Revision of IEEE Std 519-1992), pp.1-29, June 2014.
- [56] M. Liserre, F. Blaabjerg and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Applicat.*, vol.41, no.5, pp.1281-1291, Sept. 2005.
- [57] Y. Jia, J. Zhao and X. Fu, "Direct Grid Current Control of LCL-Filtered Grid-Connected Inverter Mitigating Grid Voltage Disturbance," *IEEE Trans. Power Electron.*, vol.29, no.3, pp.1532-1541, Mar. 2014.
- [58] T.C.Y. Wang, Z. Ye, G. Sinha and X. Yuan, "Output filter design for a grid-interconnected three-phase inverter," in *IEEE 34th Annu. Power Electron. Spec. Conf. (PESC)*. 2003, vol.2, pp.779-784.
- [59] N. He, D. Xu, Y. Zhu, J. Zhang, G. Shen, Y. Zhang, J. Ma and C. Liu, "Weighted Average Current Control in a Three-Phase Grid Inverter With an LCL Filter," *IEEE Trans. Power Electron.*, vol.28, no.6, pp.2785-2797, June 2013.
- [60] E. Twining and D.G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, vol.18, no.3, pp.888-895, May 2003.

- [61] W. Wu, Y. He, T. Tang and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter," *IEEE Trans. Ind. Electron.*, vol.60, no.10, pp.4339-4350, Oct. 2013.
- [62] R. Peña-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez and T. Kerekes, "A Self-commissioning Notch Filter for Active Damping in a Three-Phase LCL -Filter-Based Grid-Tie Converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6754-6761, Dec. 2014.
- [63] J. Dannehl, M. Liserre and F. W. Fuchs, "Filter-Based Active Damping of Voltage Source Converters With Filter" *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3623-3633, Aug. 2011.
- [64] J. Dannehl, C. Wessels and F. W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With Filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380-388, Feb. 2009.
- [65] M.S. Munir, J. He and Y.W. Li, "Comparative analysis of closed-loop current control of grid connected converter with LCL filter," in *Proc. IEEE Int. Electric Machines & Drives Conf.(IEMDC)*, 2011, pp. 1641-1646.
- [66] M. Wagner, T. Barth, R. Alvarez, C. Ditmanson and S. Bernet, "Discrete-Time Active Damping of LCL Filters by Proportional Capacitor Current Feedback," *IEEE Trans. Ind. Applicat.*, vol.50, no.6, pp.3911-3920, Nov. 2014.
- [67] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan and K. Weng, "Step-by-Step Controller Design for LCL-Type Grid-Connected Inverter with Capacitor–Current–Feedback Active-Damping," *IEEE Trans. Power Electron.*, vol.29, no.3, pp.1239-1253, Mar. 2014.
- [68] M. Malinowski and S. Bernet, "A Simple Voltage Sensorless Active Damping Scheme for Three-Phase PWM Converters With an Filter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1876-1880, Apr. 2008.
- [69] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," *IEEE Trans. Ind. Applicat.*, vol. 33, no. 2, pp. 542-550, Mar. 1997.
- [70] R. Pena-Alzola, M. Liserre, F. Blaabjerg, R. Sebastian, J. Dannehl and F. W. Fuchs, "Systematic Design of the Lead-Lag Network Method for Active Damping in LCL-Filter Based Three Phase Converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 43-52, Feb. 2014.
- [71] Y. Lei, W. Xu, C. Mu, Z. Zhao, H. Li and Z. Li, "New Hybrid Damping Strategy for Grid-Connected Photovoltaic Inverter With LCL Filter," *IEEE Trans. Appl. Supercond.*, vol. 24, pp. 1-8, Oct. 2014.
- [72] X. Wang, C. Bao, X. Ruan, W. Li and D. Pan, "Design Considerations of Digitally Controlled LCL-Filtered Inverter With Capacitor- Current-Feedback Active

Damping," *IEEE J. Emerg. Sel. Topics in Power Electron.*, vol. 2, pp. 972-984, Dec. 2014.

Chapter 3

3 Design and Analysis of the Control Strategy

In this chapter a stationary frame control scheme for the single stage PV inverter is presented. A typical two-loop structure is employed which consists of an outer DC link voltage loop and an inner current loop. The current control loop has been designed to enable the inverter to inject the required negative sequence compensation current into the microgrid.

Section 3.1 begins by modeling of the inverter with an LCL filter. Next, in Section 3.2, a virtual impedance Active Damping (AD) method is proposed to facilitate direct control of i_g rather than the inverter-side current i . A step-by-step method of explicitly calculating the PR and AD gains based on the inverter modeling is presented in Section 3.3. In Section 3.4, modifications to the standard PR controller are proposed to counteract resonator windup, which can potentially occur in single stage inverters due to low PV voltage. The DC link control strategy discussed in [1] is adopted for the proposed system in Section 3.5. A frequency-locked-loop is implemented to estimate the fundamental grid frequency in Section 3.6. In Section 3.7 an MPPT scheme based on the perturb-and-observe method is used to generate the reference for the DC link. An overall block diagram of the control scheme developed in Chapters 3 and 4 is shown in Figure 3.1.

The three-phase inverter shown in Figure 3.2 is a two-level, three wire, six switch inverter. The switching states of S_1 - S_6 are determined using a Sinusoidal Pulse-Width Modulation (SPWM) scheme.

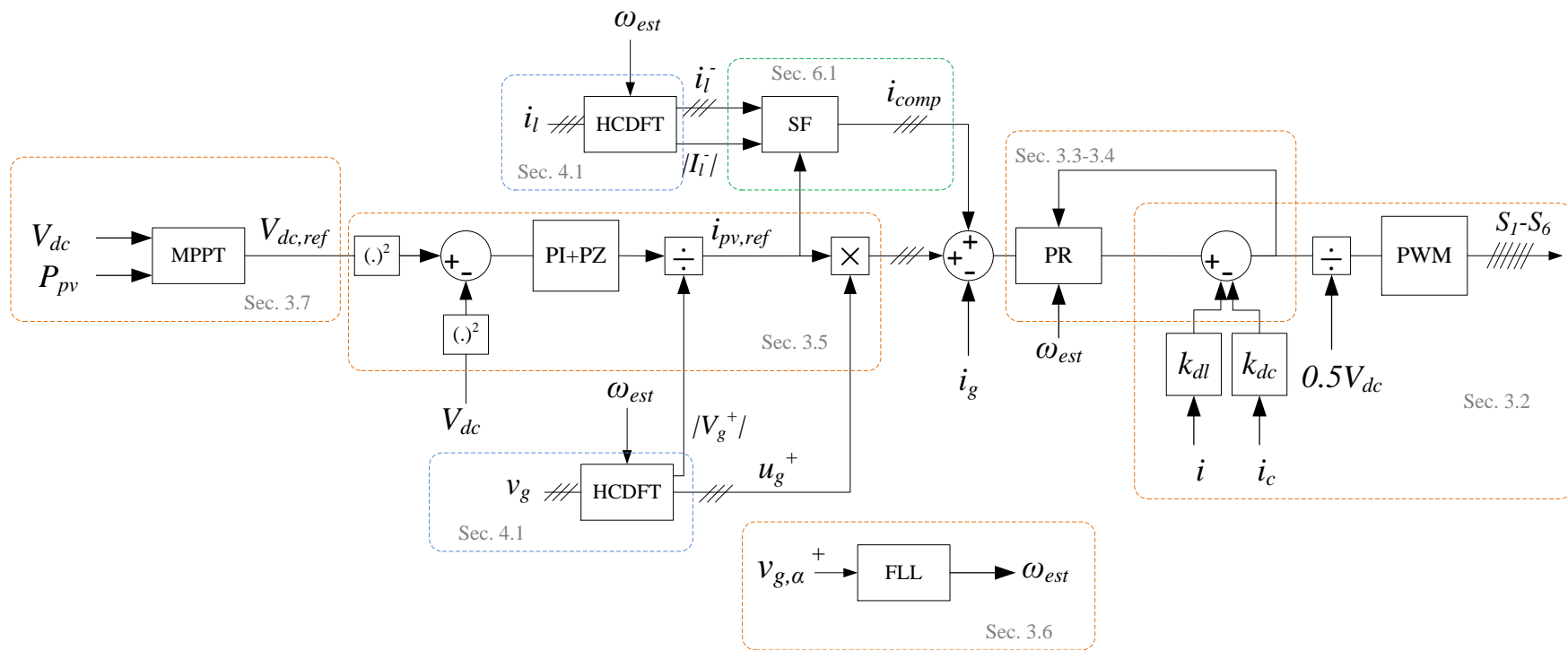


Figure 3.1: Overall block diagram of the inverter control scheme

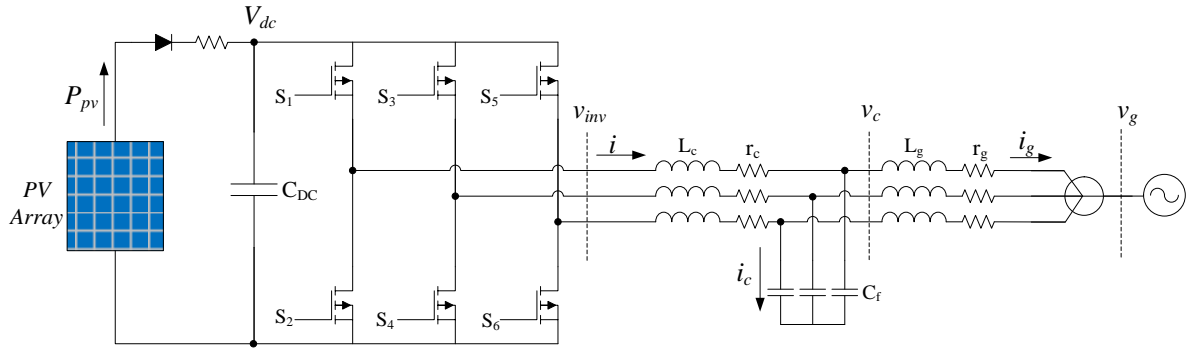


Figure 3.2: A single stage PV inverter with an LCL filter

3.1 Inverter Modeling

According to the averaged model of a six-switch, two-level converter with SPWM, the fundamental frequency component of the inverter terminal voltage v_{inv} is related to the SPWM modulation index, M , and the DC link voltage, V_{DC} by (3.1) [1].

$$v_{inv} = M \frac{V_{DC}}{2} \quad (3.1)$$

Thus the terminal voltage of the converter can be controlled by adjusting the modulation index.

The filter is composed of the inner inductance L_c , Capacitor C_f , and grid-side inductance L_g . Taking Figure 3.2 as a reference, the differential equations describing the AC filter dynamics of the inverter for each phase can be written as (3.2). Each of the energy storage elements, L_c , C_f , and L_g , in the filter contribute a first order differential equation to the system model. r_c and r_g are the parasitic resistances of L_c and L_g respectively.

$$L_c \frac{di}{dt} = v_{inv} - v_c - r_c i \quad (3.2)$$

$$C_f \frac{dv_c}{dt} = i - i_g$$

$$L_g \frac{di_g}{dt} = v_c - v_g - r_g i_g$$

Combining (3.1) and (3.2) the system can be represented in a state-space form (3.3).

$$\begin{bmatrix} \dot{i} \\ \dot{v}_c \\ \dot{i}_g \end{bmatrix} = \begin{bmatrix} -r_c/L_c & -1/L_c & 0 \\ 1/C_f & 0 & -1/C_f \\ 0 & 1/L_g & -r_g/L_g \end{bmatrix} \begin{bmatrix} i \\ v_c \\ i_g \end{bmatrix} + \begin{bmatrix} 1/2L_c V_{DC} \\ 0 \\ 0 \end{bmatrix} M + \begin{bmatrix} 0 \\ 0 \\ -1/L_g \end{bmatrix} v_g \quad (3.3)$$

Equation (3.3) represents one phase of the inverter. The states are inverter-side current, i , grid-injected current i_g , and filter capacitor voltage v_c . The state-space model for each phase can be developed independently in the ABC reference frame. Each of the three-phases is a third order, non-linear system sharing a common variable V_{DC} . Because the dynamics of the AC filter are significantly faster than those of the DC bus, the system described by (3.3) can be linearized by assuming a constant value for V_{DC} [1]. The control input of the system in (3.3) is the modulation index M . The grid voltage term v_g can be considered as a disturbance input. The parameters of the LCL filter considered are listed in Table 3.1. With those parameters, the system poles are determined from the Eigenvalues of the first matrix in (3.3) and are plotted in Figure 3.3.

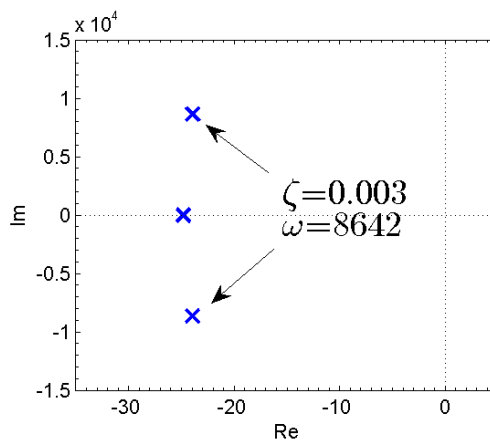


Figure 3.3: Poles of the inverter with the LCL Filter

The system (3.3) has one purely real pole and a pair of complex conjugate poles located on the left-hand side of the complex plane. The complex poles have a damping ratio of 0.003

because the parasitic resistances of the filter elements have low impedance values and cannot provide a significant level of damping.

Table 3.1: LCL filter parameter values

L_c	0.96 mH
r_c	0.016 Ω
L_g	0.25 mH
r_g	0.014 Ω
C_f	67.5 μ F

The controlled variable is the grid-side current, thus the transfer function relating the grid-side current i_g , to the system input, v_{inv} , is of interest. Neglecting the parasitic resistances of the filter components, this transfer function can be written as (3.4).

$$\frac{I_g(s)}{V_{inv}(s)} = \frac{b}{s(s^2 + \omega_n^2)}$$

$$b = \frac{1}{L_c L_g C_f} \tag{3.4}$$

$$\omega_n = \sqrt{\frac{L_g + L_c}{L_g L_c C_f}}$$

When the small parasitic resistances are neglected the transfer function (3.4) has one pole at the origin and a pair of poles that lie on the imaginary axis. The resonant frequency of the filter depends on the values of the filter components. The frequency response for the filter is plotted in Figure 3.4.

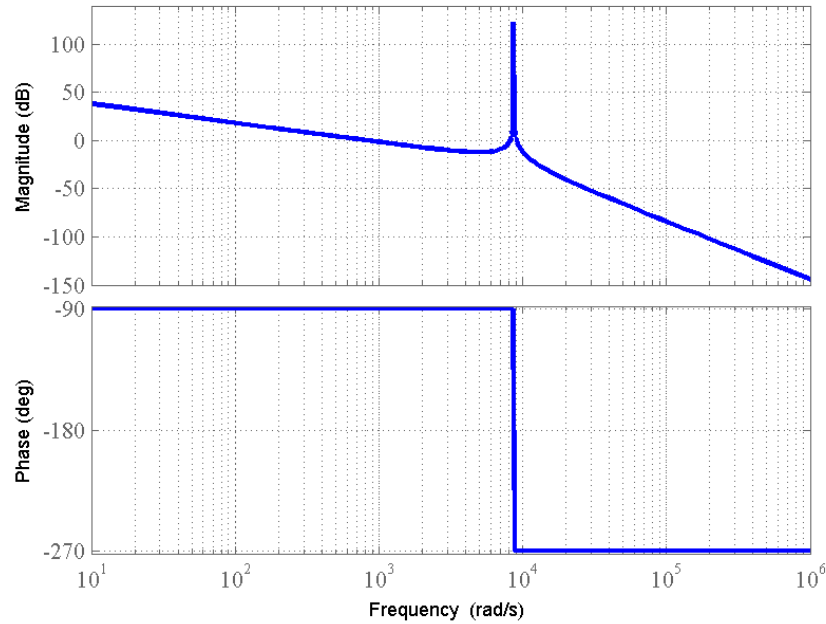


Figure 3.4: LCL filter frequency response

Figure 3.4 illustrates the characteristics of the filter to attenuate the harmonics of the switched voltage v_{inv} and produce a sinusoidal current. The transfer function in (3.4) is the equivalent admittance of the filter over a range of frequencies. For voltage harmonics at and near the resonant frequency, the filter presents an equivalent impedance of zero. Instead of attenuating harmonics at the resonant frequency, there is amplification. For the LCL filter values listed in Table 3.1 this resonance point occurs at $8.64e+3$ rad/s. The value of the resonant frequency is important from both a power quality and control system stability point of view. If no damping technique is employed, the resonance places restrictions on the bandwidth of the current control loop.

3.2 Virtual Impedance Active Damping Scheme

To solve the problem of filter resonance, active damping techniques are preferred to passive damping techniques in the literature. In the proposed control scheme, depicted in Figure 3.5 a multivariable feedback AD technique is employed. The inverter-side current i and the filter capacitor current i_c are multiplied by their respective damping coefficients k_{dl} and k_{dc} and subtracted from the output of the PR controller to yield the inverter terminal voltage reference, v_{inv} . No physical filter damping components are added. The value of the damping coefficients determines the values of virtual impedances in series with the inner inductor and with the filter capacitor. When the AD scheme in Figure 3.5 is used, the LCL filter is the

equivalent of a damped second order dynamic system from the perspective of the grid-side current controller. The multivariable feedback results in improved DC rejection compared to capacitor current alone for the AD loop. An extra degree of freedom is afforded by using two current feedback variables which allows the gains to be easily calculated to yield the desired damping ratio without the need for iteration or complex algorithms. Unlike the cascade filter methods discussed in Chapter 2, no additional integral or derivative terms are required in the control scheme.

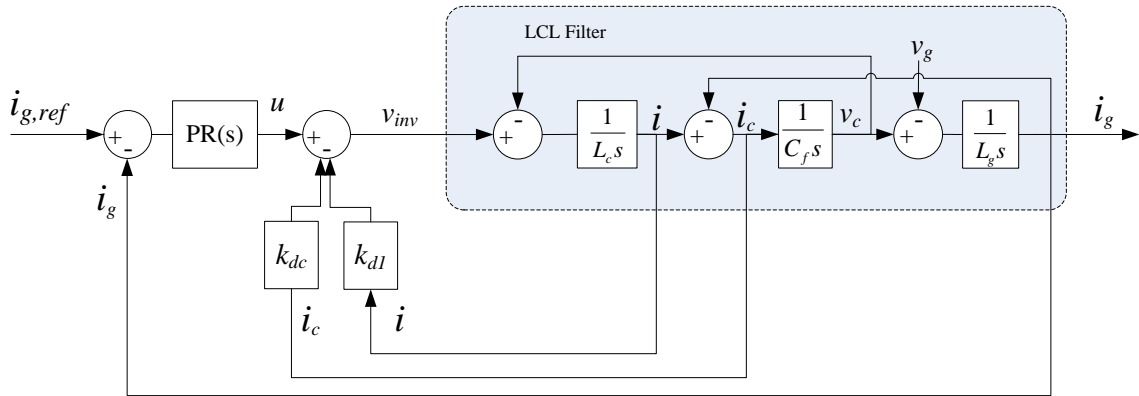


Figure 3.5: Proposed active damping scheme for an LCL filter

Since the capacitor current can be calculated from the inductor and grid current measurements, only two current sensors per phase are required to implement this scheme. The physical significance of the additional proportional feedback can be deduced by rearranging Figure 3.5 to the form of Figure 3.6.

The i feedback loop has the effect of adding a resistance, R_{eq} , which has a value of k_{dl} in series with the inner inductor. The i_c feedback loop effectively adds a complex, frequency dependant impedance, Z_{eq} , in parallel with the filter capacitor. Equating the capacitor current with the derivative of the capacitor voltage as in (3.5) is the first step to determining Z_{eq} .

$$i_c = C_f \frac{dv_c}{dt} \quad (3.5)$$

The inverter-side current is defined by (3.6)

$$i = \frac{1}{L_c s} (u - v_c - i_c k_{dc} - i k_{dl}) \quad (3.6)$$

The relationship between the inductor, capacitor, and grid-side currents is given by

$$i_c = i - i_g \quad (3.7)$$

Substituting (3.5) and (3.6) into (3.7) and simplifying yields (3.8)

$$i_c = \frac{1}{L_c s + k_{dl}} (u - v_c) - i_g - \frac{k_{dc} C_f s}{L_c s + k_{dl}} v_c \quad (3.8)$$

From (3.8) the equivalent impedance in series with the filter capacitor is (3.9)

$$Z_{eq}(s) = \frac{L_c s + k_{dl}}{k_{dc} C_f s} \quad (3.9)$$

According to (3.9) the virtual impedance in parallel with the capacitor is dependent on both damping gains.

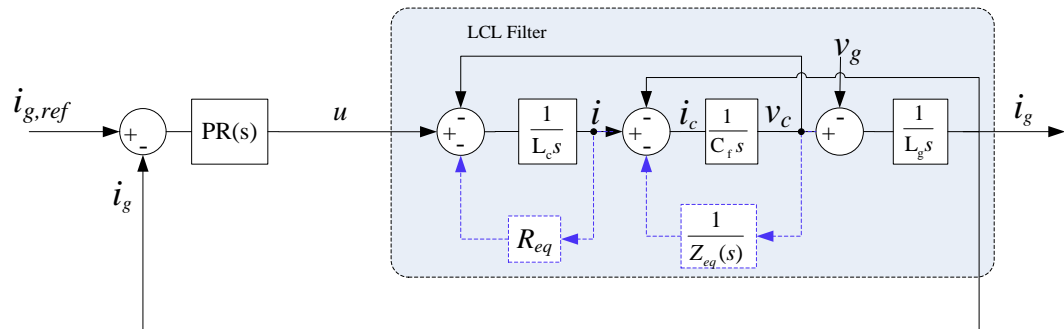


Figure 3.6: Equivalent Filter with virtual impedance active damping

3.2.1 Damping Coefficient Calculation

The equivalent transfer function of the LCL filter with the dual feedback AD scheme shown in Figure 3.5 is derived as in (3.10)

$$\frac{i_g(s)}{u(s)} = G_{i_g u}(s) = \frac{1}{L_c L_g C_f s^3 + (k_{dc} + k_{dl}) L_g C_f s^2 + (L_g + L_c) s + k_{dl}} \quad (3.10)$$

When two variables are used as feedback there is an additional degree of freedom in choosing the coefficients of the denominator polynomial of (3.10) compared to feedback of capacitor current alone. The parasitic resistance of the filter components are neglected in the analysis and design of the damping gain for the sake of simplicity. Additionally, this ensures that the gain is designed conservatively since the parasitic resistance will also contribute some passive damping to the filter. Equation (3.10) is a 3rd order dynamic system which can be rearranged into the form (3.11)

$$G(s) = \frac{1}{a(s^2 + 2\zeta\omega_n' s + \omega_n'^2)(s + m\zeta\omega_n')} \quad (3.11)$$

The system in (3.11) can be approximated as a second order system provided the magnitude of the real pole is much larger than the real portion of the complex pole pair. The ratio of the real pole to the real portion of the complex pole in (3.11) is m and must be specified by the designer of the control scheme. In [2] the minimum value for m is 5 in order to approximate (3.10) as a second order system. Equating the denominator of (3.10) with the third order system in (3.11) allows the damping gains to be calculated for a desired damping ratio ζ as in (3.12).

$$\begin{aligned} k_{dl} &= L_c C_f L_g m \zeta \omega_n'^3 \\ k_{dc} &= L_c \zeta \omega_n' (m + 2) - k_{dl} \\ \omega_n' &= \sqrt{\frac{L_g + L_c}{L_g L_c C_f (1 + 2m\zeta^2)}} \end{aligned} \quad (3.12)$$

It should also be noted that the effective resonant frequency of the compensated system, ω_n' , is reduced by a factor of $\sqrt{1 + 2m\zeta^2}$ compared to the undamped resonant frequency of the LCL filter, ω_n . This indicates increased attenuation in the region of the uncompensated resonant frequency. Increasing the value of m will result in a greater reduction in the effective resonant frequency.

The frequency response of (3.10) is plotted below in Figure 3.7 when $m = 5$ and the damping ratio is increased from 0.1 to 1.

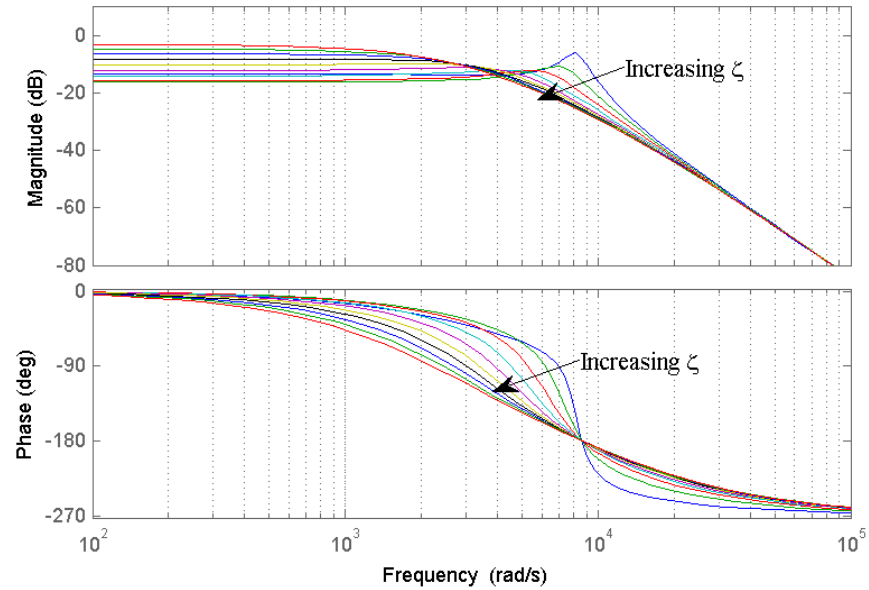


Figure 3.7: Frequency Response of the damped filter as ζ is increased from 0.1 to 1

Figure 3.8 shows the frequency response of (3.10) using the component values listed in Table 3.1 when $\zeta = 0.9$ and $m = 5$. The damping ratio is chosen as 0.9 to ensure adequate damping in case of filter parameter variation.

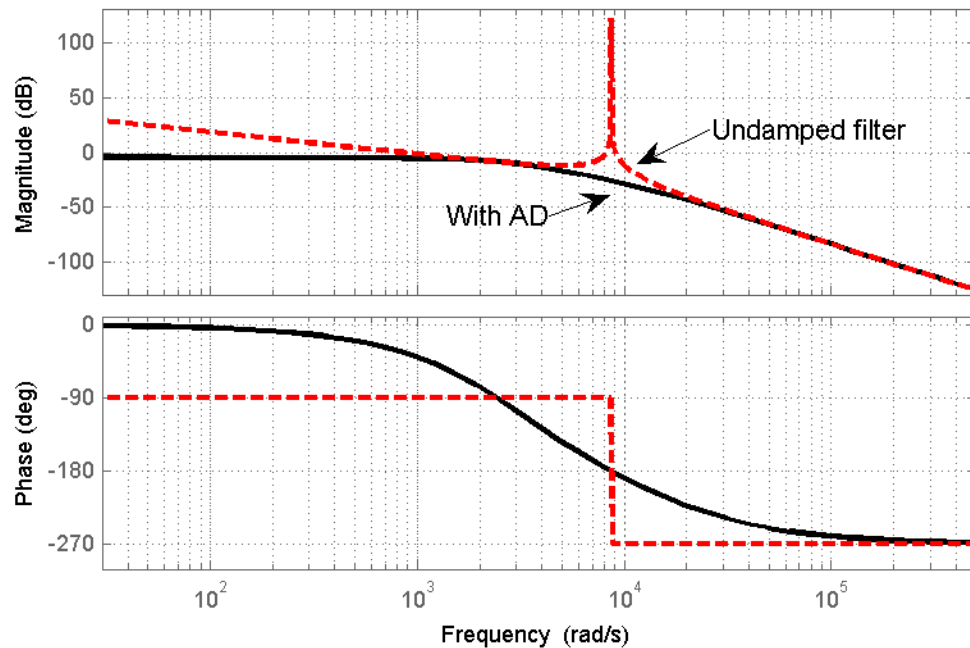


Figure 3.8: Frequency response of the LCL filter with and without AD

Because the damped filter does not include a pole at or very near the origin, the filter does not amplify lower frequency and DC components of the input. Above the resonant frequency, the magnitude of the damped and undamped frequency response is nearly identical.

The effectiveness at different values of resonant frequencies is demonstrated in Figure 3.9. The parameters for LCL filter configurations with low (0.69 kHz), medium (1.19 kHz), and high (1.69 kHz) resonant frequencies in [3] were used with (3.12) to calculate the damping gains for the same values of ζ and m as shown above. Figure 3.9 shows the frequency response of the filters with active damping.

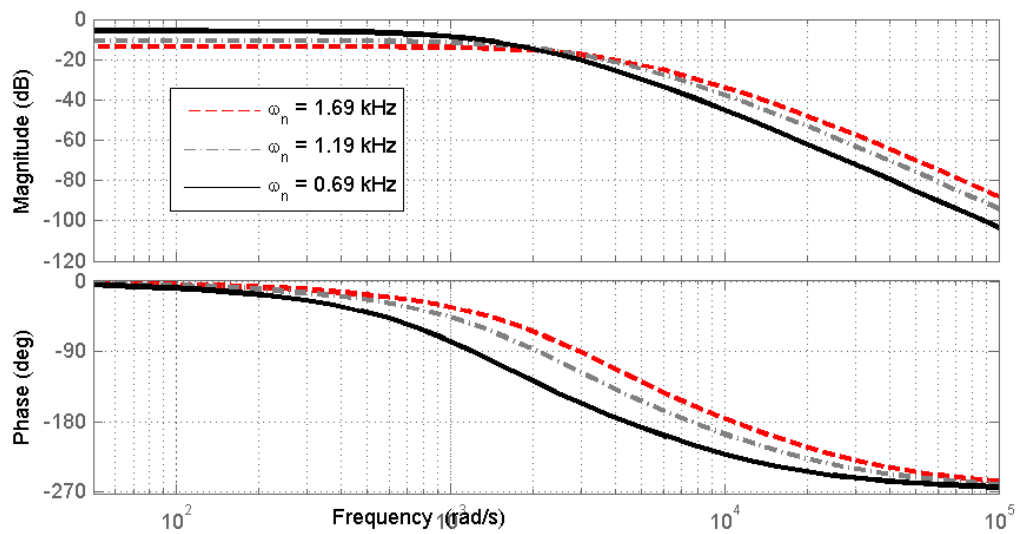


Figure 3.9: Filter response for filters with low, medium, and high natural resonance frequencies

Figure 3.9 shows that the AD scheme described above is suitable for LCL filters with a wide range of resonant frequencies.

3.2.2 Effects of Grid Inductance Variation

In addition to the inductance of the filter components and transformer, the frequency characteristics of the grid impedance can also affect the transfer function of the filter. The grid impedance can vary due to line/load switching and connection or disconnection of the microgrid from the main grid. The value of the grid-side filter inductor can also be different from the nameplate rating as a result of operating conditions and miscalculations. Of the filter damping techniques discussed in Chapter 2, multi-loop AD techniques have been

shown to have good resilience to changes in grid-side inductance [4]. Figure 3.10 shows the movement of the poles of the loop gain (3.10) as the changing grid-side inductance varies.

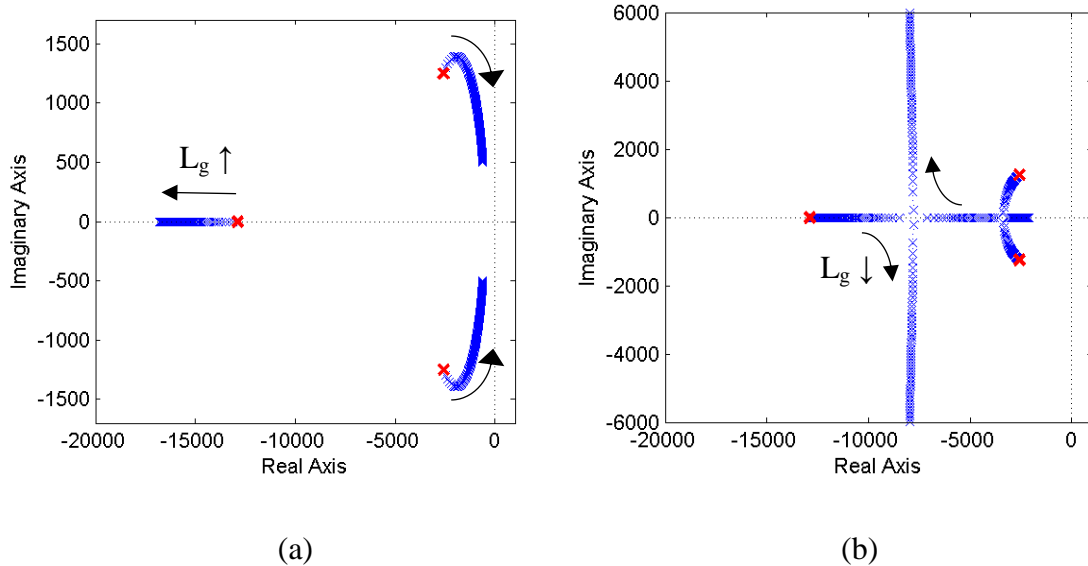


Figure 3.10: (a) Impact of a ten-fold increase and (b) decrease in L_g on open loop poles

When the grid inductance is increased while the damping gains k_{dl} and k_{dc} remain the same, the damping is somewhat decreased before returning to previous levels. The minimum damping ratio of the pole locations shown in Figure 3.10 (a) is $\zeta = 0.71$, which is still sufficiently damped to prevent instability in the current control loop. Figure 3.10(b) shows that reducing the grid-side inductance causes the complex pole pair to travel toward the real axis, until the system contains only real poles. Further decreasing L_g eventually leads to another pair of complex poles appearing at a higher frequency. This alternate resonant point can be seen in Figure 3.11 where the frequency response is plotted as L_g varies from its nominal value.

The frequency response for $L_g' = 0.1 * L_g = 25 \mu\text{H}$ exhibits underdamped characteristics. If the range of typical grid impedance values are known in advance it is advisable to calculate the damping gains based on a low grid impedance value. Increasing the grid impedance increases the system damping. If the grid inductance is decreased significantly lower than the value considered at the design stage, the system could become underdamped.

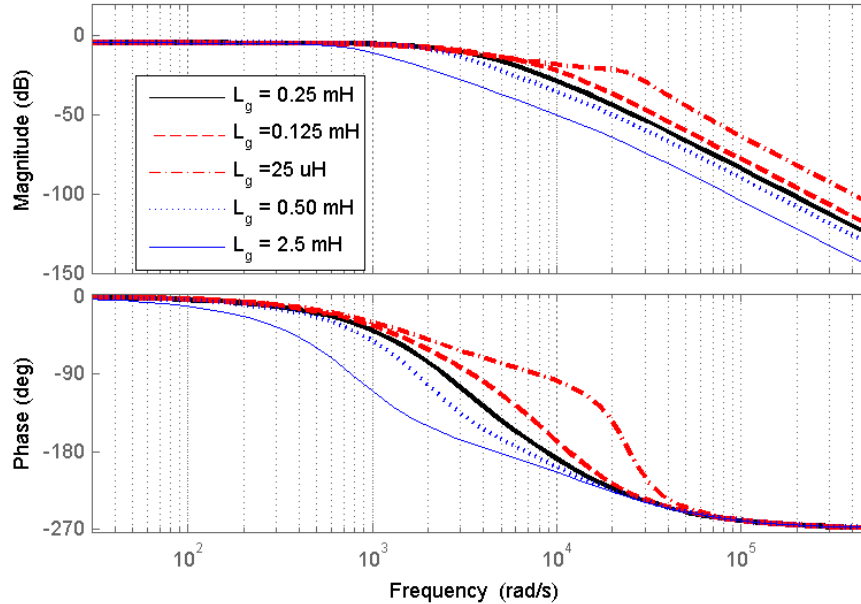


Figure 3.11: Frequency response of the LCL filter

3.3 Calculation of the Current Controller Gains

Once the necessary damping of the LCL filter has been achieved, the model of the equivalent compensated system (3.10) can be used to determine the current controller gains.

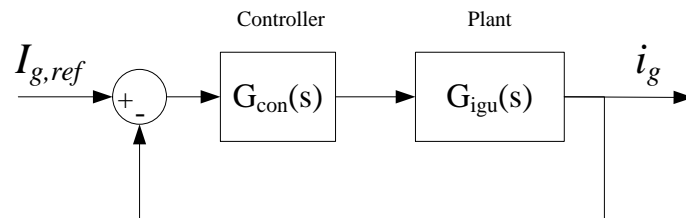


Figure 3.12: The current control loop

The plant labelled in Figure 3.12 is the transfer function (3.10) of the LCL filter with the AD loops as discussed in Section 3.2. Based on classical control theory, the closed-loop characteristics of a system can be manipulated by open-loop characteristics of the loop gain transfer function. Of particular interest are the Phase Margin (PM), which affects the transient response, and the Gain Margin (GM), which indicates the sensitivity to parameter variations. Controller design based on PM and GM specifications has been discussed in the literature [5] as systematic methods for calculating the gains with higher order filters.

A proportional resonant controller is adopted which allows for individual control of each phase of the inverter. The input of the controller is the error between the sinusoidal current reference $i_{g,ref}$, and the measured current i_g .

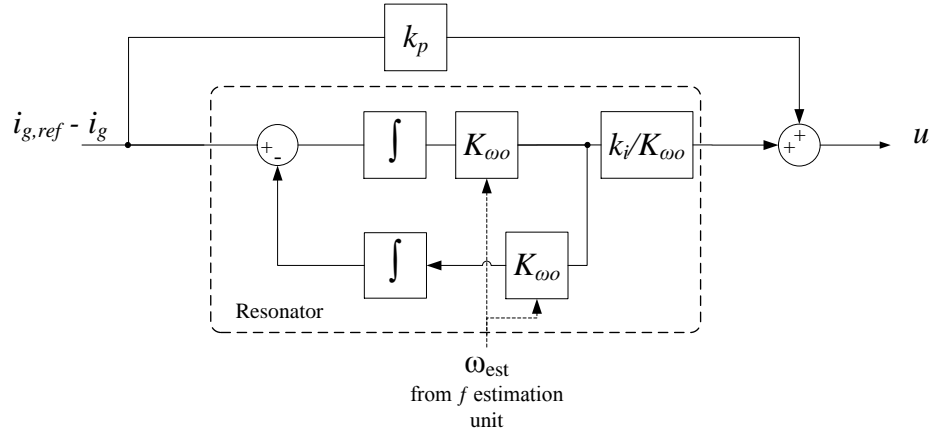


Figure 3.13: Block diagram of a proportional + resonant controller

The controller consists of two parts: a proportional term k_p , and a resonant term with gain k_i which employs two integrators. When the gains K_{ω_o} are set equal to the fundamental frequency ω_o , the resonator performs a time-domain amplitude integration of a sinusoidal signal with frequency ω_o [6]. From Figure 3.13, the transfer function of a PR controller including the proportional and resonant terms is given in (3.13).

$$PR(s) = k_p + \frac{k_i s}{s^2 + \omega_o^2} \quad (3.13)$$

The transfer function of the PR controller contains a pair of poles on the $j\omega$ axis at the fundamental frequency ω_o . This allows the PR controller to track a sinusoidal reference signal with frequency of ω_o according to the internal model principle [7]. An infinite gain at the fundamental frequency is observed in the frequency response of (3.13) as shown in Figure 3.14.

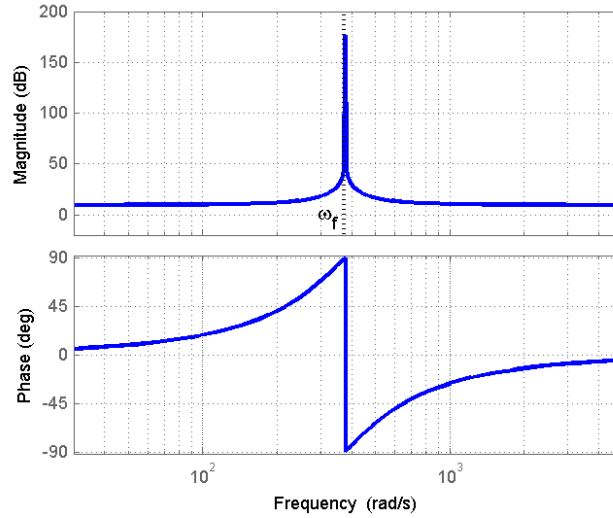


Figure 3.14: PR controller frequency response

If $K_{\omega o}$ is not tuned to the exact frequency of the input signal, or if the reference frequency varies, the controller would have imperfect tracking. To be suitable for a microgrid, the controller is required to be effective during possible times of frequency deviation. In order to adapt the controller for variable grid frequencies, the value $K_{\omega o}$ in the block diagram in Figure 3.13 is updated based on the output of the frequency estimation unit, discussed in Section 3.6.

For a PR controller the relationship between the gains k_p and k_i and the transfer function is less straight forward than for a PI controller. Rather than selecting gains for the PR controller in the ABC frame, the gains for an equivalent PI controller can be calculated and applied to the PR controller [8]. The open-loop transfer function, $P(s)$, of the system shown in Figure 3.12 is:

$$P(s) = G_{con}(s)G_{igu}(s) = \frac{k_p s + k_i}{s} \frac{1}{(\alpha_3 s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0)}$$

$$\alpha_3 = L_c L_g C_f \quad (3.14)$$

$$\alpha_2 = L_g C_f (k_{dl} + k_{dc})$$

$$\alpha_1 = L_c + L_g$$

$$\alpha_0 = k_{dl}$$

when $G_{con}(s)$ is a PI controller. In order to synthesize the controller gains, several parameters have to be chosen, namely the PM and GM. A PM of 30-60° is typically selected [5]. The

desired GM should be chosen keeping in mind the restrictions placed on the crossover frequency ω_c . Since ultimately the controller will be of the proportional resonant form, the crossover frequency should be higher than the fundamental frequency of 377 rad/s but lower than the resonant frequency of the filter, ω_n . From these criteria k_i and k_p can be explicitly calculated. In this case, GM = 12 dB and PM = 45° is selected.

The first step is to find an expression for the proportional gain k_p in terms of ω_c . This expression can then be used to calculate the crossover frequency in terms of the desired gain margin. Once ω_c is known it can be used to determine k_p . From k_p , ω_c , and the PM, the integral gain can be calculated.

In the low frequency range ($\omega < \omega_n$) the filter capacitor has little impact on the transfer function gain and the plant can be represented by a first order system (3.15) [5].

$$G_{igu}(s) \approx \frac{1}{(L_c + L_g)s + k_{dl}} \quad (3.15)$$

The gain of the controller in the region of ω_c can be approximated by the proportional gain k_p because the corner frequency of the PI controller (k_i/k_p) is lower than ω_c . Thus the approximate open-loop transfer function is (3.16).

$$G_{con}(s)G_{igu}(s) \approx \frac{k_p}{(L_c + L_g)s + k_{dl}} \quad (3.16)$$

At the crossover frequency, the gain of (3.16) is equal to 1. Calculating the magnitude of (3.16) at $s = j\omega_c$ and rearranging terms leads to an expression for the proportional gain k_p (3.17).

$$k_p = \sqrt{k_{dl}^2 + (L_c + L_g)^2 \omega_c^2} \quad (3.17)$$

To develop an expression for the crossover frequency in terms of the specified gain margin, the magnitude of the loop gain at the filter resonant frequency is examined. For the transfer function in (3.14) the -180° point occurs at the resonant frequency ω_n . The gain margin of (3.19) is given by (3.18).

$$GM = -20 \text{Log}|P(j\omega_n)| \quad (3.18)$$

Although $G_{igu}(s)$ is a third-order system, it can be approximated by a damped second order system at the resonant frequency because the damping gains were designed to move the real pole from the origin to the left hand plane much farther than the complex-conjugate pair. The second order approximation of the loop gain (3.19) is more accurate in the region of the resonant frequency than (3.16).

$$P(s) \approx \frac{(m+2)k_p}{L_g C_f m(k_{dl} + k_{dc}) \left(s^2 + 2 \frac{k_{dl} + k_{dc}}{L_c(m+2)} s + \frac{L_g + L_c}{L_g L_c C_f (1 + 2m\zeta^2)} \right)} \quad (3.19)$$

The damping ratio, ζ , and m in (3.19) are the same designer-selected parameters discussed in Section 3.2. Substituting (3.17) and (3.19) into (3.18) yields an expression for the crossover frequency based on the desired GM.

$$\omega_c = 10^{\frac{-GM}{20}} \frac{m(k_{dl} + k_{dc})}{L_c(2+m)} \sqrt{\left(\frac{2(k_{dl} + k_{dc})}{L_c(m+2)\omega_n} \right)^2 + \left(\frac{2m\zeta^2}{2m\zeta^2 + 1} \right)^2} \quad (3.20)$$

A more detailed derivation of (3.19) and (3.20) is given in Appendix C. Using the crossover frequency, the proportional gain k_p can be calculated from (3.17).

The final step in the design process is to calculate the integral gain, k_i based on the desired PM. The phase of the system at the crossover frequency, φ_c , is determined by evaluating the phase angle of the transfer function $P(s)$ in (3.14) when $s = j\omega_c$.

$$\angle P(j\omega_c) = \tan^{-1} \left(\frac{\text{Re}\{P(j\omega_c)\}}{\text{Im}\{P(j\omega_c)\}} \right) = \tan^{-1} \left(\frac{-k_p \alpha_3 \omega_c^4 + k_i \alpha_2 \omega_c^2 - k_p \alpha_1 \omega_c^2 + k_i \alpha_0}{k_i \alpha_3 \omega_c^3 + k_p \alpha_2 \omega_c^3 - k_i \alpha_1 \omega_c + k_p \alpha_0 \omega_c} \right) \quad (3.21)$$

The necessary phase of the loop gain to yield the desired phase margin is:

$$\varphi_c = PM - 180^\circ \quad (3.22)$$

Substituting (3.22) into the right hand side of (3.21) and rearranging yields an expression for the integral gain k_i .

$$k_i = k_p \omega_c \left(\frac{-\alpha_3 \omega_c^3 - \tan \varphi_c \alpha_2 \omega_c^2 + \alpha_1 \omega_c + \tan \varphi_c \alpha_0}{-\tan \varphi_c \alpha_3 \omega_c^3 + \alpha_2 \omega_c^2 + \tan \varphi_c \alpha_1 \omega_c - \alpha_0} \right) \quad (3.23)$$

The chosen phase and gain margins, the resulting crossover frequency ω_c , and gains k_p and k_i calculated using the method above are listed in Table 3.2 for the system with parameters listed in Table 3.1.

Table 3.2: Current Controller Parameters

GM	12 dB
ω_c	3640 rad/s
PM	50°
k_i	3516
k_p	4.73

Figure 3.15 shows the open loop frequency response of the system for both a PI and PR controller with the same k_i and k_p controller gains listed in Table 3.2.

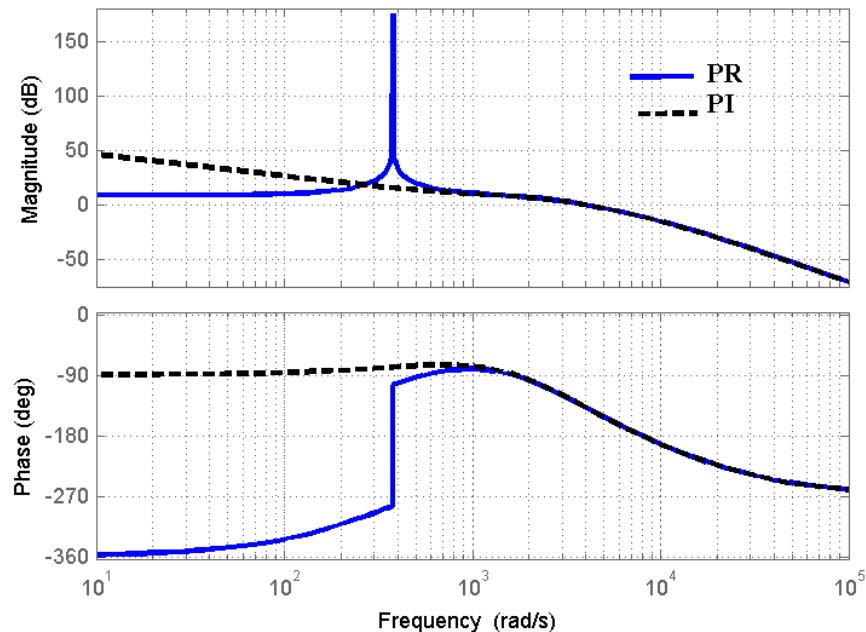


Figure 3.15: Bode plot of the loop transfer function for PI and PR controllers

Only in the low frequency region does the frequency response differ for the PI and PR controllers. Above $\omega \approx 10,000$ rad/s the phase and magnitude of the frequency response is the

same for both types of controllers. The step response of the current control loop when a PR controller is used is plotted in Figure 3.16 for an increase of 0.5 to 1.0 pu in the magnitude of the reference current.

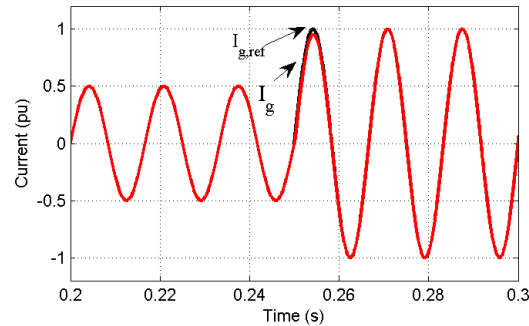


Figure 3.16: Step response of current control loop when a PR controller is used for a 100% increase in current reference magnitude at $t = 0.25$ s

Because of the resonator, the controller is able to track the sinusoidal reference signal with zero steady state error and a fast dynamic response. Although typical transient performance criteria, such as overshoot and rise time, are difficult to apply to tracking of non-DC signals, visual inspection of Figure 3.16 shows almost perfect alignment with the reference signal within a $\frac{1}{2}$ cycle of the fundamental.

3.4 Anti-Windup Scheme for a PR Controller

3.4.1 Discrete Implementation of a PR Controller.

The digital implementation of the control scheme requires discrete implementation of the continuous time PR controller. The same structure of Figure 3.13 is kept but a discrete implementation of the integrators is used. This allows the resonator gains to be updated based on the estimated frequency and requires lower computational resource consumption compared to implementing a discrete transformation of the PR transfer function (3.13) [9]. Using the Forward Euler transformation for integrator 1 in Figure 3.17 and the Backward Euler transformation for integrator 2 prevents the formation of algebraic loops [10]. Discretizing the integrators in this manner has also been shown to have a smaller deviation from the desired resonant frequency than when the Tustin approximation is used [9], [11].

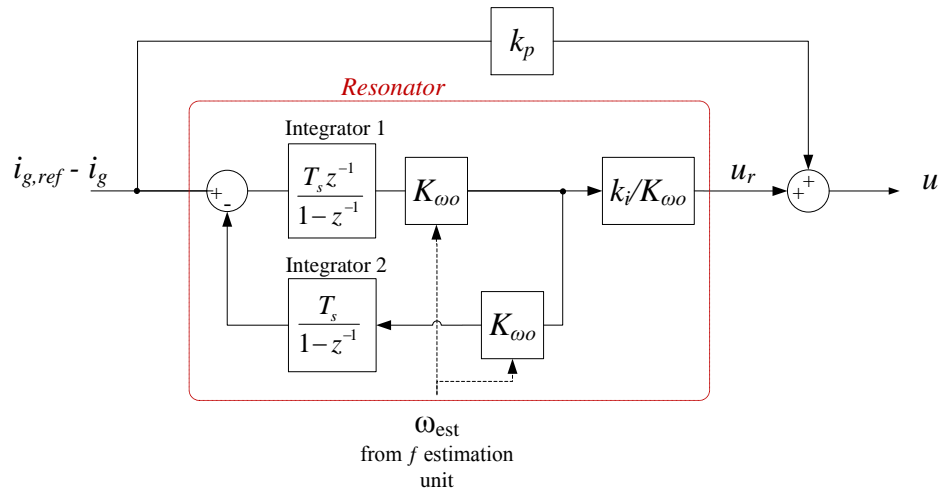


Figure 3.17: Discrete-time Proportional Resonator

3.4.2 Windup in PR Controllers

The output of the resonator, u_r , is the amplitude integration of the sinusoidal input signal $i_{g,ref} - i_g$. For a sinusoidal input with amplitude A , frequency ω , and phase φ , the amplitude of the output of the resonator in (3.13) will increase linearly at the rate of $0.5k_i A t$ as shown in (3.19) [6].

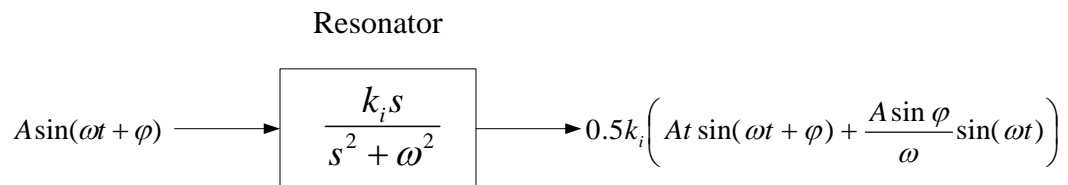


Figure 3.18: Amplitude integrator for a sinusoidal signal

Figure 3.19 shows the output of a PR controller with $k_i = 377$, $k_p = 1$ when an input signal with constant amplitude is applied.

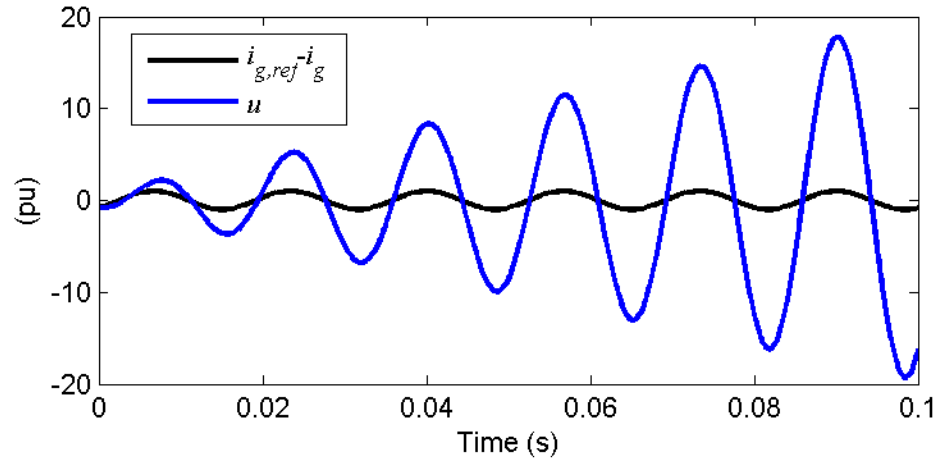


Figure 3.19: Controller output u for constant error input signal $i_{g,ref} - i_g$

If the controller is given a reference which cannot be met, the resonator will have a constant input error signal and the output will increase rapidly. This is because the integral gain is typically large to meet the control loop requirements. Even if the error returns to zero, it will take time for the output of the resonator to decrease. This phenomenon is referred to in the literature as “windup” and is a well-known problem in systems controlled by PI controllers. Unlike windup as experienced by a PI controller, it is not the individual integrators but the resonator itself which becomes wound-up in a PR controller.

Operating limits of the converter are the main cause of controller windup. For an inverter, the plant actuators are the switching signals, determined from the inverter terminal reference voltage. The amplitude of the line to line terminal voltage of the inverter is limited to $\sqrt{3}V_{DC}/2$. Increasing the reference voltage beyond this value will not result in a higher voltage at the converter terminals. Excessively high controller gains, high levels of grid voltage imbalance, low DC bus voltage, and fault conditions can all cause the inverter reference voltage to reach the saturation point. Not all events which cause actuator saturation can be accounted for at the design stage, thus some type of Anti-Windup (AW) strategy should be incorporated in the control scheme.

In the literature, the problem of windup in PR controllers has been discussed in [10], [12]-[14]. Conditional integration is shown in [14], where if the output of the controller exceeds a predefined limit, the input to the resonator is set to zero to stop further integration. The solutions to resonator windup are mainly based on AW techniques developed for PI

controllers. In [10], [12]-[15] an anti-windup technique using back-calculation as shown in Figure 3.20 is proposed.

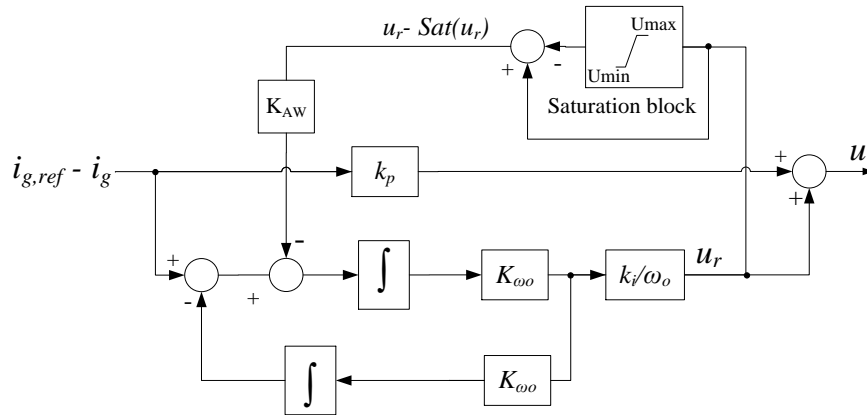


Figure 3.20: Anti-windup scheme using back-calculation [10]

In a back-calculation AW scheme for PI controllers, the amount by which the integrator output exceeds the saturation limit is subtracted from the integrator input. In Figure 3.20 this scheme is adapted for a PR controller. When the output of the resonator u_r , exceeds the maximum and minimum conditions imposed by the saturation block, the error is multiplied by the gain K_{AW} and subtracted from the input to the first integrator. The output of the saturation block in Figure 3.20 for an input signal u is defined by (3.24).

$$Sat(u) = \begin{cases} U_{\max}, & \text{If } u > U_{\max} \\ u, & \text{If } U_{\min} < u < U_{\max} \\ U_{\min}, & \text{If } u < U_{\min} \end{cases} \quad (3.24)$$

Before saturation starts, the back calculation signal $u_r - Sat(u_r)$ is equal to zero since $u_r = Sat(u_r)$. Figure 3.21 shows the output of the PR controller to the same input as in Figure 3.19 when the AW scheme is employed with $K_{AW} = 1$ and $K_{AW} = 100$.

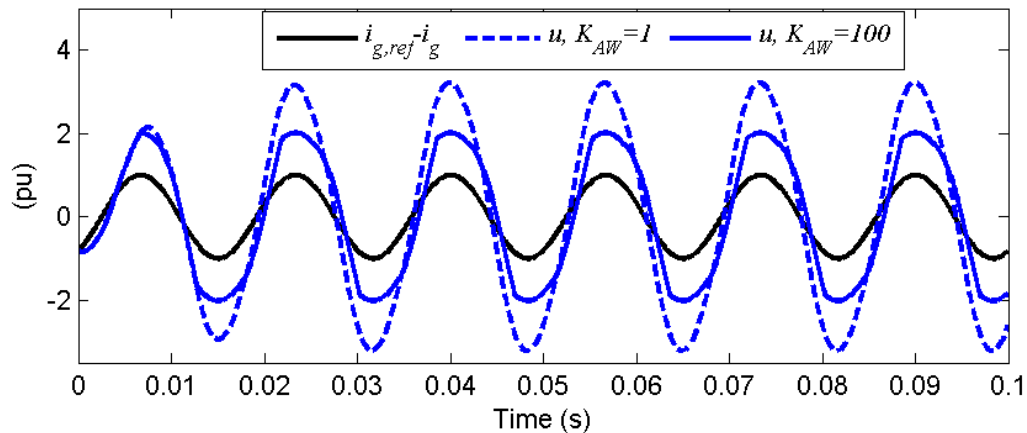


Figure 3.21: PR output for a constant error signal when a back-calculation anti-windup scheme is used

By feeding back the error between the resonator output and the saturation limits, the anti-windup scheme limits the output of the controller. If the output of the resonator increases, so does the amplitude of the signal subtracted from the resonator input, $u_r = \text{Sat}(u_r)$. This limits the output of the controller, as seen in Figure 3.21, compared to the controller output without an AW scheme shown in Figure 3.19. Figure 3.21 shows that the value of the back-calculation gain K_{AW} affects the resonator output during saturation. Increasing K_{AW} decreases the amplitude of the controller output but results in a slightly more distorted controller output. When the saturation function (3.24) is applied to a sinusoidal signal, the output contains a significant amount of harmonic distortion. Because the sinusoidal signal u_r is compared to constant saturation limits, U_{\max} and U_{\min} , the controller output u is also distorted, which can be seen in Figure 3.21.

The magnitude of the steady state output during a saturation condition is determined by the magnitude of the tracking gain, K_{AW} . Selecting a very large value for K_{AW} may cause the current control loop to become unstable, while a small value will be less effective in limiting the output of the controller. It is important to note that this method of anti-windup cannot prevent the resonator output from reaching the saturation limits, because there is no feedback signal in this case. Although [10], [12]-[15] show implementation of an anti-windup scheme for a current controller, none consider the effect of a multi-loop active damping scheme.

The modulation index has two important parameters: the amplitude and the phase angle. Although the amplitude saturates at 1, when normalized to $V_{dc}/2$, the phase angle can vary

between 0-180°. The magnitude and phase of the injected grid current depends on both the magnitude and phase angle of the inverter terminal voltage. To improve controller performance while the anti-windup scheme is active, the magnitude of the inverter reference voltage must be minimized, and the anti-windup loop must not interfere with the correct phase. In a single stage PV system this is especially important, because the bus voltage is dependent on the real power injected into the grid.

3.4.3 Proposed Anti-windup Scheme

An improved back calculation anti-windup strategy for a PR controller is presented in this section. The proposed changes from the strategy shown in Figure 3.20 reduce the current distortion and improve reference current tracking during activation of the anti-windup loop. The proposed AW scheme shown in Figure 3.22 accounts for the active damping loop. The output of the virtual impedance loop, $v_{inv,ref}$, is used for the back calculation rather than the output of the PR controller or resonator. Using the output of the virtual impedance loop allows the saturation limits to be easily calculated. If the PR controller output u is used instead, the limits of the saturation block cannot be set precisely, since the relationship between u and $v_{inv,ref}$ is not a simple algebraic one. This can result either in triggering the anti-windup loop before saturation has actually been reached if the limit is too low, or operating in the non-linear region of SPWM modulation if the limits are set too high. The second advantage of the scheme shown in Figure 3.22 is more accurate tracking of the phase of the reference current during input saturation. This is the result of adding the feedback signal e_{bc} to the input of the second integrator.

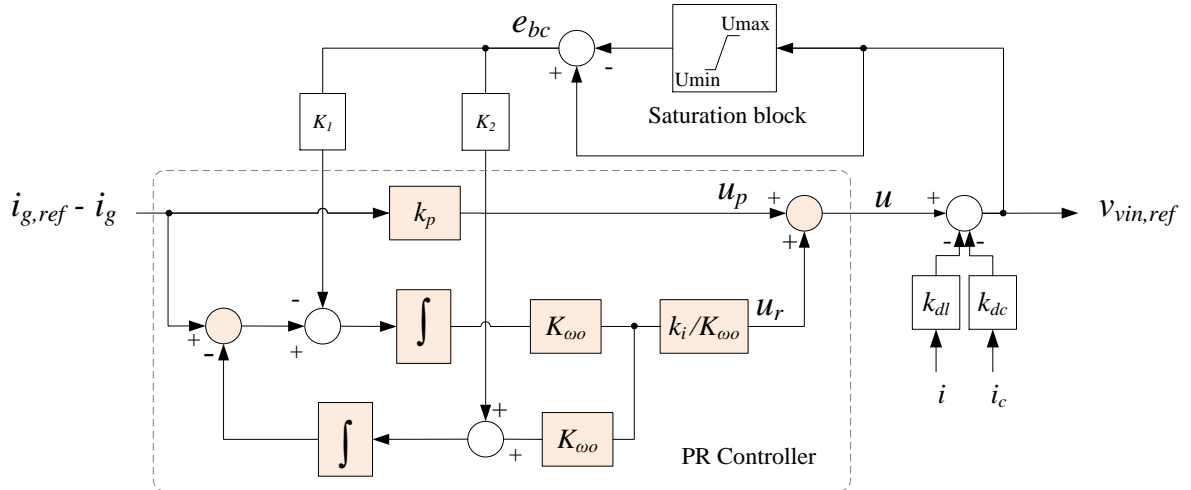


Figure 3.22: Proposed Anti-Windup scheme for PR based current controller with an AD loop

Two gains K_1 and K_2 are added to the conventional PR structure as shown in Figure 3.22. When the inverter terminal voltage reference $v_{inv,ref}$ is within the acceptable range, the feedback signal e_{bc} is then equal to zero, and the controller behaves exactly as a standard PR controller. When $v_{inv,ref}$ exceeds the limits imposed by the DC link voltage the output of the saturation block will be clipped, and the feedback signal e_{bc} will no longer be zero. The limits U_{max} and U_{min} in Figure 3.22 are set to $+V_{DC}/2$ and $-V_{DC}/2$ respectively, where V_{DC} is the DC link voltage. Some over modulation is possible, however the relationship between the modulation index and the terminal voltage becomes non-linear. The strategy is to keep the output $v_{inv,ref}$ as close as possible to the limit to remain in the region of approximate linearity.

As mentioned in [10], analysis of the anti-windup scheme is complicated. This is due the non-linearity of the relationship between the modulation index, DC link voltage, and inverter terminal voltage during SPWM over-modulation, as well as the non-linear saturation function (3.24). However, some insight into the effect of the second feedback term can be gained by examining the equivalent structure of Figure 3.23.

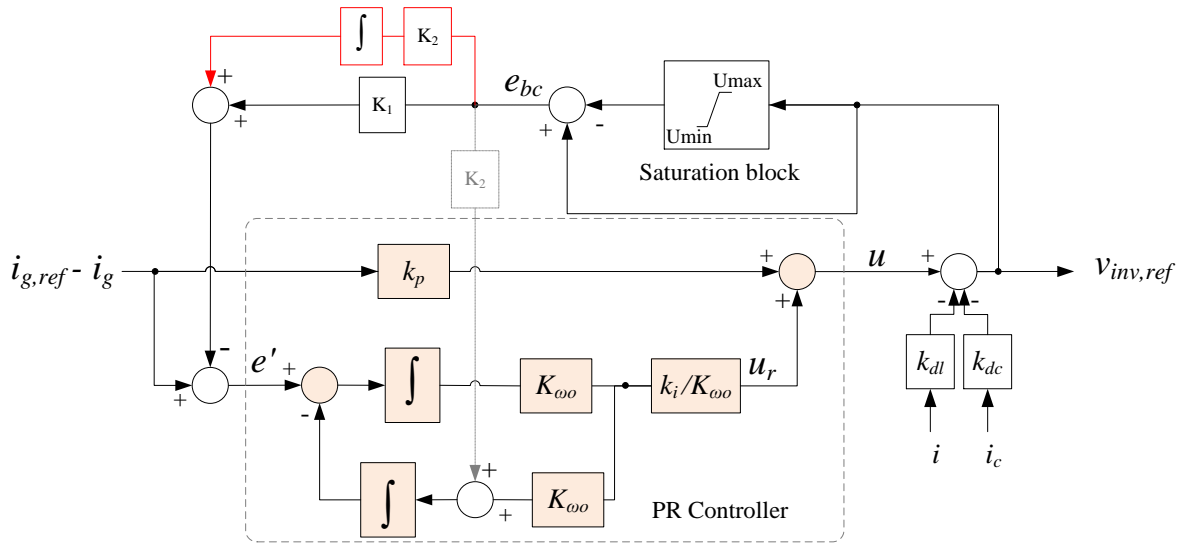


Figure 3.23: Equivalent block diagram of Modified PR controller

When the anti-windup loop is engaged, the input to the resonator is no longer the error between the reference and actual value of the grid side current, e . Instead, the equivalent error e' is

$$\begin{aligned} e' &= e - \left(K_1 e_{bc} + K_2 \int e_{bc} dt \right) \\ e_{bc} &= v_{inv,ref} - Sat(v_{inv,ref}) \end{aligned} \quad (3.25)$$

Thus, adding the back calculation signal to the second integrator allows for additional filtering of the feedback e_{bc} without the need for implementing separate integrators. The second gain also reduces the steady state output $v_{inv,ref}$ compared to purely proportional feedback.

In the frequency domain, the output of the PR controller u is described by (3.26).

$$U(s) = \left(k_p + \frac{k_i s}{s^2 + \omega_o^2} \right) E(s) - \left(\frac{\omega_o k_i (K_1 s + K_2)}{s^2 + \omega_o^2} \right) E_{bc}(s) \quad (3.26)$$

The second term on the right hand side of equation (3.26) shows the “filtering” effect the PR controller has on the back calculation signal $C(s)$. The frequency response of the second term in the right hand side of (3.26) is shown in Figure 3.24.

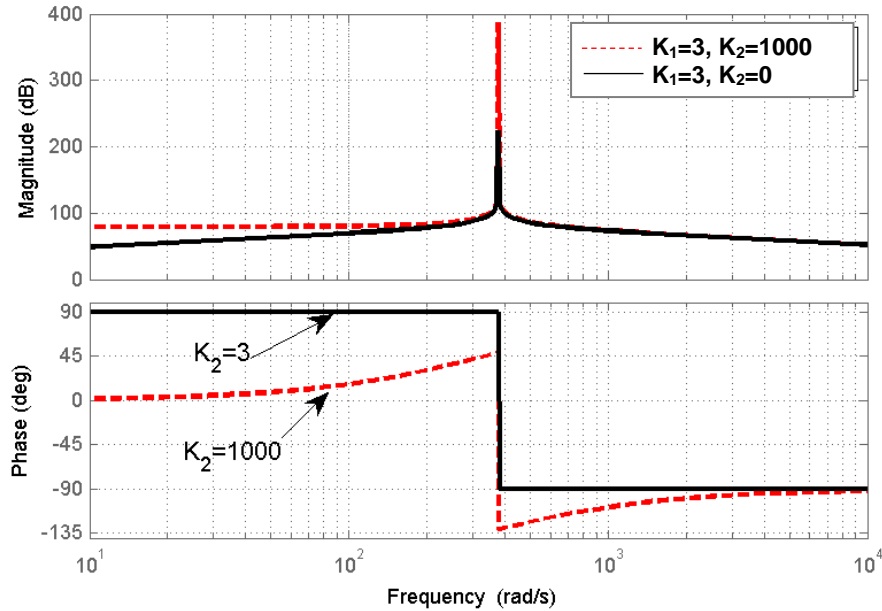


Figure 3.24: Frequency response of the gain of the back calculation signal for normalized value of $K_2 = 0$ and $K_2 = 500$

Including the integral feedback, ($|K_2| > 0$), introduces a phase lag at the frequency

$$\omega = \frac{K_2}{K_1} \quad (3.27)$$

When ω is chosen in the vicinity of the fundamental frequency, there is a 45° phase reduction of the fundamental components of the anti-windup feedback variable $E_{bc}(s)$. It is this phase shift which affects the phase of the current under saturated conditions. If the current i_g is in phase with $i_{g,ref}$ and differs only in magnitude, then the error, e , must also be in phase with i_g . To eliminate the error to the resonator, e' , the compensating signal must also be in phase with the error. However, the compensating signal e_{bc} is in phase with the inverter terminal voltage $v_{inv,ref}$ but the current i_g lags $v_{inv,ref}$. This means that the phase of e_{bc} is also leading that of i_g , and causes the equivalent error e' to be out of phase with the controller input e . By adjusting the ratio in (3.27) the phase shift between the plant input and the signal e_{bc} , can be altered to improve the phase tracking of the current reference when the anti-windup loop is active.

3.4.4 Anti-windup Gain Selection

There are two aspects to be considered in choosing the gains for AW loop: stability of the control loop, and steady state performance while the loop is active. The gains must be chosen such that the output of the virtual impedance loop $v_{inv,ref}$ is limited sufficiently. The magnitude of the reference voltage during saturation conditions depends on the current error e , and on the gains K_I and K_2 . A higher gain K_I will decrease the magnitude of the output u , but excessively large values can cause oscillations in the modulating index and high levels of harmonic distortion. In [10] normalization for the anti-windup gains is shown to remove the effect of the changes in the controller input and output. The normalized values of both K_I and K_2 are defined by (3.28).

$$\hat{K} = \frac{e_{\max}}{U_{\max}} = \frac{i_{g,\max}}{0.5V_{DC}} K \quad (3.28)$$

The normalized gain \hat{K} is obtained by multiplying the gain K by the maximum error input e_{\max} and dividing by the maximum output U_{\max} . For the PV system under consideration this corresponds to the maximum inverter current $i_{g,\max}$ and $0.5V_{DC}$.

The first gain, K_I , is selected using an empirical method to achieve a damped transient response and steady state limiting of $v_{inv,ref}$ at the maximum anticipated error with the gain K_2 set to zero. When the normalized gain $K_I = 1$ the current controller has the maximum error input, the modulation index has a peak value of 3.1 during activation of the AW loop as shown in Figure 3.25. Increasing K_I to 3 reduces the peak modulation index to a value of 1.9 pu peak. Further increasing K_I has a diminishing effect on the amplitude, thus the normalized value of K_I is set to 3.

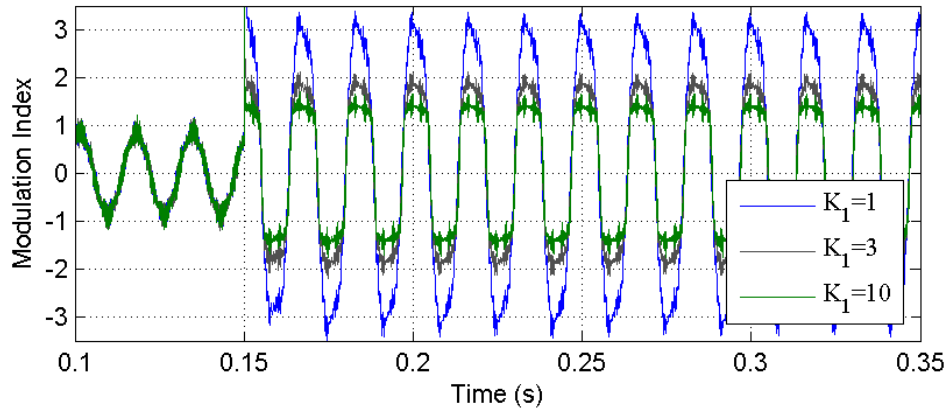


Figure 3.25: Modulation index for phase A with maximum error input and $K_2 = 0$

Next, K_2 is tuned to achieve good phase matching at the nominal power factor of 1.0 using $K_2 \approx 377K_1$ as the starting point. Following this empirical method resulted in normalized values of $K_1 = 3$ and $K_2 = 1000$. The dq axis current components are shown in Figure 3.26 and the modulation index for phase A is shown in Figure 3.27. Figure 3.27 shows that when $K_2 > 0$ the amplitude of the modulation index kept closer to the saturation limit.

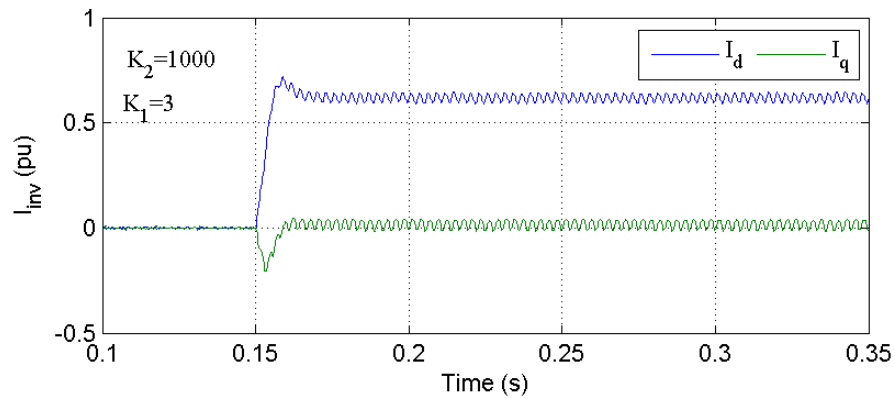


Figure 3.26: dq axis inverter current for $K_2 = 1000$

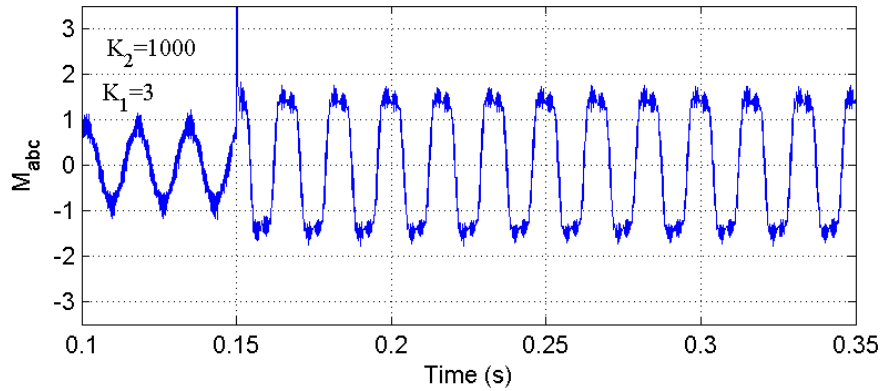
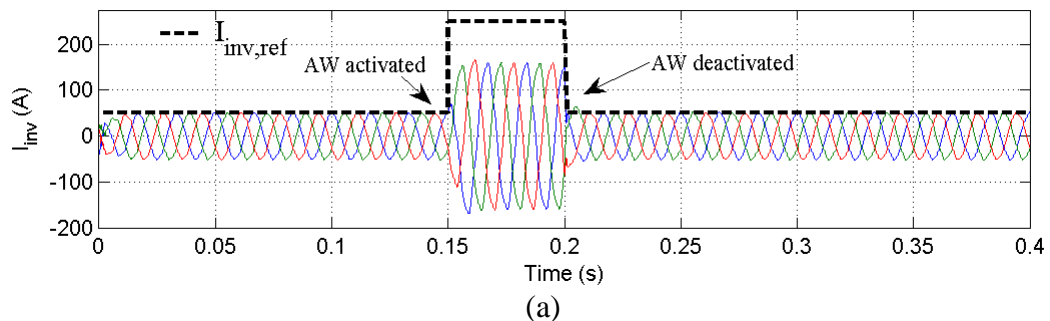


Figure 3.27: Modulation index for phase A with $K_2 = 1000$

3.4.5 Extension to Three-Phase, Three-Wire Inverters

A three-wire system can contain only positive and negative sequence variables, but it is impossible for zero sequence currents to flow in a three-wire system. Following deactivation of the AW loop however, a zero sequence quantity can be observed in the output of the PR controllers. This can cause the inverter reference voltage to be unbalanced and increases current distortion and imbalance. In the test shown in Figure 3.28 the inverter is originally running under normal conditions without activation of the anti-windup loop. At $t = 0.15$ s the current reference increases causing the modulation index to saturate and the anti-windup loop to engage until $t = 0.2$ s when the current reference decreases back to the same value as prior to $t = 0.15$ s. Although the current reference and grid conditions are the same for $t < 0.15$ s and $t > 0.2$ s, after the AW loop is deactivated the PR controller outputs u_{abc} and the modulation index are unbalanced which can be seen in Figure 3.28(b)&(c) respectively. The summation of the PR controller outputs for phases A, B, and C are shown in Figure 3.28(d). According to (2.2) this is equal to three times the zero sequence component of u_{abc} .



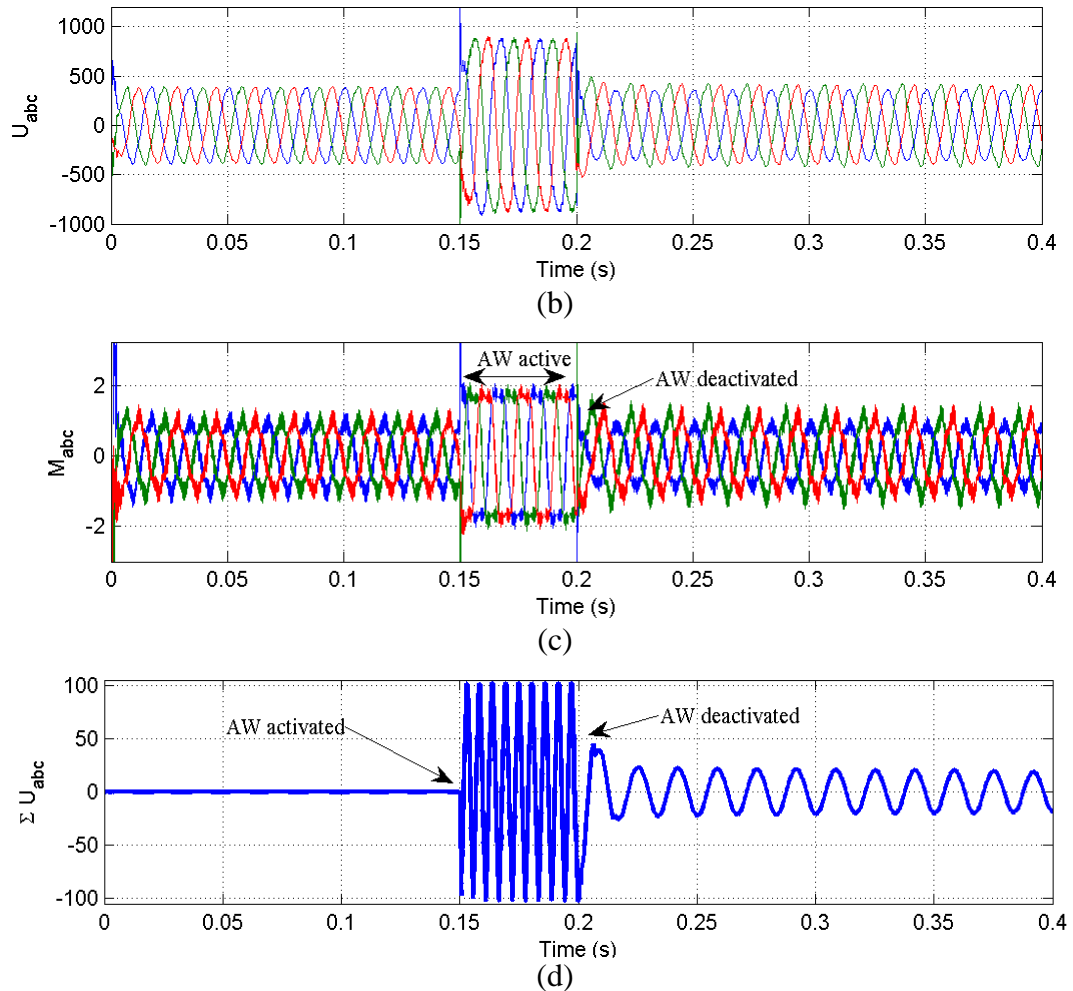


Figure 3.28: (a) Inverter current, (b) PR controller output (d) modulation index, and (c) summation of the three phase controller outputs

After the AW loop is deactivated the current also has slightly higher distortion. The Total Harmonic Distortion (THD) of the inverter current before and after the AW loop is activated is listed in Table 3.3.

Table 3.3: Current THDs before and after saturation

$t < 0.15$ s	$t > 0.2$ s
THD $I_A = 2.8\%$	THD $I_A = 3.4\%$
THD $I_B = 2.8\%$	THD $I_B = 4.4\%$
THD $I_C = 2.8\%$	THD $I_C = 3.0\%$

To solve this problem a slight modification has been made to the controller structure, as shown in Figure 3.29.

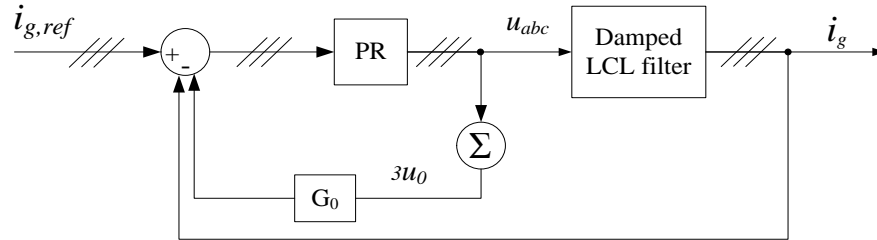


Figure 3.29: Zero sequence elimination loop

To eliminate circulating zero sequence harmonics in the controller, the outputs of the A, B and C phase PR controllers, u_a , u_b , and u_c , are added together to calculate the zero sequence component u_0 (3.29)

$$u_0 = \frac{1}{3}(u_a + u_b + u_c) \quad (3.29)$$

which is multiplied by the gain G_0 and subtracted from the current reference for each phase. The zero sequence feedback loop in Figure 3.29 essentially “reuses” the PR controllers to control the u_0 with the reference amplitude for u_0 being zero. The magnitude of G_0 affects the rate at which the zero sequence is eliminated following deactivation of the anti-windup loop as well as the reduction in the zero sequence controller output u_0 during activation of the AW loop. The value of G_0 in this case selected empirically as $100/3$.

The results from the same test illustrated in Figure 3.28 when the zero-sequence feedback loop is included are shown in Figure 3.30. When the zero sequence feedback loop is included, the controller output and the modulation index are both balanced and return to the pre-saturation values as seen in Figure 3.30(b) and (c) respectively. Once the current reference is reduced and the AW loop deactivates, Figure 3.30(d) shows that the summation of the controller outputs returns to zero, so there is no zero sequence component.

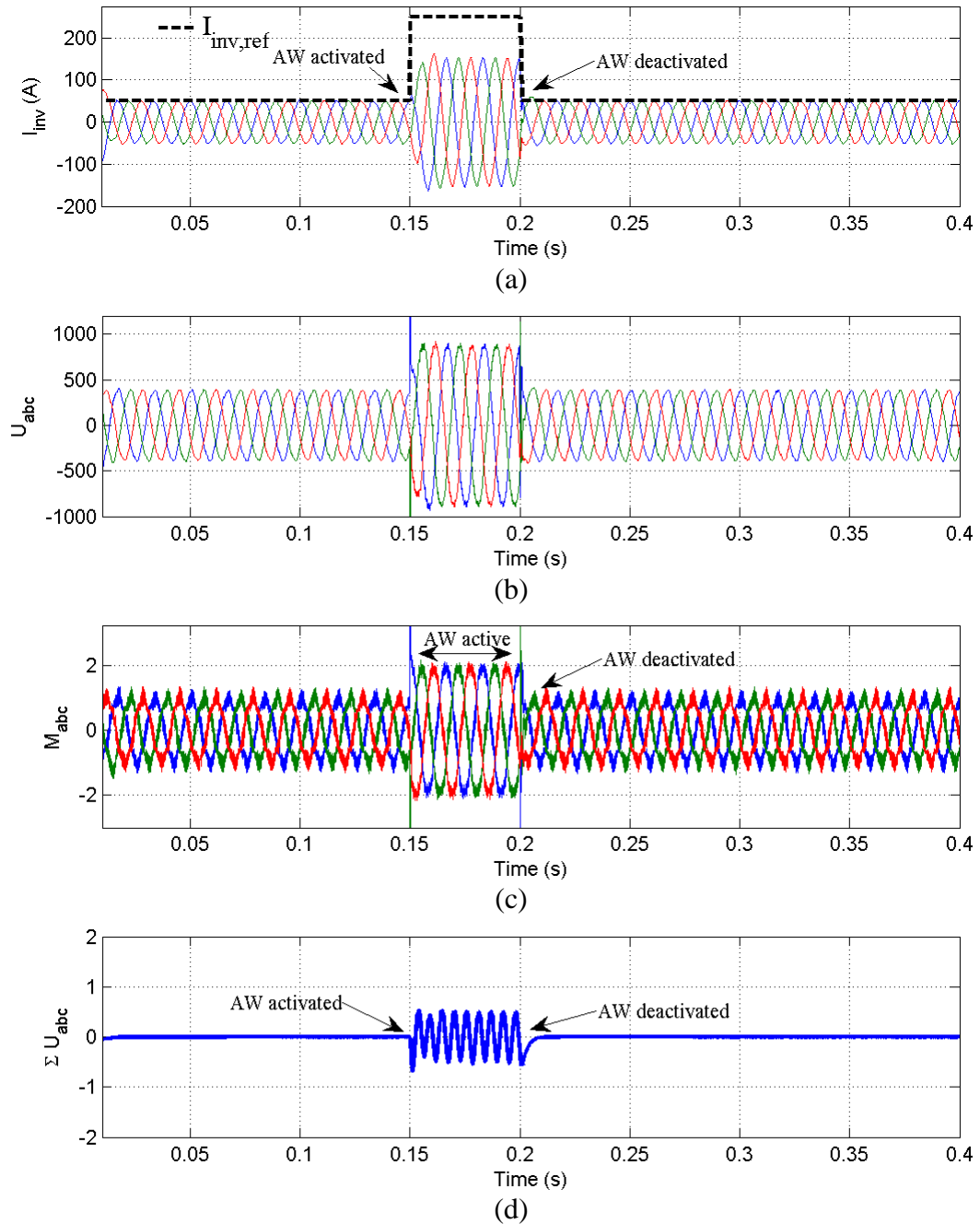


Figure 3.30: (a) Inverter current, (b) PR controller output (d) modulation index, and (c) summation of the three phase controller outputs when zero sequence feedback loop is employed

The inverter current shown in Figure 3.30(a) has a THD of 2.8% in all three phases during $t < 0.15$ s and $t > 0.20$ s. During activation of the AW loop the THD of the inverter current is 2.4% for all three phases.

An alternative solution is to use a PR controller for only two of the three phases and to calculate u_c using (3.30).

$$u_c = -u_a - u_b \quad (3.30)$$

However, this will result in significantly higher levels of distortion in the controller output, and consequently the current, while the anti-windup loop is active. The inverter current and modulation index are shown in Figure 3.31 when (3.30) is used to calculate u_c . The current in Figure 3.31(a) is unbalanced while the AW loop is active. Although the modulation indices in Figure 3.31(b) are highly distorted while the AW loop is active, following deactivation M_{abc} is balanced.

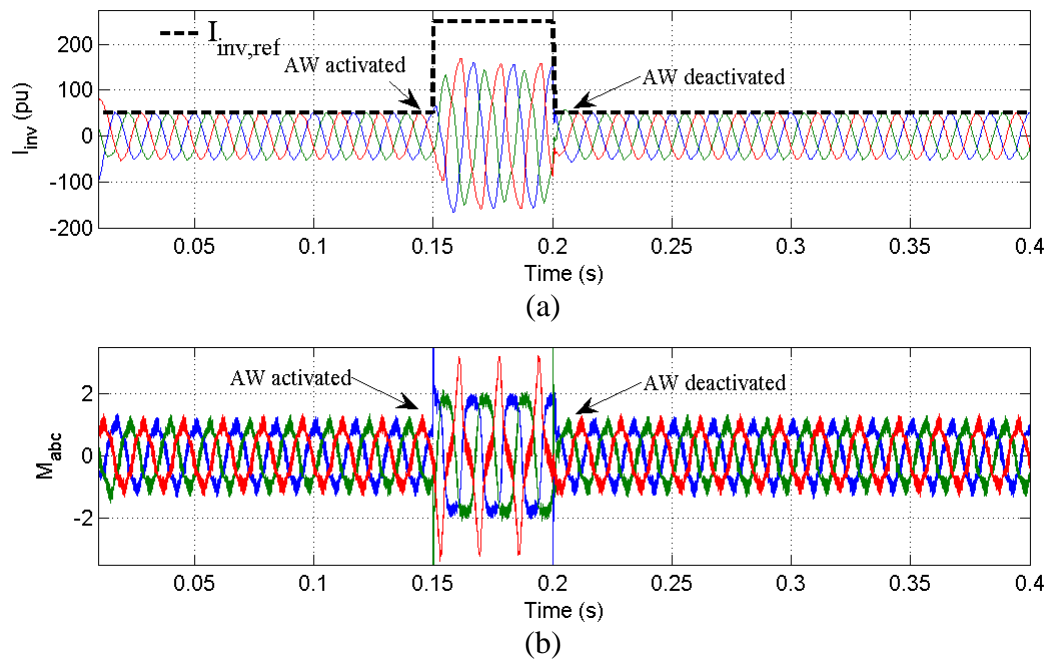


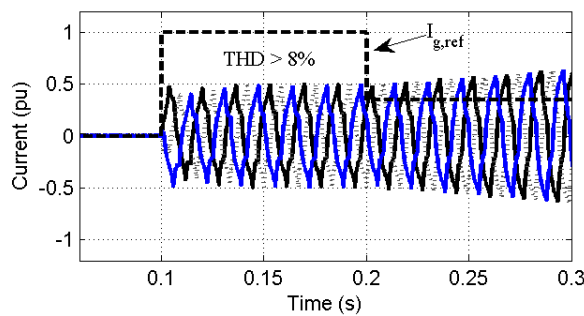
Figure 3.31: (a) Inverter current and (b) modulation index when only two PR controllers are used

From $0.15 \text{ s} < t < 0.2 \text{ s}$, while the AW loop was active, the current THDs were 4.5%, 12.1% and 11.7% for phases A, B and C respectively. This is significantly higher than the 2.4% for all three phases when the zero sequence feedback loop was used in Figure 3.30(a).

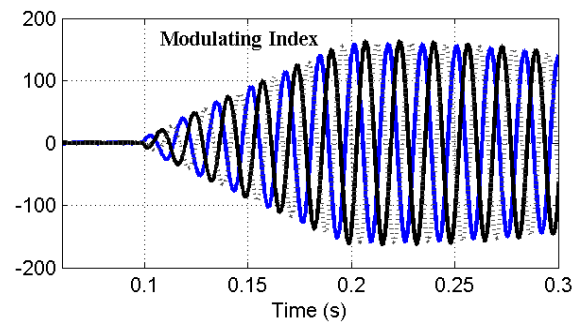
3.4.6 Performance Comparison of the Proposed Anti-Windup Scheme

To test the performance of the anti-windup scheme, an ideal DC voltage is used in place of the PV generator at the DC link. A reference current is given to the PR controllers to

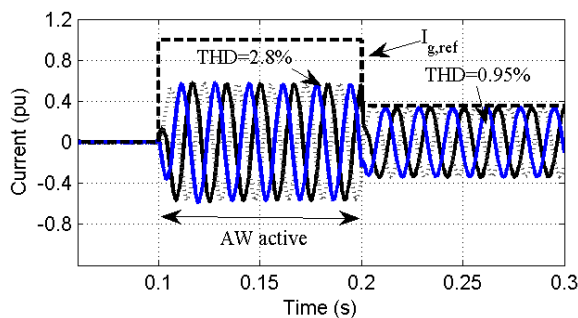
deliberately cause saturation of the modulating index. A current reference with zero quadrature component and a magnitude of 1 pu is given to the current controller. The step in the reference current at $t = 0.1$ s results in saturation of the modulation index, until the current reference is reduced to 0.35 pu 6 cycles later. The results are illustrated in Figure 3.32. Although the dq transformation is not used in the control strategy, the rotating reference frame currents are shown in Figure 3.32(g)&(h) to compare the phase angle of the current with the anti-windup loop activated. Figure 3.32(a) and (b) shows the result when no anti-windup strategy is used. In only 6 cycles, the inverter voltage reference grows to 158 times the saturation limit, and even when the current reference decreases the controller output only decreases slowly, as seen in Figure 3.32(b). Figure 3.32(a) shows the current injected into the grid. A high level of current distortion is visible due to the over-modulation.



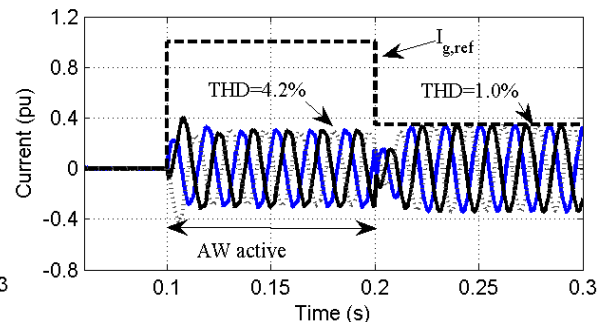
(a)



(b)



(c)



(d)

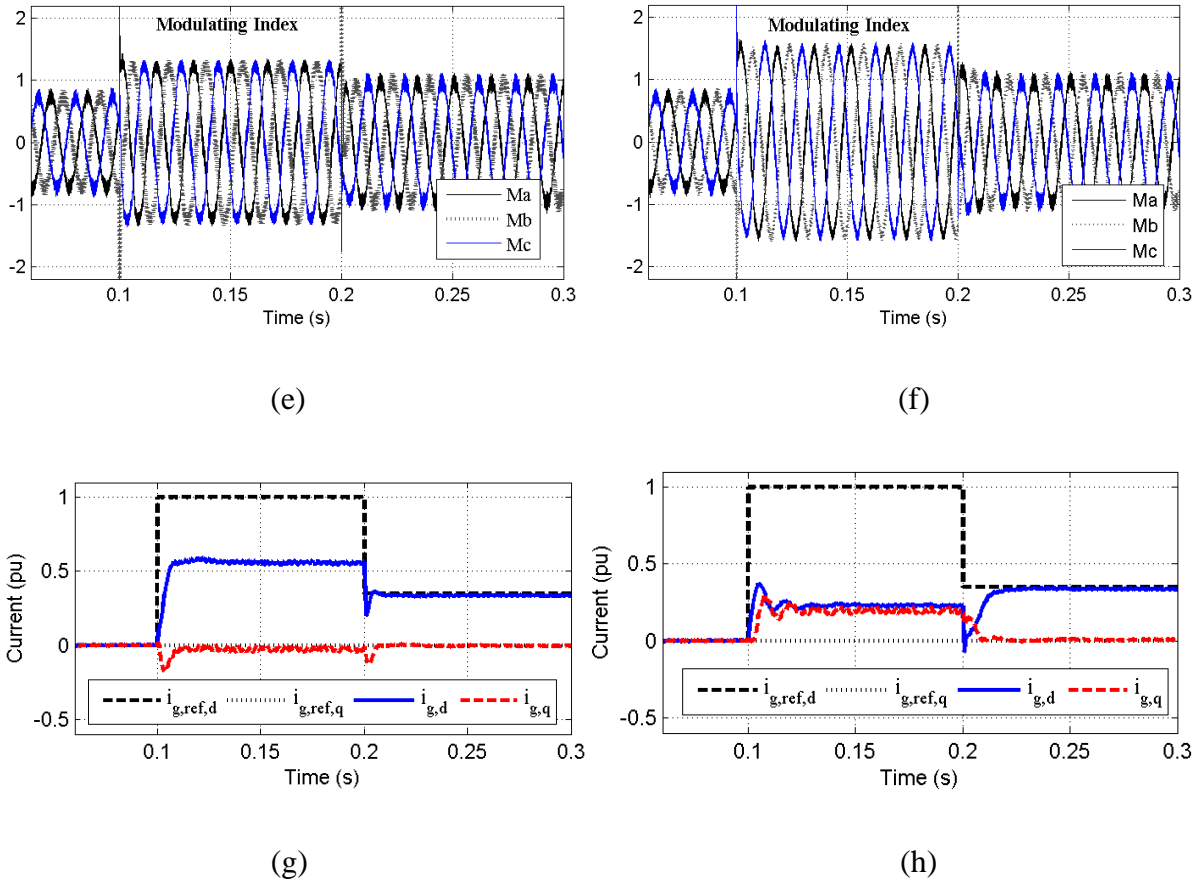


Figure 3.32: Inverter current (a) and modulation index (b) without anti-windup, inverter current (c), modulation index (e) and dq frame current (g) with the proposed AW scheme, and with the AW scheme from [10](d)(f)(h)

When the proposed anti-windup strategy is used, Figure 3.32(c)(e)(g) shows that even during activation of the windup loop the THD of the output current is below the maximum of 5%. Figure 3.32(g) shows that the current closely follows the phase angle of the reference, even though the inverter cannot inject a high enough current to meet the reference. Once the current reference is reduced, the controller quickly tracks the new reference and returns to normal operation. Figure 3.32(d),(f),(h) show that the AW strategy in [10] results in poorer limitation of the input variable, a higher THD, and a phase shift of approximately 45° from the reference current phase. A more oscillatory transient response is observed in Figure 3.32(d) as compared to the proposed strategy.

3.5 DC Link Voltage Control

For a single stage solar power conversion system, the terminals of the PV array are directly connected to the DC link of the inverter. Because the power produced by the array is directly

dependent on the voltage of the array, real power of the system is controlled by controlling the DC bus voltage of the inverter. The DC voltage control loop is shown in Figure 3.33.

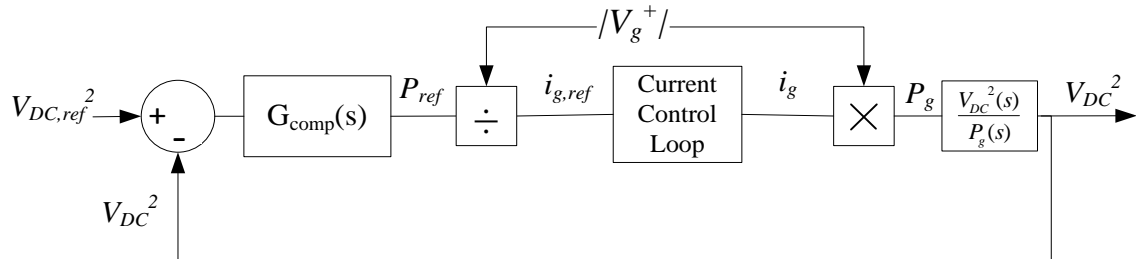


Figure 3.33: Bus voltage control loop

The method in [1] has been adopted in this work to control the DC bus voltage. The control variable is the square of the voltage. In the dual loop strategy a PI controller is used to generate the appropriate current references. The current control loop in labeled in Figure 3.33 can be approximated as a unity gain because the bandwidth is significantly (i.e. more than 10 times) higher than that of the DC link voltage controller loop [1]. The gains are determined by the desired system bandwidth based on the transfer function (3.31) [1].

$$G_{vp}(s) = \frac{V_{DC}^2(s)}{P_g(s)} = \frac{2}{C_{DC}} \left(\frac{\tau_0 s + 1}{s} \right) \quad (3.31)$$

$$\tau_0 = \frac{2 L_{eq} P_{g,0}}{3 V_{g,pk}^2}$$

The equivalent inductance of the filter is $L_{eq} = L_c + L_g$ for the LCL filter configuration [16]. Equation (3.31) indicates that the stability of the system depends on the value of the time constant τ_0 , which is related to the output power output, P_g of the inverter and the grid voltage v_g . A pole-zero compensator is included to increase the phase margin at the worst case, $P_{g,0} = 0$ W, to ensure stability over the whole range of power output. The controller and compensator transfer function is given by (3.32).

$$G_{comp}(s) = \left(\frac{s + p_{comp}}{s + z_{comp}} \right) \frac{k_{dc,p}s + k_{dc,i}}{s} \quad (3.32)$$

The PI controller gains $k_{dc,p}$ and $k_{dc,i}$ are determined based on the desired bandwidth of 200 rad/s. The pole and zero locations of the compensator are chosen to add a 45° phase boost at the crossover frequency. The frequency response of the open loop transfer function $G_{VP}(s)G_{comp}(s)$ is shown in Figure 3.34 below.

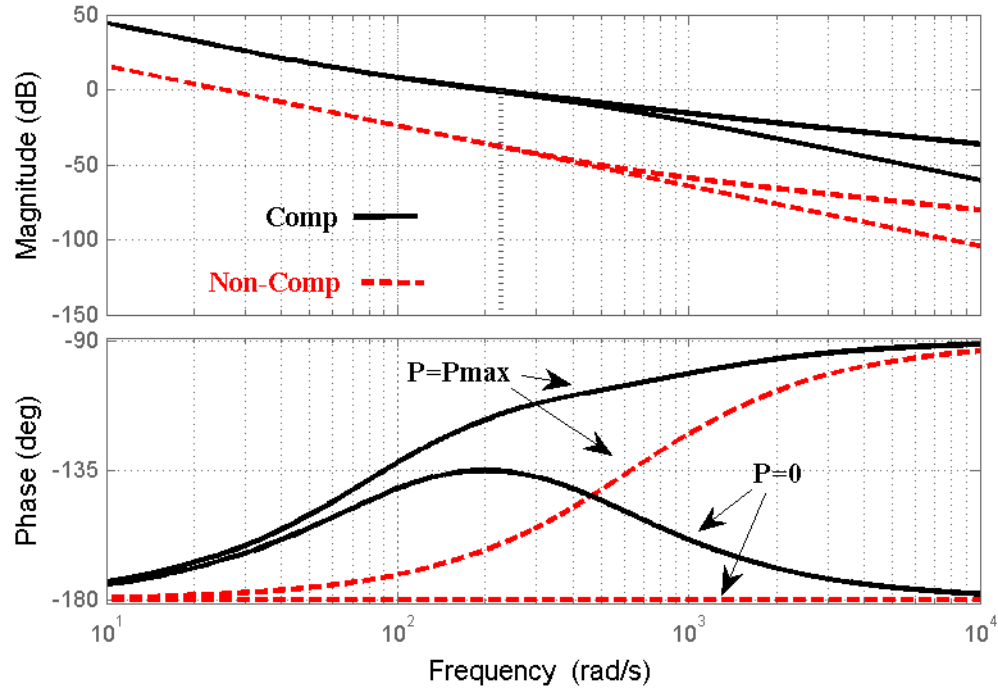


Figure 3.34: Frequency response of the compensated and non-compensated forward loop gains at maximum and minimum output power

When the inverter is injecting an unbalanced three-phase power to the grid, the DC link voltage oscillates at two times the line frequency. If the oscillation is not removed, the bandwidth of the loop must be limited to provide sufficient attenuation of the oscillatory component to avoid distorting the current reference [17]. The second order notch filter of (3.33) is used to attenuate the double line frequency component in the measured DC link voltage, V_{dc} .

$$G_{notch}(z) = \frac{s^2 + \omega_{2f}^2}{s^2 + \omega_{2f} / Q s + \omega_{2f}^2} \quad (3.33)$$

The location of the notch is determined by the frequency ω_{2f} which is set to $2\pi 120$ rad/s. The quality factor Q is chosen as 1.

Although the output of the DC link voltage controller is a DC value, a sinusoidal reference signal must be given to the PR controllers. The amplitude of the current reference is obtained by dividing the output of the PI controller by the peak of the positive sequence component of the grid voltage $|V_g^+|$. The sinusoidal reference current $i_{pv,ref}$ is generated by multiplying the positive sequence three-phase template signals $u_{g,abc}^+$ by the reference current amplitude. Both $|V_g^+|$ and $u_{g,abc}^+$ are calculated using the half-cycle DFT, which is discussed further in Chapter 4.

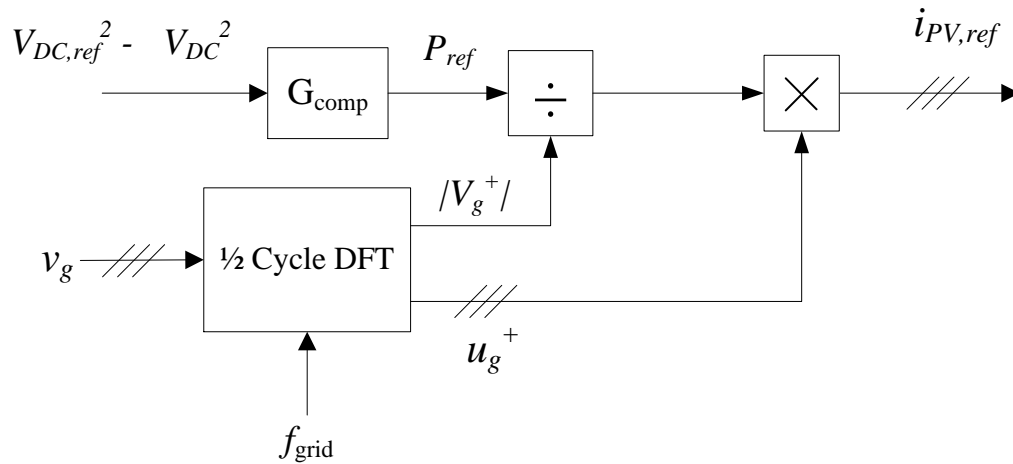


Figure 3.35: Sinusoidal reference current generation

3.6 Frequency Estimation

In the conventional grid, the frequency is tightly regulated. Only very small deviations from the nominal frequency are permitted. In a microgrid however, the lower system inertia may result in greater frequency deviations. Additionally, transient events, and grid connection/disconnection may cause changes in the fundamental frequency which need to be tracked by the control system to ensure proper performance and synchronization with the rest of the grid/microgrid. Phase-Locked Loops (PLLs) are commonly used in the literature for this task. However, it is unnecessary to estimate the phase angle in the proposed control scheme.

Frequency-Locked Loops (FLLs) are simple to implement, do not require trigonometric calculations, and are more immune to phase angle transients than are PLLs [18]. In the proposed inverter control scheme a simple frequency locked loop is used to estimate the grid

frequency based on the positive sequence grid voltage. A block diagram of the FLL is shown in Figure 3.36. The FLL is composed of the SOGI discussed in Chapter 2 along with an additional integrator. This third integrator detects the input frequency by adjusting the value of ω_{est} until the SOGI output V' is equal to the input V_{α^+} .

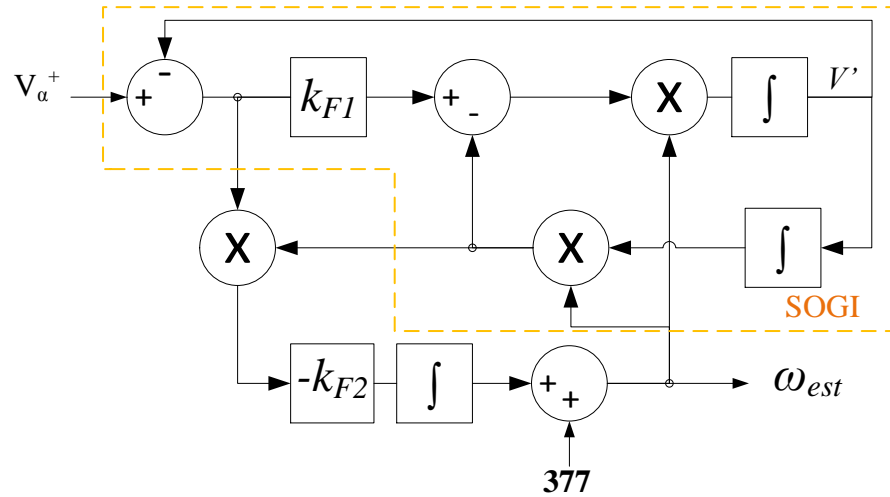


Figure 3.36: Frequency Locked Loop

The gains k_{F1} and k_{F2} determine the settling time of the FLL, and are set to $\sqrt{2}$ and 1 respectively to achieve a settling time of 0.038 s [18]. The output of the FLL is the estimated frequency ω_{est} . Only one phase voltage is required as the input for the FLL. The α component of the positive sequence voltage at the PCC is used as the input. This ensures that even if the voltage is unbalanced the performance of the frequency estimation unit is not affected. The positive sequence calculation method used to obtain V_{α^+} is described in Chapter 4.

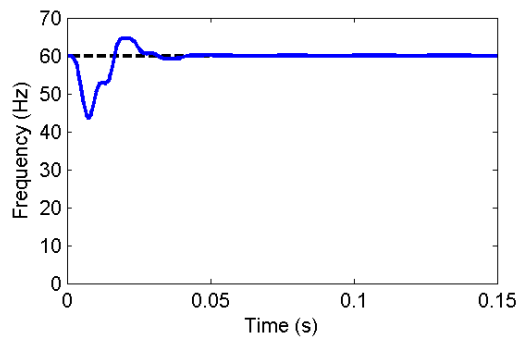


Figure 3.37: Output of the FLL

3.7 Maximum Power Point Tracking

The curves shown in Figure 3.38 indicate that the power production of the PV generator depends on both the environmental conditions and the terminal voltage of the array. In the system under consideration the power is adjusted by controlling the DC bus voltage of the inverter. The operating conditions which result in the maximum power are called the Maximum Power Point (MPP). Because the voltage of the MPP varies with irradiance, temperature and other conditions such as partial shading, an algorithm must be implemented to track the MPP.

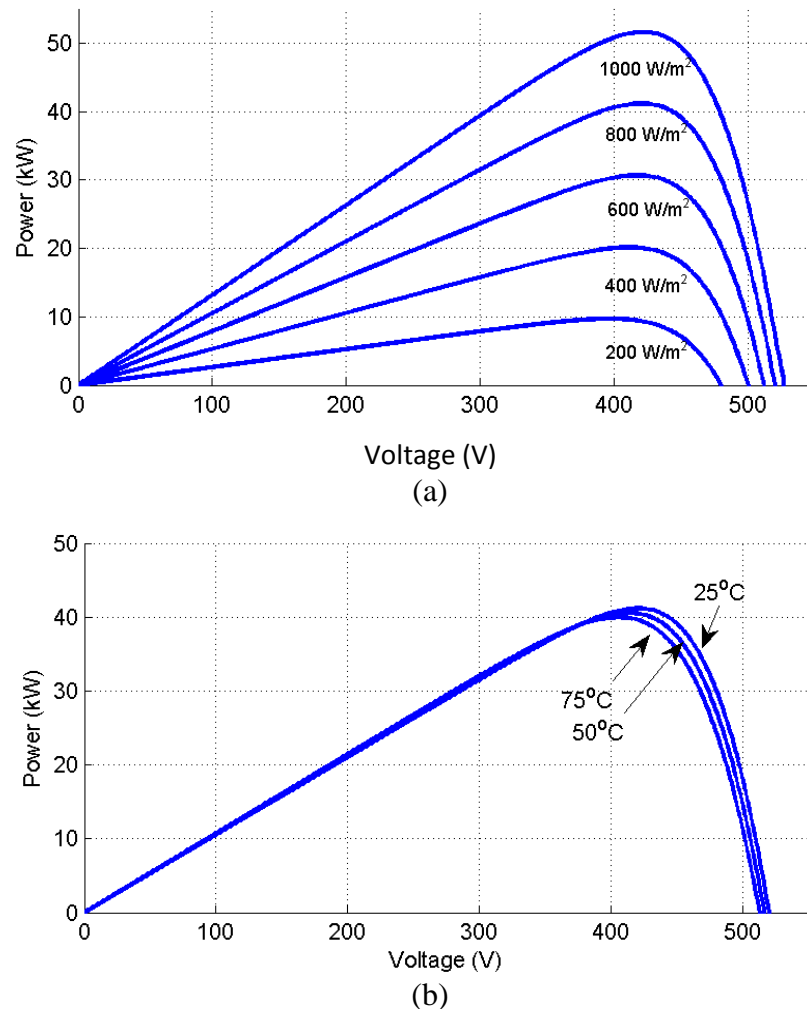


Figure 3.38: Effect of irradiance on P-V curve (a) and effect of temperature variation (b)

Many techniques, known as Maximum Power Point Tracking (MPPT) algorithms have been proposed in the literature [19]-[27]. Hill climbing techniques such as the perturb and observe (P&O) and incremental conductance (INC), are some of the simplest and most prevalent in

practical applications [28]. These two techniques have been shown to be equivalent both mathematically and experimentally by the authors in [29]. For a single stage inverter, the standard P&O algorithm either decreases or increases the DC bus reference voltage by a fixed step size depending on the change in power from the previous step. The voltage must oscillate since all scenarios lead to a perturbation of the voltage. The INC algorithm has an additional step which measures the derivative of the current and does not alter the voltage reference if this is the case because the system is presumed to have reached the steady-state. As with all hill climbing algorithms using a fixed perturbation step the algorithm may be unable to reach the true MPP depending on the starting voltage and width of the voltage step. As shown in [29], although the INC algorithm theoretically allows for zero oscillation, the conditions can rarely be met and both methods result in virtually identical performance.

In this thesis the goal is to examine the effect of negative sequence load current compensation, on the primary function, which is power conversion. For this reason the most widely used algorithm, the P&O technique is adopted. A slight modification however has been made to the P&O algorithm to allow the voltage to reach a steady value. The algorithm shown in Figure 3.39 also compares the change in power to a certain minimum threshold. If this is the case, the change in voltage for the next step will be set to zero. This takes advantage of the fact that at the MPP the slope of the P-V curve is almost zero, and only small changes in power occur between voltage steps. Keeping in mind the analysis of [29], this modification results in a specific implementation of the INC algorithm. The value of P_{min} can be set according to the maximum slope of the P-V curve under low irradiance conditions. In this case the value has been set to 0.1% of P_{max} or 50 W. A higher value of P_{min} would result in greater potential power loss, while smaller values were found to be difficult to distinguish from noise in the signal. The modification does not guarantee the complete removal of oscillations in all circumstances, but for a minimal increase in complexity and no reduction in speed of tracking the voltage oscillation inherent in the standard P&O algorithm can be removed.

Figure 3.39 shows the P&O algorithm used in this control scheme. The first step in the algorithm is to calculate the difference between the DC link voltage and PV power at the current time step, n , and the previous step, $n-1$. If the change in power is less than P_{min} , the voltage reference is held constant. Otherwise, the sign of the voltage change is checked. If

the voltage has decreased and power has increased, the voltage reference is decremented. If power has decreased, the voltage is incremented. If the voltage and the power have increased from the previous step, the voltage reference will be increased. Otherwise, the voltage reference decreases. The value of the voltage perturbation, ΔV , and the time step of the algorithm are chosen according to the guidelines given in [28] as 4 V and 50 ms respectively. The performance of the P&O algorithm is demonstrated in Chapter 6.

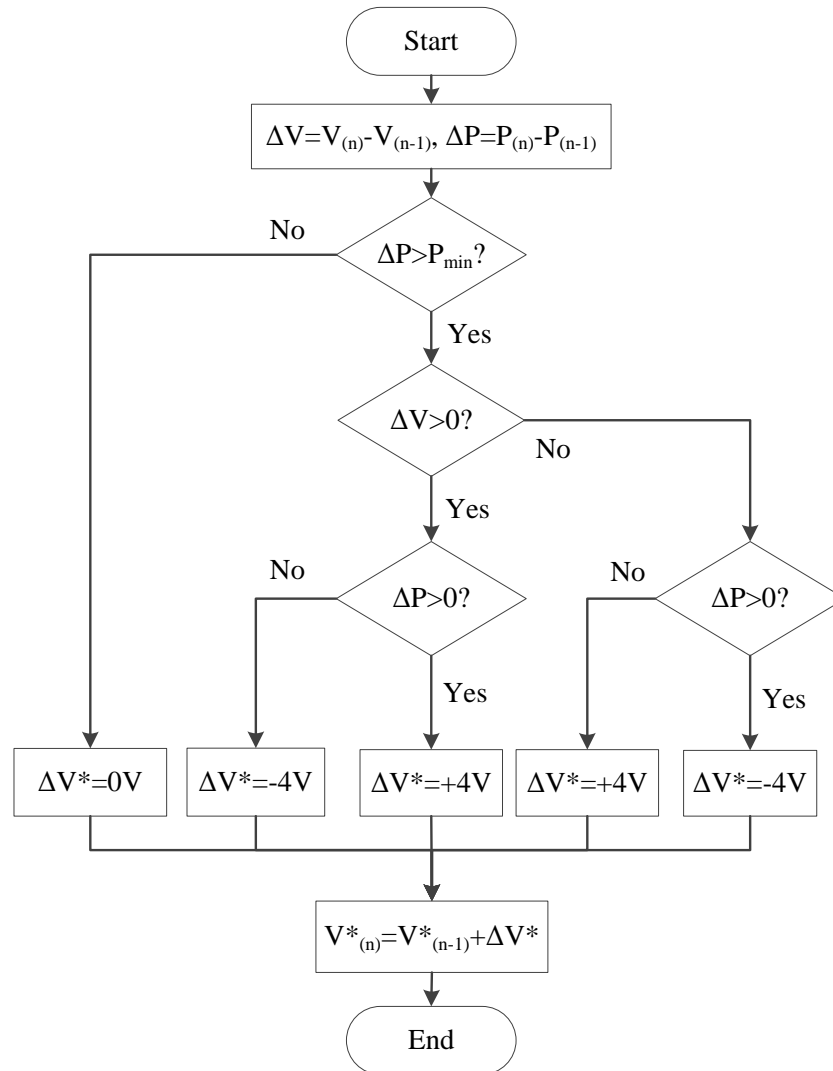


Figure 3.39: P&O MPPT algorithm

3.8 Conclusion

In Chapter 3 a control scheme for a three-phase PV inverter has been designed and analyzed. A linear model of the LCL filter is presented. An active damping scheme for the inverter is proposed and described. This method uses feedback of both the inverter-side current and the

filter capacitor current to damp the resonance of the LCL filter. Because two feedback variables are used, the damping ratio can be directly specified and no iteration is required in calculating the feedback gains. Using the inner inductor current in addition to the capacitor current increases the phase margin and reduces the low frequency gain. Using the transfer function of the damped LCL filter, a method of calculating the gains for a PR controller based on phase and gain margin specifications has been shown. The current control loop had a $\frac{1}{2}$ cycle step response time. A modification is proposed for a PR controller to prevent resonator windup. The proposed anti-windup scheme compares the output of the active damping loop to a maximum and minimum value based on the DC link voltage. If the limits are exceeded, the difference is subtracted from the input of the resonator. Compared to previously proposed anti-windup methods for PR controllers, the scheme presented in this chapter has been shown to more accurately track the phase of the current reference. The DC link voltage control scheme discussed in [1] is considered. An FLL was designed to estimate the grid frequency. Finally, the well-known P&O technique for maximum power point tracking has been adopted.

3.9 References

- [1] A. Yazdani and R. Iravani, *Voltage-Sourced Converters in Power Systems*. Toronto, Canada: Wiley, 2010.
- [2] K. Ogata, "Basic Control Actions and Response of Control Systems," in *Modern Control Engineering*, 3rd ed., Upper Saddle River, NJ: Prentice Hall, 1997, pp. 230.
- [3] J. Dannehl, F.W. Fuchs, S. Hansen, and P.B. Thøgersen, "Investigation of Active Damping Approaches for PI-Based Current Control of Grid-Connected Pulse Width Modulation Converters With LCL Filters," *IEEE Trans. Ind. Applicat.*, vol.46, no.4, pp.1509-1517, Jul.-Aug. 2010.
- [4] J. Xu, S. Xie and T. Tang, "Evaluations of current control in weak grid case for grid-connected LCL-filtered inverter," *IET Power Electron.*, vol. 6, no. 2, pp. 227-234, Feb. 2013.
- [5] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan and K. Weng, "Step-by-Step Controller Design for LCL-Type Grid-Connected Inverter with Capacitor-Current-Feedback Active-Damping," *IEEE Trans. Power Electron.*, vol.29, no.3, pp.1239-1253, Mar. 2014.
- [6] X. Yuan, W. Merk, H. Stemmler and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for

- current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Trans. Ind. Applicat.*, vol. 38, no. 2, pp. 523-532, Mar. 2002.
- [7] B.A. Francis and W.M. Wonham, "The internal model principle for linear multivariable regulators," *Appl. Math. Optimization*, vol. 2, no. 2, pp. 170-194, 1975.
- [8] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu and F. Liu, "Parameter Design of a Two-Current-Loop Controller Used in a Grid-Connected Inverter System With LCL Filter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4483-4491, Nov. 2009.
- [9] A.G. Yepes, F.D. Freijedo, O. Lopez and J. Doval-Gandoy, "High-Performance Digital Resonant Controllers Implemented With Two Integrators," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 563-576, Feb. 2011.
- [10] S. A. Richter and R. W. De Doncker, "Digital proportional-resonant (PR) control with anti-windup applied to a voltage-source inverter," in *Proc. 14th European Conf. Power Electron.and Applicat.(EPE)*, 2011, pp. 1-10.
- [11] A.G. Yepes, F.D. Freijedo, J. Doval-Gandoy, O. López, J. Malvar and P. Fernandez-Comesaña, "Effects of Discretization Methods on the Performance of Resonant Controllers," *IEEE Trans. Power Electron.*, vol.25, no. 7, pp.1692-1712, July 2010.
- [12] N. Bottrell and T.C. Green, "Comparison of Current-Limiting Strategies During Fault Ride-Through of Inverters to Prevent Latch-Up and Wind-Up," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3786-3797, July 2014.
- [13] R. Teodorescu, F. Blaabjerg, U. Borup and M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," in *Proc. IEEE 19th Annu. Appl. Power Electron. Conf. and Expo.(APEC)*, 2004, vol.1, pp. 580-586.
- [14] A. Ghoshal and J. John, "Anti-windup schemes for proportional integral and proportional resonant controller," presented at *Nat. Power Electron. Conf., IIT-Roorkee*, 2010.
- [15] R. Mishra and A. Shukla, "A Proportional Resonator-based control scheme to suppress AC components in circulating current of Modulator Multilevel Converter," in *Proc. IEEE 39th Annu. Conf. Ind. Electron. Soc.(IECON)*, 2013, pp.6170-6175.
- [16] R. Peña-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez and T. Kerekes, "A Self-commissioning Notch Filter for Active Damping in a Three-Phase LCL -Filter-Based Grid-Tie Converter," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6754-6761, Dec. 2014.
- [17] T. Messo, J. Jokipii, J. Puukko and T. Suntio, "Determining the Value of DC-Link Capacitance to Ensure Stable Operation of a Three-Phase Photovoltaic Inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 665-673, Feb. 2014.

- [18] P. Rodríguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu and F. Blaabjerg, "Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions," *IEEE Trans. Ind. Electron.*, vol.58, no.1, pp.127-138, Jan. 2011.
- [19] A.K. Abdelsalam, A.M. Massoud, S. Ahmed and P. Enjeti, "High-Performance Adaptive Perturb and Observe MPPT Technique for Photovoltaic-Based Microgrids," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1010-1021, Apr. 2011.
- [20] M.A.G. de Brito, L. Galotto, L.P. Sampaio, G. de Azevedo e Melo and C. A. Canesin, "Evaluation of the Main MPPT Techniques for Photovoltaic Applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 1156-1167, Mar. 2013.
- [21] K.H. Hussein, I. Muta, T. Hoshino and M. Osakada, "Maximum photovoltaic power tracking: an algorithm for rapidly changing atmospheric conditions," *IEE Proc. Gener. Transm. Distrib.*, vol. 142, no. 1, pp. 59-64, Jan. 1995.
- [22] S.K. Kollimalla and M.K. Mishra, "A Novel Adaptive P&O MPPT Algorithm Considering Sudden Changes in the Irradiance," *IEEE Trans. Energy Convers.*, vol. 29, no. 9, pp. 602-610, Sept. 2014.
- [23] Yihua Hu, Wenping Cao, Jiande Wu, Bing Ji and D. Holliday, "Thermography-Based Virtual MPPT Scheme for Improving PV Energy Efficiency Under Partial Shading Conditions," *IEEE Trans. Power Electron.*, vol. 29, no.11, pp. 5667-5672, Nov. 2014.
- [24] Q. Mei, M. Shan, L. Liu and J.M. Guerrero, "A Novel Improved Variable Step-Size Incremental-Resistance MPPT Method for PV Systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2427-2434, June 2011.
- [25] F. Liu, S. Duan, F. Liu, B. Liu and Y. Kang, "A Variable Step Size INC MPPT Method for PV Systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2622-2628, July 2008.
- [26] K. Sundareswaran, S. Peddapati and S. Palani, "MPPT of PV Systems Under Partial Shaded Conditions Through a Colony of Flashing Fireflies," *IEEE Trans. Energy Convers.*, vol. 29, no. 6, pp. 463-472, June 2014.
- [27] V.V.R. Scarpa, S. Buso and G. Spiazzi, "Low-Complexity MPPT Technique Exploiting the PV Module MPP Locus Characterization," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1531-1538, May 2009.
- [28] N. Femia, G. Petrone, G. Spagnuolo and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Trans. Power Electron.*, vol. 20, no. 7, pp. 963-973, July 2005.
- [29] D. Sera, L. Mathe, T. Kerekes, S.V. Spataru and R. Teodorescu, "On the Perturb-and-Observe and Incremental Conductance MPPT Methods for PV Systems," *IEEE J. Photovolt.*, vol. 3, no. 3, pp. 1070-1078, July 2013.

Chapter 4

4 Calculation of the Negative Sequence Current Component

In this chapter the method used for calculating the negative sequence of the load current is shown and compared to existing techniques for calculating negative sequence components. For control applications the calculation of sequence components must be accomplished in real time using no more than the available processing power. Several techniques for the calculation of symmetrical components were presented in Chapter 2. In this chapter, the work presented in [1] is extended for the calculation of the negative sequence current component using a compensated Half-Cycle Discrete Fourier Transform (HCDFT). Section 4.1 provides a brief introduction to the Discrete Fourier Transform (DFT). The method for calculating the accurate negative sequence components is then derived. This method is evaluated and compared with existing algorithms in section 4.2. Section 4.3 describes the integration of the HCDFT into the inverter control structure.

4.1 Negative Sequence Calculation

The DFT is a well-established method of processing power system signals for protection, monitoring, and control applications [2]. It is well suited for noisy environments because harmonics can be eliminated. The output of the DFT algorithm for a signal $x(n)$ with frequency f_g sampled at f_s , is a phasor quantity X_N . It can be calculated from (4.1).

$$X_N = \frac{2}{N} \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi}{N}n} \text{ where } N = \frac{f_s}{f_g} \quad (4.1)$$

If the input signal is a continuous time sinusoid defined by (4.2), then (4.1) can be rewritten as (4.3),

$$x(t) = \cos(2\pi f t + \theta) \Rightarrow x(n) = \cos\left(\frac{2\pi}{N}n + \theta\right) \quad n=0,1 \dots N-1 \quad (4.2)$$

$$X_N = \frac{2}{N} \sum_{n=0}^{N-1} \cos\left(\frac{2\pi}{N}n + \theta\right) e^{-j\frac{2\pi}{N}n} \quad (4.3)$$

where N is the number of samples per period of the fundamental. According to Euler's formula (4.4) the exponential term in (4.3) can be decomposed into a real and an imaginary component (4.5).

$$e^{-j\frac{2\pi}{N}n} = \cos\left(\frac{2\pi}{N}n\right) - j\sin\left(\frac{2\pi}{N}n\right) \quad (4.4)$$

$$X_N = \frac{2}{N} \sum_{n=0}^{N-1} \cos\left(\frac{2\pi}{N}n + \theta\right) \cos\left(\frac{2\pi}{N}n\right) - j \frac{2}{N} \sum_{n=0}^{N-1} \cos\left(\frac{2\pi}{N}n + \theta\right) \sin\left(\frac{2\pi}{N}n\right) \quad (4.5)$$

The two terms on the right hand side of (4.5) are respectively referred to as the real filter and the imaginary filter. The outputs of the two filters are the fundamental component of the original input signal and its 90° phase shift. From these two values the amplitude of the signal and the phase angle can be calculated. If the DFT output X_N is recalculated each time a new sample is added, at each sample time the angle will shift forward by $2\pi/N$ radians. In the time domain this leads to a counter clockwise rotation of the measured angle. Following a disturbance in the input signal (change in amplitude or phase), the correct output will be reached once N post-disturbance samples have been obtained. For the full-cycle DFT this translates into a fixed settling time of one cycle of the fundamental frequency, i.e. 16.6 ms for a 60 Hz signal.

This can be observed in Figure 4.1. A sinusoidal input signal with frequency $f_g = 60$ Hz is shown in Figure 4.1(a) along with phasor magnitude estimated by a full-cycle DFT algorithm with $N = 64$. At $t = 0.25$ s the amplitude of the input signal drops by 50%. The DFT magnitude reaches its new value at $t = 0.266$ s, which is one cycle after the disturbance to the input. Figure 4.1(b) shows the rotating phase angle measured by the DFT.

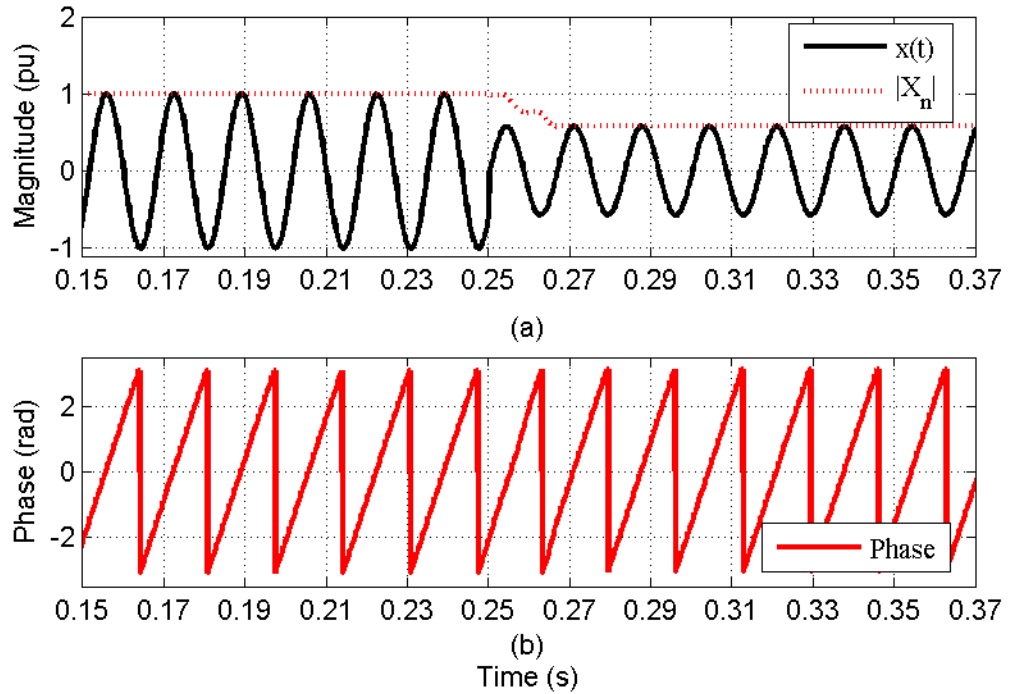


Figure 4.1: (a) Input signal and DFT magnitude and (b) phase

4.1.1 The Half-Cycle DFT

Another well-known phasor estimation technique is the Half-Cycle DFT, given by (4.6).

$$X_N = \frac{2}{M} \sum_{n=0}^{M-1} x(n) e^{-j \frac{\pi}{M} n} \quad \text{where } M = \frac{N}{2} = \frac{f_s}{2f_g} \quad (4.6)$$

The coefficients of the real and imaginary filters for the HCDFT are calculated by (4.7).

$$\begin{aligned} \text{Re} : \cos\left(\frac{\pi}{M} n\right) \\ \text{Im} : \sin\left(\frac{\pi}{M} n\right) \end{aligned} \quad n = 0, 1, \dots, (M-1) \quad (4.7)$$

M samples per half cycle are taken as inputs for the HCDFT. Because it needs only half the number of samples required for the full cycle DFT, the HCDFT has a settling time of one half of a cycle, which is 8.333 ms for a 60 Hz grid. Figure 4.2 shows the response of the half and full cycle DFT algorithms.

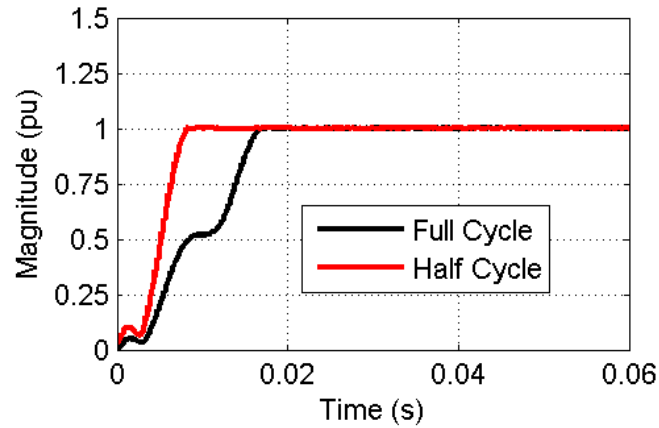
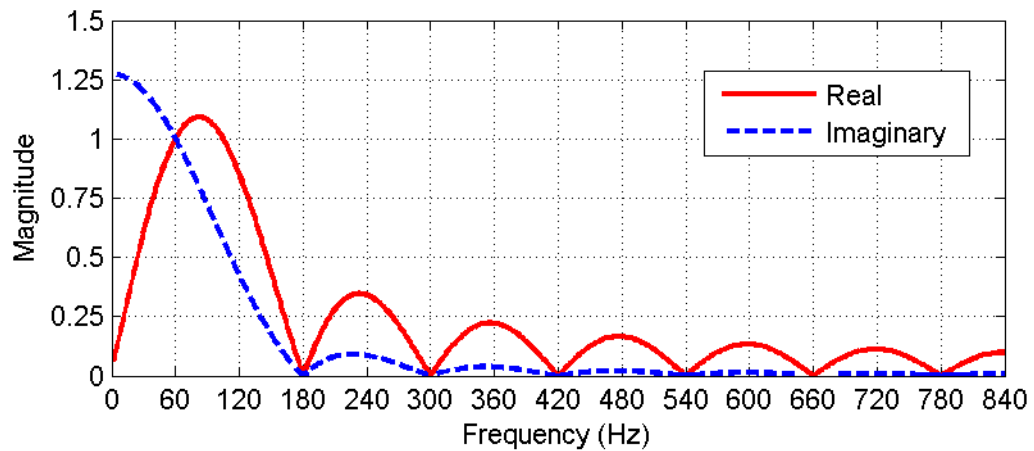


Figure 4.2: Settling time of the Full and Half cycle DFT

The shorter window length of the HCDFT also results in a poorer frequency response, as even harmonics are no longer completely rejected. For the application in this thesis however, it is an acceptable trade-off for the shorter settling time. The limits for even harmonics are much lower than for the odd harmonics, most concerning are the 5th, 7th, and 11th harmonics, which can be completely eliminated by the HCDFT. The frequency responses of the real and imaginary filters of the HCDFT are shown in Figure 4.3.



(a)

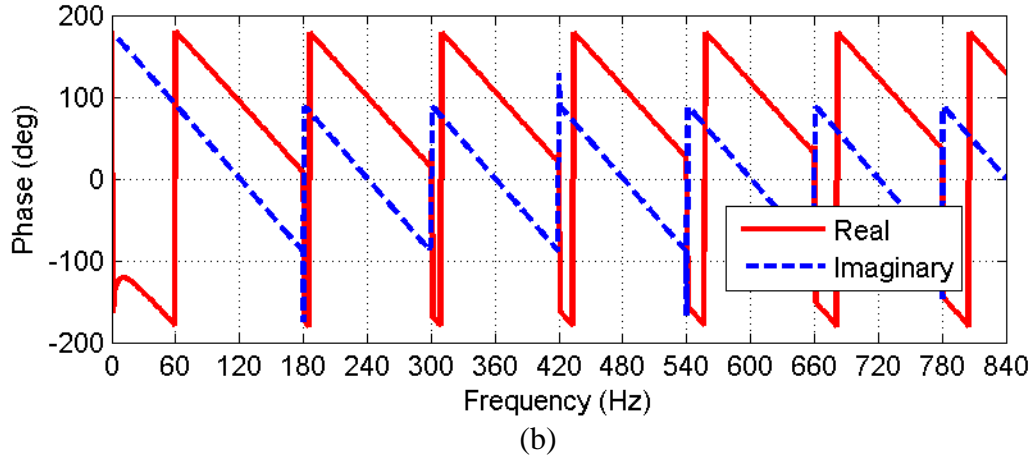


Figure 4.3: (a) Magnitude and (b) phase of the discrete-time frequency response of the HCDFT

The frequency response shows that the HCDFT completely rejects all odd harmonics of the fundamental and attenuates the even harmonics. The harmonics of interest in most power systems, i.e. the 3rd, 5th, 7th, and 11th, are filtered by the HCDFT.

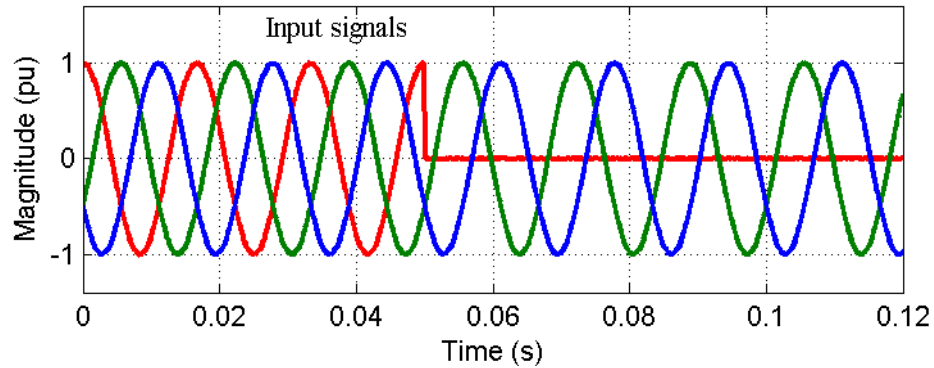
Because the HCDFT has a sampled signal for its input, only signals up to $f_s/2$ can be properly represented. A typical way to solve this problem is to process the signal through an anti-aliasing filter prior to performing the DFT. No anti-aliasing filter has been used in the proposed control scheme since the frequency $f_s/2$ corresponds to the 32nd harmonic. Stringent limits are placed on such high order current harmonics and which also limits possible errors due to aliasing. An anti-aliasing filter could be readily included if it is deemed to be worth the additional implementation complexity.

4.1.2 Negative Sequence Calculation in the Phasor Domain

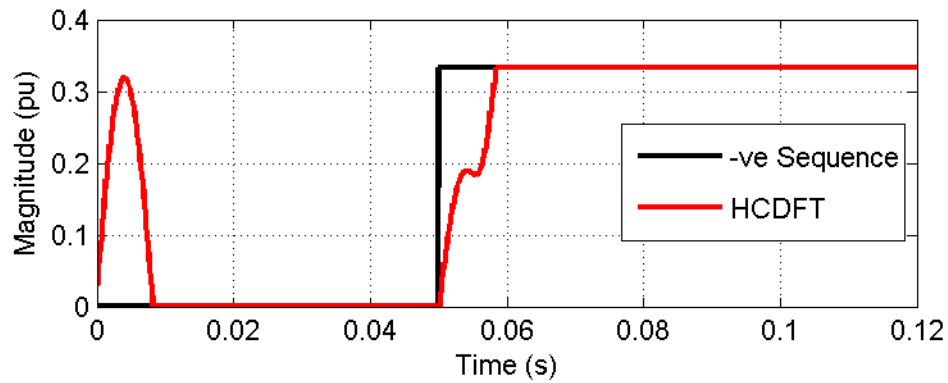
The symmetrical sequence components of a three-phase system, introduced in Chapter 2, are redefined for convenience in (4.8). Equation (4.8) can be applied to the phasor of the DFT, or directly to the outputs of the real and imaginary filters using ISC theory.

$$\begin{bmatrix} f^0 \\ f^- \\ f^+ \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}, \quad a = 1 \angle 120^\circ \quad (4.8)$$

Figure 4.4 shows the magnitude of the negative sequence calculated by the HCDFT when the load is suddenly removed from one phase. Prior to the load being removed, all three phases are balanced. The response time of the negative sequence calculation is equal to the settling time of the HCDFT, or $\frac{1}{2}$ cycle.



(a)



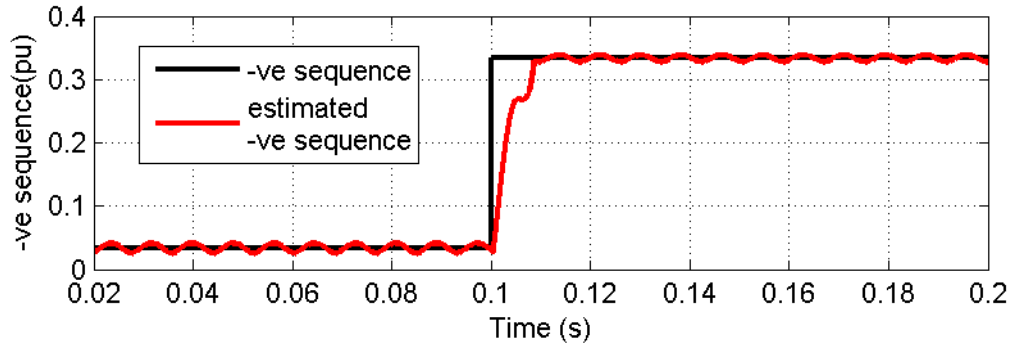
(b)

Figure 4.4: (a) Three-phase load current, and (b) the magnitude of the $-ve$ sequence calculated by the HCDFT

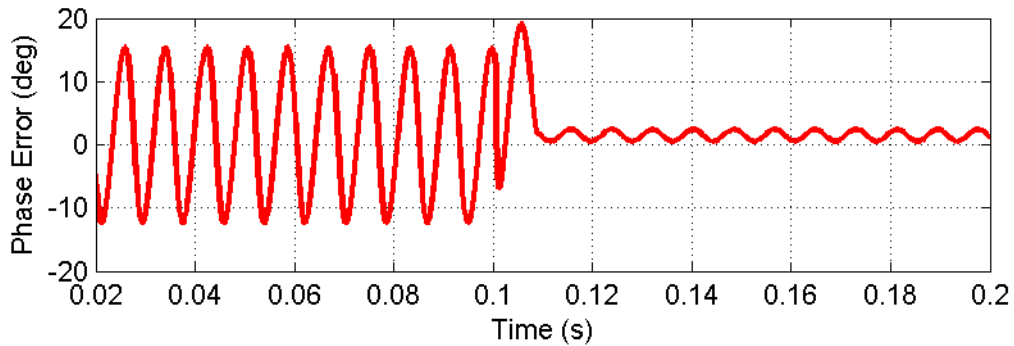
4.1.3 Numerical Compensation for Off-Nominal Frequency

When the grid frequency varies from the nominal value, the negative sequence phasor estimated by the HCDFT will contain errors because $f_g \neq f_s/N$. If the three-phase signals are unbalanced, significant errors can be observed in the magnitude and phase of the calculated sequence values. Figure 4.5(a) shows the magnitude of the negative sequence output of the HCDFT for a 60.9 Hz input. In this case, the error does not settle to zero and the magnitude has a noticeable AC component. Figure 4.5(b) shows the error in the estimated phase angle.

When the negative sequence component is small, the angle error has a large oscillating component with an amplitude of over 15° as well as a DC error.



(a)



(b)

Figure 4.5: (a) Negative sequence magnitude and (b) phase error under off nominal frequency conditions, with $f_g = 60.9\text{Hz}$

There are several ways of dealing with the problem of variable grid frequency. One way is to implement a variable sampling rate such that the number of samples per cycle remains constant. Another technique, known as “adaptive windowing”, is to adjust the number of samples per cycle N , based on the grid frequency so that $f_s/N \approx f_g$. The first method is complicated to implement in a microcontroller which relies on fixed sampling frequency. The second method will result in non-negligible error unless a very high sampling frequency is used. Following the method proposed in [1], a numerical compensation method is used in combination with adaptive windowing. Reference [1] presents a quantification of the error resulting from the frequency variation, as well as a method of numerically compensating the resulting error. However, the focus is on extracting the angle of the positive sequence

voltage. All derivations are done for a full-cycle DFT. To meet the controller performance requirements outlined in Chapter 1, the HCDFDFT is used in this thesis to compute the negative sequence current.

4.1.4 Estimated Error of the Fundamental Phasor due to Off-Nominal Frequency

The method outlined in [1] for quantifying the error and calculating the accurate phasor has been adapted in the following section to compute the negative sequence quantities using a HCDFDFT algorithm. The input signal $x(n)$ is assumed to be a sampled sinusoid an amplitude V_m , phase angle of θ and frequency f_g (4.9).

$$x(n) = V_m \cos\left(\frac{2\pi f_g}{f_s} n + \theta\right) \quad (4.9)$$

The calculated HCDFDFT can be written as (4.10).

$$X_N = \frac{2V_m}{M} \sum_{n=0}^{M-1} \cos\left(\frac{2\pi f_g}{f_s} n + \theta\right) e^{-j\frac{\pi}{M}n} \quad (4.10)$$

If the HCDFDFT filter is designed for a nominal frequency f_n such that

$$f_n = \frac{f_s}{2M}, \quad (4.11)$$

Then (4.10) can be rewritten as (4.13).

$$X_N = \frac{V_m}{M} \sum_{n=0}^{M-1} \left(e^{jn\pi\left(\frac{f_g}{f_n}-1\right)} e^{j\theta} + e^{-jn\pi\left(\frac{f_g}{f_n}+1\right)} e^{-j\theta} \right) \quad (4.12)$$

$$X_N = \frac{V_m}{M} e^{j\theta} \frac{1 - e^{j\pi\left(\frac{f_g}{f_n}-1\right)}}{1 - e^{j\pi\left(\frac{f_g}{f_n}-1\right)}} + \frac{V_m}{M} e^{-j\theta} \frac{1 - e^{-j\pi\left(\frac{f_g}{f_n}+1\right)}}{1 - e^{-j\pi\left(\frac{f_g}{f_n}+1\right)}} \quad (4.13)$$

If the corrected fundamental phasor, X_{Ng} , without the error accrued due to frequency mismatch, is defined in (4.14), (4.13) can be written in terms of the accurate phasor and its complex conjugate X_{Ng}^* (4.15).

$$X_{N_g} = V_m e^{j \frac{\pi f_g}{M f_n} (M-1) + \theta} \quad (4.14)$$

$$X_N = X_{N_g} \frac{e^{-j \frac{\pi f_g}{f_n} \left(1 - \frac{1}{M}\right)} 1 - e^{j \pi \left(\frac{f_g}{f_n} - 1\right)}}{M} + X_{N_g}^* \frac{e^{j \frac{\pi f_g}{f_n} \left(1 - \frac{1}{M}\right)} 1 - e^{-j \pi \left(\frac{f_g}{f_n} + 1\right)}}{M} \quad (4.15)$$

$$X_N = X_{N_g} k_1 + X_{N_g}^* k_2 \quad (4.16)$$

Equation (4.16) indicates that the estimated phasor X_N and the accurate phasor X_{N_g} are related by two complex error coefficients, k_1 and k_2 . Using trigonometric substitutions, k_1 and k_2 can be expressed by the trigonometric functions (4.17)(a) and (4.17)(b).

$$k_1 = |k_1| e^{j\theta_1} = \frac{1}{M} \frac{\cos\left(\frac{\pi f_g}{2 f_n}\right)}{\sin\left(\frac{\pi}{2M} \left(\frac{f_g}{f_n} - 1\right)\right)} e^{j \frac{\pi}{2} \left(\frac{f_g}{f_n} \left(\frac{1}{M} - 1\right) + \frac{1}{M} + 1\right)} \quad (a) \quad (4.17)$$

$$k_2 = |k_2| e^{j\theta_2} = \frac{1}{M} \frac{\cos\left(\frac{\pi f_g}{2 f_n}\right)}{\sin\left(\frac{\pi}{2M} \left(\frac{f_g}{f_n} + 1\right)\right)} e^{j \frac{\pi}{2} \left(\frac{f_g}{f_n} \left(1 - \frac{1}{M}\right) + \frac{1}{M} - 1\right)} \quad (b)$$

Since it is the accurate negative sequence phasor which is of interest, (4.16) can be combined with the equation for symmetrical components (4.18) to calculate the negative sequence phasor X_N^- .

$$3X_N^- = \begin{bmatrix} 1 & a^2 & a \end{bmatrix} \begin{bmatrix} X_{n,a} \\ X_{n,b} \\ X_{n,c} \end{bmatrix} \quad (4.18)$$

$$3X_N^- = (X_{N_g,a} k_1 + X_{N_g,a}^* k_2) + a^2 (X_{N_g,b} k_1 + X_{N_g,b}^* k_2) + a (X_{N_g,c} k_1 + X_{N_g,c}^* k_2)$$

Using the equality,

$$a^* = a^2, \quad (4.19)$$

equation (4.18) can be rewritten as (4.20).

$$3X^{-N} = k_1(X_{Ng,a} + a^2X_{Ng,b} + aX_{Ng,c}) + k_2(X_{Ng,a} + aX_{Ng,b} + a^2X_{Ng,c})^* \quad (4.20)$$

It can be observed from (4.18) that the first and second set of brackets on the right hand side of (4.20) are equivalent to the negative and positive sequence components of the accurate phasor respectively. Equation (4.20) can then be simplified as (4.21).

$$X^{-N} = k_1(X_{Ng}^{-}) + k_2(X_{Ng}^{+})^* \quad (4.21)$$

Rearranging (4.21) yields an expression for the accurate negative sequence phasor X_{Ng}^{-} .

$$X_{Ng}^{-} = \frac{1}{k_1} \left(X^{-N} - k_2 X_{Ng}^{+*} \right) \quad (4.22)$$

In order to develop an expression for X_{Ng}^{-} containing only the HCDFT output and compensating coefficients, the same procedure can be followed for the positive sequence accurate phasor X_{Ng}^{+} .

$$3X^{+N} = \begin{bmatrix} 1 & a & a^2 \\ X_{n,a} \\ X_{n,b} \\ X_{n,c} \end{bmatrix} \quad (4.23)$$

$$X^{+N} = k_1 X_{Ng}^{+} + k_2 X_{Ng}^{+*}$$

$$X_{Ng}^{+} = \frac{1}{k_1} \left(X^{+N} - k_2 X_{Ng}^{+*} \right) \quad (4.24)$$

Substituting (4.24) into (4.22) and rearranging the terms yields an expression for calculating the accurate negative sequence phasor (4.27).

$$X_{Ng}^- = \frac{1}{k_1} \left(X_{-N}^- - k_2 \frac{1}{k_1} \left(X_{+N}^+ - k_2 (X_{Ng}^-)^* \right)^* \right) \quad (4.25)$$

$$X_{Ng}^- \left(1 - \frac{|k_2|^2}{|k_1|^2} \right) = \frac{X_{-N}^-}{k_1} - \frac{k_2}{|k_1|^2} X_{+N}^{+*} \quad (4.26)$$

$$X_{Ng}^- = \frac{k_1^* X_{-N}^- - k_2 X_{+N}^{+*}}{|k_1|^2 - |k_2|^2} \quad (4.27)$$

Following the same procedure outlined above for the accurate positive sequence phasor X_{Ng}^+ results in the expression of (4.28).

$$X_{Ng}^+ = \frac{k_1^* X_{+N}^+ - k_2 X_{-N}^{-*}}{|k_1|^2 - |k_2|^2} \quad (4.28)$$

In addition to numerical compensation of the off-nominal frequency, adaptive windowing is implemented to limit the maximum frequency error to be compensated. The window lengths and corresponding range of f_g are listed in Table 4.1. This improves the performance in the presence of off-nominal frequency harmonics. Real and imaginary filters for $M = 31-34$ corresponding to $f_g = 57.4 \text{ Hz} - 61.9 \text{ Hz}$ are stored. This range of frequencies was chosen to reflect the maximum anticipated variations in the microgrid frequency.

Table 4.1: HCDFT Filter length

Frequency	M
$f_g > 61.0 \text{ Hz}$	31
$59.2 \leq f_g \leq 61.0 \text{ Hz}$	32
$57.4 \leq f_g < 59.2 \text{ Hz}$	33
$f_g < 57.4 \text{ Hz}$	34

Although the magnitudes of the compensating coefficients defined in (4.17) are trigonometric functions of the grid frequency and the filter length, a quadratic and linear approximation can be found for $|k_1|$ and $|k_2|$ respectively, as shown in (4.29). Using the approximate equation

also prevents dividing by zero error when the grid frequency is exactly equal to the nominal frequency.

$$|k_1| \approx g_{1M} \left(f_g - \frac{f_s}{2M} \right)^2 - 1$$

$$|k_2| \approx g_{2M} \left(f_g - \frac{f_s}{2M} \right)$$
(4.29)

The gains of g_{1M} and g_{2M} in (4.29) have fixed values which depend on the value of M and were determined by plotting the $|k_1|$ and $|k_2|$ in (4.17) vs f_g and using the curve matching feature in Matlab®. These values and are listed in Table 4.2.

Table 4.2: Coefficients of approximate gain equation

Frequency	g_{1M}	g_{2M}
$f_g > 61.0$ Hz	1.0699×10^{-4}	-8.3264×10^{-3}
$59.2 \leq f_g \leq 61.0$ Hz	1.1409×10^{-4}	-8.3377×10^{-3}
$57.4 \leq f_g < 59.2$ Hz	1.2124×10^{-4}	-8.3249×10^{-3}
$f_g < 57.4$ Hz	1.2842×10^{-4}	-8.2876×10^{-3}

The angles of the error coefficients θ_1 and θ_2 are calculated based on the measured grid frequency using (4.17).

$$\theta_1 = \frac{\pi}{2} \left(\frac{2Mf_g}{f_s} \left(\frac{1}{M} - 1 \right) + \left(\frac{1}{M} + 1 \right) \right)$$

$$\theta_2 = \frac{\pi}{2} \left(\frac{2Mf_g}{f_s} \left(1 - \frac{1}{M} \right) + \left(\frac{1}{M} - 1 \right) \right)$$
(4.30)

No approximation is necessary to calculate the angles in (4.30).

4.2 Verification of the Compensation Algorithm

4.2.1 Performance of the Compensated HCDFT

Matlab/Simulink® is used to test the performance of the compensated negative sequence phasor algorithm. A sampling rate of 3840 Hz is chosen, corresponding to a filter length of 32 samples per $\frac{1}{2}$ cycle at the nominal frequency of 60 Hz. In each case, white noise with a 45 dB Signal to Noise Ratio is added to the input signal to better simulate current sensor input.

For case 1, the same conditions used in the test in Figure 4.5 have been applied to the compensated phasor. The results, shown in Figure 4.6, show that the numerically compensated negative sequence phasor has a negligible steady state error even for the greatest possible relative frequency deviation, $\Delta f = |f_g - f_s / M|$. The angular error is less than 0.1° . Adjusting the filter length M depending on f_g as shown in Table 4.1 ensures that the error between the filter frequency and the grid frequency Δf will never be more than 1 Hz over the range $55 > f_g > 64$ Hz.

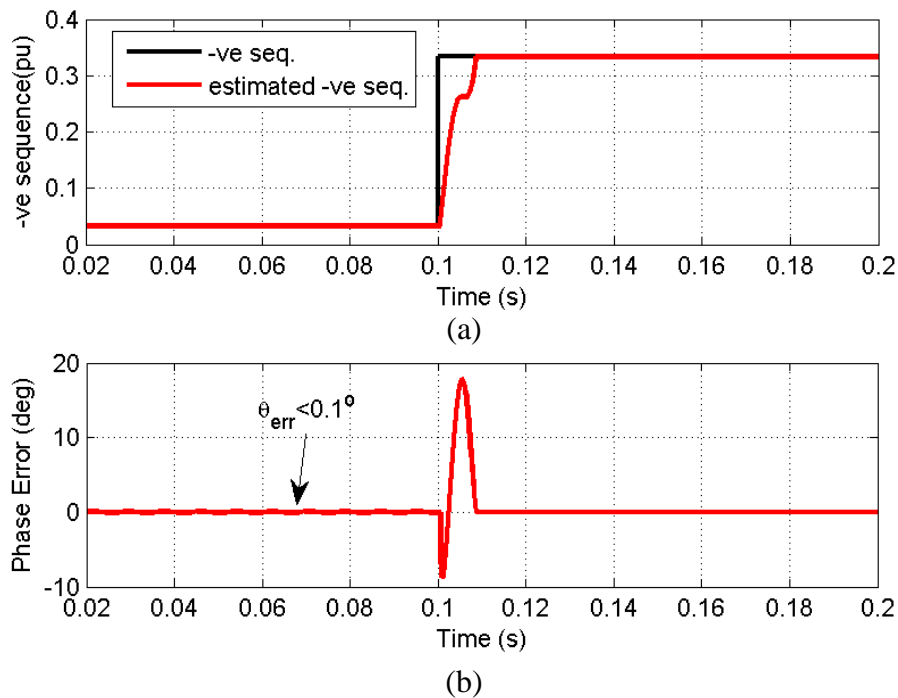
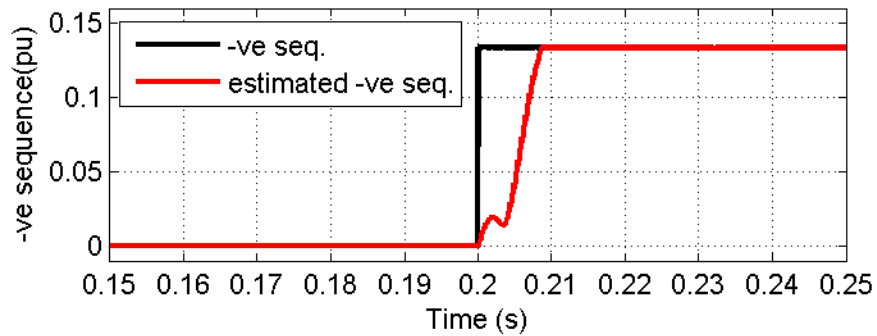


Figure 4.6: Case 1, Compensated negative sequence (a) phasor magnitude and (b) phase for $f_g = 61$ Hz

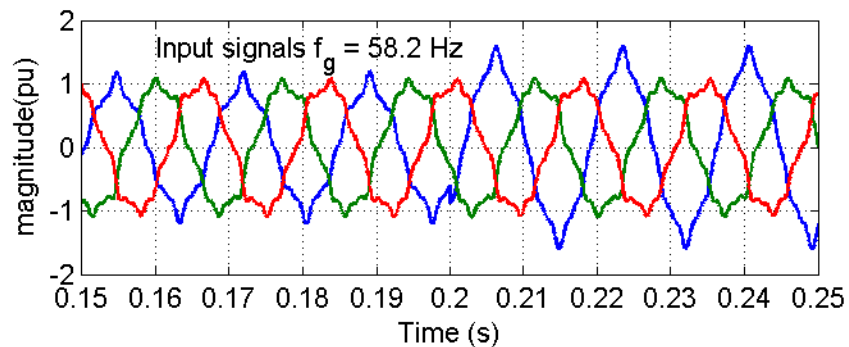
Because the input to the algorithm is a distribution system current which may be highly unbalanced and distorted, the performance of the algorithm under such conditions is

important. Case 2 examines the performance under harmonic conditions. Like the uncompensated HCDFT, the proposed technique completely eliminates odd harmonics. However, for off-nominal system frequency operation, the odd harmonics will be attenuated but not completely eliminated, except for integer multiples of the sampling frequency. The greater the relative frequency deviation Δf , the lower the harmonic attenuation.

In case 2, the input signal contains 5th, 7th, and 11th harmonics with a THD of 11.0% of the positive sequence current. The 3rd harmonic is not considered here because the VSC is connected through a delta-wye transformer which “traps” the 3rd harmonic components. Initially the three phases are balanced. At $t = 0.2$ s an unbalance is created which results in a 20% negative sequence component. An under-frequency grid condition is simulated with $f_g = 58.2$ Hz, shown in Figure 4.7(b). An over-frequency condition for $f_g = 61.0$ Hz is also simulated and plotted in Figure 4.8(b).

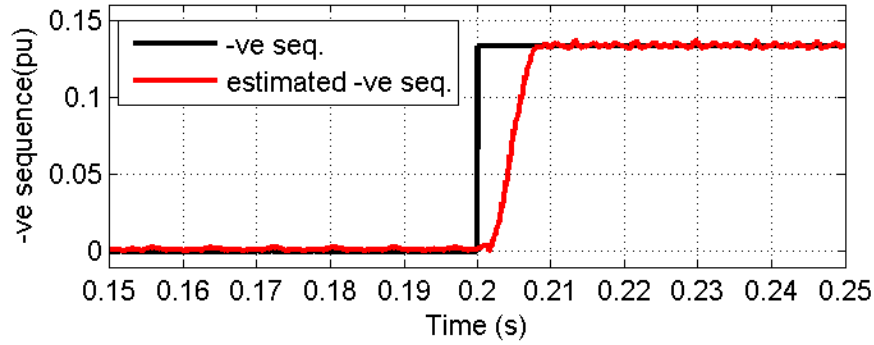


(a)

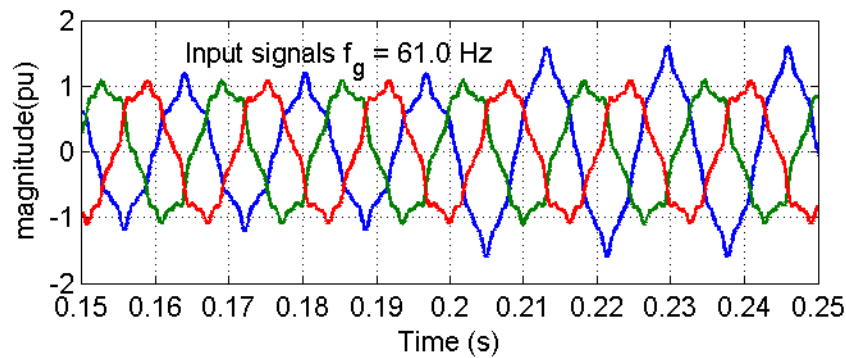


(b)

Figure 4.7 Case 2, (a) Negative sequence output with $f_g = 58.2$ Hz and (b) input signals containing 5th, 7th, and 11th harmonics with THD of 11.2%



(a)



(b)

Figure 4.8: Case 2, (a) Negative sequence for $f_g = 61.0$ Hz and (b) input signals containing 5th, 7th, and 11th harmonics with THD of 11.2%

At 58.2 Hz the grid frequency corresponds exactly to the nominal frequency for a filter length of $M = 33$. After the half-cycle transient, the HCDFT is able to completely filter out the harmonics as seen in Figure 4.7(a). Although the input signals in Figure 4.7(b) are highly distorted, the measured magnitude using the HCDFT is accurate.

For the second simulation of Case 2 an over-frequency condition is considered. A 1 Hz frequency deviation is simulated and the input signals shown in Figure 4.8(b) contain the same harmonic as in the input signals in Figure 4.7(b) with a THD of 11.2%. Although the frequency deviation is actually less than in the first simulation (+1.0 Hz vs. -1.8 Hz), the output of the HCDFT is slightly more distorted. This is because the ratio of the grid frequency and the sampling frequency is not an integer. The numerical compensation scheme corrects the error at the fundamental frequency but can only partially compensate the harmonic component. However, Figure 4.8(a) shows that even under these conditions, the

calculated negative sequence component contains only a small oscillatory error (approximately 0.22%). Such a small error does not have an appreciable impact on the current injected into the grid by the inverter.

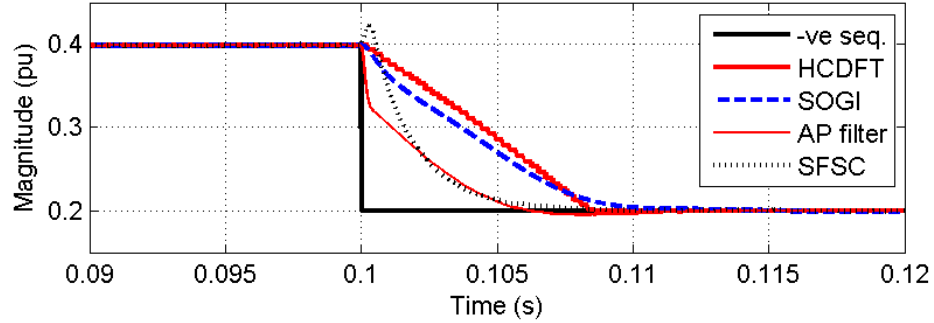
4.3 Comparison with Conventional Techniques

In the following cases, the efficacy of the proposed HCDFT technique is compared with the SOGI and APF based sequence extraction algorithms, which have been discussed in Chapter 2. These techniques are chosen for their prevalence in the literature and similarities with the HCDFT. All three methods require estimation of the grid frequency. The methods are compared on the basis of suitability for the PV control structure, the criteria being: quick settling time and immunity to harmonic distortion.

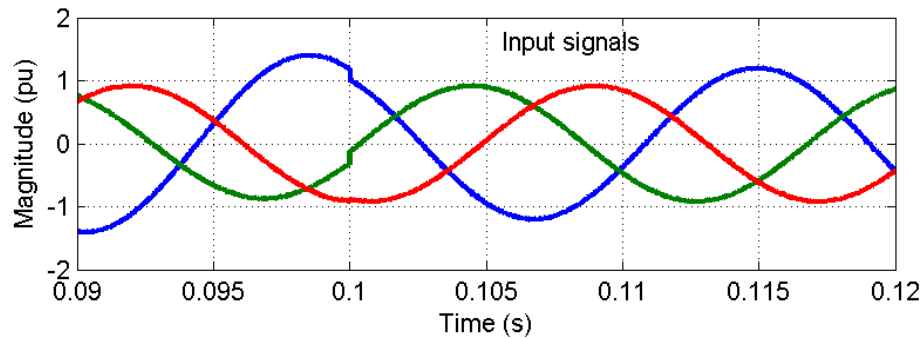
4.3.1 Settling Time

In Case 3, the settling times of four techniques are compared for an undistorted input at the nominal frequency. The input in Case 3 contains a 40% negative sequence until $t = 0.1$ s, when there is a 50% decrease in the magnitude of the negative sequence. The results are plotted in Figure 4.9 for All-Pass, SOGI, DQ, and HCDFT algorithms.

The SFSC and AP filter methods have the shortest response time of 5.1 ms and 5.4 ms respectively. Because the differentiation in the SFSC technique amplifies noise, it requires additional low-pass filtering, which slows the response. The settling times of the SOGI and HCDFT are 8.8 ms and 8.3 ms respectively. Although the AP filter and SFSC methods both have a shorter response time than the HCDFT, the difference is only 2.7 ms. In test cases 4 and 5, only the HCDFT, SOGI and AP filter techniques are applied. This is because the performance of the SFSC method is too poor to allow a meaningful comparison.



(a)

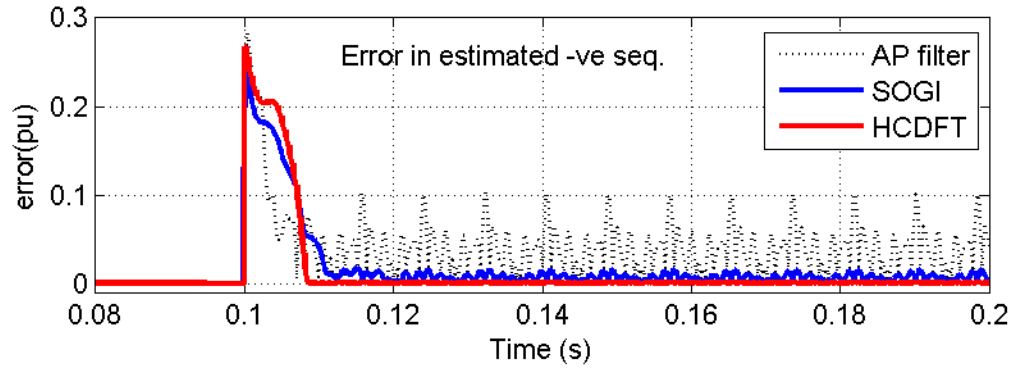


(b)

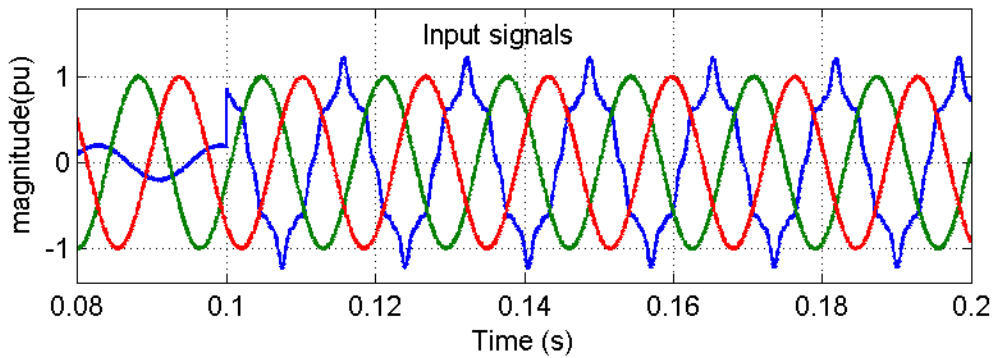
Figure 4.9: (a) Settling time of HC-DFT, SOGI, $dq0$, and APF method of sequence calculation (b) to 50% decrease in the negative sequence

4.3.2 Unbalanced Harmonics

The next scenario, Case 4, compares the performance of the HCDFT, SOGI and AP filters under unbalanced harmonic distortion. At 0.1 seconds, a non-linear load with 5th, 7th, and 11th, harmonics is added to phase A. The input signal, seen in Figure 4.10(b) has a THD of 10.0% in phase A, this corresponds to the maximum allowable level of harmonic distortion over a very short interval (3 s), as defined by IEEE 519-2014 [3]. Figure 4.10(a) shows the error between the measured and the actual negative sequence fundamental component. As expected, the performance of the AP filter performance has been affected most significantly, since the filter has a unity gain over the whole frequency spectrum. The SOGI extraction technique shows improvement over the AP filter, however, there is still more distortion visible than for the compensated HCDFT output.



(a)



(b)

Figure 4.10: (a) Negative sequence calculated by HC-DFT, APF, and SOGI techniques and (b) unbalanced harmonic input with $f_g = 60.5$ Hz

4.3.3 Balanced Harmonics

In Case 5, the performance under balanced harmonics is compared. All even and odd harmonics up the 11th harmonic are present, minus the triplen harmonics which are not considered in a three-wire system. The THD is 14% and the grid frequency is 59.8 Hz. The calculated negative sequence magnitudes and the input signals are shown in Figure 4.11. From Figure 4.11(a) it can be seen that even though the HCDFT does not completely eliminate the even harmonics, it outperforms the SOGI, and AP filter techniques. It is noted that the settling time of the HCDFT is unaffected by the harmonic content of the input.

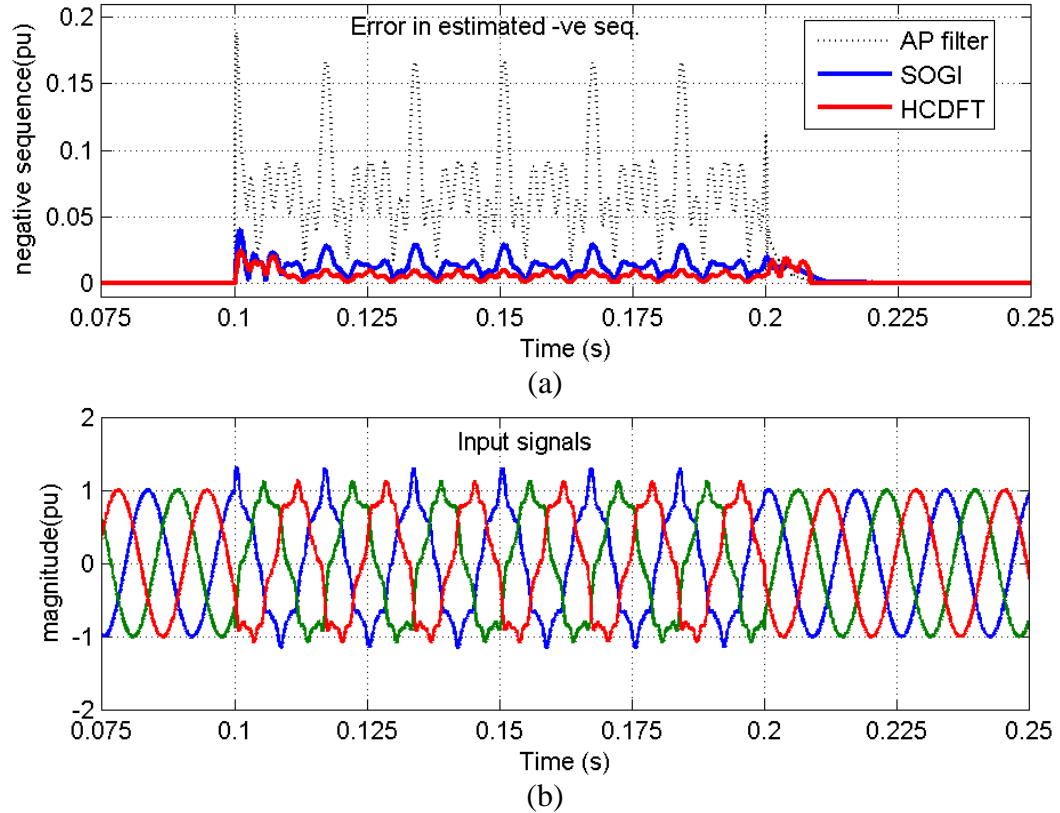


Figure 4.11: (a) Output of negative sequence calculation algorithms, and (b) balanced, highly distorted input with $f_g = 59.8$ Hz

4.4 Calculation of the Compensation Reference Current

The proposed control structure uses the stationary reference frame with AC rather than DC control signals. For this application it is not necessary for the controller to calculate the phasor values. Figure 4.12 depicts the current reference calculation unit for compensating the negative sequence load current. First, the HCDFT is applied to the three-phase load current i_l . The output of the real and imaginary HCDFT filters, R_l and I_l , respectively, are used as inputs to (4.18) to calculate the instantaneous positive and negative sequence components. This produces the real and imaginary components of the positive and negative sequences, R_l^+ , I_l^+ , R_l^- , I_l^- . Equation (4.27) is implemented in the numerical compensation block of Figure 4.12 as a set of complex multiplications. The output of this block is the compensated sinusoidal negative sequence current R_{lg}^- and its 90° phase shift I_{lg}^- . Together these two signals are the equivalence of the negative sequence $\alpha\beta$ components. To obtain the reference compensation current, the negative rotation inverse Clarke transformation (4.31) is

applied directly to the outputs of the compensation block. The final current reference given to the PR controllers is the summation of the negative sequence reference i_l^- and the positive sequence output of the DC link voltage control loop, $i_{pv,ref}$.

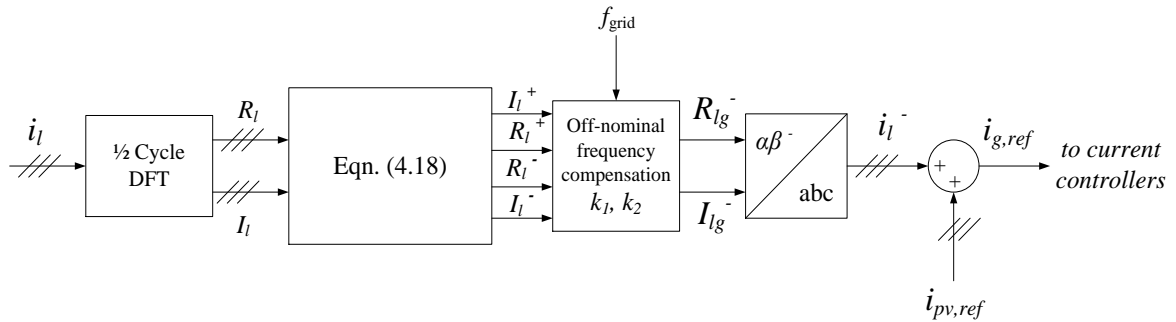


Figure 4.12: Compensating current reference calculation

$$i_{abc}^- = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{\alpha}^- \\ i_{\beta}^- \end{bmatrix} \quad (4.31)$$

4.5 Conclusion

In this chapter the DFT is briefly reviewed and an off-nominal frequency compensation technique following the method of [1] is derived for a HCDFT algorithm. Using (4.27) the accurate fundamental negative sequence component can be calculated even during off-nominal grid frequencies. This method has been tested under various harmonic conditions and its performance has been compared to that of the conventional techniques described in the literature. The results show that the compensated HCDFT is more resilient to harmonic filtering characteristics than the other techniques, without sacrificing the speed of response. The inverse Clarke transformation can be directly applied to the outputs of the frequency compensation block to obtain the ABC frame compensating currents.

4.6 References

- [1] F. Baradarani, M.R. Dadash Zadeh and M.A. Zamani, "A Phase-Angle Estimation Method for Synchronization of Grid-Connected Power-Electronic Converters," *IEEE Trans. Power Del.*, vol.30, no.2, pp.827-835, Apr. 2015.

- [2] H. Henao, T. Assaf and G.A. Capolino, "The discrete Fourier transform for computation of symmetrical components harmonics," in *Proc. Power Tech. Conf.*, 2003, vol.4, pp.6.
- [3] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," IEEE Std 519-2014 (Revision of IEEE Std 519-1992), pp.1-29, June 2014.

Chapter 5

5 Compensation of Unbalanced Load for Different Operating Conditions of a PV Array

In Chapter 3 and Chapter 4 a control scheme has been proposed for a PV inverter to allow for compensation of negative sequence load current. A test system has been built in Matlab/Simulink® to study the performance of a PV system with the control scheme shown in Figure 3.1. In this chapter, the effect of unbalanced load compensation on a PV array with a single-stage converter is examined.

Perturbations in the voltage of the DC bus will have an impact on real power production from the PV array because the PV array and the inverter are connected at the DC link. Compensating negative sequence load current will lead to an oscillation in the power and voltage at the DC link. Two case studies are described in this chapter. The first case study compares different regions of operation on the Power-Voltage (P-V) curve of the PV array, and the second study compares different irradiance levels.

For the first case study in Section 5.1, the effect of the location of the operating point on the P-V curve is investigated. Three conditions for the PV array are simulated. Although the VSC is operating at the same DC link voltage and supplying the same power in each case, the DC link voltage oscillations caused by load compensation are of different magnitudes depending on whether the PV array voltage is below, above, or equal the voltage at the MPP, V_{mpp} . Since the PV array is likely to be operated at or near the MPP the majority of the time, it is important to assess the impact of load balancing on power production at the MPP. In Section 5.2 the effect of compensating an unbalanced load is compared for different levels of solar irradiance ranging from 20-80% of the maximum expected irradiance. A range of irradiance and temperature conditions have been simulated and the power loss of the PV array due to load compensation has been compared.

A single-line diagram of the test system considered for the case studies is shown in Figure 5.1. The grid is modelled as a balanced three-phase 60 Hz voltage source connected to bus B1 through an inductance $L_{gr} = 0.2$ mH and resistance $r_{gr} = 29.3$ m Ω . Both balanced and

unbalanced linear loads are connected at bus B1 along with the PV system. The PV inverter is connected to the network through a delta-wye step-up transformer.

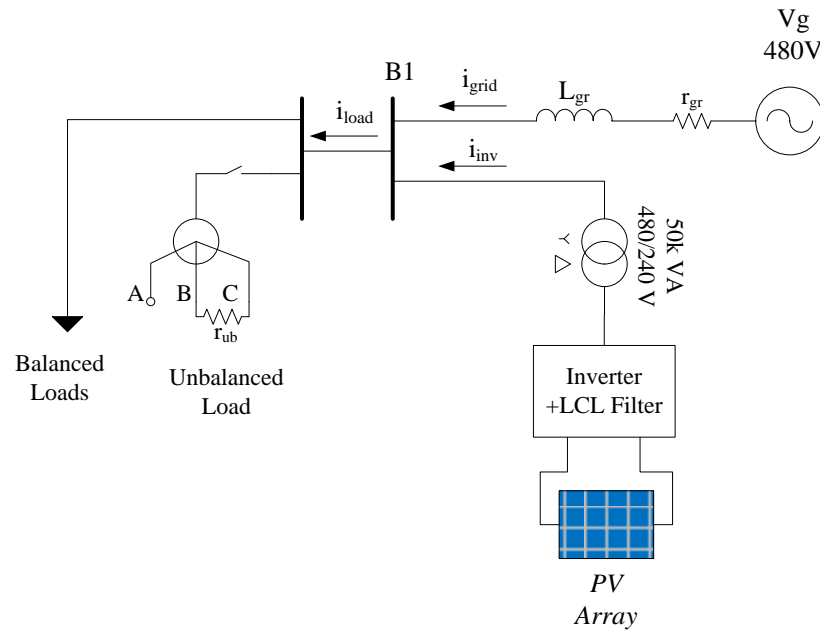


Figure 5.1: Distribution network simulated in Chapter 5

5.1 Case 1: PV Curve Region of Operation and Effect of Unbalance Compensation

The DC link voltage and power oscillation is one focus of the test. From the PV perspective, it is important to minimize oscillation in the array terminal voltage to maximize the energy production from the system. For the inverter, reducing the DC bus voltage ripple is also an important consideration. Excessive ripples can cause over-voltage, excessive voltage stress, controller saturation, and current distortion. One solution is to increase the capacitance of the DC bus to smooth ripples out. However, this increases the cost and size of the VSC [1]. In the following simulations the inverter is equipped with a 3248 μF DC link capacitor, C_{DC} . The capacitor is sized with no consideration for the second harmonic voltage oscillations which allows more insight into the effect of unbalance compensation on the PV array. Figure 5.2 shows the power relationships at the DC link of the inverter.

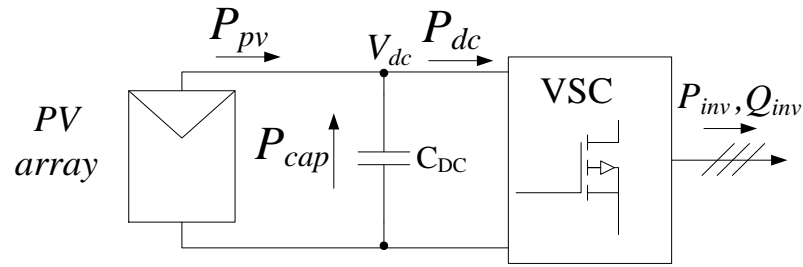


Figure 5.2: Power relationship with DC link connections of the PV system

The instantaneous power injected to the grid is labeled P_{inv} in Figure 5.2. P_{dc} , P_{cap} , and P_{pv} are the total DC link power, capacitor power, and PV array power respectively.

Unlike an ideal voltage source, the current-voltage (I-V) characteristics of a PV array have three distinct regions of operation: the Constant Current (CC) region below the MPP voltage, the Maximum Power Point (MPP) region, and the Constant Voltage (CV) region above V_{mpp} . The regions are labeled in Figure 5.3.

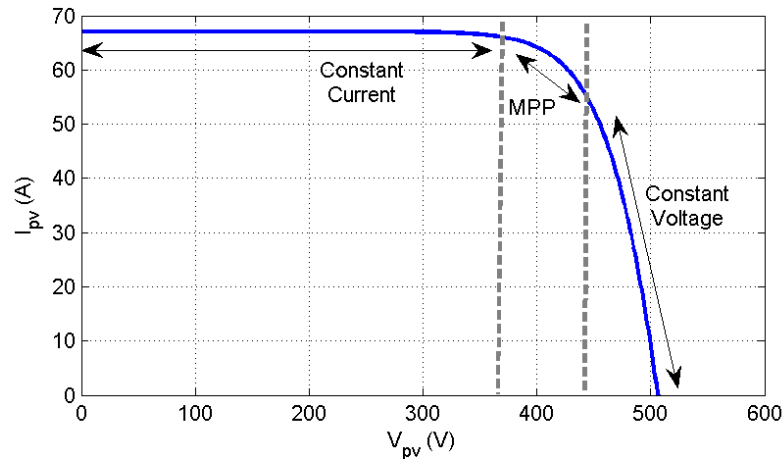


Figure 5.3: Regions of the I-V curve for a PV array

In this simulation the effect of the region of operation on the Power-Voltage (P-V) curve on the performance of the system is examined. The results are compared to the case where the inverter is operating solely as an active power filter with no generation source connected at the DC link. Three different P-V curves have been simulated. Each curve intersects at 435 V and 27.4 kW, as seen in Figure 5.4. For curve 1 in 435 V corresponds to the MPP. On curve 2, 435 V falls in the CC region and on curve 3 it falls in the CV region. The details of the array simulated to generate curves 1, 2, and 3 are listed in Table 5.1. Detailed modeling of the PV panels is discussed in Appendix A.

Table 5.1: Array parameters for Case 1

	Curve 1	Curve 2	Curve 3
Series panels	16	25	14
Parallel panels	16	9	26
T (°C)	30	37	28
IR (W/m ²)	510	850	790

The MPPT algorithm is disabled for this experiment because the PV array is deliberately made to operate away from the MPP in two of the three curves. A constant voltage reference is given to the DC link voltage controller to ensure an accurate comparison between the three regions of operation.

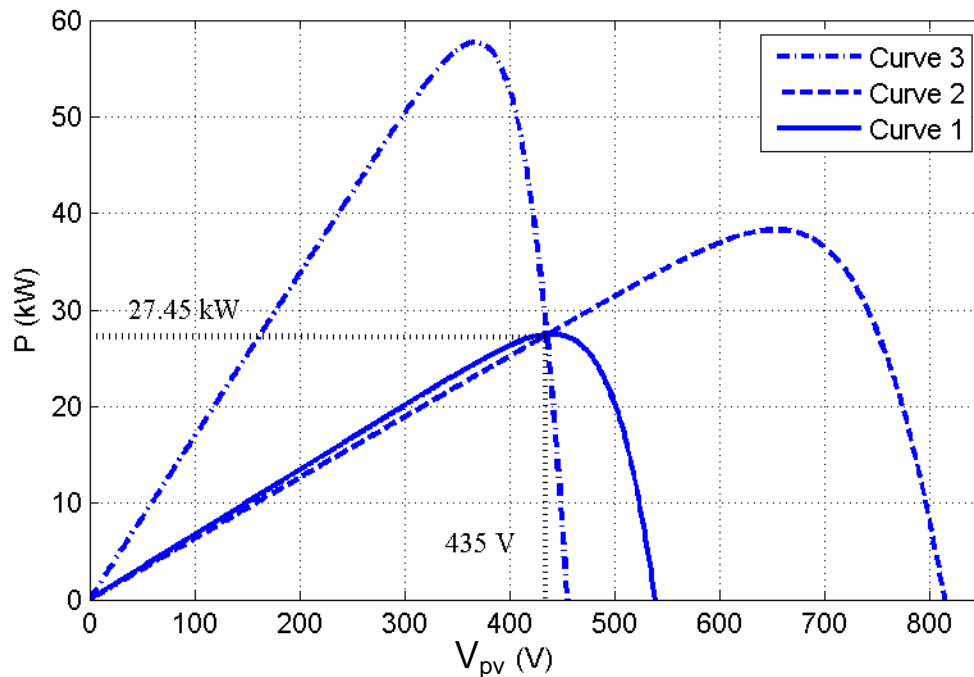


Figure 5.4: Three PV characteristic curves used in Case 1

Initially the inverter injects balanced currents into the grid (floating state for the APF mode). An unbalanced condition is created at $t = 0.3$ s when a 24Ω , 9.16 kW (0.183 pu) resistive load, r_{ub} , connected between phases B and C is switched on. The value of the single phase

load is selected so as to allow the inverter to fully compensate the load without exceeding power ratings. Once the single phase load is connected, the inverter supplies the full negative sequence current to the load. The test is conducted four times. First, the PV array is disconnected and the inverter operates solely as an active power filter. Next, each of the three curves is simulated and the inverter operates simultaneously in both compensation and power conversion mode.

The DC link voltages during negative sequence compensation for each case are plotted together in Figure 5.5. The reference voltage, $V_{pv,ref}$, is also shown. The total DC link power, P_{dc} , for MPP, CC, and CV regions of operation is plotted in Figure 5.6. Capacitor power P_{cap} and PV array power P_{pv} are plotted in Figure 5.7 and Figure 5.8 respectively.

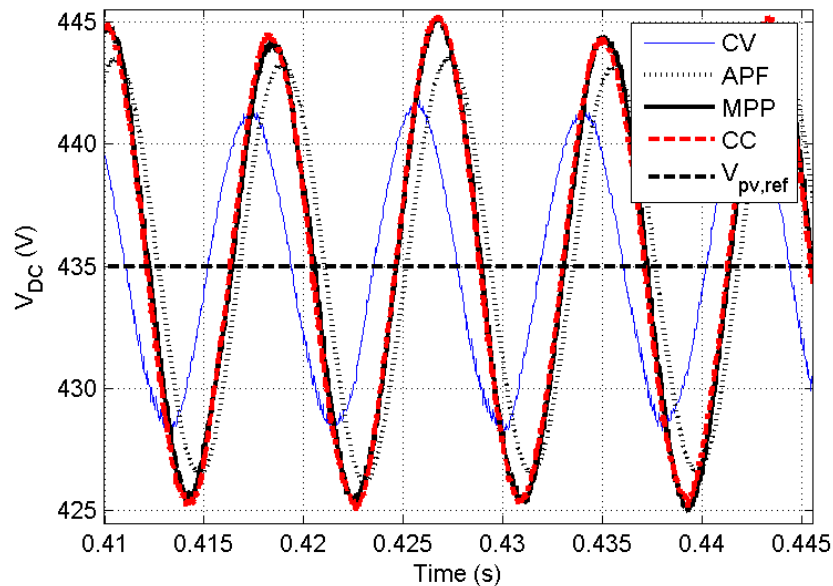


Figure 5.5: Steady state DC bus voltage waveforms during negative sequence compensation for Active Power Filter (APF), Constant Current (CC), Constant Voltage (CV), and Maximum Power Point (MPP) operation

Although the average DC link voltage and negative sequence current are the same in each case, Figure 5.5 shows that the region of operation affects the DC link voltage oscillation. The DC link voltage for the Constant Current and MPP mode during negative sequence compensation was almost identical according to Figure 5.5. The amplitude of the voltage

oscillation is higher in the CC and MPP case than when the inverter operates in Active Power Filter mode. The lowest oscillation amplitude occurs when the PV array matches curve 3 and is operated in the Constant voltage region.

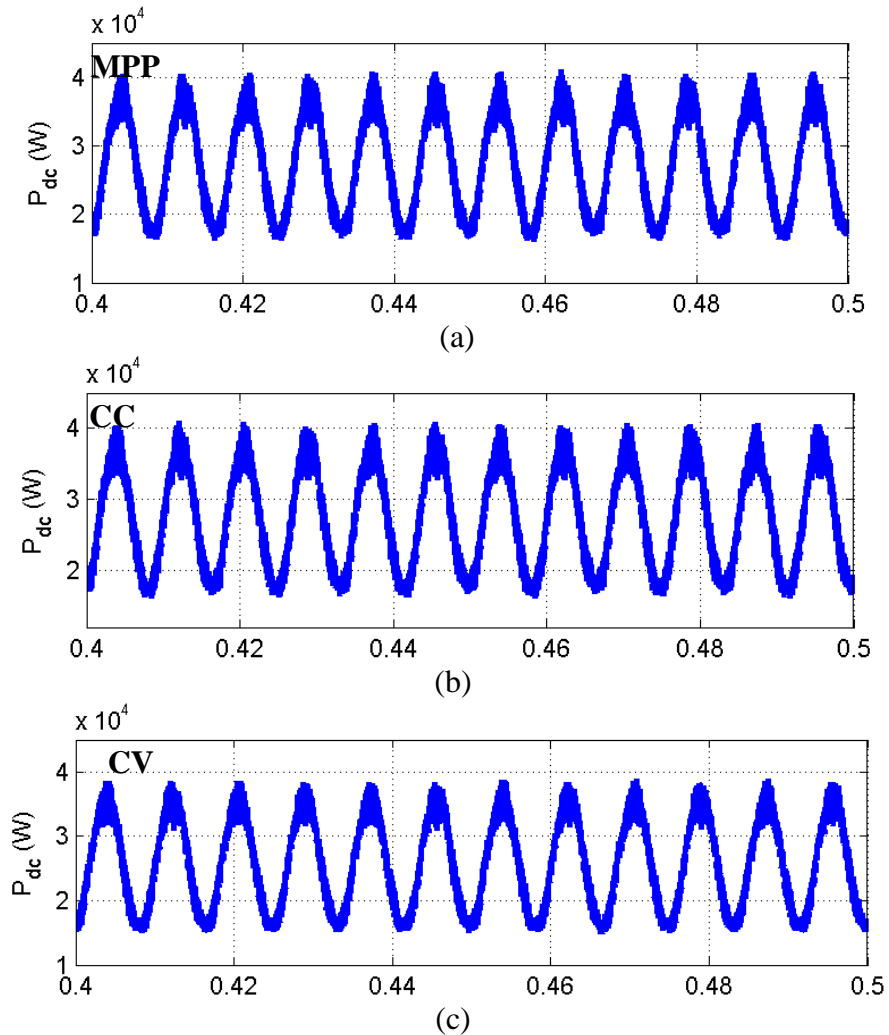


Figure 5.6: Total DC link power, P_{dc} during negative sequence compensation for (a) MPP region, (b) CC region, and (c) CV region

The total DC link power for each region of operation is similar since the same unbalanced load is compensated in each case. This is illustrated by Figure 5.6(a)-(c).

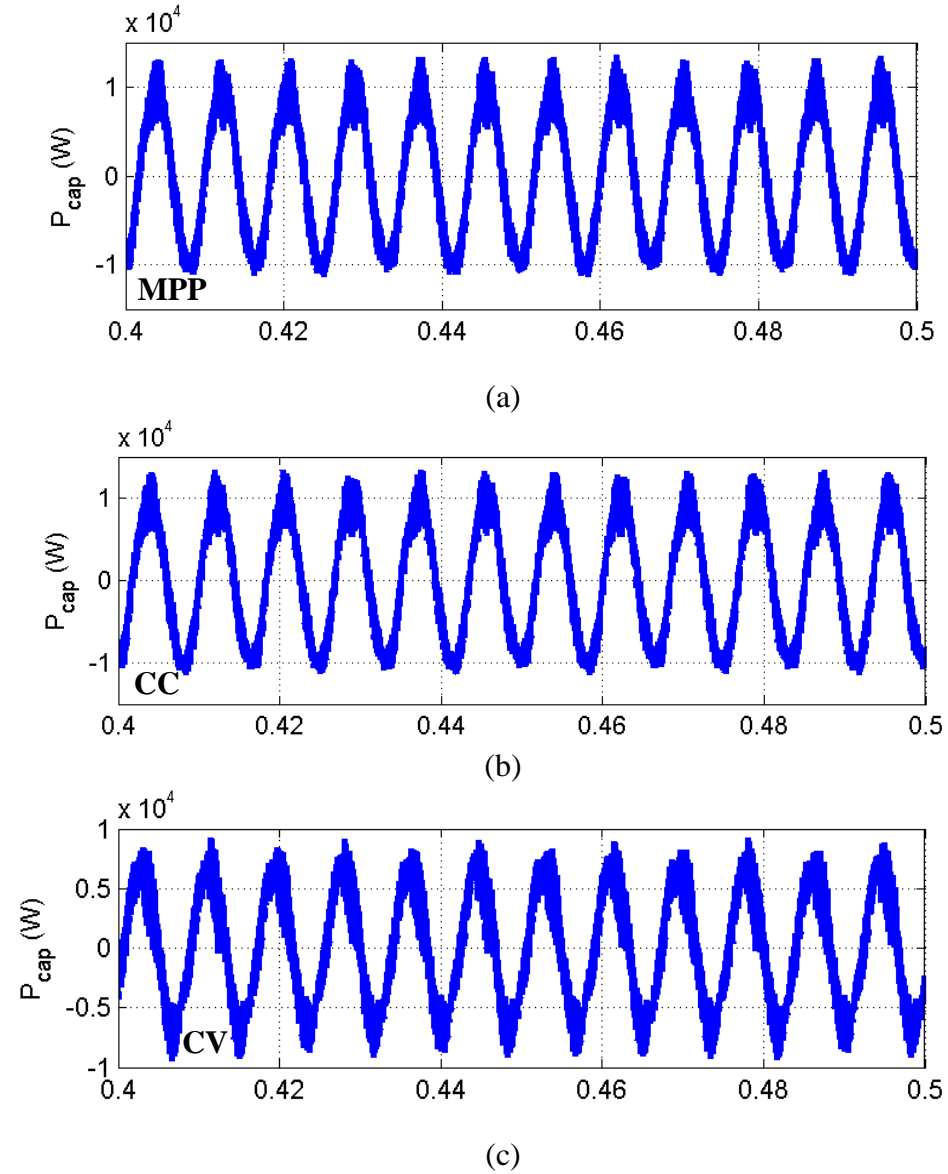
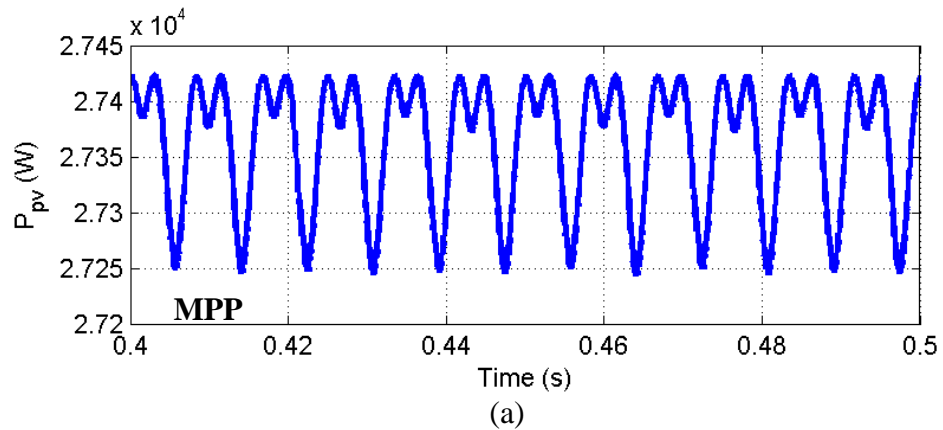


Figure 5.7: Capacitor power during negative sequence compensation P_{cap} for (a) MPP region (b) CC region, and (c) CV region



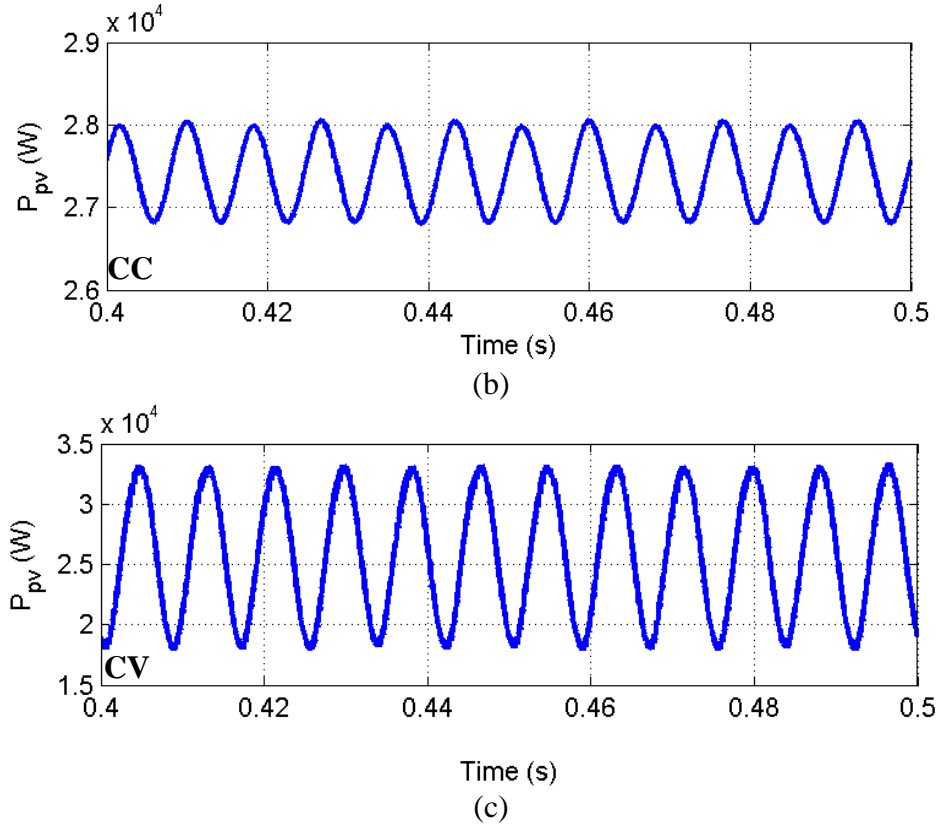


Figure 5.8: PV array power during negative sequence compensation, P_{pv} in (a) MPP region, (b) CC region, and (c) CV region in the CV region

Figure 5.8(a) shows the oscillation in the PV power is the lowest when the inverter operates at the MPP. However, it is also the most distorted. This is because of the opposite signs of dP_{pv}/dV_{pv} on either side of the MPP. Voltage excursions above the MPP have a negative characteristic while below they have positive slope. The PV power shows the largest oscillation in the CV region (Figure 5.8(c)). At the same time, the capacitor power oscillation, shown in Figure 5.7(c), has the smallest oscillation. Figure 5.7(c) and Figure 5.8(c) indicate that a higher portion of the ripple in P_{dc} is supplied by the PV array rather than by the capacitor in the CV region. This explains why the lower DC link voltage had a smaller ripple in the CV region compared with operating in the CC or MPP region in Figure 5.5.

5.1.1 Analysis of DC Link Voltage Ripple in APF Mode

The expected voltage ripple in the DC bus can be calculated by the power balance equation between the VSC input power P_{dc} and the instantaneous three phase output power P_{inv} . According to Figure 5.2, if the losses in the inverter are neglected this relationship can be written as (5.1).

$$P_{dc} = P_{cap} + P_{pv} = P_{inv} \quad (5.1)$$

To simulate nighttime operation, the PV array is initially disconnected and the inverter acts solely as an APF providing the compensating current needed to balance the load. Thus (5.1) can be written as (5.2), in APF mode.

$$P_{dc} = P_{cap} = P_{inv} \quad (5.2)$$

The power in the capacitor P_{cap} can be written in terms of the DC link voltage V_{dc} (5.3).

$$P_{cap} = V_{dc} \left(C_{DC} \frac{dV_{dc}}{dt} \right) \quad (5.3)$$

After $t = 0.3$ s when the inverter is compensating the unbalanced load, the instantaneous power injected into the grid is:

$$P_{inv} = \frac{3}{2} V^+ I^- \cos(2\omega t + \theta) \quad (5.4)$$

where V^+ and I^- are the amplitude of the positive sequence voltage and negative sequence current respectively. Substituting (5.3) and (5.4) into (5.2) yields:

$$V_{dc} \left(C_{DC} \frac{dV_{dc}}{dt} \right) = \frac{3}{2} V^+ I^- \cos(2\omega t + \theta) \quad (5.5)$$

The DC link voltage has both a DC value V_0 and an oscillating component $v(t)$ and is expressed in (5.6).

$$V_{dc} = V_0 + v(t) \quad (5.6)$$

Substituting (5.6) into (5.5) yields (5.7).

$$C_{DC} \left(V_0 \frac{dv(t)}{dt} + v(t) \frac{dv(t)}{dt} \right) = \frac{3}{2} V^+ I^- \cos(2\omega t + \theta) \approx C_{DC} V_0 \frac{dv(t)}{dt} \quad (5.7)$$

The approximation in (5.7) is valid with an assumption that the amplitude of the oscillation is much less than the average DC link voltage. From (5.7) the oscillating component of the DC link voltage during compensation is:

$$v(t) = \frac{3}{4} \frac{V^+ I^-}{C_{DC} V_0 \omega} \sin(2\omega t + \theta) \quad (5.8)$$

According to (5.8), the amplitude of the oscillatory voltage component is dependent on the amount of negative sequence compensation, the average value of the bus voltage, and the size of the DC bus capacitor. Increasing the bus capacitor or voltage and/or reducing the negative sequence compensation will all contribute positively to reduce the oscillation in the bus voltage. Based on (5.8), the expected amplitude of the DC link voltage oscillation is 8.6 V. According to Figure 5.5, which shows the DC link voltage during negative sequence current compensation, the amplitude of the DC voltage oscillation is 8.5 V, which closely agrees with the theoretical value.

5.1.2 Analysis of the DC Link Voltage Ripple in the Constant Voltage Region

With the PV array connected to the terminals of the DC bus the inverter output power during unbalanced compensation is (5.9).

$$P_{inv} = P_{comp} + P_{avg} \quad (5.9)$$

The component P_{avg} of the output power is the real power generated by the PV array and P_{comp} is the oscillating power due to the negative sequence compensation current. Only the PV array contributes to P_{avg} , but both the DC link capacitor and the PV array will play a role in supplying P_{comp} .

When the inverter is operating in APF mode, a decrease in the DC capacitor voltage causes power to be injected into the grid. Power is absorbed when capacitor voltage increases. In the constant voltage region, dP_{pv}/dV_{pv} has the same sign for the PV array as for the capacitor.

Since the PV array is contributing to the power oscillation required for supplying an unbalanced current, less oscillation is experienced in the DC capacitor. This reduces the amount of voltage ripple during negative sequence load current compensation.

The reduction in the amplitude of the DC link voltage oscillation can be quantified by approximating the PV array power in the CV region with (5.10)

$$P_{pv} = m_{cv} (V_{OC} - V_{pv}) \quad (5.10)$$

where m_{cv} is a constant equal to the approximate slope of the P-V curve and V_{OC} is the open-circuit voltage of the PV array. Substituting (5.3), (5.10), and (5.9) into the power balance equation in (5.1) results in (5.11).

$$m_{cv} (V_{OC} - V_{dc}) + C_{DC} V_{dc} \frac{dV_{dc}}{dt} = \frac{3}{2} V^+ I^- \sin(2\omega t + \theta) + P_{avg} \quad (5.11)$$

Again, the DC link voltage can be written as (5.12)

$$V_{dc} = V_0 + \hat{v} \sin(2\omega t) \quad (5.12)$$

Replacing V_{dc} with (5.12) in (5.11) yields (5.13).

$$2\omega C_{DC} V_0 \hat{v} \cos(2\omega t) - m_{cv} \hat{v} \sin(2\omega t) = \frac{3}{2} V^+ I^- \sin(2\omega t + \theta) \quad (5.13)$$

$$m_{cv} (V_{OC} - V_0) = P_{avg}$$

Next, (5.13) is rearranged to calculate the amplitude of the oscillation and phase angle.

$$\hat{v} = \frac{3}{2} \frac{V^+ I^-}{\sqrt{(2\omega C_{DC} V_0)^2 + m_{cv}^2}} \quad (5.14)$$

$$\theta = \tan^{-1} \left(-\frac{2\omega C_{DC} V_0}{m_{cv}} \right)$$

The value of m_{cv} is estimated by selecting two points (v_1, p_1) and (v_2, p_2) in the region of $V_{pv} = 435$ V on curve 3 in Figure 5.4 and substituting them into (5.15).

$$m_{cv} = \left| \frac{p_2 - p_1}{v_2 - v_s} \right| \quad (5.15)$$

Choosing points (425,37310) and (435,27150) result in $m_{cv} = 1016$. The expected amplitude of the DC link voltage oscillation is then 6.2 V, which is confirmed by DC link voltage shown in Figure 5.5. According to (5.14), the amplitude of the voltage oscillation in the CV region is reduced as the value of m_{cv} increases. When the slope of the P-V curve is large enough that the value of m_{cv} is close to $2\omega C_{dc}V_0$, it can have an impact on the magnitude of the voltage oscillations.

5.2 Case 2: Negative Sequence Compensation Under Different Irradiance Levels

The effect of negative sequence compensation on the power generation of the PV array is examined under different irradiance levels in Case 2. For Case 2, a series of irradiance and temperature conditions are simulated for the PV generator connected to the same network shown in Figure 5.1. Figure 5.9 shows the P-V curves of the simulated PV array for different environmental conditions. For each P-V curve shown in Figure 5.4 the unbalanced load in Figure 5.1 is switched on to examine the impact of unbalanced load compensation on the PV array when irradiance varies between 200-800 W/m². The maximum irradiance considered in this study is 800 W/m² because at higher irradiance values the inverter has insufficient additional capacity to compensate the load. At lower irradiance levels (IR < 200 W/m²) the DC link voltage at the MPP is too low to compensate the negative sequence load considered in this study.

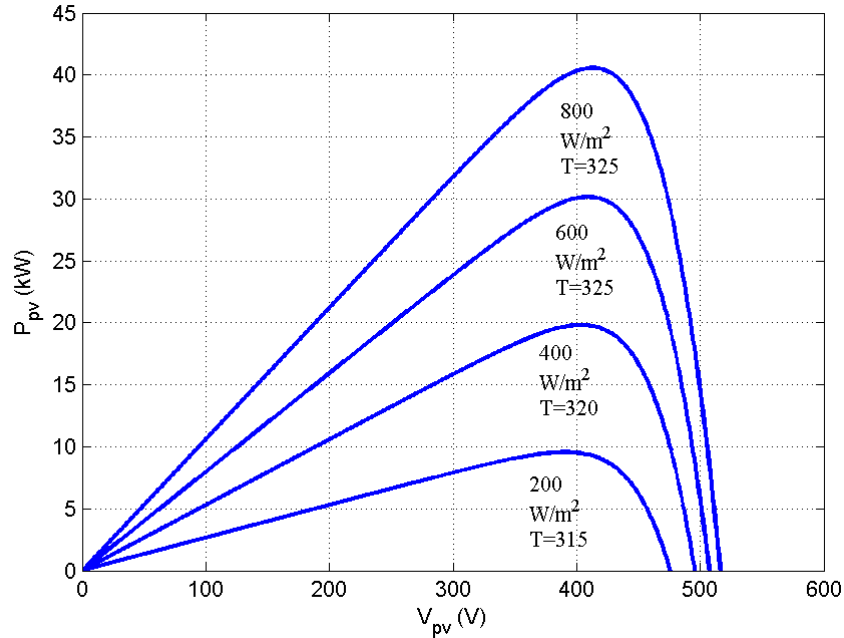


Figure 5.9: PV curves for irradiance from 200-800 W/m^2

Initially the PV system is running at the MPP and injecting balanced power into the grid. At $t = 0.3$ s the unbalanced load r_{ub} is switched on, and the PV inverter begins to compensate the full negative sequence load current. Figure 5.10 shows the load current used for all four IR levels. It can be observed that prior to $t = 0.3$ s the current is balanced. Following the switching of r_{ub} , the three-phase load currents become unbalanced. Despite the unbalanced load current, the current drawn from the grid remains balanced, as seen in Figure 5.11(a)-(c) which shows the grid current when irradiance is 200, 400, 600, and 800 W/m^2 respectively. Because the negative sequence load current is fully compensated by the inverter, the grid voltage remains balanced.

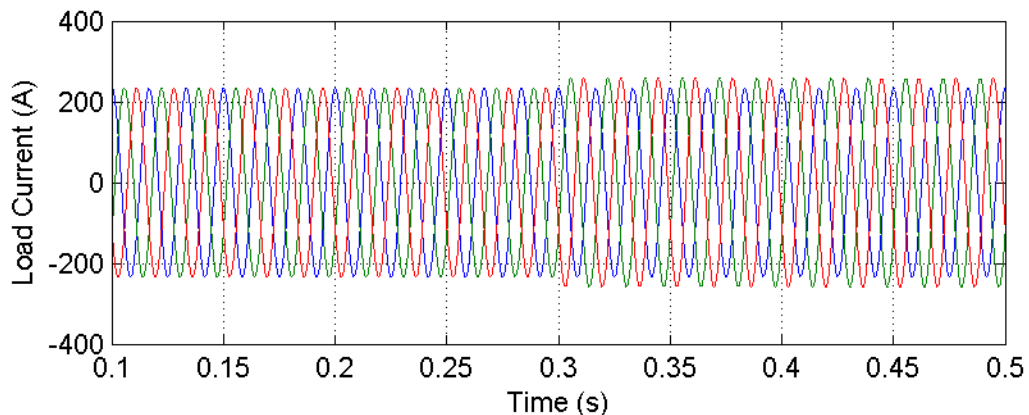


Figure 5.10: Load current for case 2

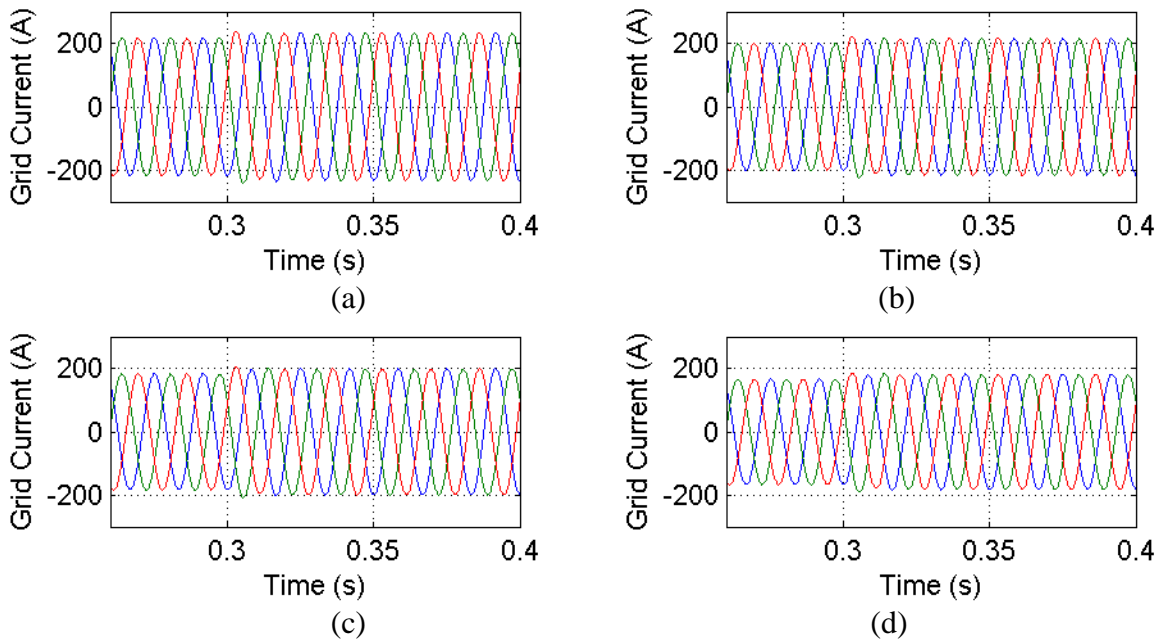


Figure 5.11: Grid current when irradiance is (a) 200, (b) 400, (c) 600, and (d) 800 W/m^2

The inverter current is shown in Figure 5.12(a)-(c). At the lowest irradiance level of 200 W/m^2 , Figure 5.12(a), the inverter current has the highest imbalance of 100% while at 800 W/m^2 the inverter current has a 24% imbalance. This is because as the irradiance level increases, the output power and current of the inverter also increases while the negative sequence load current remains constant.

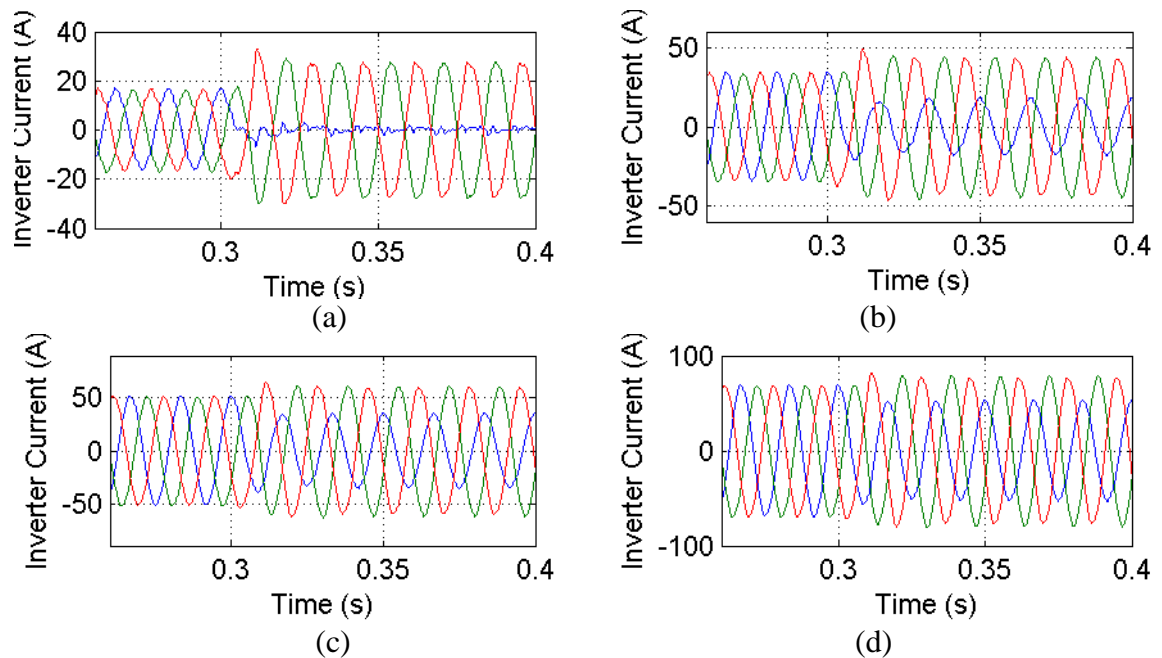


Figure 5.12: Inverter current when irradiance is (a) 200, (b) 400, (c) 600, and (d) 800 W/m^2

Figure 5.13 shows the DC link voltage for each irradiance level. When the inverter current is balanced up until $t = 0.3$ s, the DC link voltage is equal to V_{mpp} . Once the inverter begins to compensate the unbalance load, the voltage begins to oscillate at two times the line frequency, as discussed in Section 5.1. This voltage ripple causes the array to operate around the MPP rather than at the MPP, leading to a drop in the average power output of the PV array.

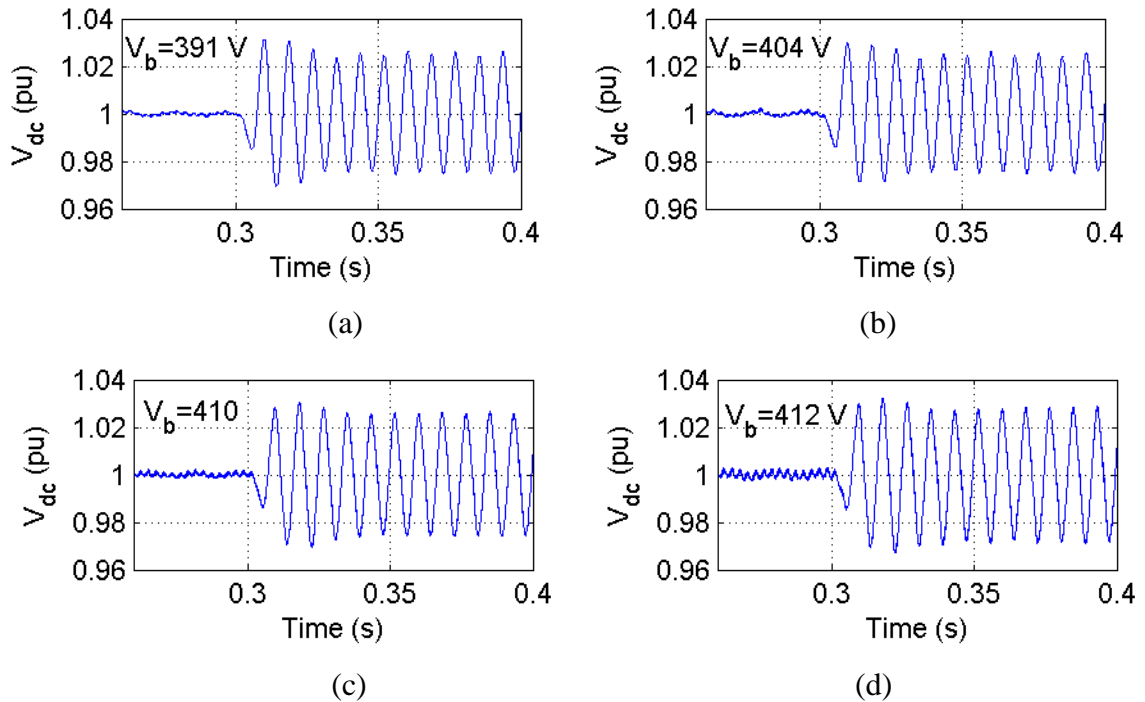


Figure 5.13: DC link voltage for irradiance of (a) 200, (b) 400, (c) 600, and (d) 800 W/m^2

The average PV output power in each case has been normalized according to (5.16) and is plotted in Figure 5.14.

$$P_{avg,N} = \frac{P_{avg}}{P_{mpp}} \quad (5.16)$$

When the inverter begins injecting a negative sequence current a drop in the average power output of the PV array can be seen in Figure 5.14 for each irradiance level. This power loss is due to the ripple in the DC link voltage shown in Figure 5.13.

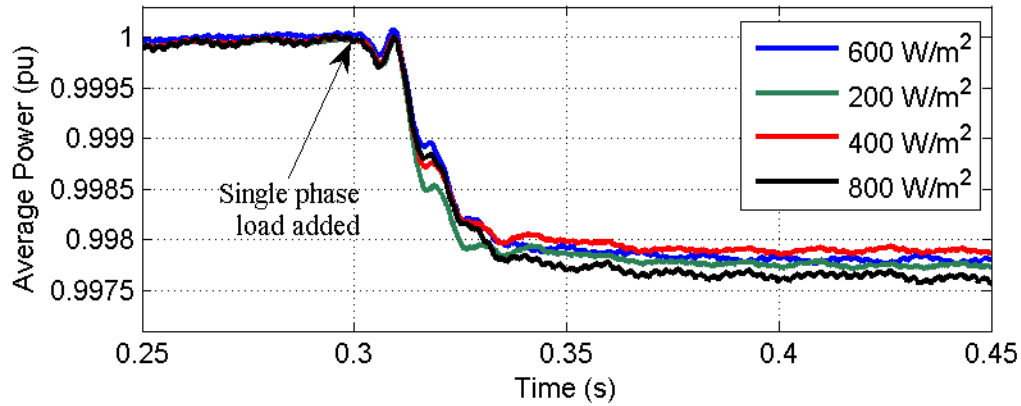


Figure 5.14: Average PV array power before and during negative sequence current compensation

In [2] a formula is presented for calculating the power loss from the rms value of the ripple in the array voltage and the power at the MPP (5.17).

$$\frac{P_r}{P_{mpp}} \approx \left(\frac{v_{rms}}{V_{mpp}} \right)^2 \left(1 + \frac{V_{mpp}}{2N_s a V_T} \right) \quad (5.17)$$

In (5.17) N_s is the number of series PV cells, a is the diode ideality constant and V_T is the diode thermal voltage, which are given in Appendix A. The power loss due to the negative sequence power ripple can be approximately calculated from (5.17) and the simulation results show a close agreement. Figure 5.13(a)-(d) shows that the ratio of the DC link voltage ripple amplitude to MPP voltage remains quite close at each of the irradiance levels. According to (5.17) this should equate to a similar percentage of power loss at each irradiance level. In Figure 5.14 it is seen that regardless of the irradiance level, the average power output of the PV array dropped by approximately 0.225% in response to compensating a 0.183 pu load unbalance. However, since there was a higher average power, the total power loss increased with increasing irradiance.

The MPP voltage for the curves shown in Figure 5.9 varies from 391V at 200 W/m² to 412 V at 800 W/m². The amplitude of the voltage oscillation was quite close in each case, however slightly higher (2.9%) DC link voltage oscillations were observed at 800 W/m² compared to 200 W/m² (2.55%). This discrepancy is in spite of the fact that at lower irradiance the operating voltage drops 5% between the highest and lowest irradiance levels. Intuitively from (5.8) a higher voltage ripple would be expected at low irradiance levels because of the

reduction in the average DC link voltage. Although each PV profile results in the same percentage of power loss, at a higher irradiance this translates into greater total lost energy.

5.3 Conclusion

The analysis and simulations in the preceding sections highlight several important factors for dual-purpose single-stage PV inverters. The coupling between the inverter DC link voltage and the PV array voltage is shown to affect P_{pv} during unbalanced load compensation. Increasing the DC link capacitor can reduce (but not entirely eliminate) the effect of the double-line frequency power oscillation on the DC link voltage.

The results shown in section 5.2 indicate that the best performance in terms of limiting the DC link voltage ripple are obtained when the PV array is operating in the constant voltage region of the I-V curve. In both the CC and MPP regions the amplitude of the oscillation is greater than for the APF mode but in the CV region the amplitude is lower. It is shown that the reduction in voltage ripple is related to the slope of the P-V curve at the operating point. In a microgrid with limited storage capability, there may be times when PV power curtailment is needed. This is accomplished by shifting the voltage reference away from the MPP. Based on the results of described in Section 5.1, it is recommended to move the reference point higher than the MPP voltage which will result in a smaller DC voltage ripple than if the reference is moved to the constant current region.

When the system is running at the MPP, compensating the negative sequence load current will result in a drop in power due to the oscillating DC link voltage. Higher irradiance and compensating current will increase the amount of power loss. However, for a 0.183 pu power oscillation, only around a 0.225% decrease in the average PV output power was observed. At 800 W/m^2 this only amounted to a reduction of 97.3 W.

The results of cases 1 and 2 in this chapter demonstrate the ability of a single stage PV inverter to compensate negative sequence load current at various irradiance levels provided the inverter has sufficient excess capacity.

5.4 References

- [1] N. Hur, J. Jung and K. Nam, "A fast dynamic DC-link power-balancing scheme for a PWM converter-inverter system," *IEEE Trans. Ind. Electron.*, vol.48, no.4, pp.794-803, Aug. 2001.

- [2] C.R. Sullivan, J.J. Awerbuch and A.M. Latham, "Decrease in Photovoltaic Power Output from Ripple: Simple General Calculation and the Effect of Partial Shading," *IEEE Trans. Power Electron.*, vol.28, no.2, pp.740-747, Feb. 2013.

Chapter 6

6 Control of a PV Inverter for Negative Sequence Current Compensation in a Microgrid

In this chapter, the performance of the proposed VSC controller for a PV system is validated in a Matlab/Simulink® simulation environment. The main objective of the simulation studies described in Chapter 6 is to verify the performance of the proposed control scheme in Figure 3.1 under different loading and grid conditions. To achieve these objectives, 5 case studies are presented herein.

Case study 1 examines the operation of the system when the unbalanced load exceeds the available capacity of the inverter. A compensation current scaling method is described to reduce the negative sequence reference current during high irradiance conditions. In case study 2 the negative sequence compensation is tested in a network with unbalanced feeder impedances. The third case study shows the performance of the PV system when a balanced non-linear load is connected to the network. The transient response of the system due to rapidly changing loads is demonstrated in case study 4. The performance of the controller in a hybrid diesel-PV microgrid is shown in case study 5. The results of the case studies show that the proposed control scheme is capable of simultaneous real power injection and negative sequence current compensation. The negative sequence current reference scaling prevents excessively high current reference values. The proposed negative sequence reference calculation technique is shown to cause no additional inverter current distortion during harmonic load current distortion. This is demonstrated by comparison with an identical system operating only in power conversion mode. The numerical compensation technique described in Chapter 4 is shown to prevent errors in the HCDFT due to spectral leakage during grid frequency deviations.

6.1 Case Study Test Network

Figure 6.1 shows a single-line diagram of the system simulated in case studies 1-4. The grid is modelled by a stiff voltage source connected by an equivalent impedance Z_{grid} consisting of an inductance $L_{gr} = 0.2$ mH and resistance $r_{gr} = 29.3$ m Ω . For case studies 1-4 the X/R ratio of the grid impedance is chosen to be 2.57, as a low X/R ratio is characteristic of low voltage networks. A collection of linear loads, both balanced and unbalanced are connected at bus

B1. The PV generator and the inverter and passive LCL filter are connected to the rest of the grid by a transformer with a delta-wye configuration. The current i_{grid} is drawn from the grid and i_{inv} is the current produced by the PV inverter on the Wye-side of the transformer.

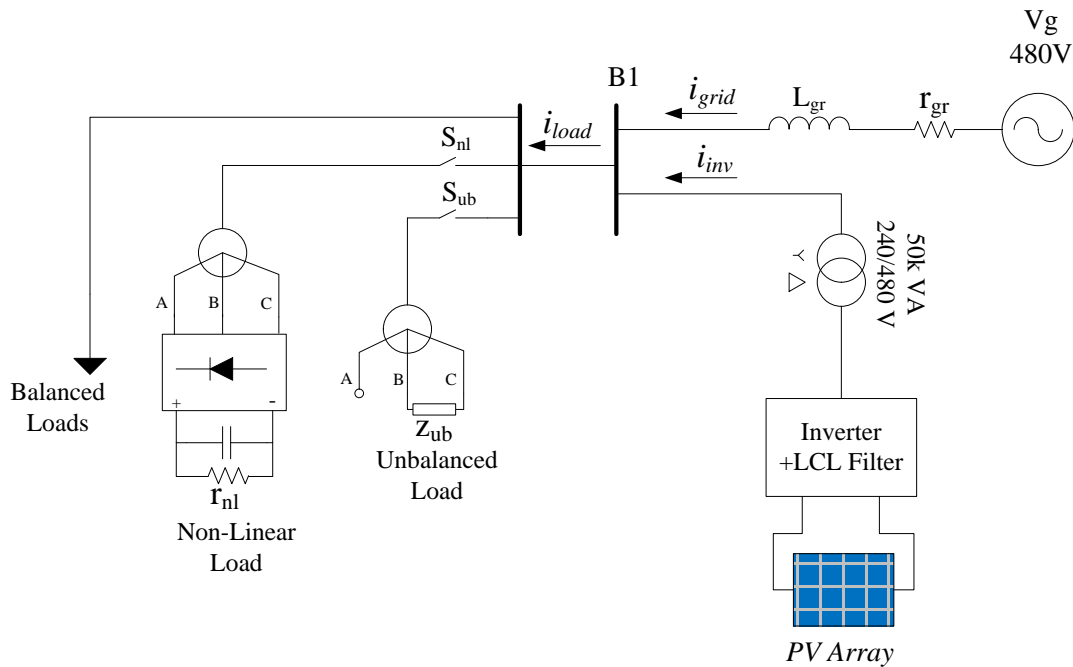


Figure 6.1: Single line diagram of the test system used in cases 1-4

6.2 Case Study 1: Compensation Current Scaling

It is likely that the inverter will experience times where compensating the entire negative sequence load current would exceed the inverter ratings and cause damage to the inverter. This could occur due to an unbalanced fault, highly unbalanced loading, or high real power production. The first case study illustrates the performance of the system when the unbalanced load current exceeds the excess capacity of the inverter. An algorithm for scaling the negative sequence compensation current is discussed in Section 6.2.1. This algorithm ensures the current reference does not exceed the ratings of the inverter. The performance of MPPT during negative sequence compensation and changing irradiance is also demonstrated.

6.2.1 Magnitude Scaling for Limiting Negative Sequence Current

To prevent damage to the PV system it is important to limit the current reference to I_{max} which is the current rating of the inverter. To give priority to real power generation, the

amplitude of the negative sequence reference current I_{comp} should be limited according to I_{max} and the positive sequence current reference $I_{pv,ref}$ (6.1).

$$I_{comp} = \begin{cases} i_{load}^-, & (-I_{max} + I_{pv,ref}) \leq i_{load}^- \leq (I_{max} - I_{pv,ref}) \\ (I_{max} - I_{pv,ref}), & i_{load}^- \geq (I_{max} - I_{pv,ref}) \\ (-I_{max} + I_{pv,ref}), & i_{load}^- \leq (-I_{max} + I_{pv,ref}) \end{cases} \quad (6.1)$$

The negative sequence current reference signals are sinusoidal, and using a DC limit to implement (6.1) will cause distortion in the reference signal. Instead, the negative sequence reference is reduced by multiplying the measured negative sequence load by a scaling factor. Figure 6.2 shows the block diagram of the reference scaling algorithm, denoted as ‘SF’ in the overall control scheme in Figure 3.1. The HCDFT algorithm used to calculate the negative sequence components can also be used to compute i_{l-pk}^- , which is the amplitude of the negative sequence reference. The output of the DC link voltage PI controller, $i_{pv,ref}$, is passed through the low-pass filter block, LPF, and added to the amplitude of the negative sequence reference, and passed through a saturation block with limits $\pm I_{max}$. The PV current reference is subtracted from the output of this block and divided by the peak of the negative sequence, to generate the DC scaling factor SF .

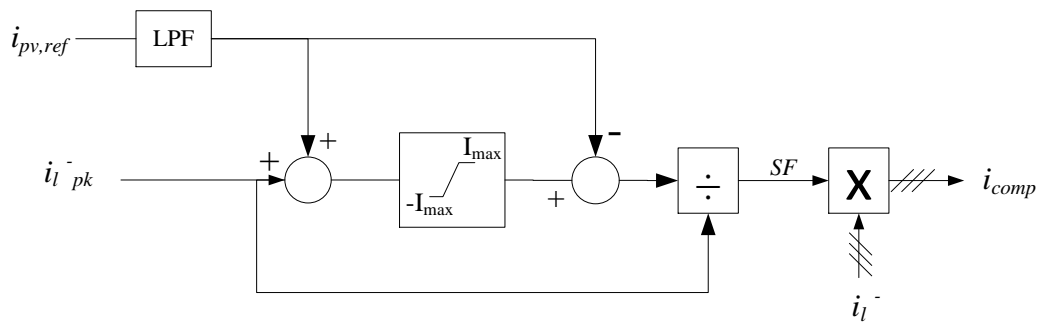


Figure 6.2: Negative sequence reference current limiting

If the negative sequence reference is less than the maximum minus the real power current requirement, the scaling factor, SF , is equal to 1. Otherwise, SF is equal to the maximum negative sequence current divided by the peak of the negative sequence load current. The sinusoidal negative sequence load current, i_l^- , is multiplied by the scaling factor which gives the actual compensating current reference i_{comp} .

6.2.2 Simulation Results

For case study 1, the switch S_{ub} connected to the unbalanced load is in the closed position for the duration of the test. The switch S_{nl} remains open. Throughout the scenario, the total load is constant. The resistive load $z_{ub} = 4.8 \Omega$ connected between phases B and C draws an oscillating three-phase power with a peak of 45.5 kW. Initially the maximum power of the PV array is 51.0 kW, which is equal to the full power and current rating of the inverter. The P-V curves for case study 1 are shown in Figure 6.3. At $t = 0.61$ s the irradiance drops from 1000 W/m^2 to 600 W/m^2 as seen in Figure 6.4. Although in practical situations insolation and temperature rarely undergo drastic changes, the rapid change is simulated to demonstrate the performance of the system during an extreme change in PV power output. The new peak power of the array is 30.3 kW.

When the PV power is high, only a small amount of the inverter capacity is available for negative sequence compensation. The compensating current reference is initially scaled by a factor of 0.03, as shown in Figure 6.3, based on the output of the scaling block in Figure 6.2. This allows priority to be given to real power production. When the irradiance decreases the PV power output drops and a greater portion of the negative sequence load current can be compensated by the inverter. Figure 6.6 shows the scaling factor increase to 0.47 following the drop in irradiance. The three-phase power supplied by the grid is shown in Figure 6.7. While the PV output is close to its rated current carrying capacity, the grid supplies almost all the negative sequence current drawn by the load. As a result, a large oscillation in the power supplied by the grid can be observed in Figure 6.7. Once the irradiance drops and the inverter is able to compensate a higher percentage of the unbalanced load, this oscillation decreases by almost 50%

From the DC link voltage shown in Figure 6.8 it can be seen that the MPPT algorithm is able to track the maximum power voltage, while the VSC is compensating the negative sequence load current. Despite the oscillation in the DC link voltage, the output of the MPPT algorithm, V_{ref} in Figure 6.8 settles at V_{mpp} .

When the irradiance level decreases, the converter has additional capacity now available to compensate the load. A larger negative sequence current is injected by the inverter which results in a higher DC voltage oscillation after $t = 0.61$ s as can be seen in Figure 6.8.

Due to the unbalanced current drawn by the load, the voltage at bus B1 is also unbalanced. The negative sequence component of the voltage at B1 is shown in Figure 6.9(b). When the PV inverter is able to compensate more of the negative sequence current, a smaller unbalanced voltage drop occurs over the line impedance and the magnitude of the negative sequence voltage is also reduced. Before 0.61 s the load voltage has a 1.6% negative sequence component, calculated as in (6.2).

$$UB\% = \frac{V_{pk}^-}{V_{pk}^+} \times 100\% \tag{6.2}$$

After 0.61 s the voltage contains a 0.89% unbalance. The positive sequence voltage is shown Figure 6.9(a).

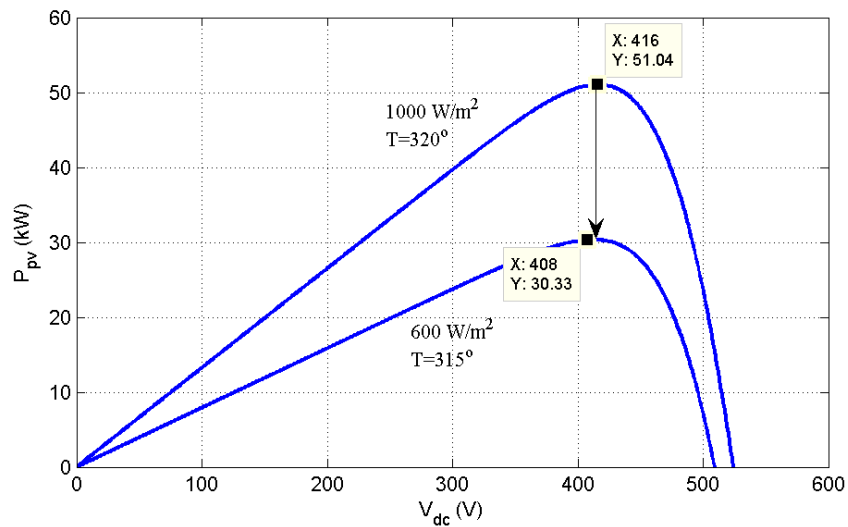


Figure 6.3: PV curves for case study 1

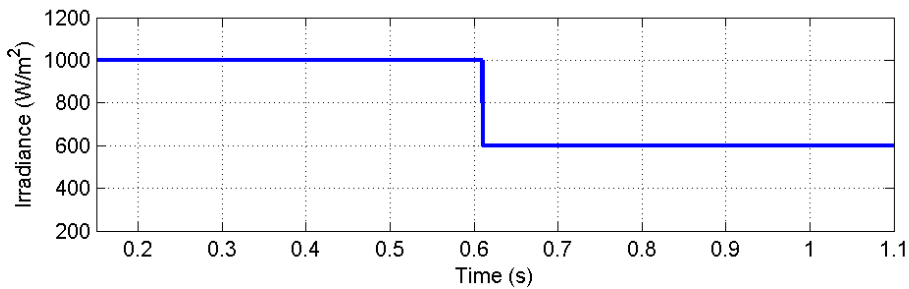


Figure 6.4: Irradiance of the PV array for case study 1

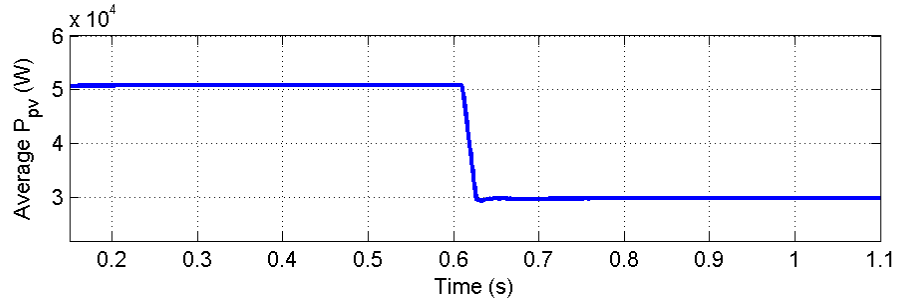


Figure 6.5: Moving- average of the power of the PV array

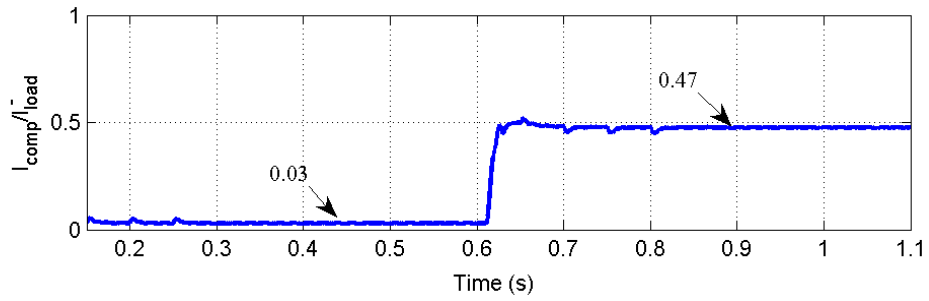


Figure 6.6: Scaling factor limiting the negative sequence inverter current I_{comp}

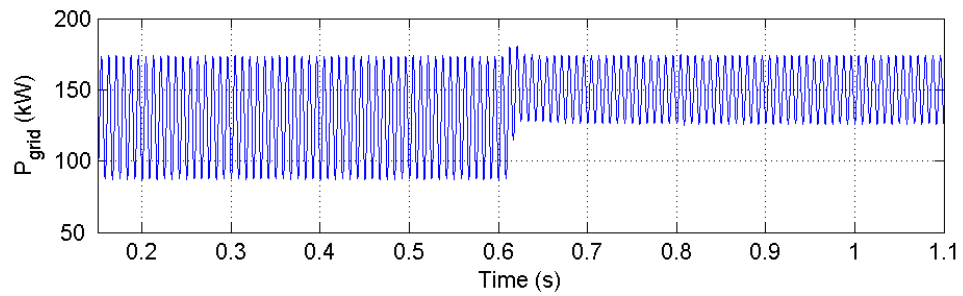


Figure 6.7: Grid power for case study 1

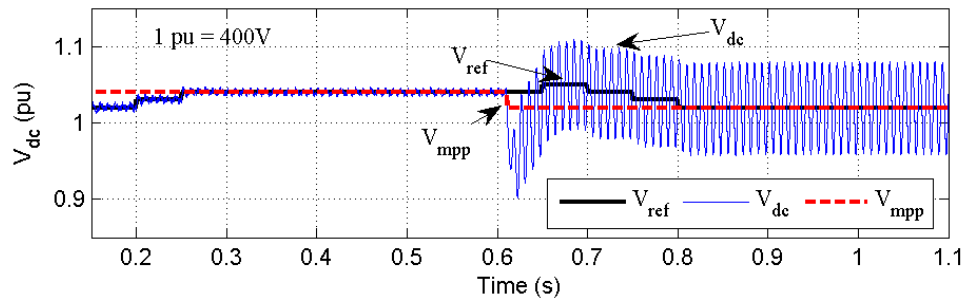


Figure 6.8: DC link voltage

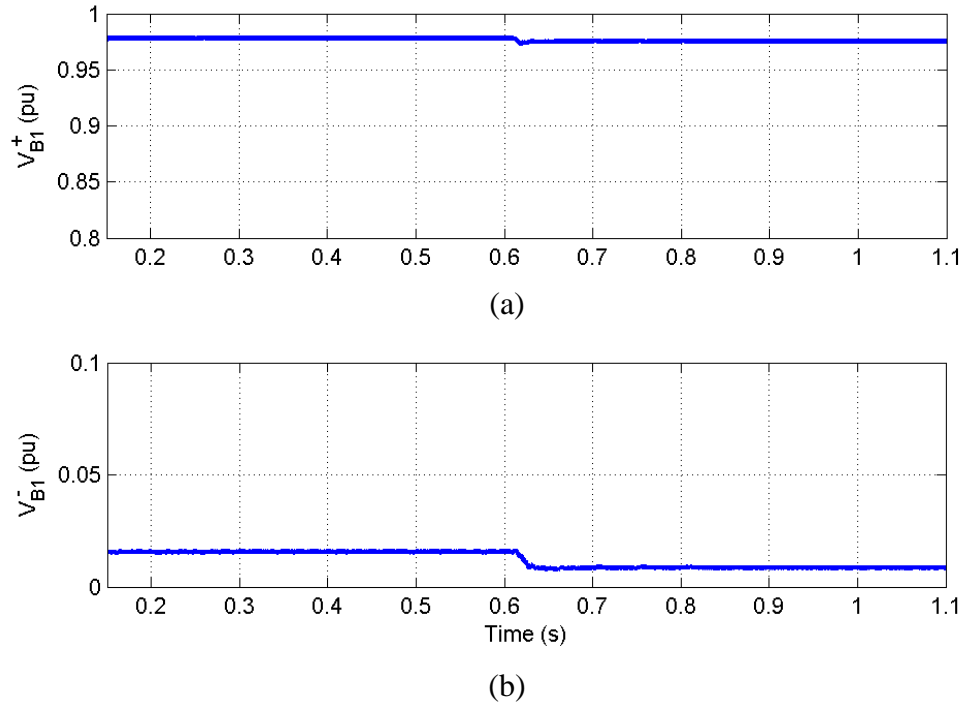


Figure 6.9: (a) Positive and (b) negative sequence voltage at bus B1

The results of case study 1 show that the inverter is able to provide partial compensation of the negative sequence load if the full negative sequence current exceeds the excess capacity of the inverter. The scaling block limits the compensating current reference according to the current rating of the inverter and the output of the DC link voltage controller. When the irradiance decreases the inverter is able to supply more compensating current. The negative sequence current compensation also reduces the negative sequence voltage.

6.3 Case Study 2: Unbalanced Grid Impedance

In a distribution system the causes of unbalance in the network are not limited to unbalanced loading. Untransposed lines and unequal feeder lengths can all result in unbalanced line impedances. Case study 2 explores the impact of an inherently unbalanced system on the ability of the PV inverter to provide load balancing services. To simulate an unbalanced grid, the equivalent grid impedance Z_{gr} is no longer the same for each phase. Instead, the line impedances of phases B and C are 50% and 10% greater respectively than that of phase A, although the X/R ratio has been maintained the same for all phases. The line impedances used in the first test of case 2 are listed in Table 6.1.

Table 6.1: Feeder impedances for case study 2

Phase	Line Impedance (Ω)
$Z_{gr,A}$	$0.029315+j0.0754$
$Z_{gr,B}$	$1.5 * Z_{gr,A}$
$Z_{gr,C}$	$1.1 * Z_{gr,A}$

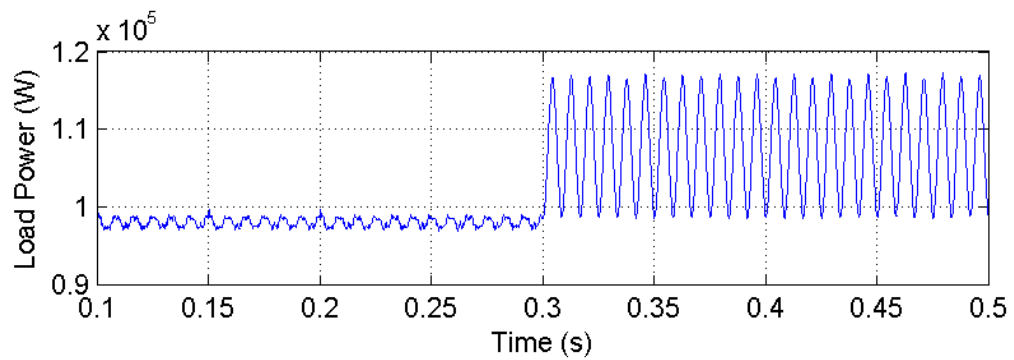
For case 2 the non-linear load is disconnected from the grid and switch S_{nl} is open. The PV array conditions are $IR = 700 \text{ W/m}^2$, $T = 325 \text{ K}$. Initially, only balanced loads are connected to bus 1. At $t = 0.3 \text{ s}$ S_{ub} closes connecting the single phase load $z_{ub} = 21.6 + j2.18 \Omega$. The test is carried out both with and without activation of the negative sequence compensation loop.

Although the load is balanced before $t = 0.3 \text{ s}$, the three phase power drawn from the grid is unbalanced, as can be seen from the oscillation in Figure 6.10(a). The positive and negative sequence voltages at bus B1 are shown in Figure 6.10(b)&(c). Figure 6.10(c) shows the voltage at B1 has a 0.38% imbalance before the single phase load z_{ub} is connected both with and without negative sequence compensation by the inverter. Because Z_{gr} is not symmetric there is an unbalanced voltage drop across the line impedance which causes the voltage at bus 1 to be unbalanced. Once the single phase load is added, the negative sequence voltage increases to 0.74% of the positive sequence voltage without negative sequence compensation and 0.43% with negative sequence compensation.

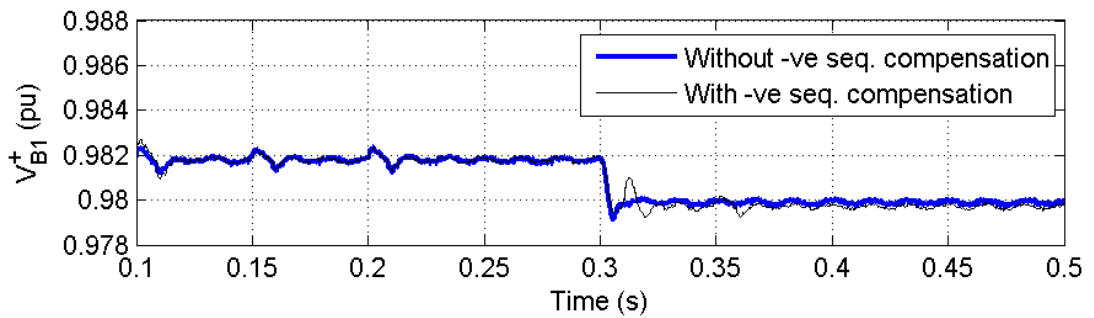
The negative sequence load and grid currents are shown in Figure 6.10(d). When the negative sequence load current is completely compensated by the inverter, the grid supplies only positive sequence current to the load. However, because of the unbalanced voltage drop on the line, the voltage still contains a negative sequence component as seen in Figure 6.10(b). A close-up of the negative sequence current before connection of the single-phase load is shown in Figure 6.10(e). The load current contains a negative sequence component with amplitude of 0.64 A before $t = 0.3 \text{ s}$ when only balanced loads are connected.

When the current is not compensated by the inverter, the single-phase load creates a ripple in the real and reactive three-phase power supplied by the grid. When the current compensation loop is active the oscillation in the grid power is eliminated as shown in Figure 6.10(f). The

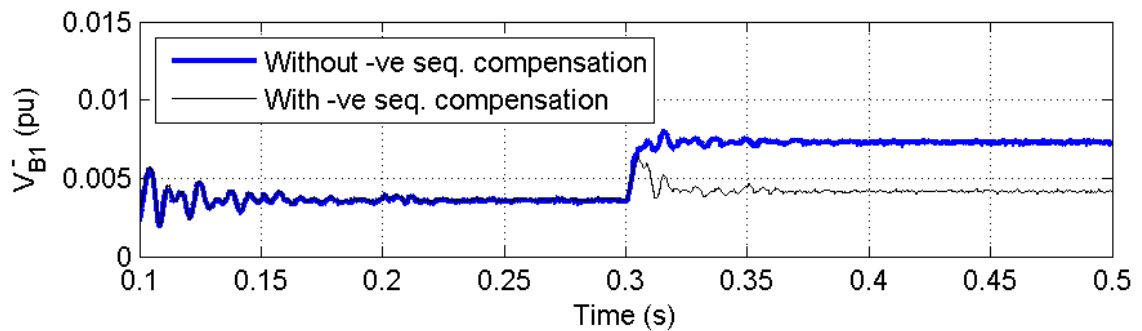
DC link voltage and average PV current are shown in Figure 6.10(g) and Figure 6.10(h) respectively for the case where the inverter provides negative sequence current compensation. Figure 6.10(h) shows a 0.23% decrease in the average output power of the PV array after $t = 0.3$ s. This corresponds to ripple in the DC link voltage in Figure 6.10(g). The change in PV power prompts the MPPT to decrease the voltage away from V_{mpp} at $t = 3.5$. A total decrease in the PV output power of 0.31% after compensation begins is observed in Figure 6.10(g).



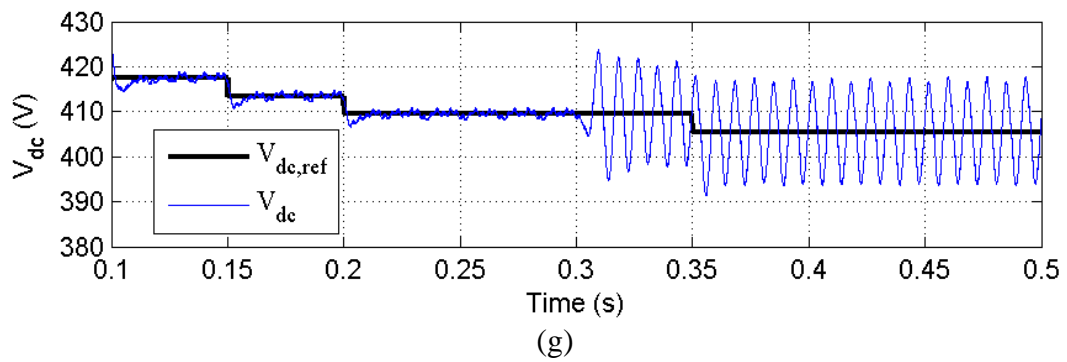
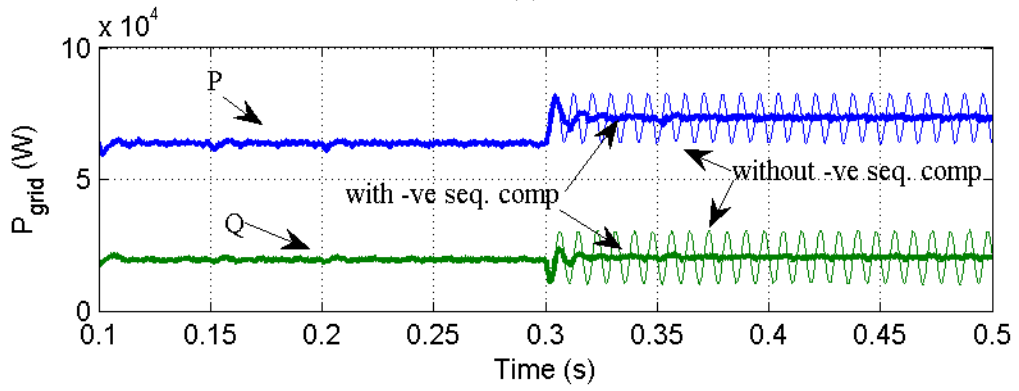
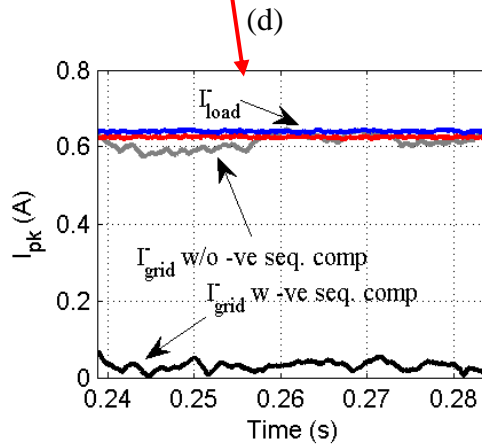
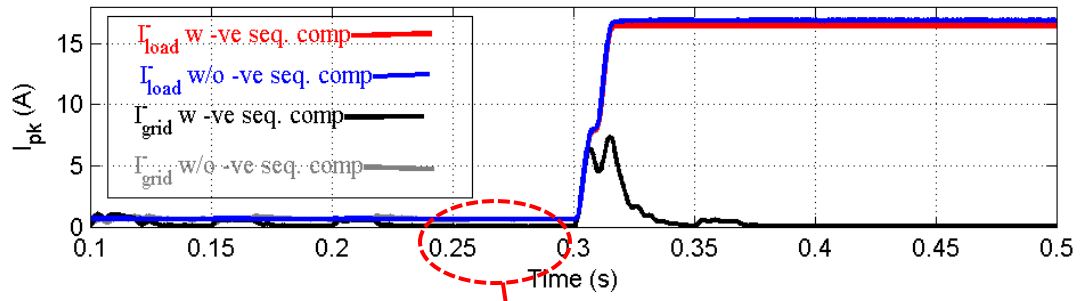
(a)



(b)



(c)



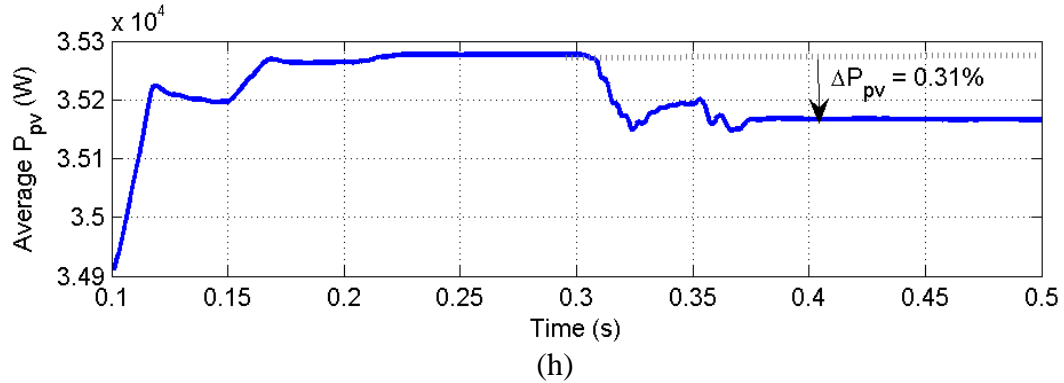


Figure 6.10: (a) Three-phase load power, (b) +ve sequence voltage (c), -ve sequence voltage, (d)-(e) -ve sequence current, (f) grid power, (g) DC link voltage, and (h) average PV power for case study 2

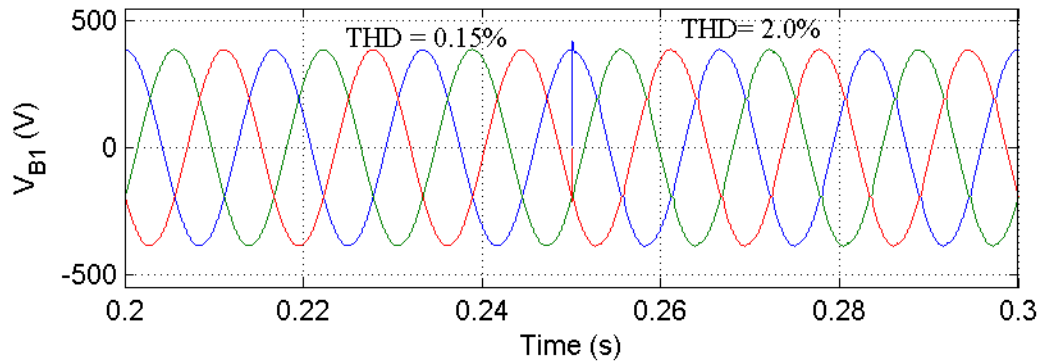
Case 2 demonstrates performance of the inverter in the presence of asymmetrical line impedances. Although negative sequence current compensation could eliminate the negative sequence voltage at bus 1, the voltage imbalance was reduced by 56% compared to the case where the compensation loop was disabled. Compensating the negative sequence current almost eliminates the oscillation in the power drawn from the grid.

6.4 Case Study 3: Non-Linear Loads

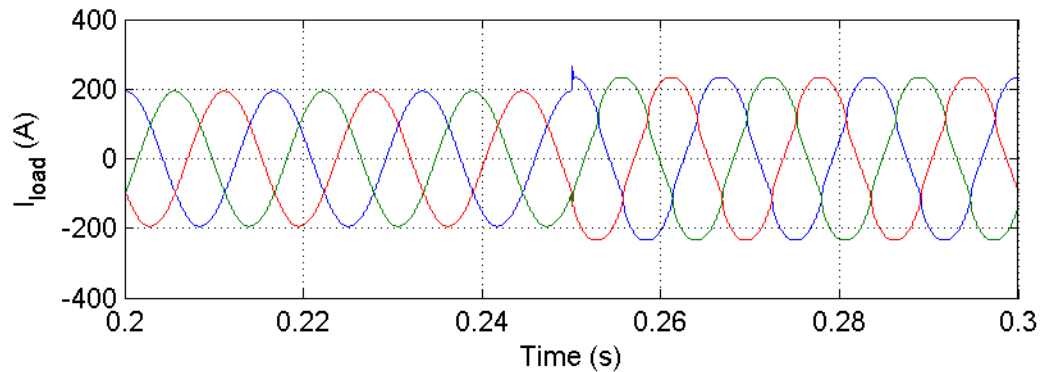
An important consideration in modern power systems is the impact of non-linear loads and sources. Non-linear loads can introduce harmonics in the voltage and current which causes deterioration in the power quality. Since the load current is used to calculate the compensating current reference, load current harmonics can introduce harmonic distortion into the current controller reference signals. This can lead to harmonics in the output current of the PV inverter. In case 3 the balanced rectifier load shown in Figure 6.1 is connected to the system to test the performance of the inverter control scheme in the presence of load current harmonics. In the first simulation for case study 3 the proposed HCDFT method of sequence extraction from Chapter 4 is used. The performance of the system using the HCDFT to measure the negative sequence current is compared to that obtained using AP filters and a DSOGI extraction technique.

In case study 3, switch S_{ub} is open and the load current remains balanced through the simulation. The line impedances are symmetrical with $L_{gr} = 0.2$ mH and $r_{gr} = 29.3$ m Ω .

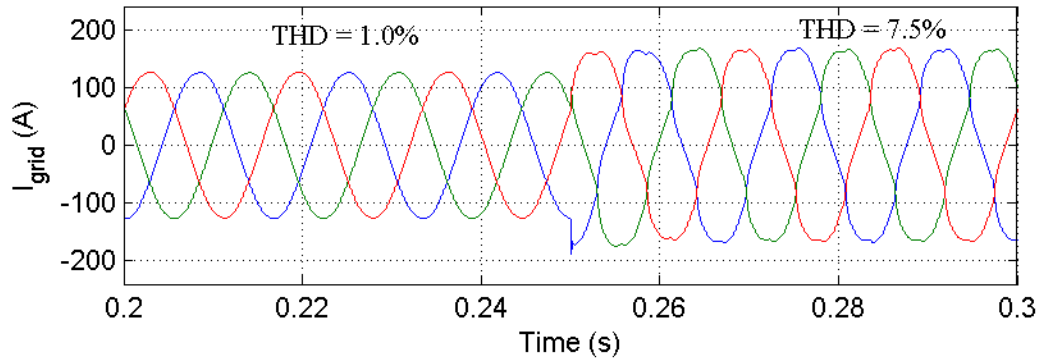
Under these conditions the inverter output should be the same both with and without the negative sequence compensation loop enabled. In case study 3, switch S_{nl} is initially open and only linear balanced loads are connected to bus B1. At $t = 0.25$ s S_{nl} is closed connecting a three-phase rectifier load to B1. The rectifier has a $15 \mu\text{F}$ output capacitor and supplies a 27.1 kW resistive load $r_{nl} = 15 \Omega$. When the non-linear load is connected the load current THD is 5.3% . The load current harmonics increase the harmonic distortion in the voltage at bus B1, shown in Figure 6.11(a). Prior to the connection of the non-linear load the voltage has a THD of 0.15% . Once the rectifier is connected, the THD increases to 2.0% . The load current is shown in Figure 6.11(b) and the grid current is shown in Figure 6.11(c).



(a)



(b)



(c)

Figure 6.11: (a) Voltage at the inverter bus and (b) load current, and (c) grid current when the HCDFT is used for case study 3

Within one half cycle of the fundamental after the non-linear load is connected, the HCDFT reference current calculator settles to zero, as shown in Figure 6.12. Even in the presence of harmonically distorted inputs the HCDFT retains a fixed settling time and nearly zero steady state error. The inverter current, is shown in Figure 6.13(a). After the non-linear load is connected, the THD increases from 1.9% to 2.5% due the distortion in the voltage at bus B1. To demonstrate the negligible impact of the compensation loop on performance under balanced harmonic load currents, the same test has been carried out with the compensation loop disabled. The PV inverter current for this case is shown in Figure 6.13(b). By comparing Figure 6.13(a) and Figure 6.13(b) it can be seen that there is no additional distortion in the inverter current due to the compensation current reference when the HCDFT is used.

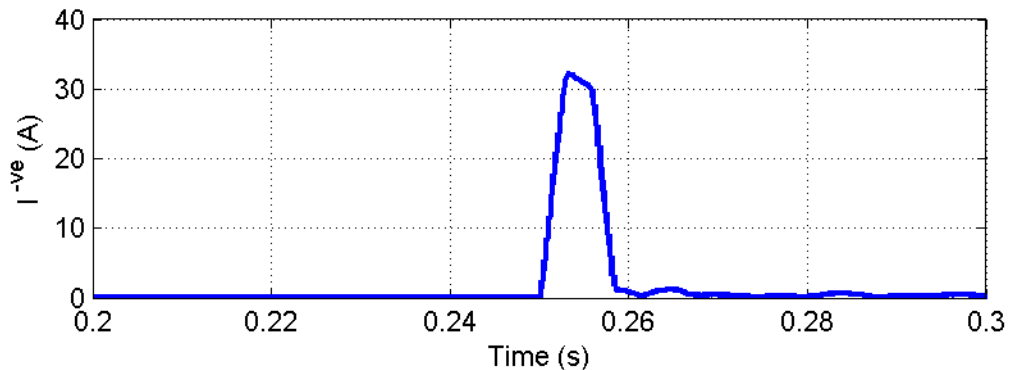


Figure 6.12: Negative sequence amplitude calculated by the HCDFT when a three-phase rectifier load is connected

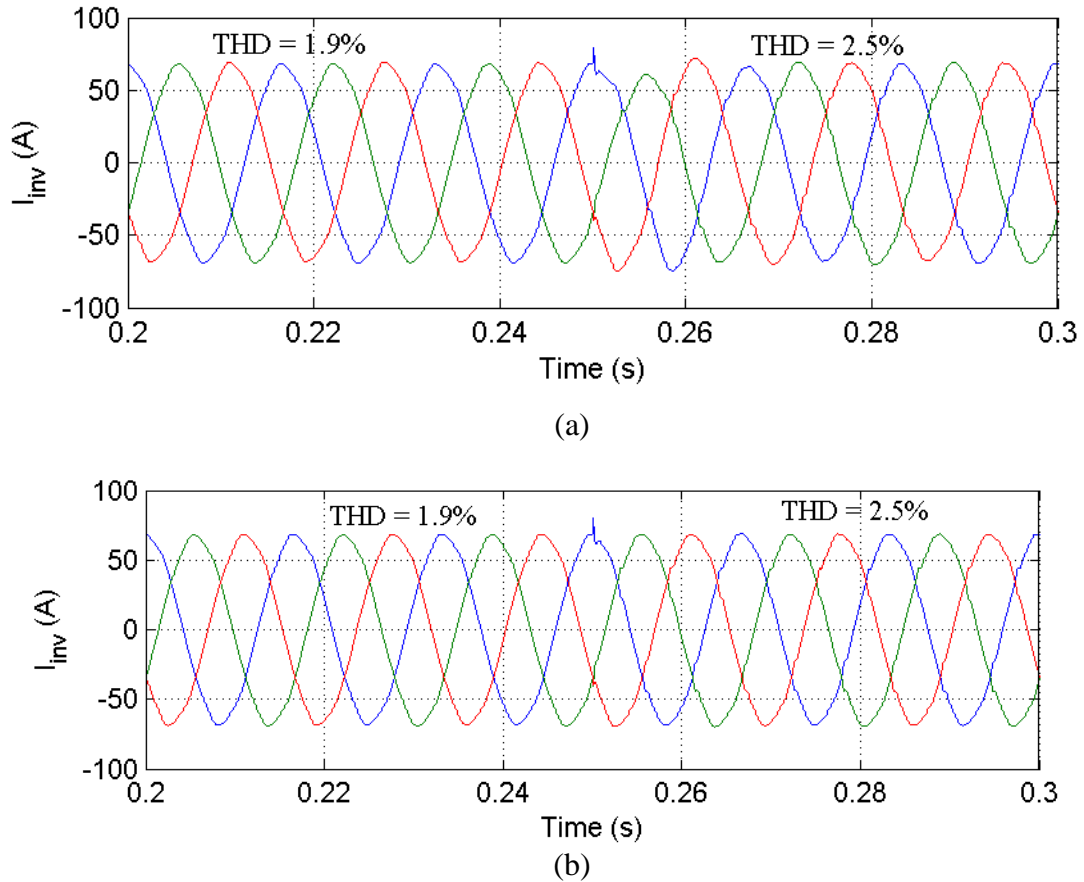


Figure 6.13: (a) Current injected by the PV inverter when the HCDFT method is used to calculate the compensation current and (b) inverter current when the compensation loop is disabled

Next, the compensation loop is re-enabled, and two conventional methods, AP filters and the SOGI, are used to calculate the negative sequence load current. Results for the AP filter and SOGI are shown in Figure 6.14 and Figure 6.15 respectively. The amplitude of the compensating current reference in Figure 6.14(a) should be zero because the system is balanced. However, the amplitude shown in Figure 6.14(a) has a non-zero output once switch S_{n1} closes. After the non-linear load is connected the inverter current using AP filters, shown in Figure 6.14(b), has a THD of 15%.

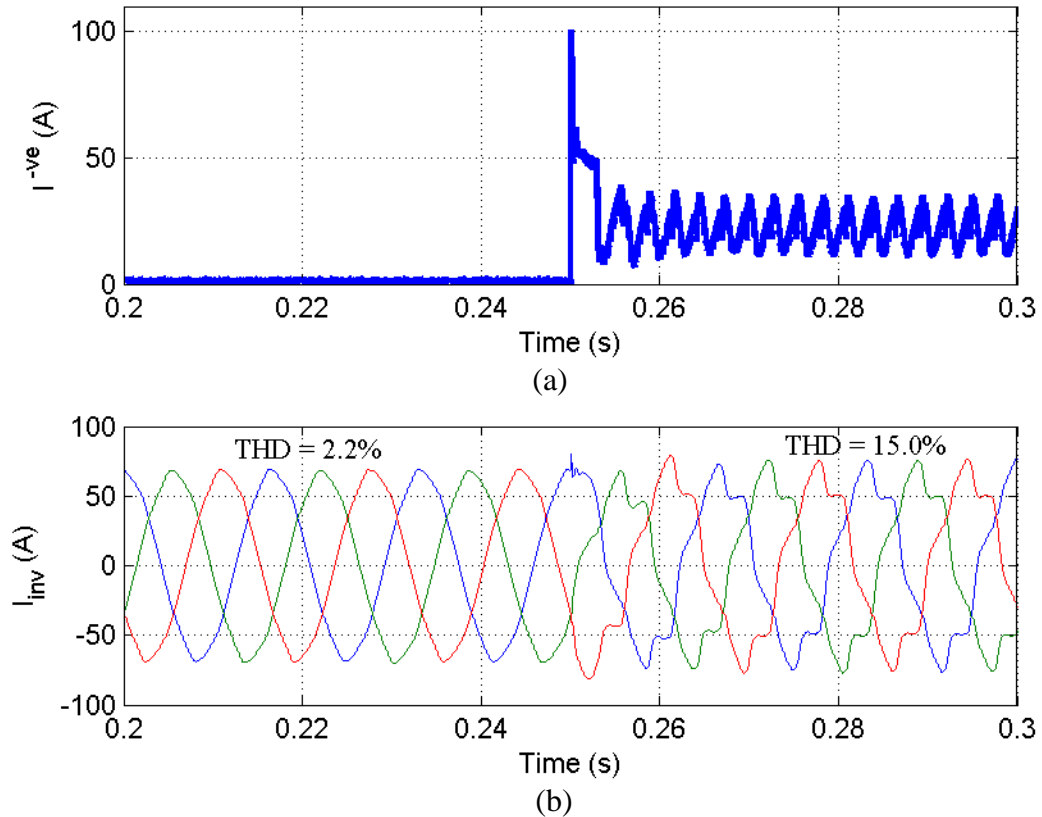


Figure 6.14: (a) Amplitude of the negative sequence reference current and (b) inverter current when AP filters are used to calculate the compensation current

Comparing Figure 6.15(a) and Figure 6.14(a) shows that the error in the reference compensation current amplitude is lower using SOGI filters. However, compared to using the HCDFT, the SOGI method produces a higher overshoot and steady-state error in the compensating current reference amplitude. This results in a higher THD in the inverter current, shown in Figure 6.15(b). The inverter current, grid current, and load voltage THDs are listed in Table 6.2 for the HCDFT, AP filters, SOGI, and with the compensation reference disabled.

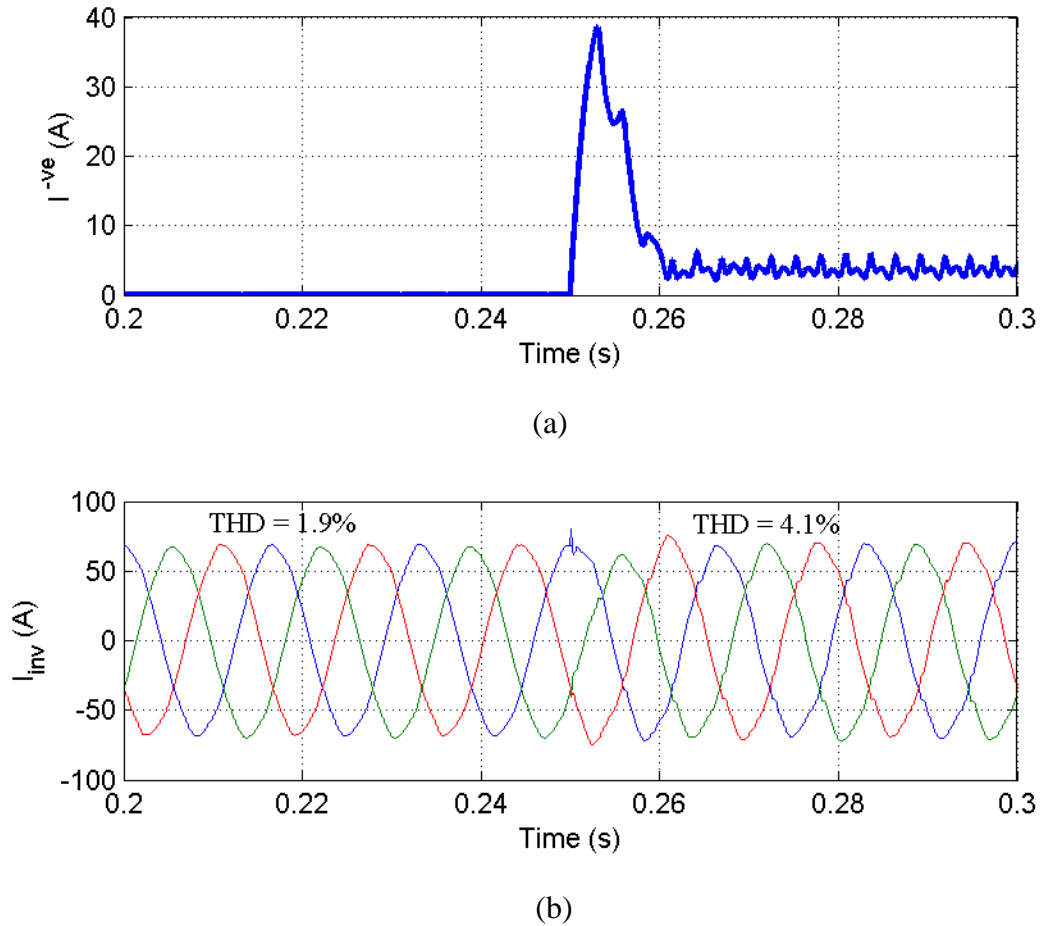


Figure 6.15: (a) Amplitude of the negative sequence current reference and (b) inverter current when SOGI filters are used to calculate the compensation current

Table 6.2: Current and voltage THDs for case study 3

Sequence calculation method	Compensation disabled	HCDFT	APF	SOGI
Inverter Current THD	2.5%	2.5%	15%	4.1%
Grid Current THD	7.5%	7.5%	10.0%	8.1%
Voltage at B1 THD	2.0%	2.0%	2.4%	2.1%

When the HCDFT is used, current and voltage THDs are the same as when the inverter is controlled in power conversion mode without compensation. These values are listed in

columns 2 and 3 of Table 6.2. Because of the resonant element in the SOGI filters, this method showed significant improvement over the AP filters. However, it could not entirely attenuate the harmonics in the load and Figure 6.15 shows increased current distortion when the rectifier load was connected. The HCDFT method has a comparable settling time to that of the SOGI reference technique, however it also shows improved steady state harmonic rejection compared to the SOGI.

Case study 3 demonstrates the performance of the HCDFT method in the presence of load current harmonics caused by non-linear loads. When the HCDFT reference calculator is employed there is no additional harmonic distortion compared to the case where no compensation current reference is added.

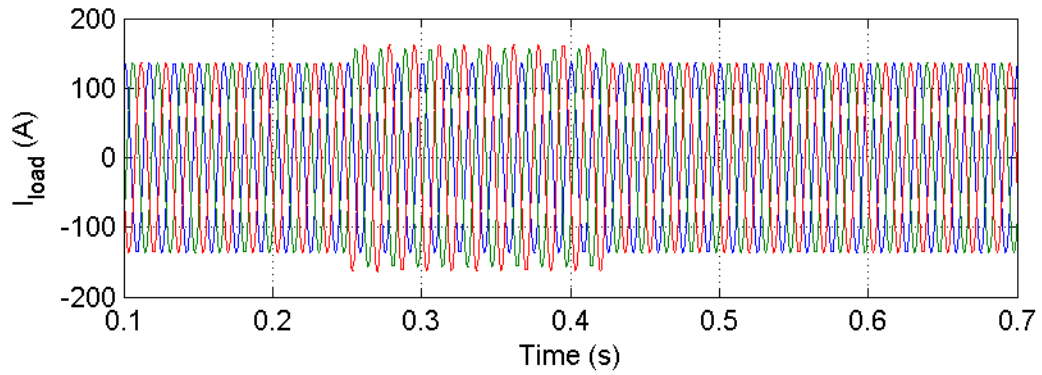
6.5 Case Study 4: Transient Unbalanced Loads

Microgrids and remote grids may be subjected to quickly varying single phase loads, such as single-phase motor start-up. Case study 4 verifies the controller performance under quick unbalanced load switching. The results show there can be interaction between the negative sequence current compensation and the P&O MPPT algorithm under such conditions.

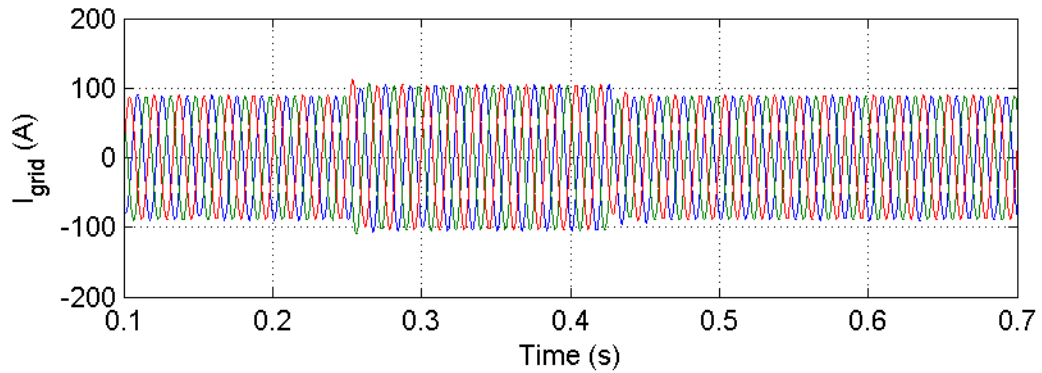
In case study 4, switch S_{ub} closes at $t = 0.25$ s, connecting the single-phase linear load $z_{ub} = 24 \Omega$ to bus B1. After 10 cycles S_{ub} opens and the load is disconnected. At 60 Hz this equates to 167 ms. This is considered “fast” since the slowest loop of the control scheme, the MPPT algorithm, runs at a time step of 50 ms, which is close to time step of the load change. The PV array experiences an irradiance level of 590 W/m^2 at a temperature of 325 K.

The load current is shown in Figure 6.16(a). From $t = 0.25$ s to $t = 4.17$ s an imbalance in the load current can be observed in Figure 6.16(a), which is caused by the single phase load. The grid current is shown in Figure 6.16(b), and the inverter current is shown in Figure 6.16(c). The transient response of the grid and inverter currents following the connection of a single phase load can be seen in Figure 6.17. Figure 6.17(a) shows that within one cycle of connecting the single-phase load, the grid current is balanced. The positive and negative sequence components of the reference current are controlled together in the ABC frame, thus

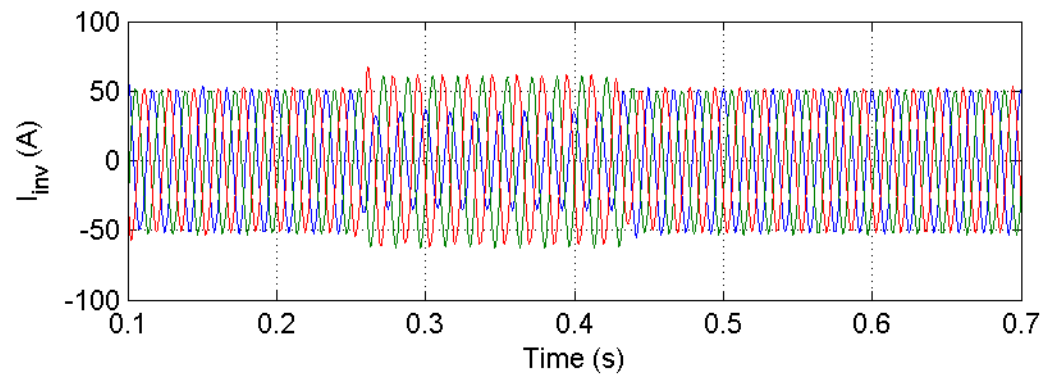
there is no difference in the transient response for a positive or negative sequence step change in the reference.



(a)



(b)



(c)

Figure 6.16: (a) Load current, (b) grid current, and (c) inverter current for case study 4

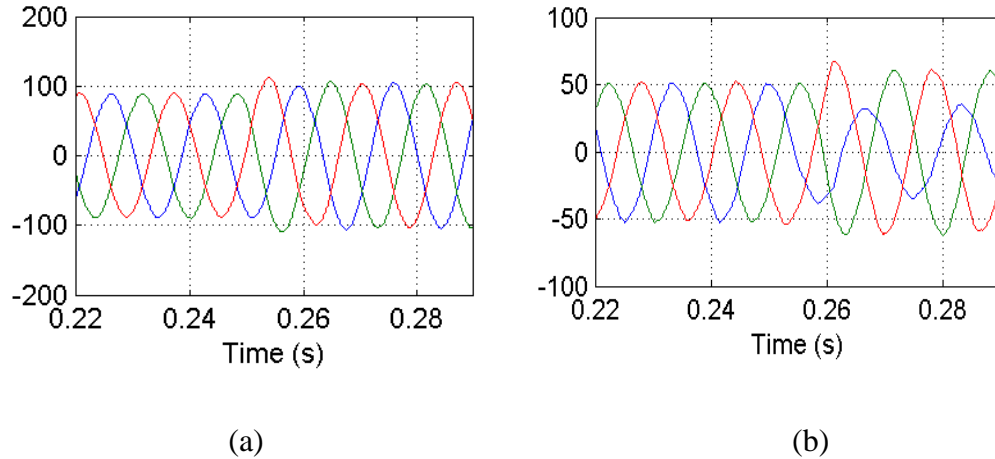


Figure 6.17: (a) Grid current and (b) inverter current transient following connection of the unbalanced load

The average power output of the PV array is shown in Figure 6.18, and the DC link voltage is shown in Figure 6.19. Before S_{ub} closes, the array is operating at the maximum power point. When the inverter begins to compensate the unbalanced load, the average power drops by 80 W (0.267%), as seen in Figure 6.18, due to the oscillation in the DC link voltage. The P&O algorithm detects the drop in power and according to the logic in Figure 3.39 the voltage reference is decremented. At the next time step of the MPPT 50 ms later, the algorithm detects that lowering the voltage reference does not cause an appreciable increase in power and so does not alter the voltage reference. When the single phase load is disconnected, the DC oscillation ripple dies out and the average power increases. This creates a true value for the condition ' $\Delta P > P_{min}$ ', while the result of the ' $\Delta V > 0$ ' condition is also true because of small oscillations in the DC link voltage measurement. Under these conditions the MPPT logic is programmed to increment the voltage reference in response to the change. Figure 6.18(b) shows that the PV power output, from $t = 0.25 - 0.3$ s is equal to the power output after the DC link voltage reference decreases at 0.3 s. The efficiency of energy harvesting is therefore unaffected by the interaction between the P&O technique and the negative sequence compensation.

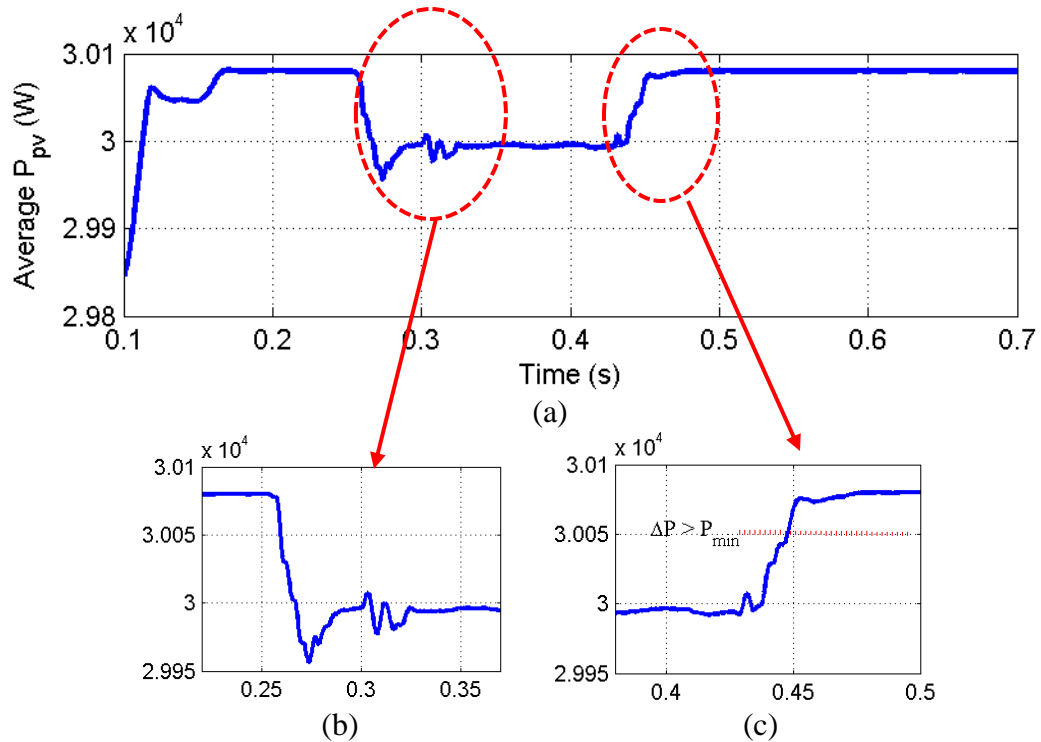


Figure 6.18: Moving-window average of PV power during Case 4

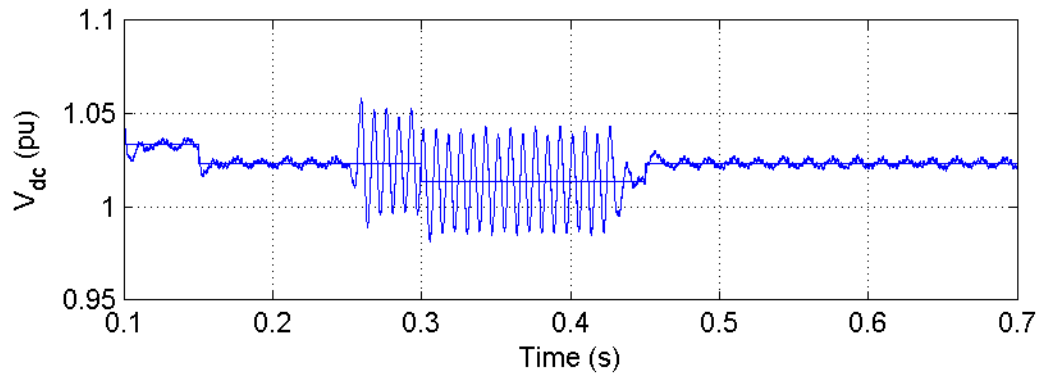


Figure 6.19: DC link voltage during case study 4

The results of case study 4 show that the inverter is able to compensate the negative sequence load current during a short (10 cycle) duration interval. Although the P&O algorithm cannot distinguish between a change in power due to environmental changes or due to the DC link voltage ripple, it does not cause additional power loss in case study 4.

6.6 Case Study 5: Phase Balancing in a Hybrid Diesel-PV Microgrid

Diesel engine driven synchronous generators are commonly used to supply electricity for small remote communities and commercial ventures. Microgrids also typically require diesel gen-sets to be used for backup when renewable sources have insufficient generation capability. Case study 5 verifies the performance of the proposed control strategy in the hybrid diesel-PV grid shown in Figure 6.20.

Unbalanced loading poses a challenge for these kinds of isolated grids. Single phase loads can cause the voltage to become unbalanced which will disrupt the operation of three-phase machine loads. The power oscillation can cause ripples in the generator torque which decreases the efficiency of the engine and puts additional stress on the shaft. Unbalanced loading also requires de-rating the generator due to higher peak to average power ratio.

The remote grid shown in Figure 6.20 is constructed in Simulink® using the SimPowerSystems® toolbox. The loads are supplied by a hybrid system consisting of a 150 kVA diesel-engine driven synchronous generator, and a 50 kVA PV system, with the control scheme shown in Figure 3.1. The current supplied by the generator is i_{gen} , and i_{inv} is the current supplied by the PV inverter on the Wye side of the transformer. The generator is controlled with a 1.67% frequency droop, which results in a maximum 0.5 Hz under/over frequency at the maximum/minimum power output respectively. An IEEE type 1 Automatic Voltage Regulator (AVR) is implemented using the predefined SimPowerSystems® block to control the terminal voltage of the generator. The AVR maintains the voltage within $\pm 5\%$ of the nominal over a ± 0.27 pu reactive power output. The generator controller parameters are listed in Appendix B. A balanced, delta connected load, $z_{p3} = 3.78 + j1.40$ is connected to bus B1. A single phase load $z_{ub} = 14.4 \Omega$ is connected to bus B1 through the switch, S_{ub} .

In case study 5, the switch S_{ub} is initially open and the grid supplies only balanced loads. At $t = 6$ s, the S_{ub} is closed, connecting the single phase load to bus B1. The irradiance and temperature of the PV panels remain constant during the test at 700 W/m^2 and $51.9 \text{ }^\circ\text{C}$ respectively.

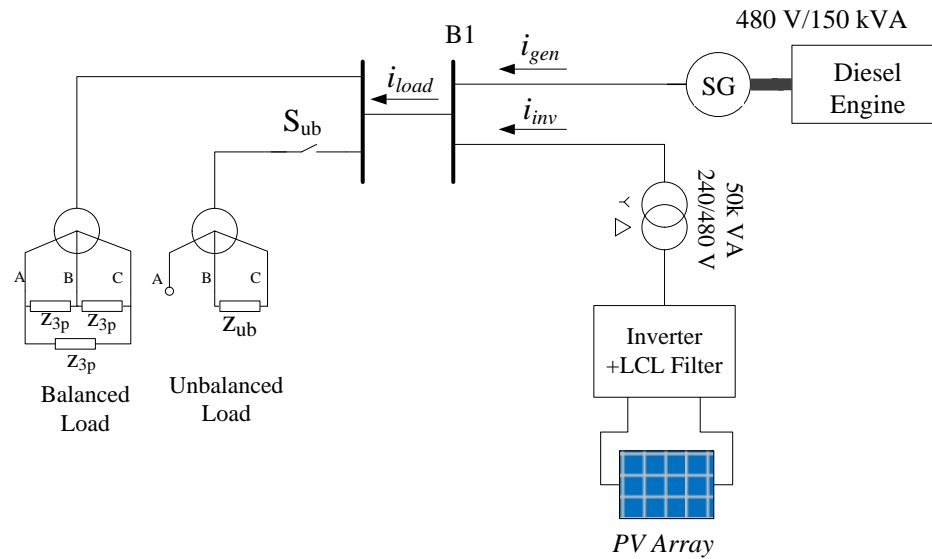


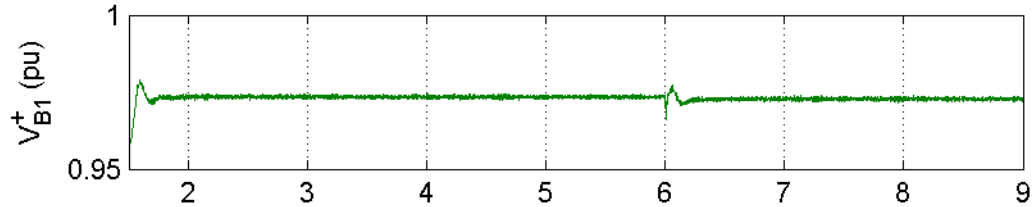
Figure 6.20: Single line diagram of the remote grid simulated in case study 5

6.6.1 System Performance without Negative Sequence Compensation

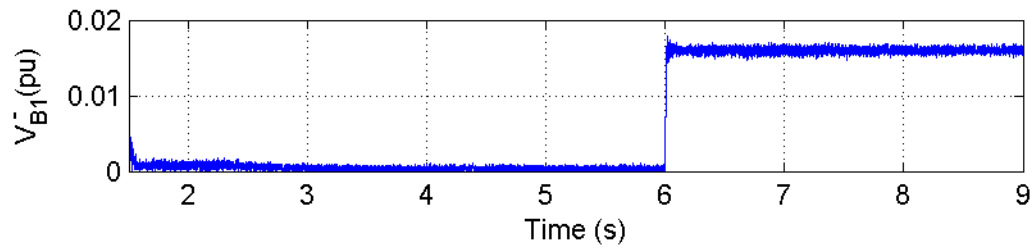
In the first test the PV inverter is run in power conversion mode only, and the negative sequence compensation reference is disabled. System voltage, current, PV power, and generator power are illustrated in Figure 6.21. The positive and negative sequence voltages at bus B1 are shown in Figure 6.21(a)&(b). Before the single-phase load is connected, the negative sequence component of the load voltage is equal to zero. At $t = 6$ s the negative sequence voltage at bus 1 increases to 1.7% due to the unbalanced current drawn by the load. The output of the diesel generator is 132 kVA at 0.9 pf lagging, prior to $t = 6$ s. Since the generator supplies the negative sequence load current, double line frequency ripples are produced in the real and reactive power output of the generator, which can be seen in Figure 6.21(c).

Figure 6.21(c) shows the generator frequency during the simulation period. Before $t = 6$ s, the generator frequency settles at 59.71 Hz. Due the low inertia of the system, the additional load switched on at $t = 6$ s causes a transient drop in the grid frequency. Following the transient the generator frequency settles to a value of 59.61 Hz.

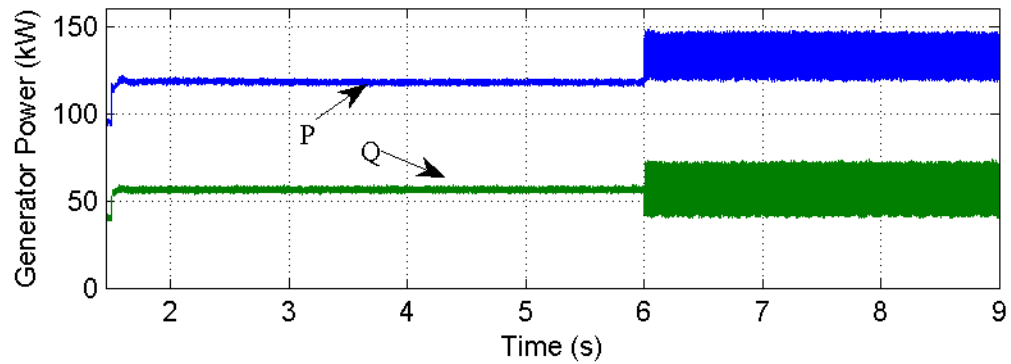
The load, generator, and inverter load currents from $t = 5.8 - 6.2$ s are shown in Figure 6.21(e)-(g) respectively. The imbalance in i_{load} and i_{gen} is visible in Figure 6.21(e) and Figure 6.21(f). The inverter current remains balanced, as shown in Figure 6.21(g) because the compensation reference has been disabled. The PV inverter supplies 35.3 kW, as seen in Figure 6.21(i), which is the maximum power for the given environmental conditions.



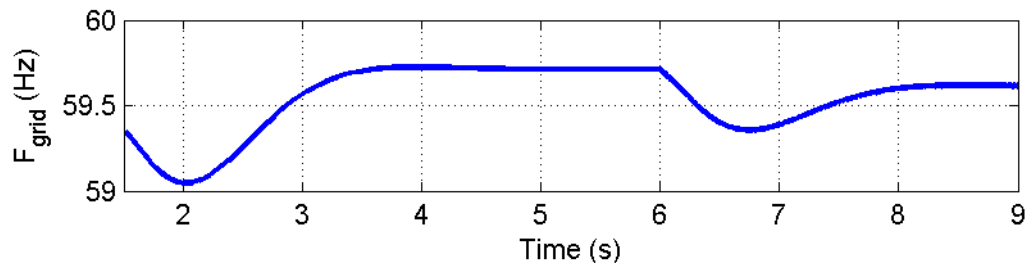
(a)



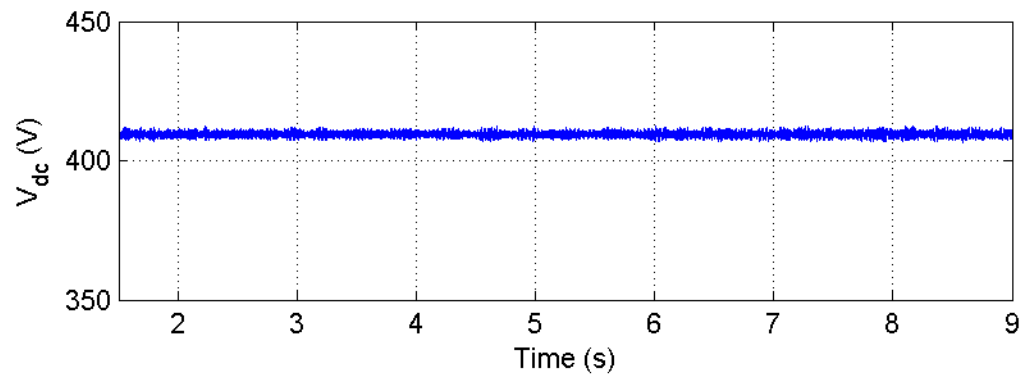
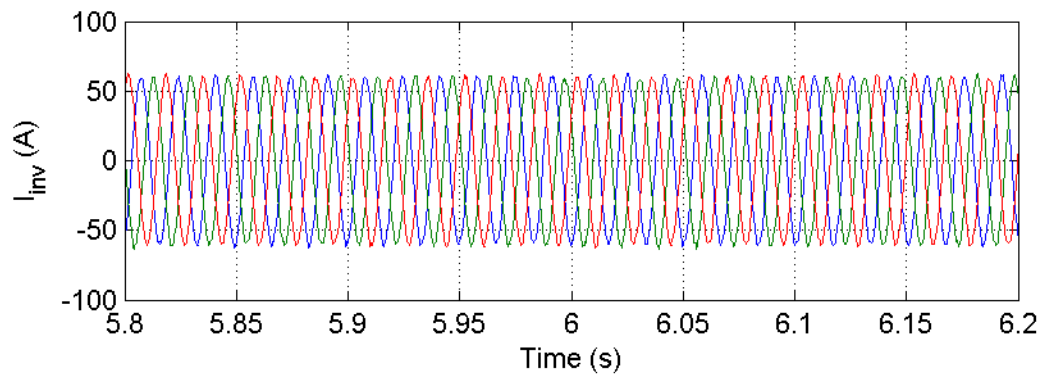
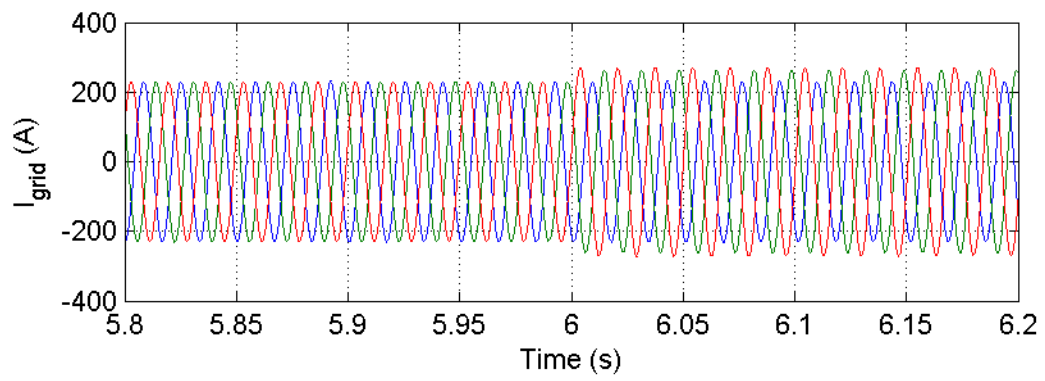
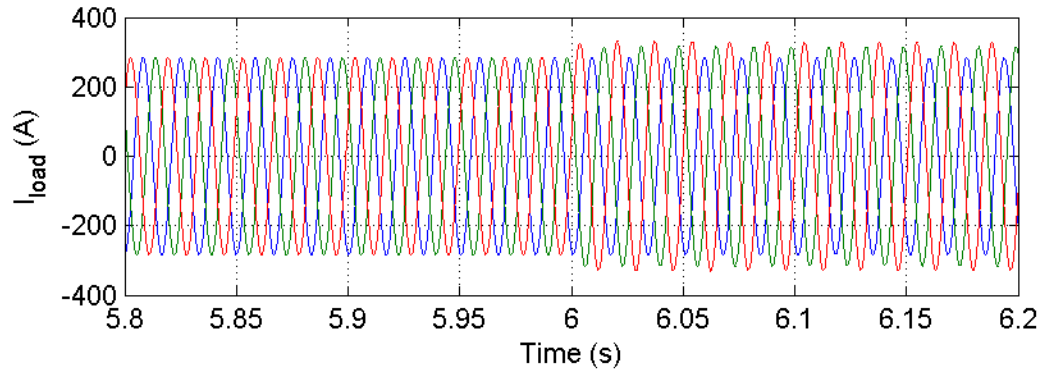
(b)



(c)



(d)



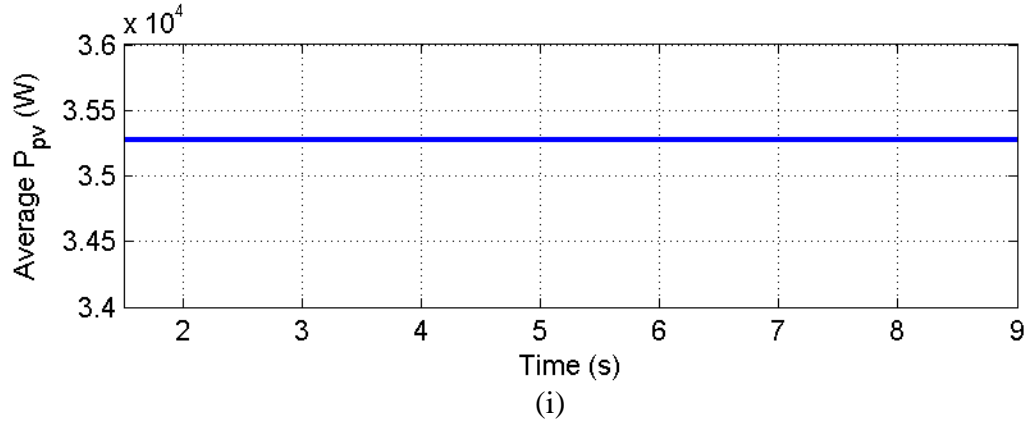


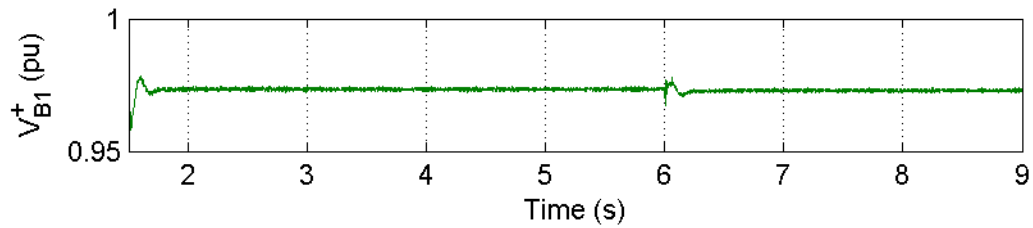
Figure 6.21: Unbalanced loading without phase balancing, (a) positive sequence voltage at bus 1, (b) negative sequence voltage at bus 1, (c) frequency, (d) real and reactive power supplied by the generator, (e) load current, (f) generator current, (g) inverter current, (h) DC link voltage, and (i) average PV array power

6.6.2 System Performance with Negative Sequence Current Compensation

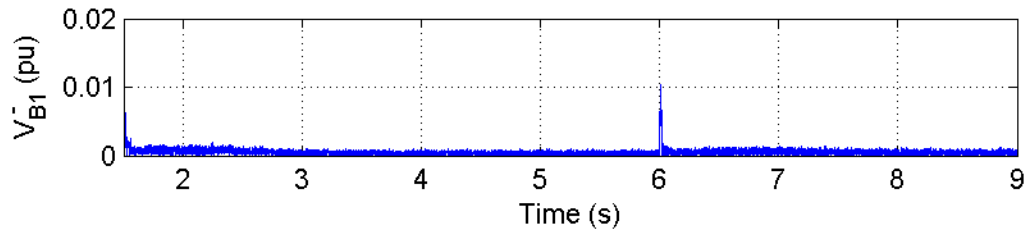
In the second simulation, the same load conditions are created, but the negative sequence load current compensation loop is activated. The results of the second simulation are shown in Figure 6.22. The positive sequence voltage at bus B1, seen in Figure 6.22(a), is the same as in the first simulation. The negative sequence voltage in Figure 6.22(b) however is still equal to zero after single-phase load is connected, because the inverter supplies the negative sequence component of the load current. At $t = 6$ s, the real and reactive power of the generator increases to supply the additional load, however the oscillation seen in Figure 6.21(c) is no longer observable in Figure 6.22(c).

Figure 6.22(d) shows that grid frequency is the same as in the first simulation. In order to demonstrate the efficacy of the HCDFT technique proposed in chapter 4, the negative sequence reference current is shown in Figure 6.22(e) along with the negative sequence load current calculated using the conventional HCDFT. Due to the grid frequency deviation, even when only balanced loads are connected the conventional HCDFT method measures a non-zero negative sequence load current. The output of the conventional HCDFT has a large oscillatory error after the single phase load is connected compared to the output of the HCDFT described in Chapter 4. When the HCDFT technique from Chapter 4 is used, the correct reference current is obtained despite the variations in grid frequency.

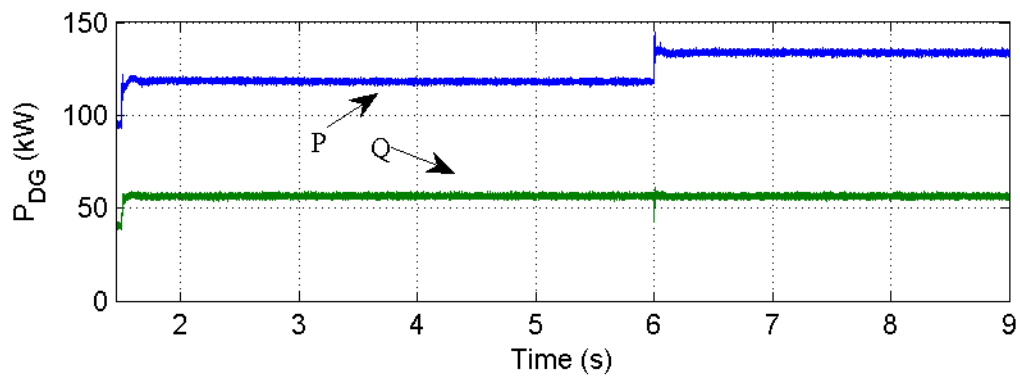
In the second simulation, the load current, shown in Figure 6.22(f), is equal to the load current from the first simulation. The grid current, however, remains balanced even after the single-phase load is connected, as shown in Figure 6.22(g), while the inverter supplied the negative sequence load current, as shown in Figure 6.22(h). Compensating the negative sequence load current induces a double line frequency ripple in the DC link voltage of the inverter, seen in Figure 6.22(i). The DC link voltage ripple results in a 268 W (0.76%) decrease in the average output from the PV array, as shown in Figure 6.22(j).



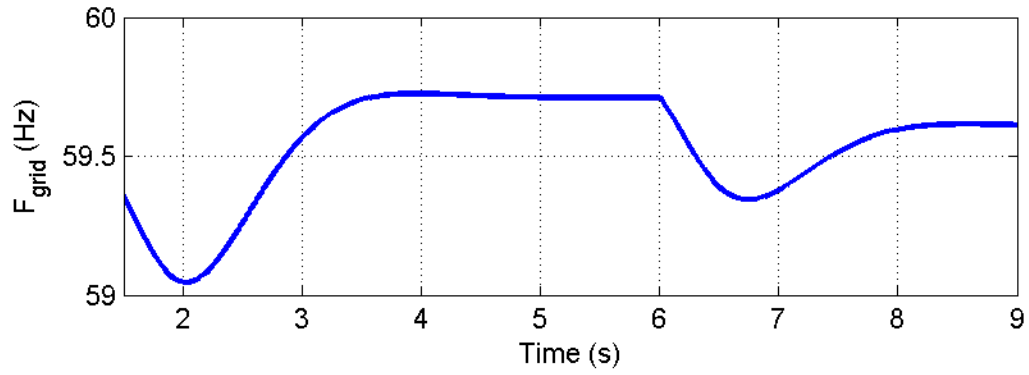
(a)



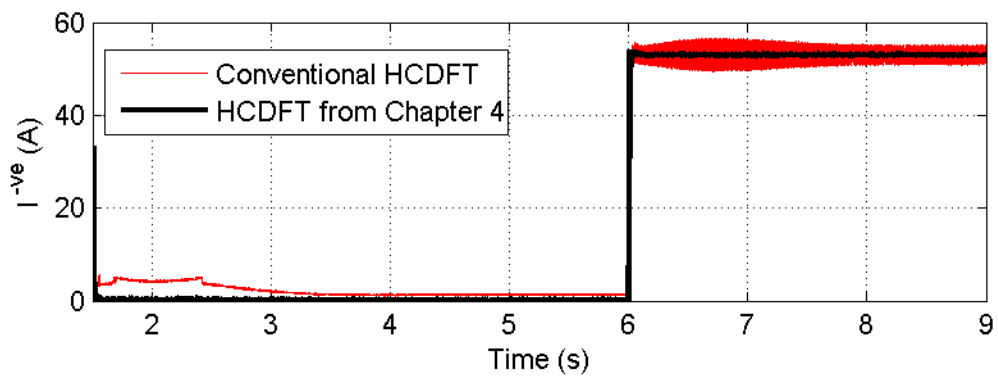
(b)



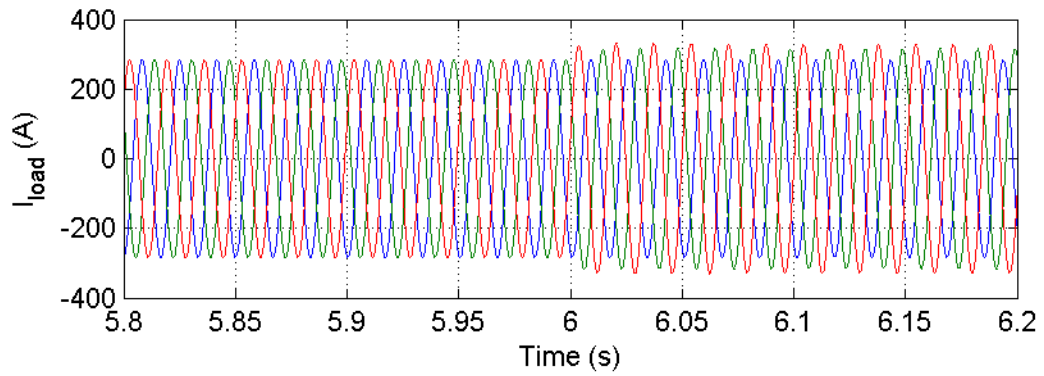
(c)



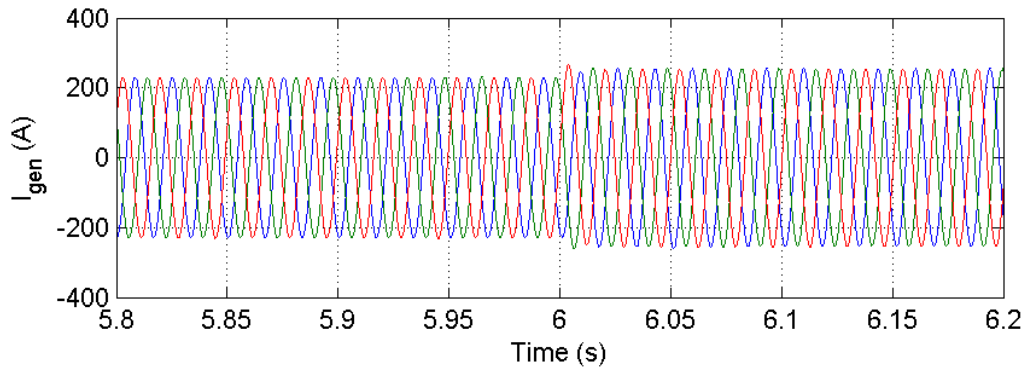
(d)



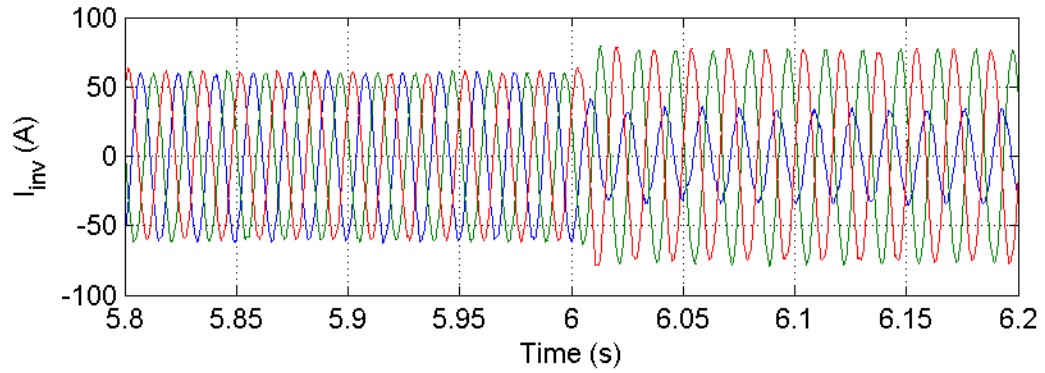
(e)



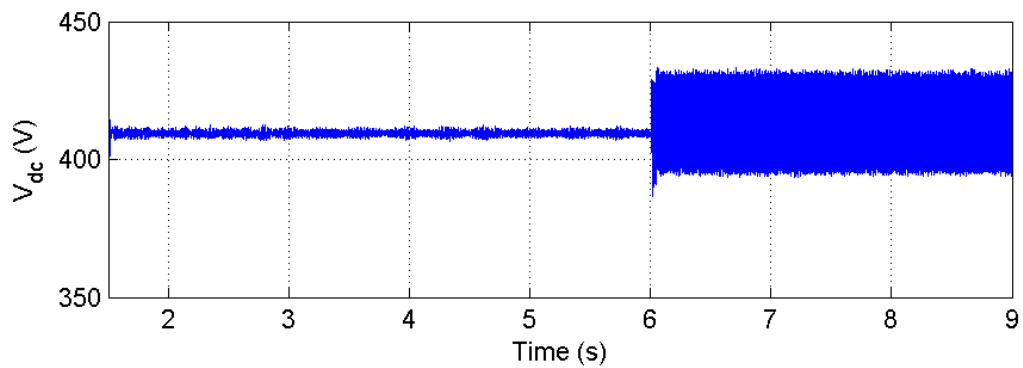
(f)



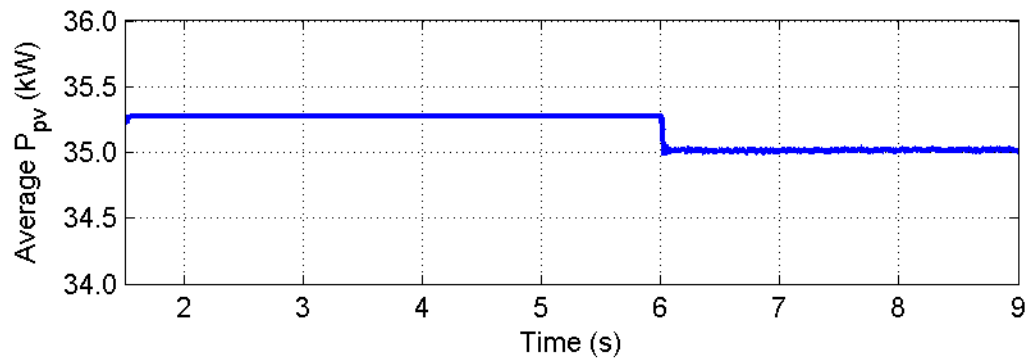
(g)



(h)



(i)



(j)

Figure 6.22: System variables when the PV inverter compensates load unbalance, (a) positive and (b) negative sequence voltages at bus 1, (c) generator real and reactive power, (d) grid frequency, (e) measured negative sequence load current, (f) load current, (g) generator current, and (h) inverter current. (i) DC link voltage, and (j) average PV power

Case study 5 demonstrates the ability of the proposed control scheme in a low inertial microgrid. Even though the grid experiences frequency deviations the proposed negative

sequence current calculation method is able to generate the correct compensation current reference. When the PV inverter compensates the negative sequence current, the voltage remains balanced even after connecting the unbalanced load. The HCDFT algorithm proposed in Chapter 4 accurately estimated the negative sequence load current, unlike the conventional HCDFT.

6.7 Conclusions

The efficacy of the proposed control scheme described in Chapters 3 and 4 has been tested by extensive simulation using Matlab/Simulink®. A number of grid conditions have been considered, including excessive negative sequence currents, line impedance asymmetry, non-linear loads and grid frequency fluctuations. The proposed control scheme allows the PV system to simultaneously inject real power and compensate the negative sequence load current using the available inverter capacity. Priority is given to real power conversion. While the inverter supplies an unbalanced current, the controller is able to continue tracking the maximum power point under changing irradiance and temperature conditions. The HCDFT sequence calculation algorithm is shown to allow the control scheme to reject harmonics in the measured load current. When the inverter is tested in a hybrid diesel-PV microgrid the compensated HCDFT algorithm discussed in Chapter 4 is shown to accurately calculate the negative sequence load current even when the frequency deviates from the nominal value.

Chapter 7

7 Summary and Conclusions

In the previous chapters, a control scheme for a three-phase VSC has been developed for simultaneous power conversion and load balancing. The control scheme has been verified through simulation in the Matlab/Simulink® environment. In Chapter 1, the concept of the microgrid is introduced. The issue of unbalance in power grids is discussed including the effect of unbalanced voltage on inductor motors and unbalanced loading of synchronous generators. Next the idea of using PV interfacing converters to provide phase balancing is introduced. The motivations and goals of the thesis are presented.

Chapter 2 provides details on symmetrical components theory, different phase balancing devices, and PV inverter control. An introduction to symmetrical components theory is given at the beginning of Chapter 2, followed by a literature review on methods for calculating compensating negative sequence currents. Previously reported dual purpose PV systems are discussed. Control considerations for inverters with LCL filters are reviewed. The issue of filter resonance is explained and previous solutions are described.

In Chapter 3, the proposed control scheme for a PV inverter is presented. A model of the VSC is developed. Based on the model of the LCL filter, a new active damping scheme is proposed using a dual variable feedback. A method of calculating the damping gains based on desired damping ratio is shown. The procedure for calculating PR controller gains based on desired frequency response characteristics is presented. Furthermore, an anti-windup scheme for a PR control is proposed and demonstrated.

An algorithm to calculate the negative sequence current reference is described in Chapter 4. In the proposed method, the half-cycle DFT is used to calculate sequence components and a numerical compensation technique is presented to reduce errors during off-nominal grid frequency. Compared with AP filters and notch filter based techniques the proposed method shows similar settling time and far superior harmonic filtering.

In Chapter 5 the interaction between active power generation and unbalanced compensation is examined through case studies. The region of operation of the PV array is shown to have

an impact on the voltage ripple at the DC link during unbalance compensation. The ability of the system to compensate unbalanced loads at various levels of solar insolation is confirmed.

Five case studies are presented in Chapter 6 to demonstrate the performance of the proposed control scheme under different grid and load conditions. Partial compensation of the unbalanced current is shown for a case where the VSC has insufficient capacity to supply the whole negative sequence. The HCDFT algorithm is shown to have good performance in the presence of non-linear loads creating harmonic current distortion. A network with unbalanced line impedance is used as the test system for one case study. The performance under unbalanced line impedances is examined. Finally, the PV system is also tested in a low inertia PV-diesel microgrid.

7.1 Summary of Major Contributions

1. In this thesis, a control strategy is proposed for a single-stage three-phase PV interfacing inverter. Using this control scheme, the system is able to compensate negative sequence load currents. The converter simultaneously accomplishes maximum power point tracking, sinusoidal current injection, and phase balancing. The control scheme does not rely on balanced source voltages to generate the reference current waveforms. The grid-side current of the inverter is controlled to ensure accurate current injection.
2. A dual-variable virtual impedance active damping scheme for an LCL filter has been proposed. Using both the inner inductor current and the filter capacitor current as the feedback variables improves the DC rejection compared to using capacitor current alone. For a specified damping ratio of the filter, the feedback gains can be explicitly calculated.
3. A modified PR controller has been proposed which prevents resonator windup for improved performance during saturation of the modulation index. The backtracking anti-windup scheme used in PI controllers has been adapted for a PR controller. The proposed scheme has more accurate phase tracking during activation of the anti-windup loop compared with the previously proposed approach. This feature is important for maximizing real power injection and preventing bus voltage collapse. The proposed strategy also showed a better transient response with less overshoot and

oscillation. The proposed anti-windup strategy was shown to allow faster recovery after a contingency scenario.

4. A sinusoidal reference current generation scheme has been proposed which uses the HCDFST to calculate the negative sequence load current and positive sequence grid voltage. Numerical compensation to prevent errors during off-nominal grid frequency has been derived. The proposed method has a half-cycle response time even during harmonic distortion. The numerical compensation method has been shown to greatly improve the performance compared to the conventional half-cycle DFT when the frequency of the diesel generator deviated during large load changes.
5. An investigation into the effect of the PV array operating conditions on unbalance compensation has been conducted using Matlab/Simulink®. The ability of the PV system to compensate negative sequence currents at different levels of irradiance is verified. The effect of negative sequence compensation on the DC link voltage was studied for different regions of the P-V curve. The results of the simulation and analysis favour shifting the operating point towards the open-circuit voltage when a reduction in real power is necessary, rather than decreasing the voltage.

7.2 Suggestions for Future Work

- Only unbalance compensation has been considered in this thesis. Harmonic currents may also degrade power quality in distribution networks. The proposed control scheme could be extended to allow harmonic currents to be selectively compensated.
- PV systems are also capable of providing reactive power support, which has not been considered in this thesis. The control scheme could be modified to allow for reactive power compensation during low irradiation and balanced conditions.
- In this thesis the VSC studied has a three-wire connection. In four-wire systems, zero sequence components are also possible in the current and voltage. Future work could include adapting the proposed control scheme for zero sequence current compensation if the PV converter has a four-wire configuration.

Appendix A: Model of the PV Array Used in Simulation

A photovoltaic cell is a semiconductor device which generates charge carriers when exposed to solar radiation. The power production depends on the efficiency of the cell, the level of solar irradiation, temperature, and other environmental conditions. The single diode PV model is shown in Figure A.1 [1].

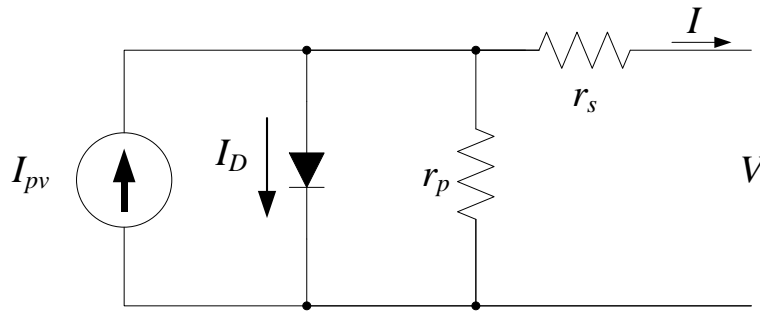


Figure A.1: Single diode model of a PV cell [1]

In Figure A.1, the solar radiation induced generation of charge carriers is modelled by the current source I_{pv} . The value of I_{pv} depends on irradiance, measured in W/m^2 . The voltage at the terminal of the cell is V and the output current is I . The diode models the properties of the p-n junction. The governing equation for the PV cell is given in (A.1).

$$I = I_{ph} - I_D - \frac{V + r_s I}{r_p}$$

$$I_D = I_{sat} \left(\exp \left(q \frac{V + r_s I}{k T a} \right) - 1 \right) \quad (\text{A.1})$$

$$q = 1.60217646 \times 10^{-19} \text{C} : \text{Electron Charge}$$

$$k = 1.3806503 \times 10^{-23} \text{J/K} : \text{Boltzmann constant}$$

$$T : \text{Temperature (K)}$$

Equation (A.1) is the Shockley diode equation, where I_{sat} is the diode saturation current, and a is the diode ideality constant. The resistances r_s and r_p are primarily dependent on the manufacturing process and materials used.

For N_s series and N_p parallel connected cells equation (A.1) is rewritten as (A.2) to calculate the total current. In (A.2) the voltage V and current I are the terminal voltage and current of the array respectively.

$$I = N_p I_{pv} - N_p I_{sat} \left(\exp \left(q \frac{VN_p + N_s r_s I}{N_s N_p k T a} \right) - 1 \right) - \frac{N_p V}{N_s r_p} - \frac{N_s r_s I}{r_p} \quad (\text{A.2})$$

Thus, equation (A.2) can be used to model a panel or array of panels as well as a single cell. The parameters experimentally determined in [1] are used to model a 51.5 kW-peak PV array, and parameters are listed in Table A.1.

The photo-generated current I_{pv} is strongly dependent on both the temperature T and the irradiance IR . This relationship is modelled as in (A.3) [1].

$$I_{pv} = (I_{pv,n} + K_{pv}(T - T_n)) \frac{IR}{IR_n} \quad (\text{A.3})$$

$I_{pv,n}$, T_n , and IR_n are the values of the photo-generated current, temperature, and irradiance respectively, at the Standard Test Conditions (STC) listed in Table A.1. K_{pv} is short circuit current/temperature coefficient provided by the manufacturer. The diode saturation current I_{sat} is strongly dependent on the temperature of the cell. This relationship is given in (A.4),

$$I_{sat} = \frac{I_{sc,n} + K_I(T - T_n)}{\exp \left(\frac{(V_{oc,n} + K_V(T - T_n))}{\frac{aq}{N_s k T}} \right) - 1} \quad (\text{A.4})$$

where $V_{oc,n}$ is the open-circuit voltage and $I_{sc,n}$ is the short-circuit current at the STC. The open-circuit voltage/temperature coefficient K_V is a parameter given in the data sheet. Each PV panel consists of 54 PV cells connected in series.

Table A.1: PV Panel/array parameters [1]

Standard Test Conditions: $T_n = 300 \text{ K}, IR_n = 1000 \text{ W/m}^2$	
$V_{oc,n}$	42.9/527(array) V
$I_{sc,n}$	8.21/131.36(array) A
$I_{pv,n}$	8.214/131.424(array) A
P_{max}	201.5/51,584(array) W
r_s	0.221 Ω
r_p	415.4 Ω
Number of Series Panels	16
Number of Parallel Panels	16
N_s	864
N_p	16
a	1.3

Equations (A.1)-(A.4) have been implemented in Matlab/Simulink® using the values listed in Table A.1 to simulate a PV generator.

References:

- [1] M.G. Villalva, J.R. Gazoli and E.R Filho, "Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays," *IEEE Trans. Power Electron.*, vol.24, no.5, pp.1198-1208, May 2009.

Appendix B: Diesel Generator Parameters

The Synchronous Machine block from the SimPowerSystems Simulink® toolbox is used in the simulations conducted in Chapter 6. The electrical portion of the generator is modelled by a sixth order state-space system. The mechanical portion of the generator is modelled by a first order system.

Synchronous Machine Parameters:

Base power, $S_b = 300$ kVA,

Base Voltage, $V_b = 460$ Vrms,

Nominal frequency, $f = 60$ Hz

Rated Speed $\omega_0 = 1800$ rpm

Stator parameters (pu):

Stator resistance, $R_s = 0.2353$, leakage inductance $L_{ls} = 0.09$, d-axis magnetizing inductance, $L_{md} = 3.13$, q-axis magnetizing inductance $L_{mq} = 2.7$

Field Parameters (referred to stator, pu):

Field resistance $R_f = 0.007436$, leakage inductance $L_{lfd} = 0.3643$

Damper windings (referred to stator, pu):

d-axis resistance $R_{kd} = 0.2164$ and leakage inductance $L_{lkd} = 1.819$, q-axis resistance $R_{kq1} = 0.05752$ and leakage inductance $L_{lkq1} = 0.3249$

Number of Poles: 2

Model of the Diesel and its Control:

The diesel engine is modelled as a first order system with a delay [1]. The proportional integral controller PI_{DG} regulates the speed of the diesel-generator set by the droop gain K_{droop} and the power output of the generator P_{gen} , by controlling the torque produced by the

actuator. The actuator is modelled by a first order system with time constant τ_2 . A delay block which represents the engine dead-time due to the piston firing delay is implemented in Simulink® as a fixed time delay of 10.6 ms. The output of the delay block is the engine torque. T_{gen} is the load torque supplied by the synchronous generator. The speed of the engine is maintained through a governor and the inertia J which represents the combined inertia of the engine and the generator.

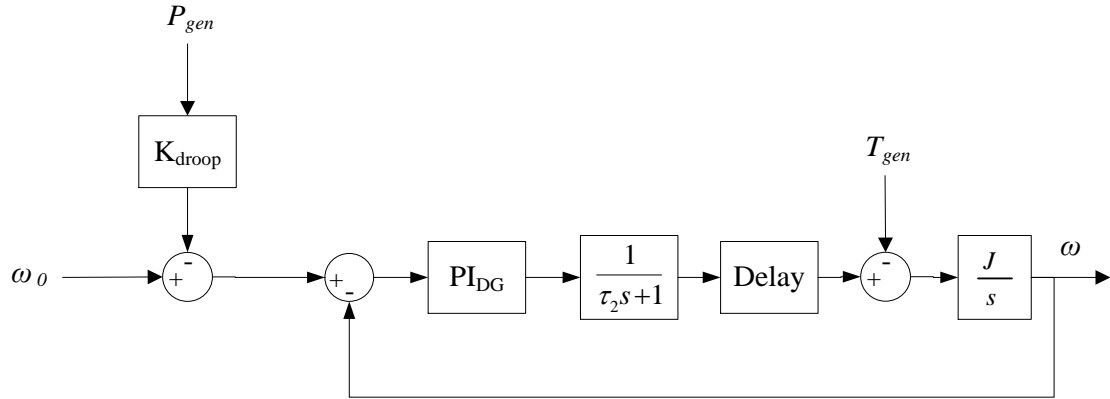


Figure B.1: Diesel engine model

Table B.1: Diesel engine parameters

K_{droop}	1/60 pu
$K_{DG,P}$	12.5
$K_{DG,I}$	12.5
τ_2	0.1 s
Delay	10.6 ms
J	0.2 pu

Automatic Voltage Regulator:

The generator output voltage control is accomplished using the Simulink® excitation system block which implements an IEEE type 1 voltage regulator combined with a DC exciter. The inputs to the excitation system are the d and q-axis components of the generator voltage, V_d and V_q in pu, and the reference voltage V_{ref} which is determined from the reactive power output of the generator, Q , and the droop gain K_{vd} . The excitation block computes the positive sequence peak voltage and passes the signal through a low-pass filter with time constant τ_r which represents the dynamics of the stator terminal voltage transducer. A first

order regulator with gain K_a and time constant τ_a controls the output field voltage V_f . A damping loop with gain K_f and time constant τ_f is included. The values of the excitation system parameters are listed in Table B.2.

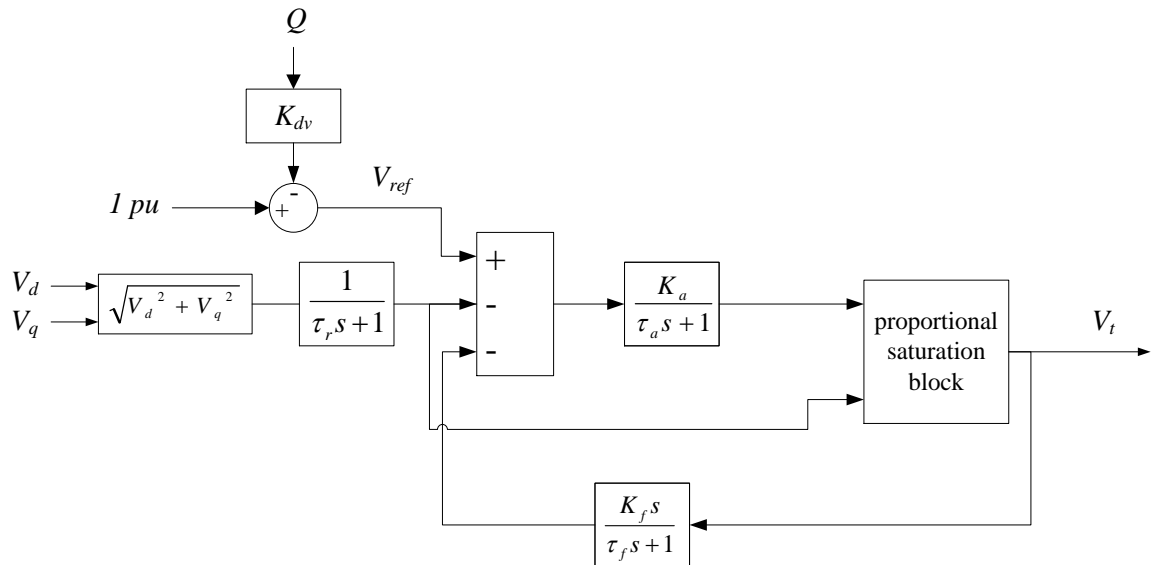


Figure B.2: Voltage regulator and excitation system for the generator

Table B.2: Excitation system parameters

K_{dv}	0.125 pu
τ_r	20e-3
K_a	250
τ_a	0.005
K_f	0.001
τ_f	0.1

References:

- [1] S. Roy, O.P. Malik and G.S. Hope, "An adaptive control scheme for speed control of diesel driven power-plants," *IEEE Trans. Energy Convers.*, vol.6, no.4, pp.605-611, Dec. 1991.

Appendix C: Derivations for Section 3.3

At the resonant frequency, the gain of the third order transfer function with the form (3.11) can be approximated by a second order function if the purely real pole is sufficiently farther to the left of the resonant pole pair on the s-plane. For values of m greater than 5 this assumption holds true [1].

$$\frac{1}{a(s^2 + 2\zeta\omega_n's + \omega_n'^2)(s + m\zeta\omega_n')} \approx \frac{1}{a(s^2 + 2\zeta\omega_n's + \omega_n'^2)m\zeta\omega_n'} \quad (\text{C.1})$$

From (3.14) and (C.1) the second order approximation of the LCL filter is:

$$G_{igu}(s) \approx \frac{1}{L_c L_g C_f (s^2 + 2\zeta\omega_n's + \omega_n'^2) m\zeta\omega_n'} \quad (\text{C.2})$$

Since the gain of the $G_{con}(s) \approx k_p$, the open loop transfer function is

$$P(s) \approx \frac{k_p}{L_c L_g C_f (s^2 + 2\zeta\omega_n's + \omega_n'^2) m\zeta\omega_n'} \quad (\text{C.3})$$

From (3.14), (C.3) can be rewritten in terms of the filter parameters and virtual impedance gains as which is equivalent to (3.19).

$$P(s) \approx \frac{k_p(m+2)}{L_g C_f m(k_{dc} + k_{dl}) \left(s^2 + 2 \frac{(k_{dc} + k_{dl})}{L_c(m+2)} s + \frac{L_c + L_g}{L_c L_g C_f (1 + 2m\zeta^2)} \right)} \quad (\text{C.4})$$

The expression for k_p in (3.17) can be simplified since $k_{dl} \ll (L_c + L_g)^2 \omega_c^2$.

$$k_p \approx (L_c + L_g) \omega_c \quad (\text{C.5})$$

From (C.4) and (C.5) the expression for the loop transfer function is (C.6).

$$P(s) \approx \frac{(L_c + L_g)\omega_c(m+2)}{L_g C_f m(k_{dc} + k_{dl}) \left(s^2 + \frac{2(k_{dc} + k_{dl})}{L_c(m+2)} s + \frac{L_c + L_g}{L_c L_g C_f (1+2m\zeta^2)} \right)} \quad (\text{C.6})$$

The magnitude of the loop gain at the resonant frequency ω_n is determined by letting $s = j\omega_n$.

$$\begin{aligned} |P(j\omega_n)| &= \left| \frac{(L_c + L_g)\omega_c(m+2)}{L_g C_f m(k_{dc} + k_{dl}) \left(-\omega_n^2 + j \frac{2(k_{dc} + k_{dl})}{L_c(m+2)} \omega_n + \frac{L_c + L_g}{L_c L_g C_f (1+2m\zeta^2)} \right)} \right| \\ &= \frac{L_c \omega_c(m+2)}{m(k_{dc} + k_{dl}) \sqrt{\left(\frac{2(k_{dc} + k_{dl})}{L_c(m+2)\omega_n} \right)^2 + \left(\frac{2m\zeta^2}{1+2m\zeta^2} \right)^2}} \end{aligned} \quad (\text{C.7})$$

Since the -180° phase occurs at the resonant frequency the magnitude of the loop gain at ω_n is related to the Gain Margin (GM) by (C.8).

$$|P(j\omega_n)| = 10^{\frac{-GM}{20}} \quad (\text{C.8})$$

Equating (C.8) with (C.7) and rearranging yields the expression for the crossover frequency in (3.20).

$$\omega_c = 10^{\frac{-GM}{20}} \frac{m(k_{dc} + k_{dl})}{L_c \omega_c(m+2)} \sqrt{\left(\frac{2(k_{dc} + k_{dl})}{L_c(m+2)\omega_n} \right)^2 + \left(\frac{2m\zeta^2}{1+2m\zeta^2} \right)^2} \quad (\text{C.9})$$

References:

- [1] K. Ogata, "Basic Control Actions and Response of Control Systems," in *Modern Control Engineering*, 3rd ed., Upper Saddle River, NJ: Prentice Hall, 1997, pp. 230.

Curriculum Vitae

Name: Elizabeth Tomaszewski

Post-secondary Education and Degrees: University of Western Ontario
London, Ontario, Canada
2008-2012 B.E.Sc.

The University of Western Ontario
London, Ontario Canada
2012-2015, M.E.Sc. Candidate

Honours and Awards: Ontario Graduate Scholarship
2013-2014

Hydro One Graduate Scholarship
Summer 2013

Related Work Experience Teaching Assistant
The University of Western Ontario
2013-2014

Research Assistant
The University of Western Ontario
2012-2015

Publications:

- [1] Elizabeth Tomaszewski and Jin Jiang, "An anti-windup scheme for proportional resonant controllers in a three-phase VSC." Conference paper under preparation for submission to PES General Meeting 2016.
- [2] Elizabeth Tomaszewski and Jin Jiang, "A PV inverter control scheme for compensation of unbalanced loads." Journal paper under preparation.